AN4397
Application note

Evaluation board for SPV1050 ULP harvester (buck-boost architecture)

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Introduction

The STEVAL-ISV020V1 is an evaluation board based on the ultralow power energy harvester and battery charger SPV1050. For any detail related to the SPV1050 features and performances please refer to the SPV1050 datasheet.

The evaluation board implements the buck-boost configuration of the DC-DC converter and has the purpose of enhancing the SPV1050 based applications development by testing the silicon performance thanks to many jumpers and test points, and by helping to find out the best system configuration to make the SPV1050 device working at the most of efficiency.

The STEVAL-ISV020V1 board is optimized to:

- Harvest energy from PV panels supplying 2.6 V ≤ V_{MP} ≤ 9 V and 10 µA ≤ I_{MP} ≤ 20 mA.
- Charge a battery with the 3.7 V undervoltage protection threshold (V_{UVP}) and 4.2 V end of charge voltage threshold (V_{EOC}).

Nevertheless, few easy changes on the application components (input and output resistor partitioning, C_{IN} capacitor) allow to use a different PV panel and source (like TEG), and a battery, by setting the V_{MPP_SET}, the V_{UVP} and the V_{EOC} thresholds according to the source and load. More in detail, operating ranges can be extended as follows: V_{MP} from 150 mV up to 18 V, I_{MP} up to 100 mA, V_{UVP} down to 2.2 V and V_{EOC} up to 5.3 V.

The STEVAL-ISV020V1 is shown in *Figure 1*.

Figure 1. STEVAL-ISV020V1 evaluation board

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1 Schematic and bill of material

The schematic, bill of material and gerber files can be downloaded from the Design resources tab of the STEVAL-ISV020V1 product folder on *www.st.com*.

Figure 2. STEVAL-ISV020V1 schematic

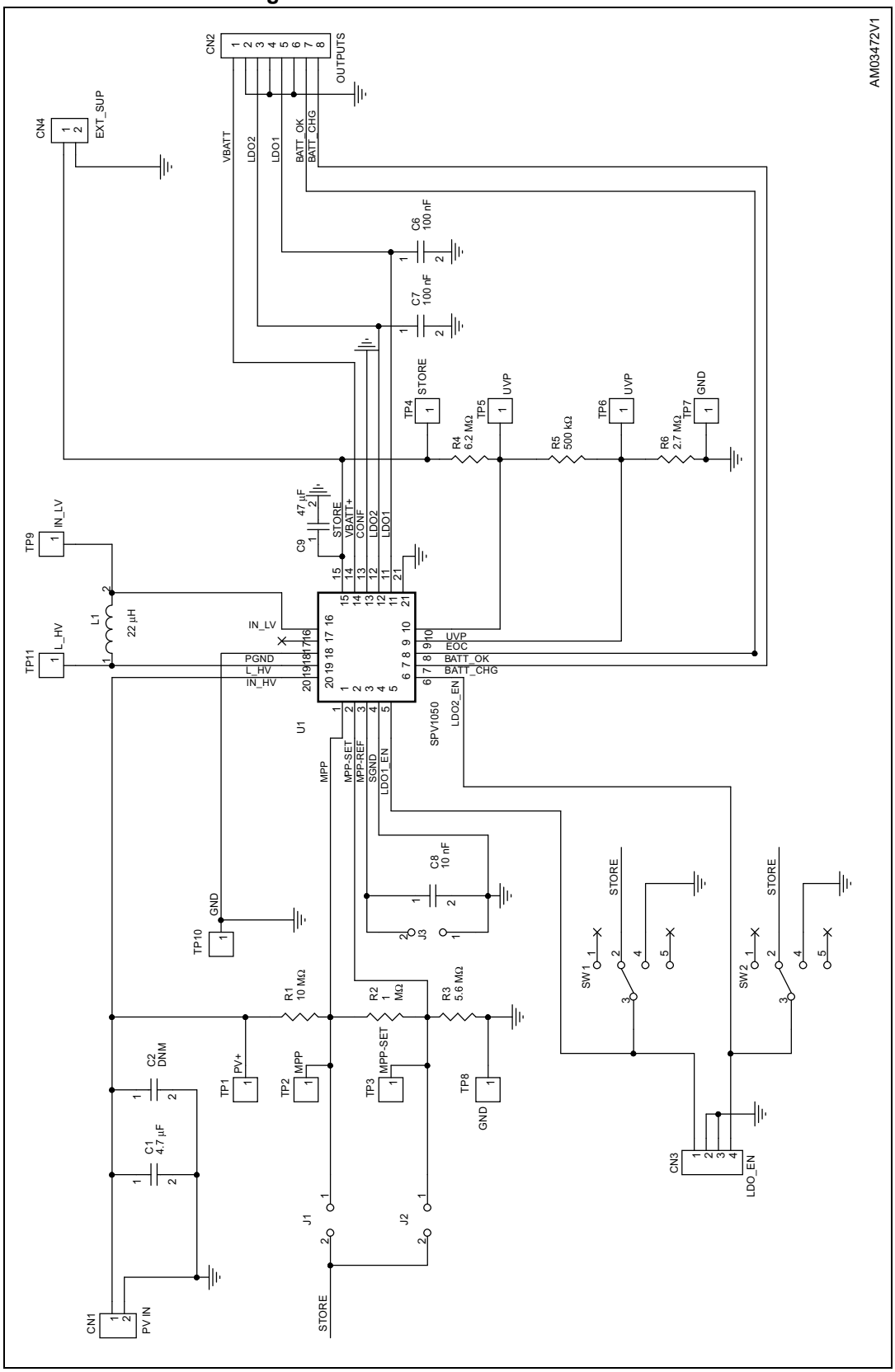


Figure 3. STEVAL-ISV020V1 application diagram

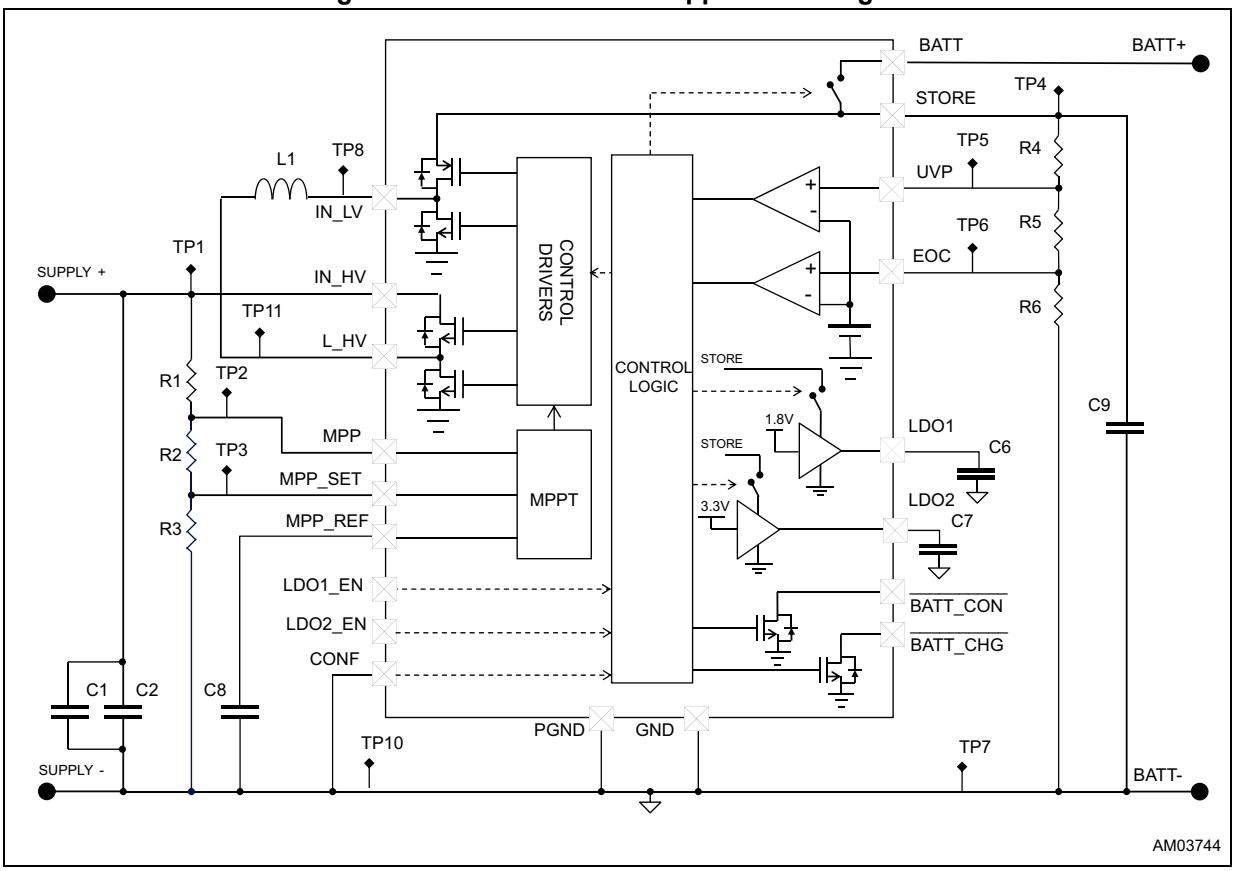


Table 1. Bill of material

Sect.	Item	Qty.	Reference	Part / value	Tolerance %	Voltage current	Watt	Technol. info.	Package	Manufacturer	Manufacturer code	More information
DC-DC input section	1	1	U1	SPV1050					VFQFPN 3 x 3 x 1 20L (code A0BR)	ST	SPV1050	Plastic socket
	2	1	CN1	2-way screw connector						TE Connectivity	282834-2	Input connector for PV panel or TEG
	3	1	C1	4.7 µF	15%	25 V			0805	Murata	GCM21BR71C 475KA73L	Input capacitance
	4	0	C2 (DNM)	4.7 µF	15%	25 V			0805	Murata	GCM21BR71C 475KA73L	
	5	3	J1, J2, J3	Jumper				Pitch 2.54 mm	TH			Enable/disable MPPT
	8	1	R1	10 MΩ	1%				0805	YAGEO	RC0805FR-0710ML	Resistor partitioning for MPP track/setting
	9	1	R2	1 MΩ	1%				0805	TE Connectivity	CRG0805F1M0	
	10	1	R3	5.6 MΩ	1%				0805	VISHAY	CRCW08055M 60FKEA	
	11	1	L1	22 µH	20%					Coilcraft	LPS4018-223ML_	DC-DC inductor
	12	1	C8	10 nF	15%	16 V		X7R	0603	Murata	GRM188R71C1 03KA01D	Voltage sampling time constant capacitance

Table 1. Bill of material (continued)

Sect.	Item	Qty.	Reference	Part / value	Tolerance %	Voltage current	Watt	Technol. info.	Package	Manufacturer	Manufacturer code	More information
Battery section	13	1	CN4	2-way screw connector						TE Connectivity	282834-2	Connector for external supply of pin STORE
	14	1	C9	47 µF	20%	10 V			0805	TDK	C2012X5R1A476M125AC	
	15	1	R4	6.2 MΩ	5%				0805	RS	RS-0805-6m2-5%-0.125W	Resistor Partitioning for UVP, EOC, protection setting
	16	1	R5	499 kΩ	1%				0805	VISHAY	CRCW0805499KFKEA	
	17	1	R6	2.7 MΩ	1%				0805	VISHAY	CRCW08052M70FKEA	
	18	1	CN2	8-way screw connector						TE Connectivity	282836-8	Connector for battery and battery status signals
LDOs section	19	2	C6, C7	100 nF	10%			X7R	0603	KEMET	C0603C104K4RAC	Tank capacitor for LDOs
	21	2	SW1, SW2	5-pin male Stripline				Pitch 2.54 mm	TH			Close 2 - 3: LDO disabled Close 1 - 2: LDO enabled Floating: external control through CN3
	23	1	CN3	4-way screw connector						TE Connectivity	282836-4	Connector for LDOs load connection

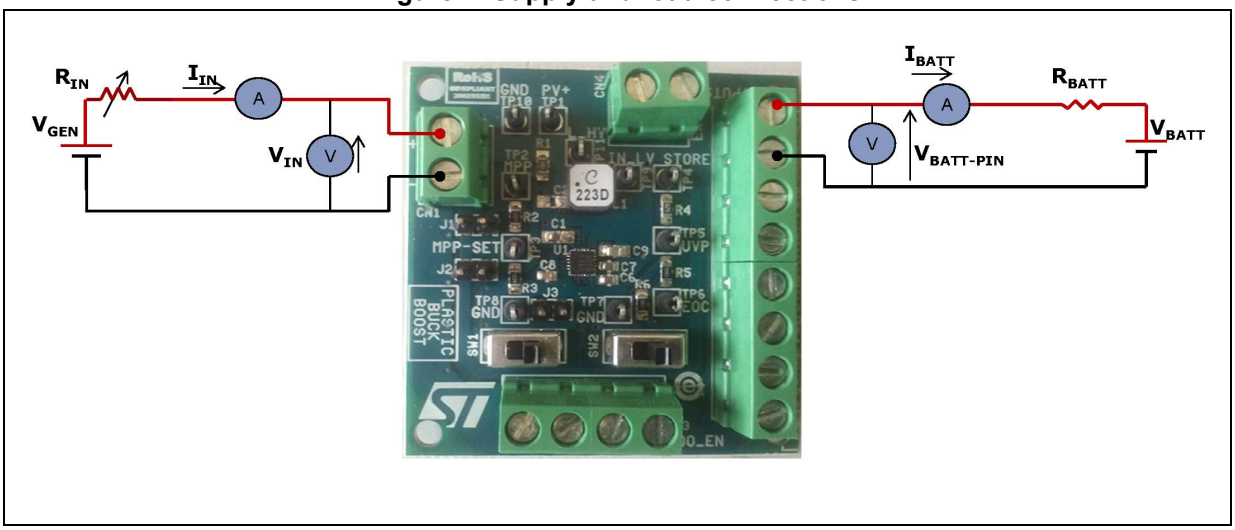
Table 1. Bill of material (continued)

Sect.	Item	Qty.	Reference	Part / value	Tolerance %	Voltage current	Watt	Technol. info.	Package	Manufacturer	Manufacturer code	More information
List of test points	24	1	TP1					True hole				PV+ pin sensing and soldering
	25	1	TP2					True hole				MPP pin sensing and soldering
	26	1	TP3					True hole				MPP-SET pin sensing and soldering
	27	1	TP4					True hole				STORE pin sensing and soldering
	28	1	TP5					True hole				ULP pin sensing and soldering
	29	1	TP6					True hole				EOC pin sensing and soldering
	30	1	TP7					True hole				GND pin sensing and soldering
	31	1	TP8					True hole				GND pin sensing and soldering
	32	1	TP9					True hole				IN_LV pin sense (for probe scope)
	33	1	TP10					True hole				GND pin sensing (for probe scope)
	34	1	TP11					True hole				L_HV pin sensing (for probe scope)

2 System setup

The system setup that can be used for the evaluation of the SPV1050 device is shown in *Figure 4*:

Figure 4. Supply and load connections



The supply system emulates the I-V characteristic of a PV panel and it is composed by a power supply V_{GEN} to determine V_{OC} and a resistor R_{IN} to determine I_{MP} and V_{MP}.

Considering the typical electrical parameters of a PV panel (V_{OC}, V_{MP}, I_{MP}, I_{SC}), the supply system has to be set as following:

- $V_{GEN} = V_{OC}$
- $R_{IN} = (V_{OC} - V_{MP}) / I_{MP}$

At the output stage a real battery can be connected to the BATT pin. The battery can be emulated by a power supply with a resistor in series.

3 Layout

From *Figure 5* to *Figure 7* show the components placement and the layout (top and bottom views) of the STEVAL-ISV020V1.

Figure 5. Layout - silkscreen view

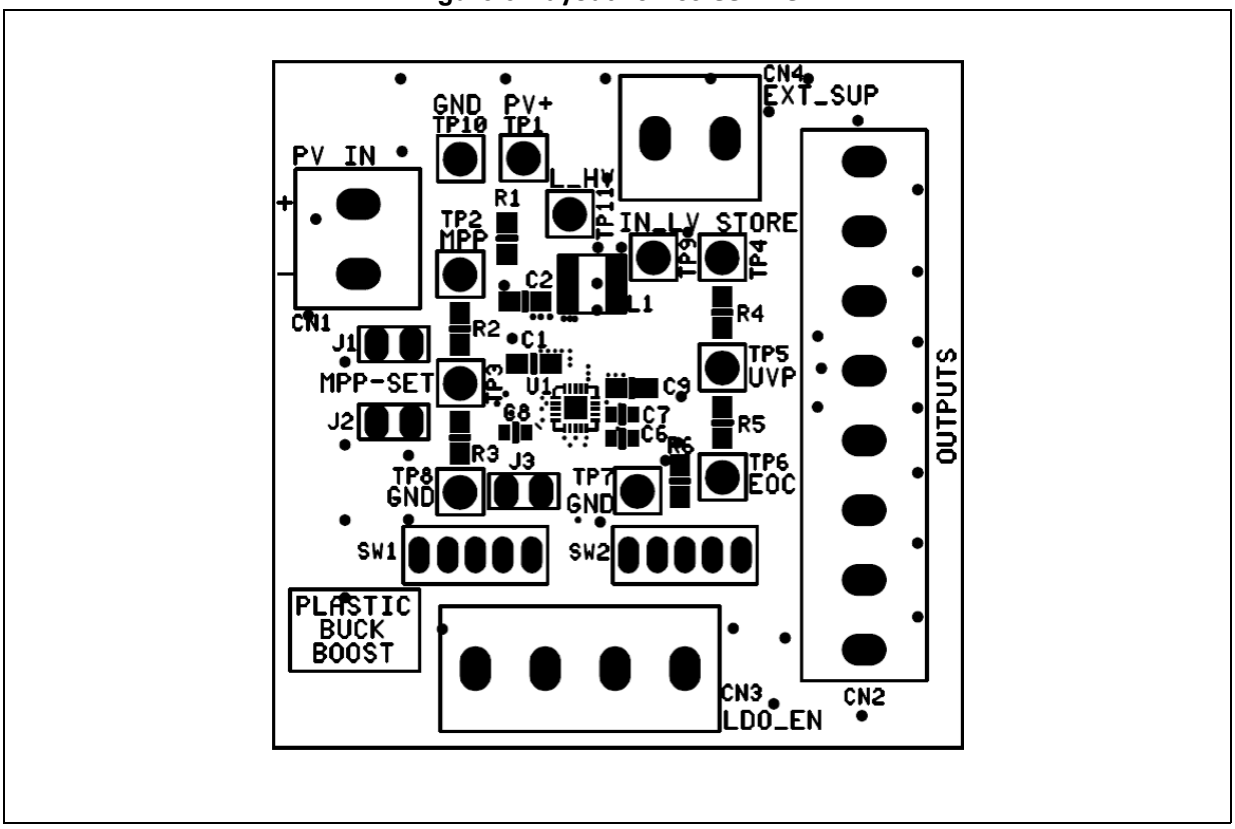


Figure 6. Layout - top view

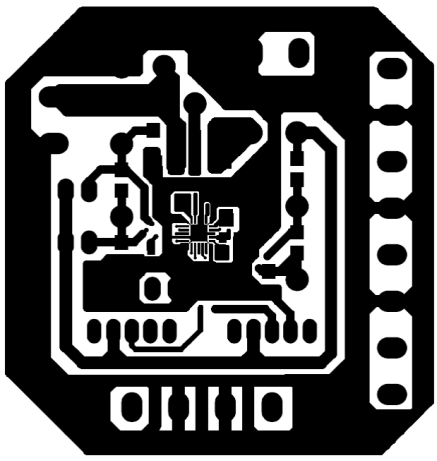
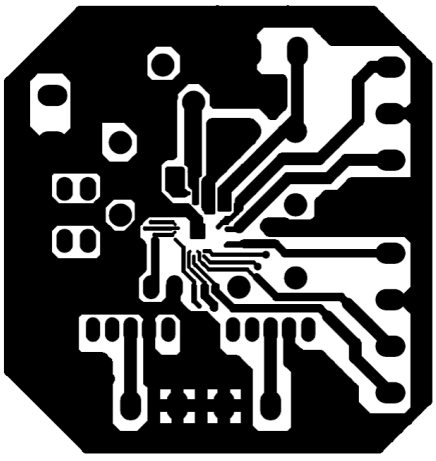


Figure 7. Layout - bottom view



The following indications must be followed in the PCB routing:

- The same ground plane has to connect the exposed pad and the pins PGND and GND.
- The capacitor on the STORE pin must be placed as close as possible to the pin.
- The capacitors on LDO1 and LDO2 pins must be placed as close as possible to the respective pins.

Details on the recommended layout solution are shown in *Figure 8* and *Figure 9*.

Figure 8. Ground plane detail

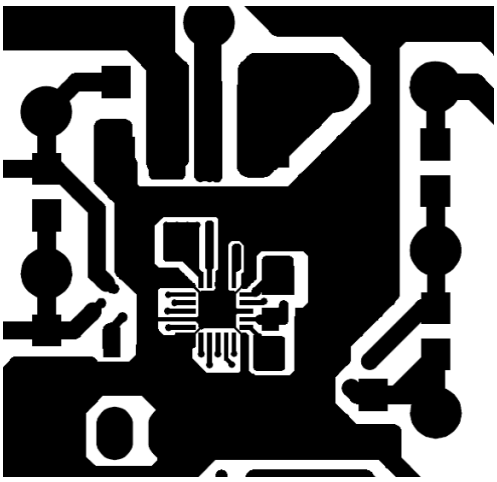
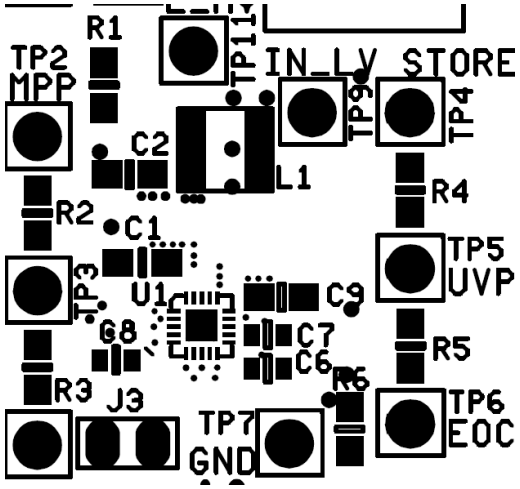


Figure 9. Components placement detail



4 Component selection

This section describes the application rules to be followed for properly selecting the components around the SPV1050 device.

4.1 MPPT setting

The “Maximum Power Point” (MPP) is set through the input resistor partitioning R1, R2 and R3.

As a preliminary rule, the voltage on the MPP pin (V_{MPP}), which depends on the voltage supplied by the selected source (V_{IN}), must be ≤ V_{UVP} (which is set by the output resistor partitioning R3, R4, R5).

So, the following equation:

Equation 1

$$V_{MPP} = V_{IN}\frac{R2+R3}{R1+R2+R3} \leq V_{UVP}$$

can be rewritten as follows:

Equation 2

$$V_{UVP} \geq V_{OC(MAX)}\frac{R2+R3}{R1+R2+R3}$$

$VOC_{(MAX)}$ stands for the maximum voltage that the source can supply (open circuit voltage).

Further, the $MPP_{RATIO} = V_{MPP\_SET} / V_{OC}$ is set by the following equation:

Equation 3

$$V_{MPP\_SET} = V_{IN}\frac{R3}{R1+R2+R3}$$

$$MPP_{RATIO} \bullet V_{OC} = V_{IN}\frac{R3}{R1+R2+R3}$$

For the PV panels the V_{MP} is typically in the range between 70% and 80% of V_{OC}.

Finally, the leakage on the input resistor partitioning must be negligible, hence typically it must be:

Equation 4

$$10\ M\Omega \leq R1 + R2 + R3 \leq 20\ M\Omega$$

4.2 Input capacitance

Every 16 seconds (typical) the SPV1050 device stops switching for 400 ms. During this time frame the input capacitor C1 is charged up to V_{OC} by the source: the voltage will rise according to the time constant (T1), which depends both on its capacitance and on the equivalent resistance R_{EQ} of the source.

In case of PV panel source, assuming I_{MP} as the minimum current at which the MPP must be guaranteed, the R_{EQ} can be calculated as follows:

Equation 5

$$R_{EQ} = \frac{V_{OC} - V_{MPP}}{I_{MP}} = \frac{V_{OC} \bullet (1 - MPP_{RATIO})}{I_{MP}}$$

Consequently:

Equation 6

$$C1 \leq \frac{T1}{R_{EQ}}$$

Figure 10 and *Figure 11* show the effect of different value of the C1 on the time constant: too high capacitance might be not charged within the 400 ms time window affecting the MPPT precision.

Figure 10. Input stage equivalent circuit

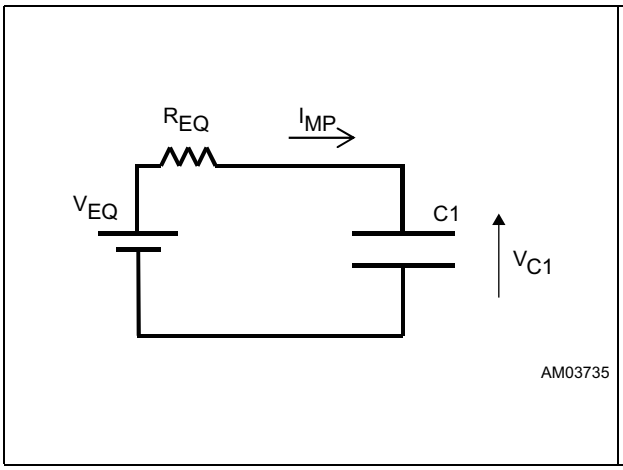
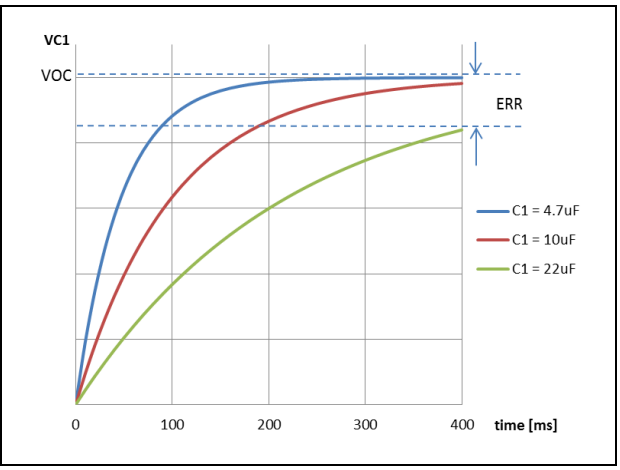


Figure 11. Effect of C1 on sampled voltage



The default C1 = 4.7 µF capacitance covers the most typical application range. The energy extracted from the harvested source, and stored in the input capacitance, is transferred to the load by the DC-DC converter though the inductor. The energy extracted by inductor depends by the sink current: the higher input currents causes higher voltage drop on the input capacitance and this may result a problem for low voltage (< 1 V) and high energy (> 20 mA) sources. In such application cases the input capacitance has to be increased or, alternatively the inductance has to be reduced.

The SPV1050 performances might be further improved by reducing the time constant (e.g. reducing input capacitance) at very low input power.

4.3 Capacitance on MPP-REF pin

It's recommended to use C8 = 10 nF in most of the application cases.

4.3.1 Inductor selection

The SPV1050 device controls the switching of the integrated DC-DC by limiting the peak current flowing through the inductor L1.

L1 = 22 µH covers the most typical application range: the lower is the series resistance of the selected inductor, the lower is its DC loss. The current capability of the selected inductor must be ≥ 200 mA.

4.3.2 Output voltage ripple

In case of battery with high series resistance and fast load transient, the capacitor on the STORE pin may momentarily discharge and cause the undesired triggering of the V_{UVP} threshold, implying the battery disconnection.

Although the fast transient might be masked by a proper capacitance between UVP and GND pins, if the battery has low peak current capability, the voltage on the STORE pin may further drop down lower than V_{UVP}.

The drawback of a C_{UVP} between UVP and GND pins is the related delay in the intervention of the end of charge protection. The consequent voltage overshoot on V_{STORE} must be always lower than the AMR of the STORE pin (5.5 V); the worst case to be considered is at maximum input power and the STORE pin in the open load.

Increasing the capacitance on the STORE pin has the drawback of affecting the output time constant and consequently delays the startup time. The same capacitor might be placed in parallel to the battery.

The selection of the battery and of the output capacitance on the STORE pin (C9) is strictly related to the following application parameters:

- The series resistance of the battery (R_{BATT})
- The EOC threshold (V_{EOC}) and the UVP threshold (V_{UVP})
- The maximum load current ($I_{LOAD(MAX)}$)
- The $T_{LOAD(ON)}$, how long the load sink ($I_{LOAD(MAX)}$)
- The maximum allowed voltage drop on LDOs outputs ($V_{DROP(MAX)}$)

The maximum current that can be supplied to the load is the sum of the currents that can be supplied by the battery ($I_{BATT(MAX)}$) and by the C9 (I_{STORE}):

Equation 7

$$I_{LOAD(MAX)} = I_{BATT(MAX)} + I_{STORE}$$

The maximum current that the battery can supply without triggering the UVP threshold is:

Equation 8

$$I_{BATT(MAX)} = \frac{V_{BATT} - V_{UVP}}{R_{BATT}}$$

The amount of charge that the C9 can supply is:

Equation 9

$$Q9 = C9 \bullet V_{DROP(MAX)}$$

Considering that I = C • dV/dt, it follows:

Equation 10

$$I_{BATT(MAX)} = I_{LOAD(MAX)} - \frac{C_{STORE} \bullet V_{DROP(MAX)}}{T_{LOAD(ON)}}$$

Thus:

Equation 11

$$C_{STORE} \geq T_{LOAD} \bullet \frac{I_{LOAD(MAX)} - I_{BATT(MAX)}}{V_{DROP(MAX)}}$$

4.3.3 UVP and EOC setting

The pins UVP and EOC have to be connected to the STORE pin by the resistor partitioning R4, R5 and R6 to setup the related thresholds by scaling down those voltage values and by comparing them with the internal bandgap voltage reference set at 1.23 V.

The design rules to setup R4, R5 and R6 are the following:

Equation 12

$$V_{BG} = V_{UVP} \quad \frac{R5 + R6}{R4 + R5 + R6}$$

Equation 13

$$V_{BG} = V_{EOC} \quad \frac{R6}{R4 + R5 + R6}$$

Further, in order to minimize the leakage due to the output resistor partitioning it has to be typically:

Equation 14

$$10\ M\Omega \leq R4 + R5 + R6 \leq 20\ M\Omega$$

5 Board description

The STEVAL-ISV020V1 board has a full set of connectors, jumpers and switches as described below:

Table 2. CN1 connector

	CN1 pin number	
	1	2
Signal	INPUT+	INPUT-

Table 3. CN2 connector

	CN2 pin number							
	1	2	3	4	5	6	7	8
SPV1050 pin signal	V_{BATT}	GND	LDO2	GND	LDO1	GND	BATT-CON	BATT-CHG

- V_{BATT}: connect this pin to the positive of the battery.
- LDO2: connect this pin to the load to be supplied at 3.3 V.
- LDO1: connect this pin to the load to be supplied at 1.8 V.
- BATT-CON: output logic pin for battery connection monitoring.
- Please notice that this is an open drain pin, which has to be pulled up by a resistor (typically 10 MΩ) to a voltage rail lower than V_{STORE}.
- BATT-CHG: output logic pin for battery charging status monitoring.
- Please notice that this is an open drain pin, which has to be pulled up by a resistor (typically 10 MΩ) to a voltage rail lower than V_{STORE}.

Table 4. CN3 connector

	CN3 pin number			
	1	2	3	4
SPV1050 pin signal	LDO1_EN	GND	GND	LDO2_EN

- LDO1_EN: input logic pin to enable/disable the LDO1. Connect this pin to the control signal from the microcontroller.
- LDO2_EN: input logic pin to enable/disable the LDO2. Connect this pin to the control signal from the microcontroller.

Table 5. CN3 connector

	CN4 pin number	
	1	2
SPV1050 pin signal	STORE	GND

- STORE: connect this pin to the tank capacitor C_{STORE}.
- GND: system ground.

The MPPT function can be disabled by pulling up the pin MPP-SET and unsoldering the resistor R2. In this case the duty cycle of the switching converter will be regulated according to the fixed end of charge voltage connected to the J3.

Table 6. J1, J2, J3: enable/disable MPPT

	J1	J2	J3
Function	LEAVE IT OPEN (signal monitoring)	OPEN: MPPT ENABLED CLOSE: MPPT DISABLED(1)	LEAVE OPEN IF J2 IS OPEN. CONNECT TO EXTERNAL REFERENCE VOLTAGE IF J2 is CLOSED

1. The R2 must be unsoldered.

Table 7. SW1, SW2: enable/disable LDOs

	SW1	SW2
Function	CLOSE 3 - 4: LDO1 DISABLED CLOSE 2 - 3: LDO1 ENABLED FLOATING: EXTERNAL CONTROL BY CN3	CLOSE 3 - 4: LDO2 DISABLED CLOSE 2 - 3: LDO2 ENABLED FLOATING: EXTERNAL CONTROL BY CN3

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
15-May-2014	1	Initial release.
16-Jun-2016	2	Updated *Section 4.3.2: Output voltage ripple on page 14* (added test).