AN2264
APPLICATION NOTE

Three-Phase SMPS for low power applications with VIPer12A

Introduction

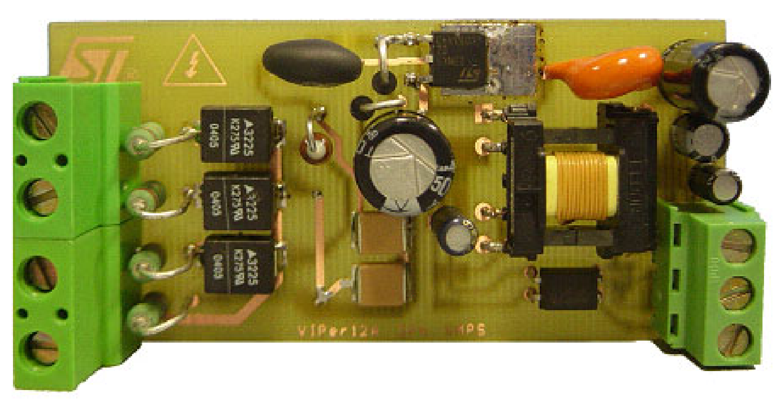
Some industrial applications require a so called 'ultra-wide' input voltage range (between 90 and 450Vac). Due to the variations of the main, input voltages up to 450Vac are typical in three-phase applications. A maximum input voltage of 450Vac requires the use of very high voltage components, increasing cost, size, the weight and the overall complexity of the power supply. Hence, the market is looking for solutions with low cost and good performance.

Thi document introduces a cost effective solution for low power high voltage power supplies. The proposed solution consists of in an off-line SMPS and a low cost front-end regulation circuit for input voltage limiting. Such a circuit allows proper operation of the power converter avoiding the use of voltage over-rated components, both passive and active. The circuit is suitable for any off-line SMPS topology since it includes a switching transistor connected between the input rectifier and the DC bulk capacitor (STMicroelectronics patent pending). The series switch limits the DC input voltage of the power converter by means of a suitable driving circuit; thus the SMPS primary transistor can be selected as a standard part as well as a smart power primary IC.

Typical end applications of this solution can be found in the industrial market in the range below 5W, such as three-phase and single phase power meter, industrial bias power supply and auxiliary SMPS for high voltage street-lighting, where the input voltage can range between 90Vac and 450Vac and 1000V power MOSFETs are currently used.

As an example of industrial applications, a flyback converter for supplying an electronic power meter is considered. The use of the proposed approach in a power converter designed for 265Vac maximum input voltage allows the operating input voltage to be extended up to 450Vac or higher with no damages to the converter components. Thus, the major benefit of such solution is a significant cost saving thanks to the reduction of components voltage rating.

Figure 1. Board Prototype



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1 Application Description

The present SMPS has been designed according to the following specifications:

Table 1. Operating conditions

Parameter	Value
Input Voltage Range	90 to 450 Vac
Input Frequency Range	50/60 Hz
Output Voltage 1	V1=5V
Output Voltage 2	V2=3.3V
Output Current 1	I1=10mA
Output Current 2	I2=100mA
Output Power (peak)	550mW
Line Regulation	+/- 1%
Load Regulation	+/- 1%
Output Ripple Voltage 1	50mV
Hold-up capability	> 40 ms (*)
Safety	EN60950
EMI	EN55022 class B

(*) Considering the STPM01 roll over time (31ms) and the Memory M95040 write time per data (5ms).

In addition to the previous specs, the power supply has to be compliant also with the standards of electricity meters, i.e. IEC 62052-11 and IEC 62053-21, since it has been specifically developed for such an application. The main prescriptions are listed here below:

- **Input connection and voltage marking (EN62052-11):**

Table 2. Three-Phase Electricity Meter Voltage Marking

Meter	Rated System Voltage (V)
Single-phase 2 wire 120V	120
Single-phase 3 wire 120V (120V to the mid-wire)	240
Three-Phase 3 wire 2-element (230 V between phases)	400
Three-Phase 4 wire 3-element (230 V phase to neutral)	400

- **Pulse Voltage Test (EN62052-11):**

  - Pulse waveform: according IEC 60060-1

  - Voltage rise time: ±30%

  - Voltage fall time: ±20%

- Source impedance: 500Ω ± 50Ω
- Source Energy: 0.5J ±0.05J
- Rated Pulse Voltage: 4000V
- Test Voltage Tolerance: +0 -10%

- Mean input power : 2W according to EN62053-21 (Switching power supplies with peak power values exceeding the specified value are also permitted)
- Temperature Range: -25°C ± 3°C ÷ +70°C ± 2°C (EN 62052-11)

2 Circuit Description

The schematic of the board is shown in *Figure 2.*

A 3-phase 4-wire bridge is used for mains rectification because the neutral rectification is needed to ensure proper operation in case of missing neutral connection or neutral mis-wiring.

A varistor is connected between each line and neutral to guarantee pulse voltage test immunity according to the EN62052-11 standard.

The input EMI filter is a simple undamped LC-filter for both differential and common mode noise suppression.

The circuit for input voltage limiting is connected between the input EMI filter and the bulk capacitor C4. Such a circuitry includes a Power MOSFET and a self driven control section. The MOSFET Q1 is a standard N-Channel 500V 3.3Ω in D-PAK package, mounted on a small copper area to improve thermal performance. The self driven control section consists of a voltage divider and zener diodes. The resistors R1, R2 and R3 ensure the gate-source charge for the switch, while the zener diodes D3 and D4 set the maximum voltage value (360V) across the bulk capacitor.

An NTC limits the inrush current and ensures Q1 operation inside its safe operating area.

The flyback converter is based on VIPer12AS, a member of the VIPerX2A family, which combines a dedicated current mode off-line PWM controller with a high voltage power MOSFET on the same silicon chip. The switching frequency is fixed at 60kHz by the IC internal oscillator allowing, to optimize the transformer size and cost. The transformer reflected voltage has been set to 60V, providing enough margin for the leakage inductance voltage spike and no snubber circuit is needed with a consequent cost saving.

As soon as the voltage is applied on the input of the converter the high voltage start-up current source connected to the drain pin is activated and starts to charge the V_{dd} capacitor C8 through a constant current of 1mA. When the voltage across this capacitor reaches the V_{ddon} threshold (about 14V) the VIPer12AS starts to switch. During normal operation the smart power IC is powered by the auxiliary winding of the transformer via the diode D7. No spike killer for the auxiliary voltage fluctuations is needed thanks to the wide range of the V_{dd} pin (9-38V). The primary current is measured using the integrated current sensing for current mode operation.

The output rectifier D6 has been chosen in accordance with the maximum reverse voltage and power dissipation; in particular a 0.5A-80V Schottky diode, type TMBAT49, has been selected.

The output voltage regulation is performed by secondary feedback on the 5V output dedicated to the display, while the 3.3V output, dedicated to the logic part and the microcontroller, is linearly post-regulated from the 5V output. This operation is performed by a very low drop voltage regulator, L4931ABD33, in SO-8 package. The voltage regulator delivers up to 100mA, ensuring good reliability with no heat sink. The feedback network ensures the required insulation between the primary and secondary sections. The optotransistor directly drives the VIPer12AS feedback pin which controls the IC operation.

A small LC filter has been added to the 5V output in order reduce the high frequency ripple with reasonable output capacitors value.

The flyback transformer is a layer type based on E13 core and N27 ferrite, manufactured by Pulse Eldor, and ensures safety insulation in accordance with the EN60950. *Figure 4.* shows the main features of the transformer.

The whole power supply has been realized on a double side 35um PCB in FR-4, measuring 78 x 38 mm.

Figure 2. Circuit Schematic

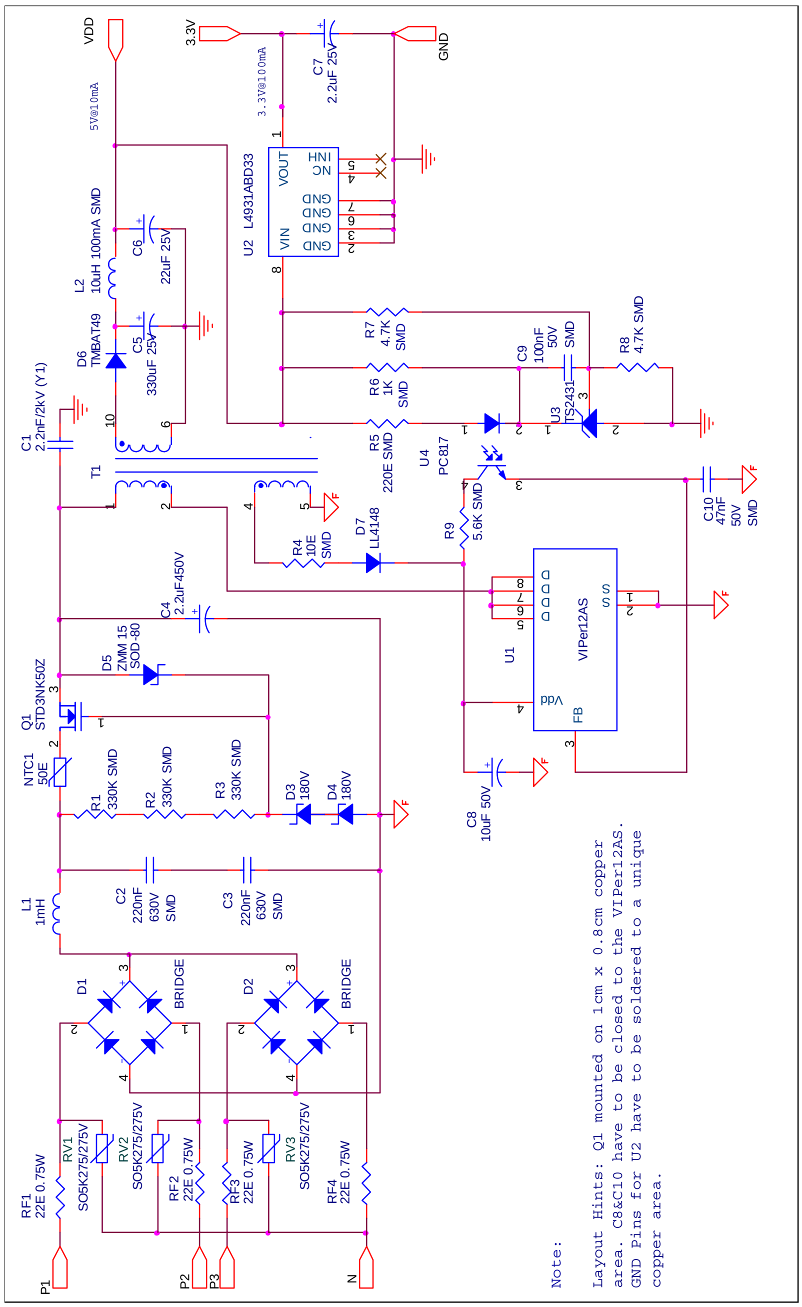
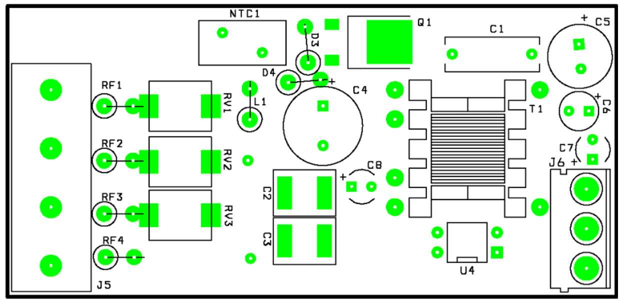
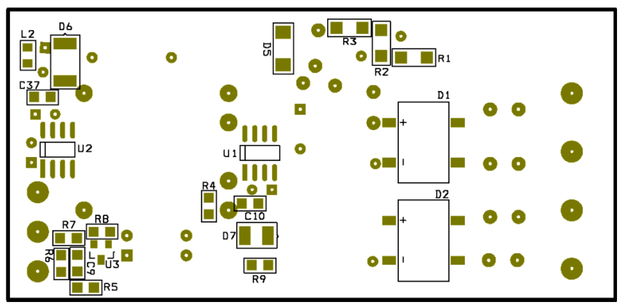


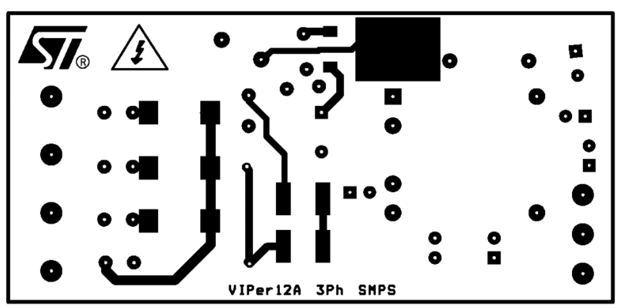
Figure 3. PCB Layout



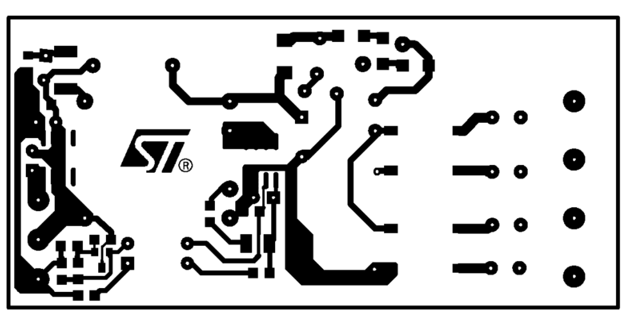
Top side-silk screen (in scale)



Bottom side- silk screen (in scale)

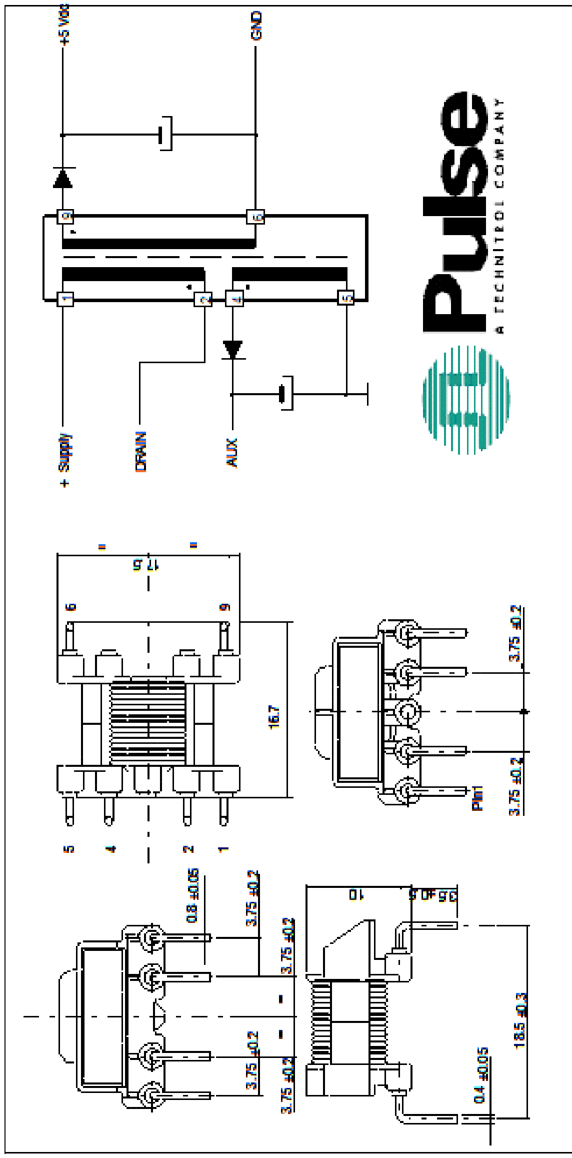


Top side-copper tracks (in scale)



Bottom side-copper tracks (in scale)

Figure 4. Flyback Transformer



Primary Inductance:	2.2mH ±20%
Primary Leakage Inductance (%L_p):	< 2%
Primary to secondary turn ratio:	11
Auxiliary to secondary turn ratio:	3

Table 3. Bill of Materials

Reference	Value	Description
CON1, CON2		Hartmann/ptr, 2 poles, type PK 7402, 380V_{AC} 16A
CON3		Hartmann/ptr, 3 poles, type PK 3503, 380V_{AC} 16A
C1	2.2nF/2kV	Cera-Mite Corporation 44LD22 Y1 Ceramic Capacitor 20%
C2, C3	220nF 630V	TDK C5750X7R2J224M SMD Ceramic Capacitor 20%
C4	2.2uF450V	Rubycon Aluminium Radial Lead Electrolytic Capacitor YK Series 29mA 20%
C5	330uF 25V	Rubycon Aluminium Radial Lead Electrolytic Capacitor ZL Series 56mR 995mA 20%
C6	22uF 16V	Rubycon Aluminium Radial Lead Electrolytic Capacitor ZA Series 270mR 350mA 20%
C7	2.2uF 50V	Panasonic ECA1HHG2R2 NHG-A Radial Lead Electrolytic Capacitor 18mA 20%
C8	10uF 50V	Panasonic ECA1HHG100 NHG-A Radial Lead Electrolytic Capacitor 39mA 20%
C9	100nF 50V	muRata GRM40X7R104Z50 SMD Ceramic Capacitor 20%
C10	47nF 50V	muRata GRM40X7R473Z50 SMD Ceramic Capacitor 20%
D1, D2	BRIDGE	General Instruments DF10S SMT Diode Bridge 1000V 1A
D3, D4	ZY180V	DO-41 Zener Diode 180V 2W 5%
D5	ZMM 15/SOD-80	Mini-Melf Zener Diode 15V 0.5W 5%
D6	**TMBAT49**	**STMicroelectronics** Small Signal Schottky Diode 80V 0.5A
D7	LL4148/SOD-80	SOD-80 General Purpose Rectifier 75V 200mA
L1	1mH	Epcos B78108-S1105J , Bobbin Core BC 130mA 13R 10%
L2	10uH	TDK GLF2012T100M SMD Signal-Use SMD Inductor 125mA 20%
NTC1	50E	UEI 10SP050L Inrush Current Suppressor 50R 2A 10%
Q1	**STD3NK50Z**	**STMicroelectronics** N-Channel Mosfet 500V 2.3A 3.3R
RF1, RF2, RF3, RF4	22E 0.75W	Yageo Resistor, wire wound, fusible, 22R 0.75W 5%
RV1, RV2, RV3	SO5K275/275V	Epcos B72650M271K72 SMD Varistor 275V_{AC} 8.6J
R1, R2, R3	330K SMD	Resistor, Metal Film 0.25W 5%
R4	10E SMD	Resistor, Metal Film 0.25W 5%
R5	220E SMD	Resistor, Metal Film 0.25W 5%
R6	1K SMD	Resistor, Metal Film 0.25W 5%
R7	4.7K SMD	Resistor, Metal Film 0.25W 5%
R8	4.7K SMD	Resistor, Metal Film 0.25W 5%
R9	5.6K SMD	Resistor, Metal Film 0.25W 5%

Table3. Bill of Materials (Continued)

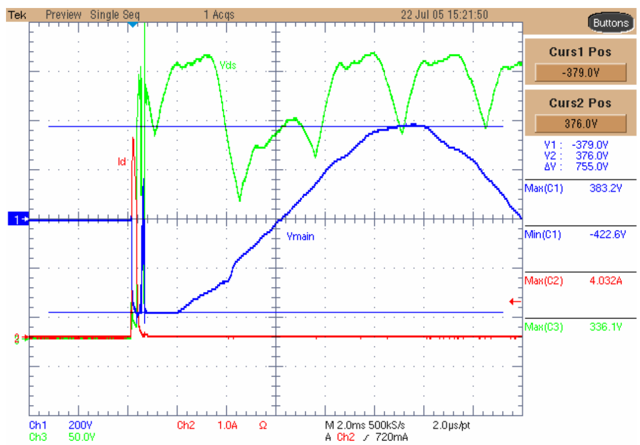
Reference	Value	Description
T1	2432.0015C	E13 TIW Pulse Eldor Switch Mode Transformer
U1	**VIPer12AS**	**STMicroelectronics** Off Line SMPS Primary IC 730V 0.4A 27R
U2	**L4931ABD33**	**STMicroelectronics** Very Low Drop Voltage Regulator 3.3V 300mA 1%
U3	**TS2431**	**STMicroelectronics** Programmable Shunt Voltage Reference 1%
U4	PC817	Sharp Optocoupler 5kV

3 Experimental Results

3.1 Input Voltage Limiting Circuit

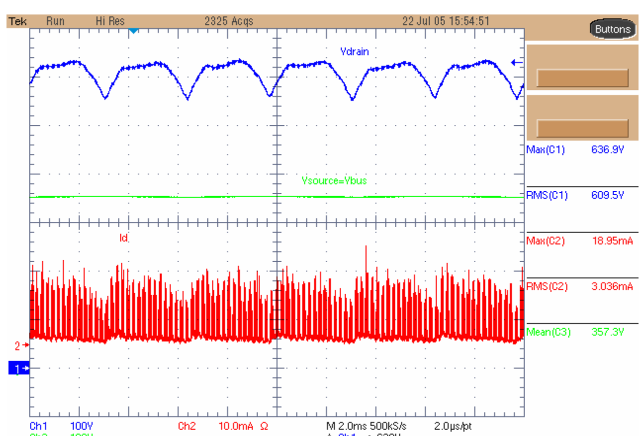
The main waveforms of the input voltage limiting circuit are shown in *Figure 5.* In particular the waveforms refer to the start-up and the steady-state operations at 450Vac and full load ,which are the worst conditions for the device. The advantages of this solution are evident. It limits the DC voltage at the given reference value, in this case 360V, and avoides the use of over-rated components compared to the standard off-line power supply.

Figure 5. MOSFET STD3NK50Z Operation at FULL LOAD and Vin = 450 Vrms



Start-Up

CH1: INPUT VOLTAGE (Blue)
CH2: DRAIN CURRENT (Red)
CH3: DRAIN-SOURCE VOLTAGE (Green)



Steady State

CH1: DRAIN VOLTAGE (Blue)
CH2: DRAIN CURRENT (Red)
CH3: SOURCE VOLTAGE (Green)

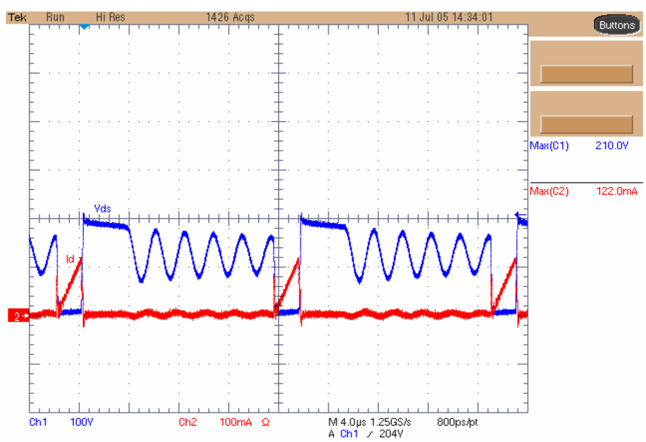
3.2 Steady State Behaviour

Several measurements have been performed on the SMPS in steady state operation, for different values of the main voltage and load condition. The measured values are:

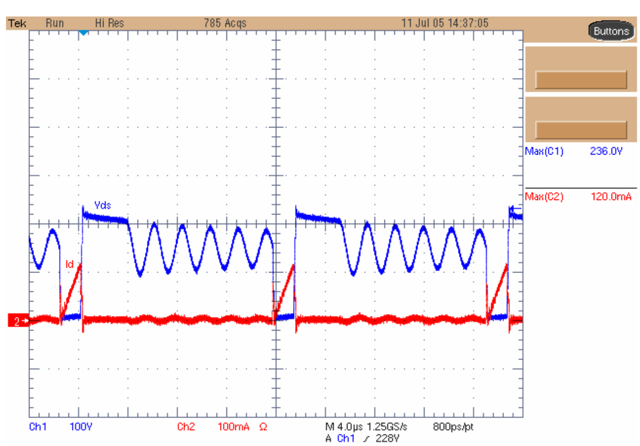
- The peak Drain Current through the VIPer12A
- The peak Drain Voltage across the VIPer12A
- The Peak Drain Voltage across the input MOS
- The Peak Drain Current through the input MOS
- The Reverse Voltage across the output Diode
- The Output Voltage
- The input power consumption

Figure 6. shows some waveforms during the normal operation at full load:

Figure 6. VIPer12AS Vds & Id at FULL LOAD

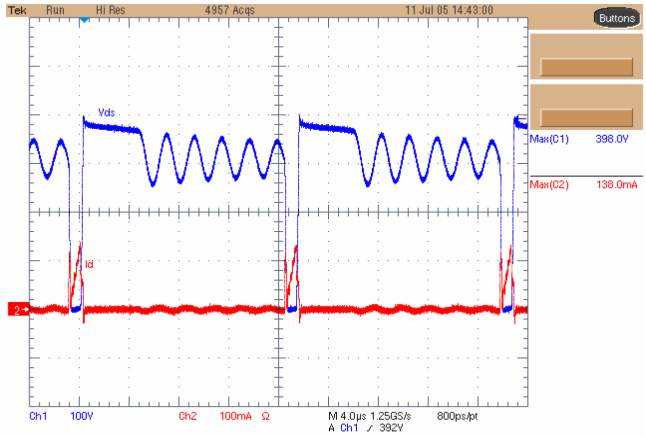


Vin=90 Vrms - 50Hz

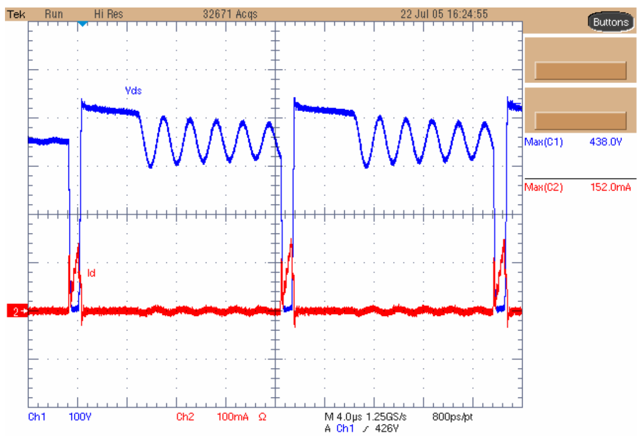


Vin = 110 Vrms - 50Hz

Figure 6. VIPer12AS Vds & Id at FULL LOAD (continued)

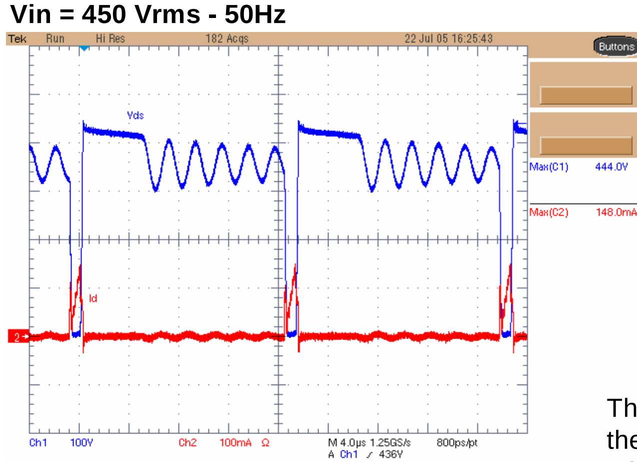


Vin = 230 Vrms - 50Hz



Vin = 380 Vrms - 50Hz

Vin = 450 Vrms - 50Hz



CH1: DRAIN VOLTAGE (Blue)
CH2: DRAIN CURRENT (Red)

Vin (Vac)	Vdsmax(V)	Idpk(mA)
90	210	122
110	236	120
230	398	138
380	438	152
450	444	148

The table lists the measured values of the drain peak voltage and current at minimum, nominal and maximum input mains voltage, during normal operation at full load. The voltage peak, which is 444V, assures a reliable operation of the VIPer12AS power switch with a good margin against the maximum B_{VDSS}.

Table 4. Full Load (Iout ≈100mA)

Input	
Vin [Vrms]=	90
Iin [mArms] =	10.7
Pin [W] =	0.93

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	100	1
Pout [W] =	0.5	

EFF.=54%

Input	
Vin [Vrms]=	110
Iin [mArms] =	9.2
Pin [W] =	0.93

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	100	1
Pout [W] =	0.5	

EFF.=54%

Input	
Vin [Vrms]=	230
Iin [mArms] =	6.5
Pin [W] =	1.12

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	100	1
Pout [W] =	0.5	

EFF.=45%

Table 4. Full Load (Iout ≈100mA) (continued)

Input	
Vin [Vrms]=	380
Iin [mArms] =	4.4
Pin [W] =	1.6

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	100	1
Pout [W] =	0.5	

EFF.=31%

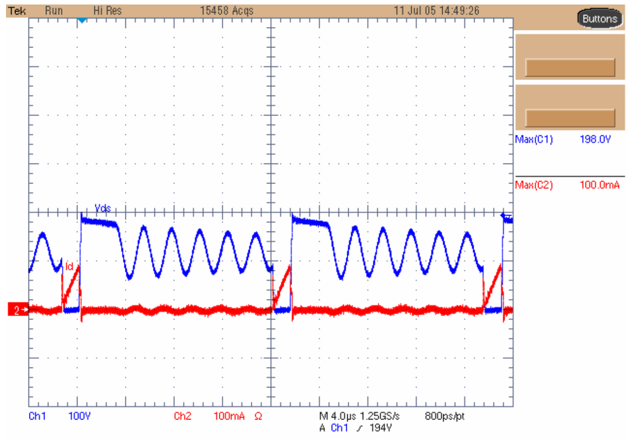
Input	
Vin [Vrms]=	450
Iin [mArms] =	4.5
Pin [W] =	2.0

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	100	1
Pout [W] =	0.5	

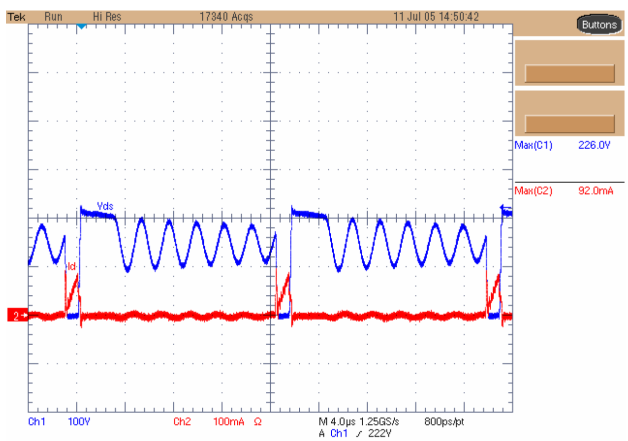
EFF.=25%

The same test has been performed on the board in half load condition, for the different values of the input voltage. In *Figure 7.* some typical waveforms are shown.

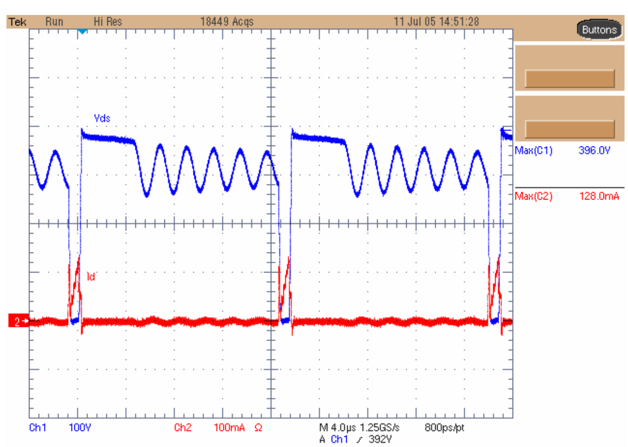
Figure 7. VIPer12AS Vds & Id at HALF LOAD



Vin = 90 Vrms - 50Hz

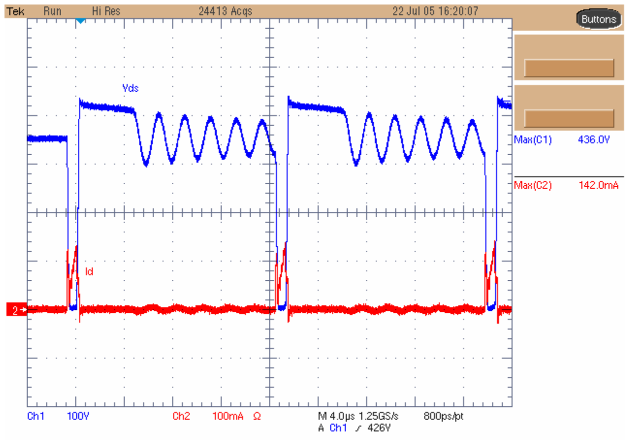


Vin = 110 Vrms - 50Hz

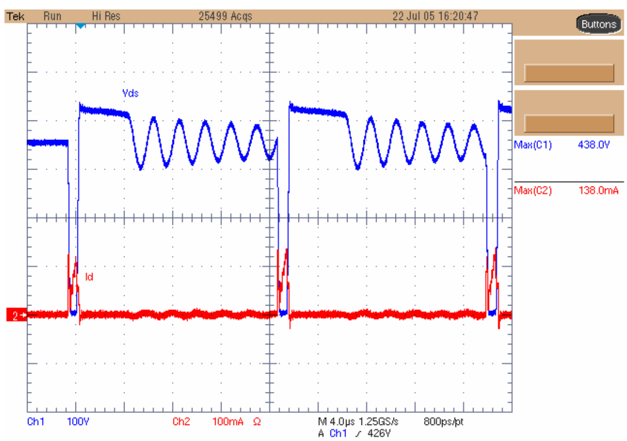


Vin = 230 Vrms - 50Hz

Figure 7. VIPer12AS Vds & Id at HALF LOAD (Continued)



Vin = 380 Vrms - 50Hz



Vin = 450 Vrms - 50Hz

CH1: DRAIN VOLTAGE (Blue)
CH2: DRAIN CURRENT (Red)

Vin (Vac)	Vdsmax(V)	Idpk(mA)
90	198	100
110	226	92
230	396	128
380	436	142
450	438	136

The table lists the measured values of the drain peak voltage and current at minimum, nominal and maximum input mains voltage, during normal operation at full load. The voltage peak, which is 438V, assures a reliable operation of the VIPer12AS power switch with a good margin against the maximum BV_{DSS}.

Table 5. Half Load (Iout≈50mA)

Input	
Vin [Vrms]=	90
Iin [mArms] =	6.9
Pin [W] =	0.58

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	50	1
Pout [W] =	0.25	

EFF.=43%

Input	
Vin [Vrms]=	110
Iin [mArms] =	6.6
Pin [W] =	0.62

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	50	1
Pout [W] =	0.25	

EFF.=40%

Input	
Vin [Vrms]=	230
Iin [mArms] =	4.8
Pin [W] =	0.77

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	50	1
Pout [W] =	0.25	

EFF.=32%

Table 5. Half Load (Iout≈50mA) (Continued)

Input	
Vin [Vrms]=	380
Iin [mArms] =	3.5
Pin [W] =	1.22

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	50	1
Pout [W] =	0.5	

EFF.=20%

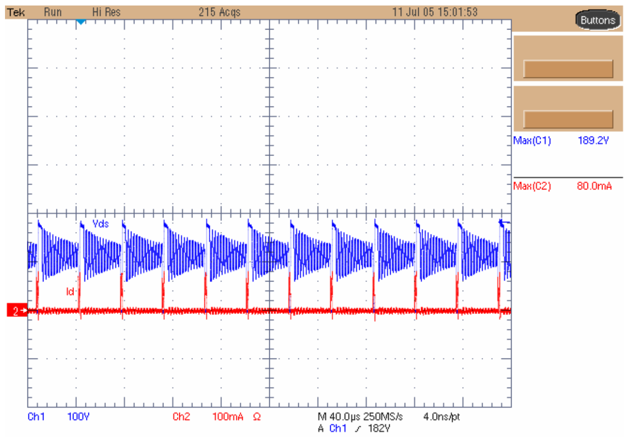
Input	
Vin [Vrms]=	450
Iin [mArms] =	3.5
Pin [W] =	1.5

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	50	1
Pout [W] =	0.25	

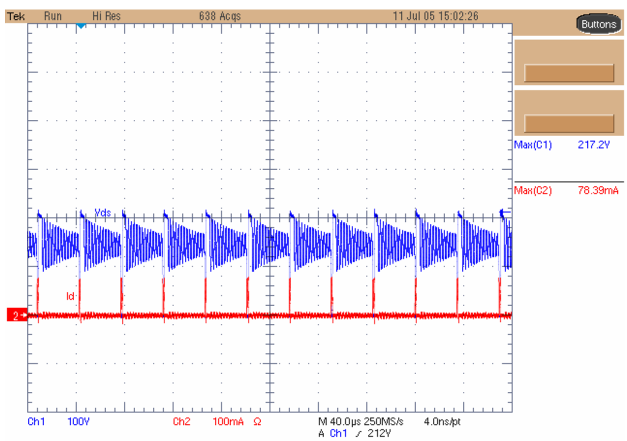
EFF.=17%

Figure 8. shows the waveforms and the results of the steady state in minimum load condition.

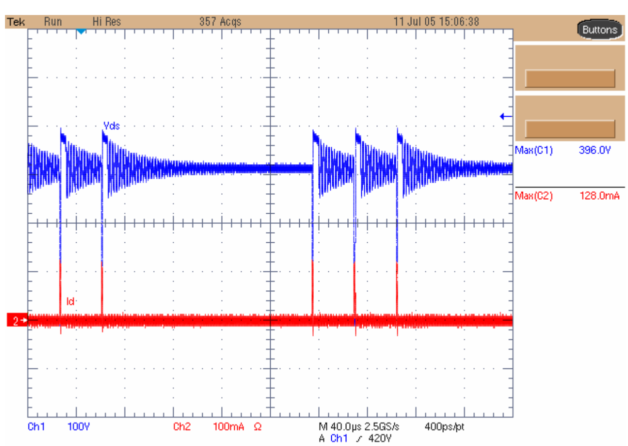
Figure 8. VIPer12AS Vds & Id at MINIMUM LOAD



Vin = 90 Vrms - 50Hz

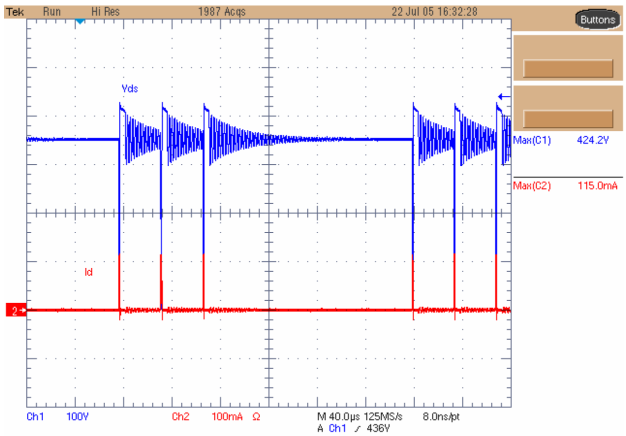


Vin = 110 Vrms - 50Hz

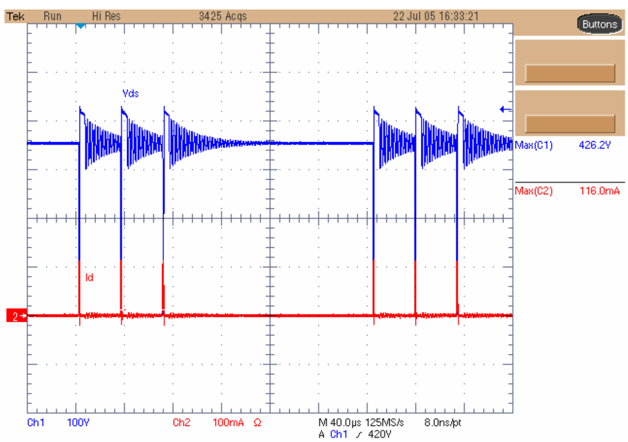


Vin = 230 Vrms - 50Hz

Figure 8.VIPer12AS Vds & Id at MINIMUM LOAD (continued)



Vin = 380 Vrms - 50Hz



Vin = 450 Vrms - 50Hz

CH1: DRAIN VOLTAGE (Blue)
CH2: DRAIN CURRENT (Red)

Also at minimum load condition, the drain voltage peak (426V) ensures a good margin against the maximum BV_{DSS}. The VIPer12A burst mode operation is ensured, saving the input power consumption.

Vin (Vac)	Vdsmax(V)	Idpk(mA)
90	189.2	80
110	217.2	78.4
230	396	128
380	424	115
450	426	116

Table 6. Minimum Load (Iout=10mA)

Input	
Vin [Vrms]=	90
Iin [mArms] =	4.1
Pin [W] =	0.29

Output		
Vout [V] =	3.302	4.989
Iout [mA] =	10	1
Pout [W] =	0.05	

EFF.=17%

Input	
Vin [Vrms]=	110
Iin [mArms] =	3.8
Pin [W] =	0.31

Output		
Vout [V] =	3.303	4.989
Iout [mA] =	10	1
Pout [W] =	0.05	

EFF.=16%

Input	
Vin [Vrms]=	230
Iin [mArms] =	3.1
Pin [W] =	0.43

Output		
Vout [V] =	3.3023	4.989
Iout [mA] =	10	1
Pout [W] =	0.05	

EFF.=12%

Table 6. Minimum Load (Iout=10mA) (Continued)

Input	
Vin [Vrms]=	380
Iin [mArms] =	2.9
Pin [W] =	0.7

Output		
Vout [V] =	3.302	4.989
Iout [mA] =	10	1
Pout [W] =	0.05	

EFF.=7%

Input	
Vin [Vrms]=	450
Iin [mArms] =	2.9
Pin [W] =	0.85

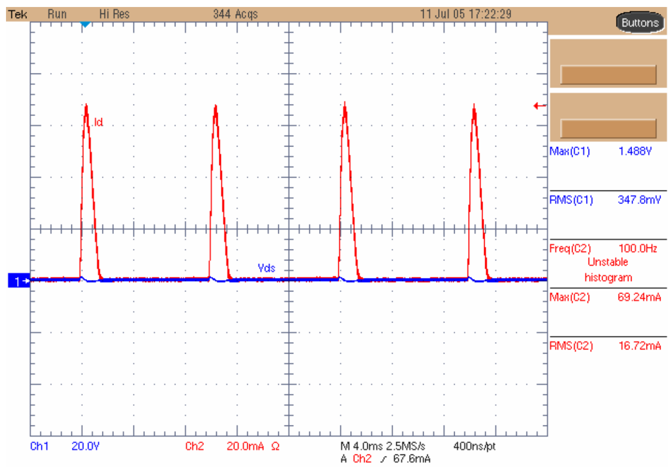
Output		
Vout [V] =	3.302	4.989
Iout [mA] =	10	1
Pout [W] =	0.05	

EFF.=6%

The steady state characterization has been made also for the input MOSFET, in terms of drain-source voltage and drain current, as shown in *Figure 9.*

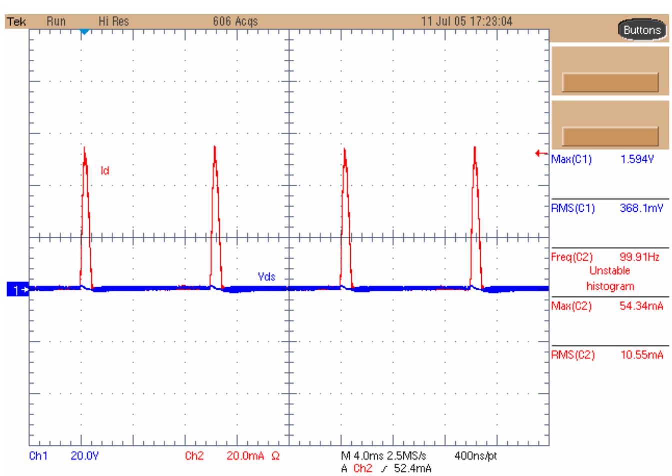
Figure 9. STD3NK50Z Vds & Id at FULL LOAD

In the voltage range below the given reference voltage, the MOSFET is fully on.



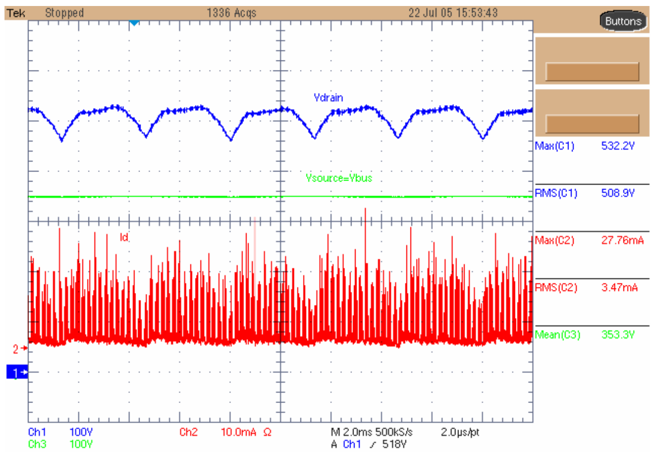
Vin = 110 Vrms - 50Hz

CH1: DRAIN-SOURCE VOLTAGE (Blue)
CH2: DRAIN CURRENT (Red)



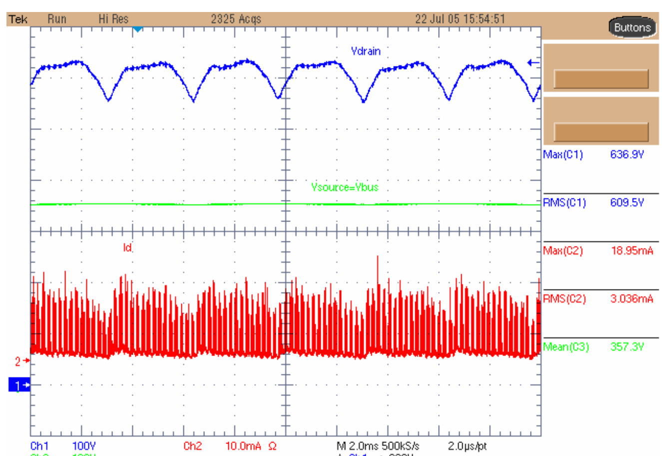
Vin = 230 Vrms - 50Hz

Figure 9. STD3NK50Z Vds & Id at FULL LOAD (continued)



Vin = 380 Vrms - 50Hz

CH1: DRAIN VOLTAGE (Blue)
CH2: DRAIN CURRENT (Red)
CH3: SOURCE VOLTAGE (Green)



Vin = 450 Vrms - 50Hz

As soon as the input rectified voltage is higher than the reference voltage, the input MOSFET is accommodating the voltage drop between the input and the regulated voltage. The peak of the drain-source voltage (around 280V) ensures a good margin against the Vds of the device.

3.3 Line And Load Regulations

In this section the line and load regulations for 5V output are given, as shown in *Figure 10.* and *Figure 11.* For the line regulation the input voltage is slowly increased from 90Vac to 450Vac; For the load regulation the output current is slowly increased from the minimum load 10mA to the maximum load100mA.

Figure 10. Line Regulation

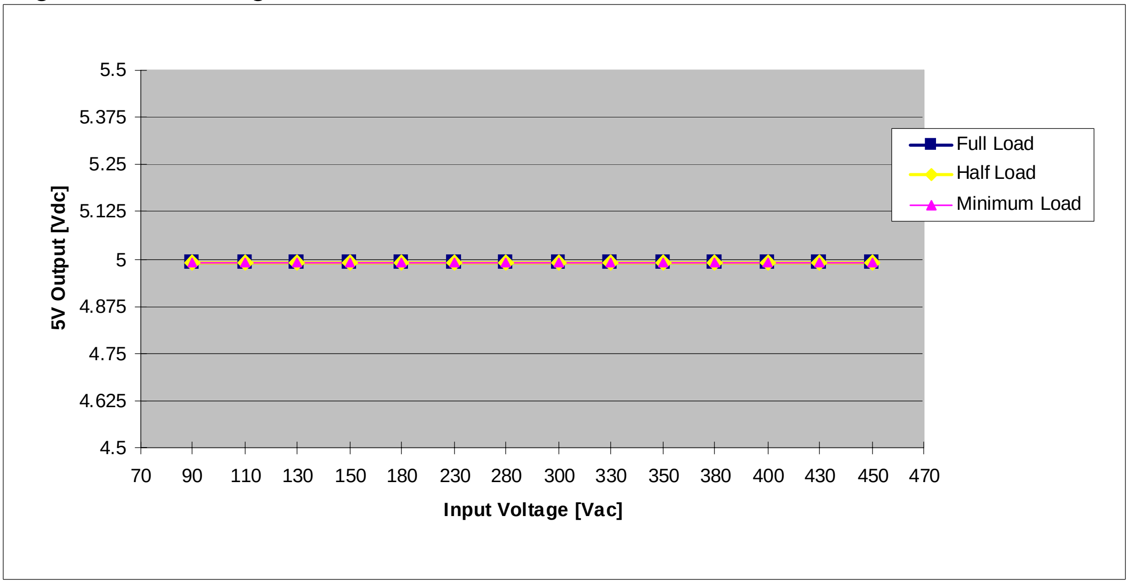
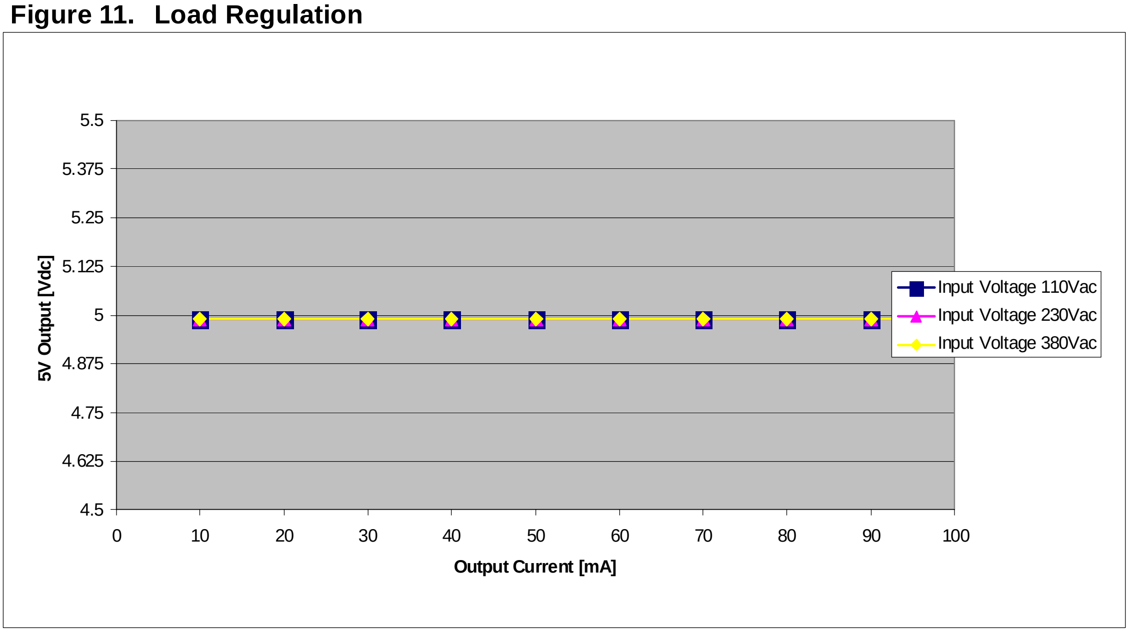


Figure 11. Load Regulation

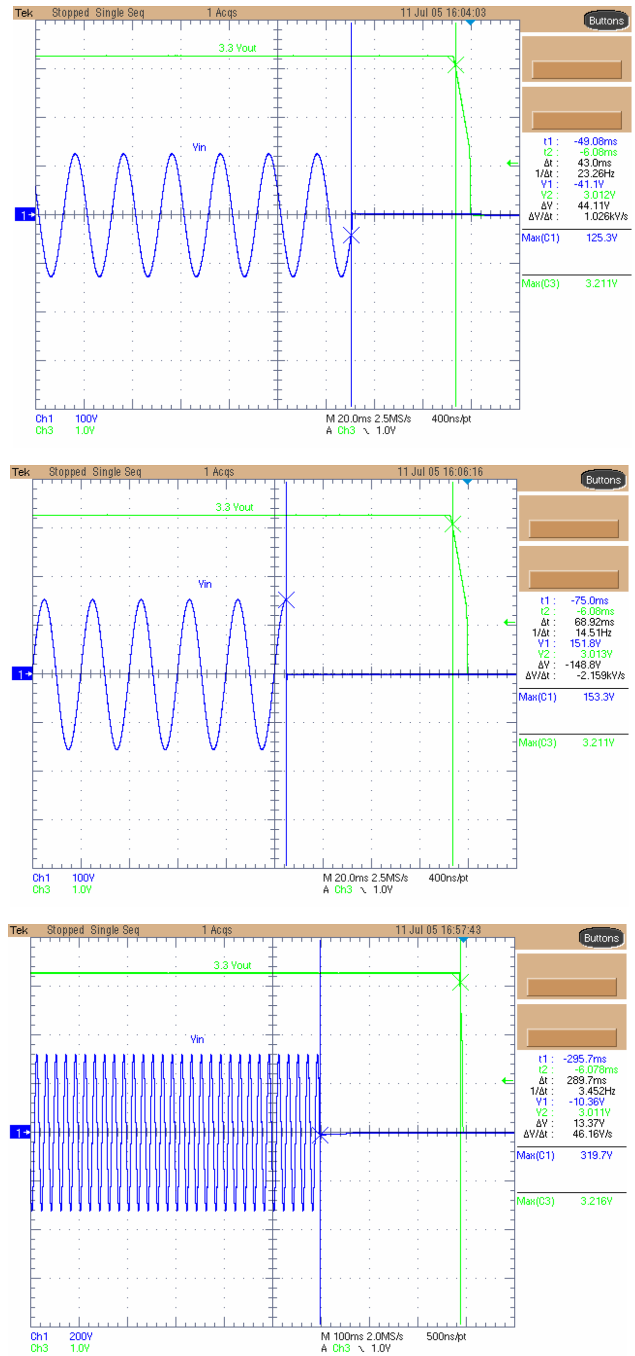


As shown in the previous pictures, the board has a line and a load regulation of +/- 0.1%.

3.4 Hold-up Time Capability

As listed in the specification table, the power supply has to guarantee at least 40mS of hold-up in any line and load condition, in order to allow the STPM01 to safely store data in the memory. As shown in *Figure 12.* the SMPS is compliant with the given specification.

Figure 12. Hold-up Time Capability at FULL LOAD



Vin = 90 Vrms - 50Hz

Vin = 110 Vrms - 50Hz

Vin = 300 Vrms - 50Hz

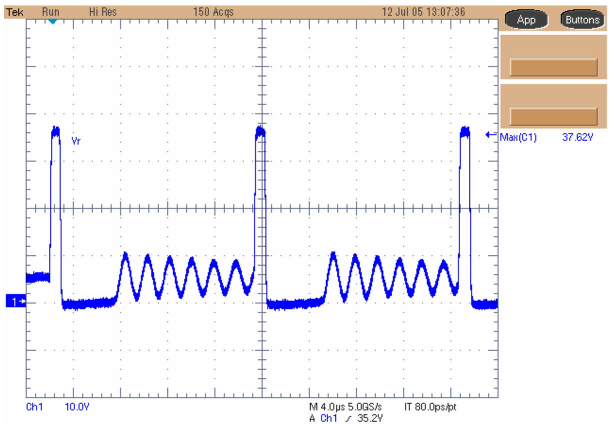
CH1: INPUT VOLTAGE (Blue)
CH3: 3.3V OUTPUT (Green)

The hold-up time capability is shown. At the minimum input voltage, which is the worst condition, the measured time is 43ms.

3.5 Additional Considerations

Thanks to the voltage limiting circuit, the maximum voltage on the drain of the VIPer is well below its maximum absolute rating, getting rid of the clamper circuit. Also the reverse voltage across the output diode is kept low allowing the use of a low voltage diode, i.e. 80V.

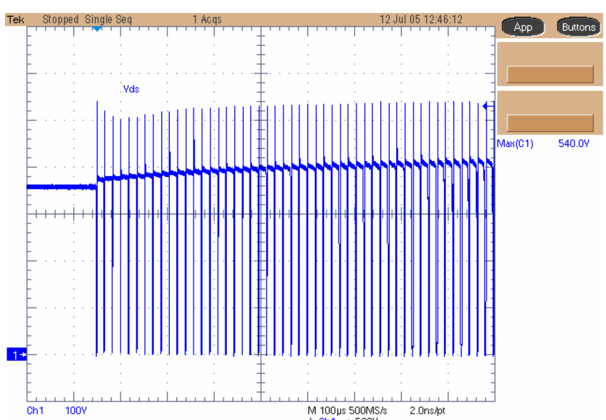
Figure 13. Waveforms



Vin = 300 Vrms - 50Hz at FULL LOAD OUTPUT DIODE REVERSE VOLTAGE

CH1: OUTPUT DIODE VOLTAGE (Blue)

The peak reverse voltage of the diode has been measured during the worst operating condition and it is indicated on the right of the picture. The margin against the maximum value is good enough to ensure the diode reliability.



Vin = 300 Vrms - 50Hz at FULL LOAD VIPer12AS Vds at Start-up

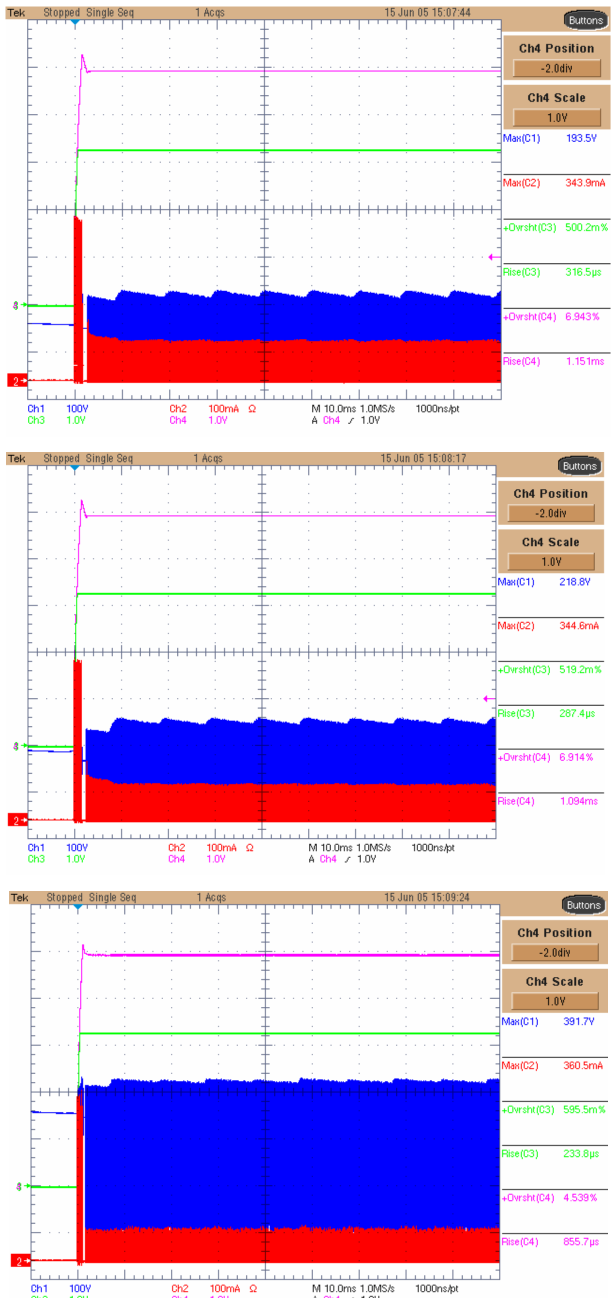
CH1: VIPer12AS DRAIN VOLTAGE (Blue)

The picture gives the measurement of the peak drain voltage (540V) at the start up with 300Vac input voltage in full load condition. Thanks to the good coupling of the transformer, the measured value has a good margin against the maximum BVDSS, avoiding the clamping circuit and improving the cost effectiveness of the solution.

3.6 Measurements At The Start-Up

In this section the typical waveforms during the start-up of the power supply are given. In particular, the full load condition is considered since it represents the heaviest case in terms of voltage and current stress, as well as the minimum load condition for loop stability and voltage stress.

Figure 14. VIPer12AS and Outputs-Start-up at FULL LOAD



Vin = 90 Vrms - 50Hz

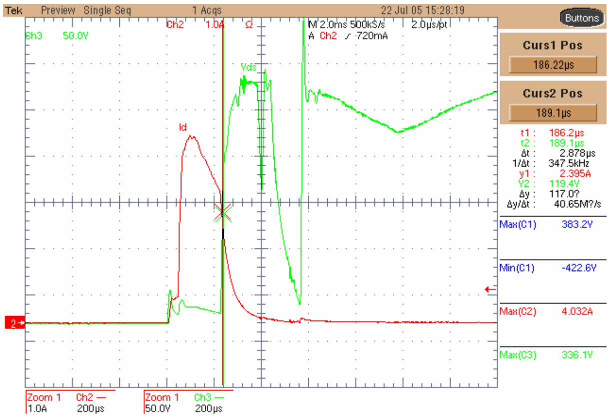
Vin = 110 Vrms - 50Hz

Vin = 230 Vrms - 50Hz

Vin (Vac)	Vdsmax(V)	Idpk(mA)
90	193.5	343.9
110	218.8	344.6
230	391	360.5

CH1: VIPer12AS DRAIN VOLTAGE (Blue)
CH2: VIPer12AS DRAIN CURRENT (Red)
CH3: 3.3V OUTPUT (Green); CH4: 5V OUTPUT (Magenta)

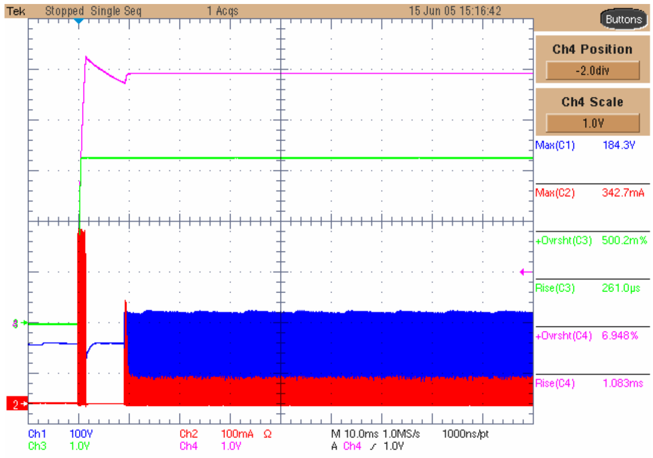
Figure 15. STD3NK50Z-1 Start-up at FULL LOAD



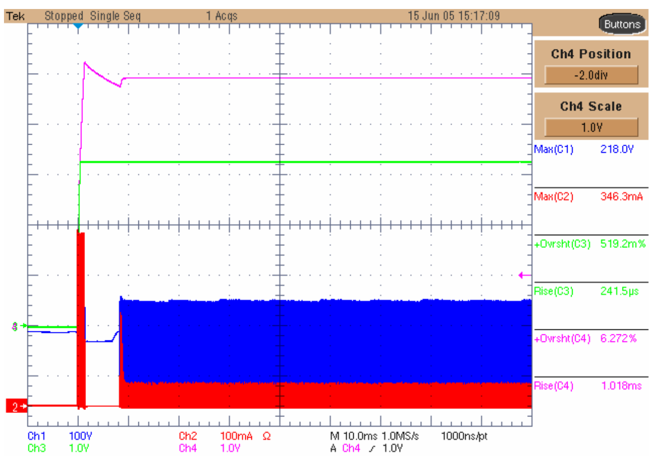
CH2: STD3NK50Z DRAIN CURRENT (Red)
CH3: STD3NK50Z DRAIN VOLTAGE (Green)

The picture gives the measurement of the input MOSFET peak drain current at the worst condition. (450Vac-full load). The cross point between the drain voltage and the drain current (120V-2.4A) is inside the safe operating area of the device.

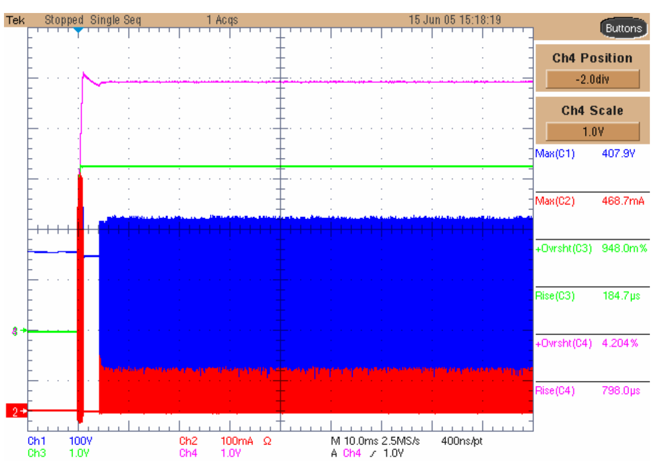
Figure 16. Start-up at MINIMUM LOAD



Vin = 90 Vrms - 50Hz



Vin = 110 Vrms - 50Hz



Vin = 230 Vrms - 50Hz

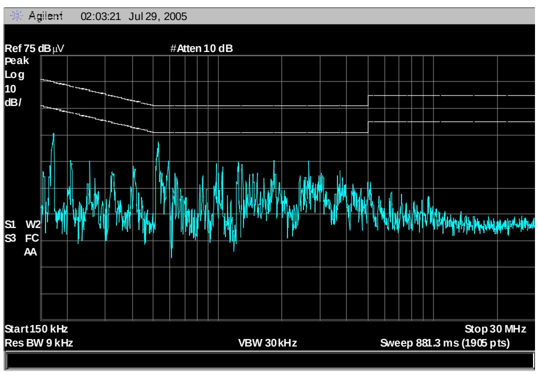
Vin (Vac)	Vdsmax(V)	Idpk(mA)
90	184.3	342.7
110	218	346.3
230	407.9	468.7

CH1: VIPer12AS DRAIN VOLTAGE (Blue)
CH2: VIPer12AS DRAIN CURRENT (Red)
CH3: 3.3V OUTPUT (Green)
CH4: 5V OUTPUT (Magenta)

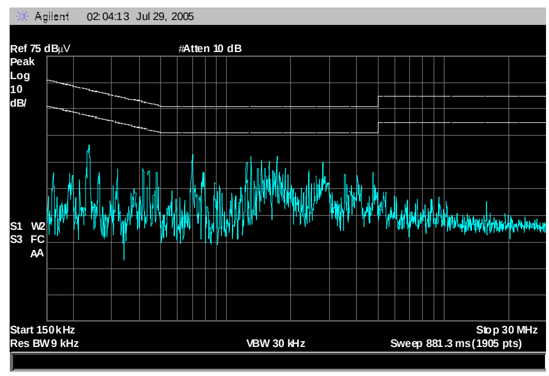
4 Conducted Emissions Test

Conducted emissions have been measured in neutral and lines wires, using peak detector and considering the EN55022 limits. The measurements have been performed at nominal values of the input voltage, i.e. 230Vac and 380Vac, and fully loaded outputs. The results are shown in *Figure 17.* Since the emission level is below both the Quasi-Peak and Average limits with acceptable margin, the power supply passes the pre-compliance test.

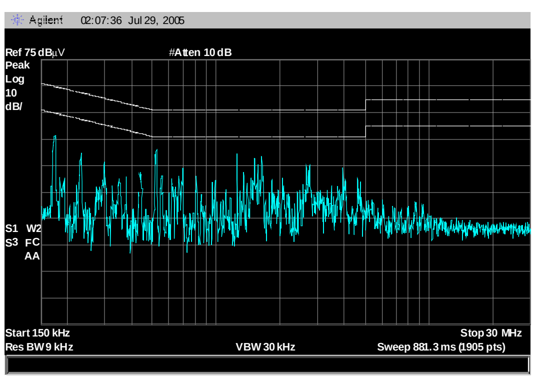
Figure 17. Conducted Emissions - at Vin=230Vac - FULL LOAD



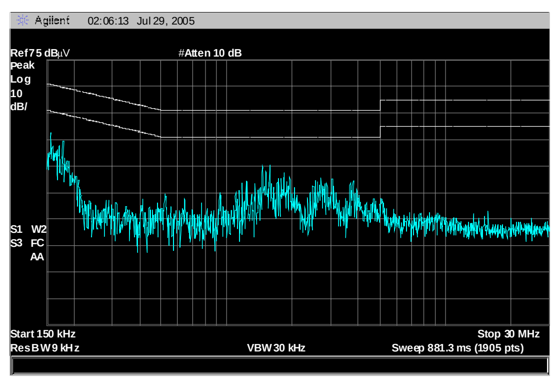
Phase L1-Peak Detector



Phase L2- Peak Detector



Phase L3- Peak Detector

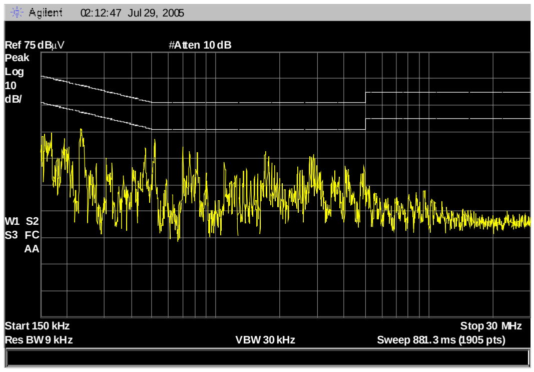


Phase N- Peak Detector

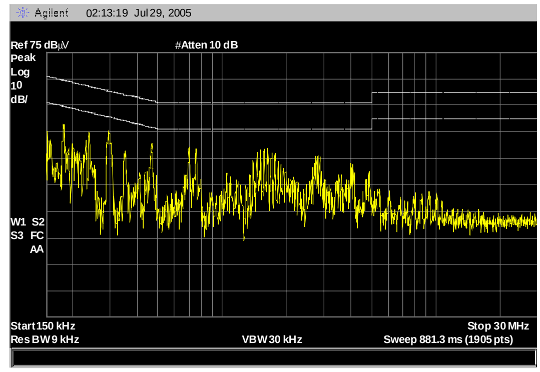
UPPER LIMIT: EN55022BCQP

LOWER LIMIT: EN55022BCAV

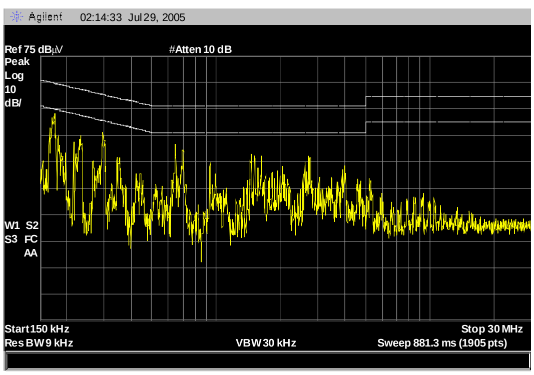
Figure 18. Conducted Emissions - at Vin=380Vac - FULL LOAD



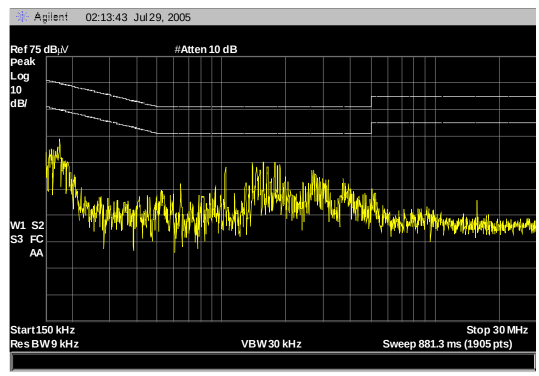
Phase L1 - Peak Detector



Phase L2- Peak Detector



Phase L3 - Peak Detector



Phase N - Peak Detector

UPPER LIMIT: EN55022BCQP

LOWER LIMIT: EN55022BCAV

5 Thermal Measurements

In order to check the reliability of the design, a thermal mapping by means of an IR camera has been done. Here below the thermal measurements on both sides of the board, at minimum, nominal, and maximum input voltage, at ambient temperature (27 °C) are shown.

Pointers 1-3 have been placed across some key components, which could affect the reliability of the circuit, which are:

- **TOP SIDE**

  - PowerMOS - Q1

  - Transformer- T1

- **SMD COMPONENTS SIDE**

  - VIPer12AS - U1

  - +5V diode - D6

  - +3.3V regulator - U2

As shown in the thermal maps, all the other points of the board are within the temperature limits, assuring reliable operation of the devices.

In fact, the highest temperature values have been measured on the MOSFET Q1, the VIPer12A and the 3.3V regulator, while for the transformer the maximum temperature rise is around 15° C.

Figure 19. Thermal Measurements

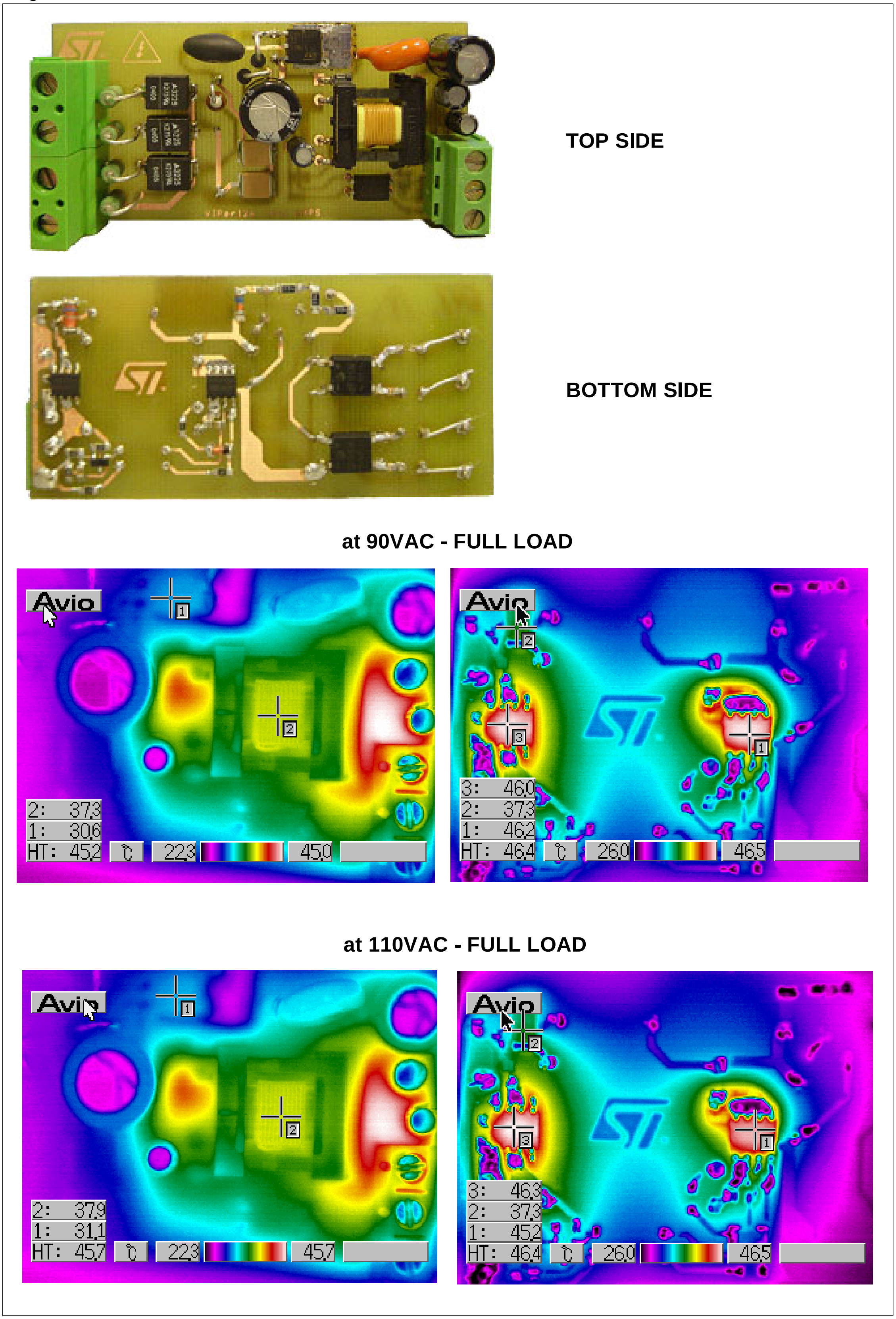
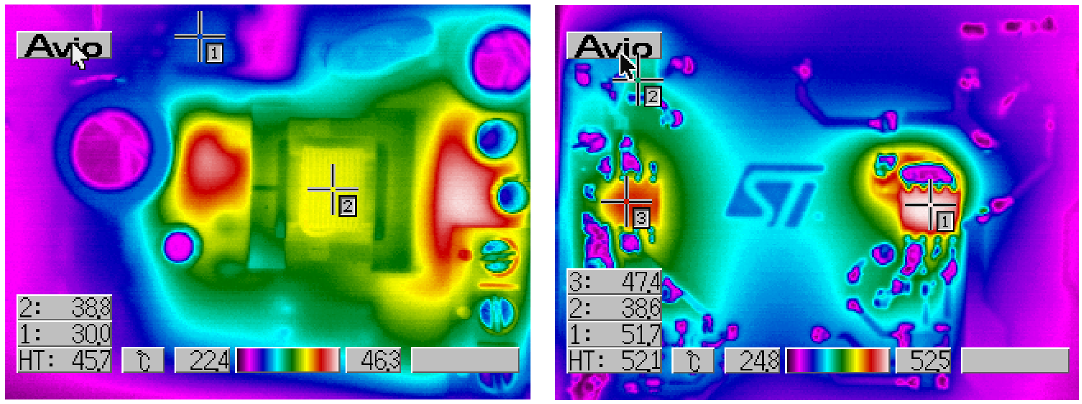
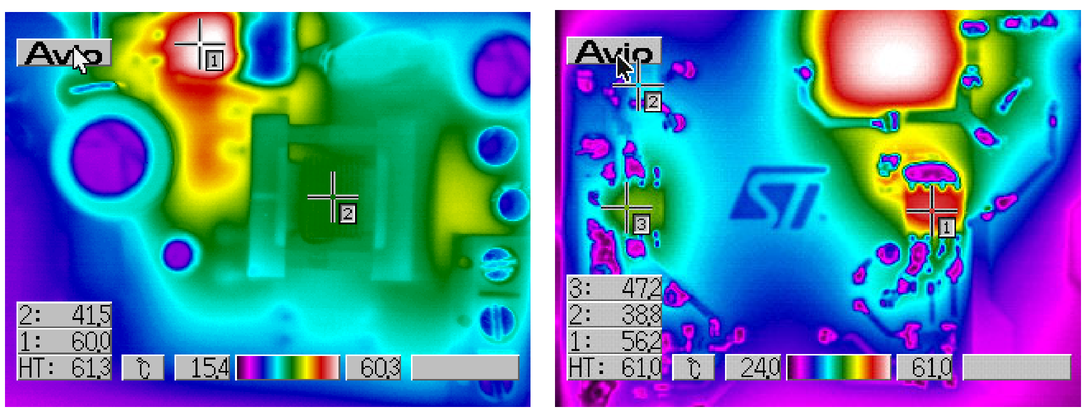


Figure 19. Thermal Measurement (continued)

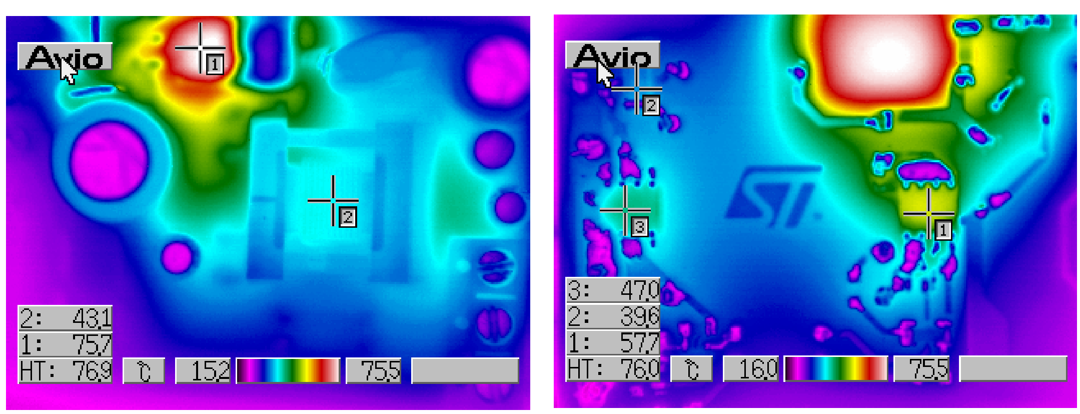
at 230VAC - FULL LOAD



at 380VAC - FULL LOAD



at 450VAC - FULL LOAD



6 Conclusions

In this document an innovative power supply has been introduced and described in order to overcome the very high voltage issue, with an optimum cost-performance trade-off.

In fact, despite the three-phase input voltage up to 450Vac, the design of the power supply has been done using standard components for off-line single-phase applications.

This has been made possible thanks to a simple voltage limiting circuit (STMicroelectronics patent pending) which always ensures no more than 400V on the DC bus. The proposed solution has been specifically developed for electronic metering applications and can be used in any low power (<5W) application where the input voltage can be as high as 450Vac or higher.

7 Revision History

Date	Revision	Changes
16-Nov-2005	1.0	First edition