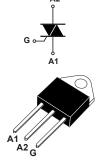


25 A standard Triacs in TOP3 package



TOP3 Insulated

Features

On-state current (I_{T(RMS)}): 25 A

Max. blocking voltage (V_{DRM}/V_{RRM}): 1200 V

Gate current (I_{GT}): 150 mA

Commutation at 10 V/µs: up to 88 A/ms

Noise immunity: 2 kV/µs

Insulated package:

2500 V rms (UL recognized: E81734)

Application



Motor starter

Induction motor speed control



Product status link

TPDV825RG TPDV1025RG

TPDV1225RG

	١
STPOWER	,

Product summary				
I _{T(RMS)}	25 A			
	TPDV825RG: 825 V			
V_{DRM}/V_{RRM}	TPDV1025RG: 1025 V			
	TPDV1225RG: 1225 V			
I _{GT}	150 mA			

Description

The TPDVxx25 series use high performance alternistor technology.

Featuring very high commutation levels and high surge current capability, these devices are well adapted to power control for inductive and resistive loads (motor, transformer...) especially on three-phase power grid. Targeted three-phase applications include heating systems, motor starters, and induction motor speed control (especially for fans).



1 Characteristics

Table 1. Absolute maximum ratings (limiting values)

Symbol	Parameters	Value	Unit			
I _{T(RMS)}	RMS on-state current (180° conduction angle) T _c = 85 °C		RMS on-state current (180° conduction angle)		25	Α
		$t_p = 2.5 \text{ ms}$		390		
I _{TSM}	Non repetitive surge peak on-state current	$t_p = 8.3 \text{ ms}$	T _j = 25 °C	250	Α	
		t _p = 10 ms		230		
I ² t	I ² t value for fusing	t _p = 10 ms	T _j = 25 °C	265	A ² s	
dl/dt	Critical rate of rise of on-state current I_G = 500 mA, dI_G/dt = 1 A/ μ s	Critical rate of rise of on-state current				
		TPDV825		800		
V_{DRM}, V_{RRM}	Repetitive surge peak off-state voltage	TPDV1025	T _j = 125 °C	1000	V	
		TPDV1225		1200		
I _{GM}	Peak gate current		8	Α		
P _{GM}	Peak gate power dissipation	40	W			
V_{GM}	Peak positive gate voltage			16	V	
P _{G(AV)}	Average gate power dissipation	1	W			
T _{stg}	Storage junction temperature range	-40 to +150	°C			
Tj	Operating junction temperature range	-40 to +125	°C			
V _{INS} ⁽¹⁾	Insulation RMS voltage, 1 minute	2500	V			

^{1.} A1, A2, gate terminals to case for 1 minute.

Table 2. Electrical characteristics (T_j = 25 °C, unless otherwise specified)

Symbol	Parameters	Quadrant		Value	Unit	
I _{GT} ⁽¹⁾	V _D = 12 V, R _I = 33 Ω		Max.	150	mA	
V _{GT}	VD - 12 V, NL - 33 12	1 - 11 - 111	Max.	1.5	V	
V_{GD}	$V_D = V_{DRM}, R_L = 3.3 \text{ k}\Omega, T_j = 125 \text{ °C}$	1 - 11 - 111	Min.	0.2	V	
t _{GT}	$V_D = V_{DRM}$, $I_G = 500$ mA, $dI_G/dt = 3$ A/ μ s	1 - 11 - 111	Тур.	2.5	μs	
IH ⁽²⁾	I _T = 500 mA	Тур.	50	mA		
IL	I _G = 1.2 I _{GT}	1 - 111	Тур.	100	mA	
'L	1.2 161	Ш	Тур.	200	ША	
dV/dt ⁽²⁾	$V_D = 67 \% V_{DRM}$ gate open, $T_j = 125 \degree C$	Min.	2000	V/µs		
(dl/dt)c ⁽²⁾	$(dV/dt)c = 200 \text{ V/}\mu\text{s}, T_j = 125 \text{ °C}$ $(dV/dt)c = 10 \text{ V/}\mu\text{s}, T_j = 125 \text{ °C}$			$(dV/dt)c = 200 V/\mu s, T_j = 125 °C$	20	A/ms
(di/dt)C(=)				88	Ailis	

^{1.} Minimum I_{GT} is guaranteed at 5 % of I_{GT} max.

DS7040 - Rev 4 page 2/10

^{2.} For both polarities of A2 referenced to A1



Table 3. Static electrical characteristics

Symbol	Test conditions				Unit
V _{TM} ⁽¹⁾	$I_{TM} = 35 \text{ A}, t_p = 380 \mu\text{s}$	T _j = 25 °C	Max.	1.8	V
V _{TO} ⁽¹⁾	threshold on-state voltage T_j = 125 °C Max				V
R _D ⁽¹⁾	Dynamic resistance $T_j =$		Max.	19	mΩ
I _{DRM} /I _{RRM}	$V_{DRM} = V_{RRM}$	T _j = 25 °C	Max.	20	μA
		T _j = 125 °C	iviax.	8	mA

1. For both polarities of A2 referenced to A1

Table 4. Thermal resistance

Symbol	Parameters	Value	Unit	
P.,	Junction to case (DC)	Max.	1.5	
R _{th(j-c)}	Junction to case (AC) for 360 ° conduction angle (F = 50 Hz)	Max.	1.1	°C/W
R _{th(j-a)}	Junction to ambient	Тур.	50	

DS7040 - Rev 4 page 3/10



1.1 Characteristics (curves)

Figure 1. Max. rms power dissipation versus on-state rms current (F = 50Hz, curves limited by (dl/dt)c)

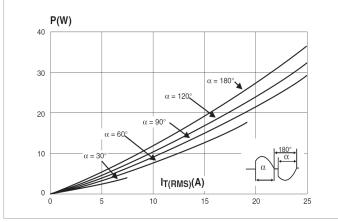


Figure 2. Max. rms power dissipation and max. allowable temperatures (T_{amb} and T_{case}) for various R_{th}

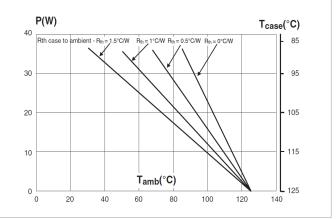


Figure 3. On-state rms current versus case temperature

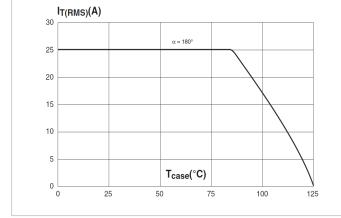


Figure 4. Relative variation of thermal impedance versus pulse duration

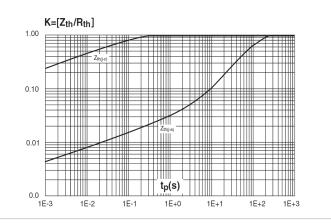


Figure 5. Relative variation of gate trigger current and holding current and latching current versus junction temperature

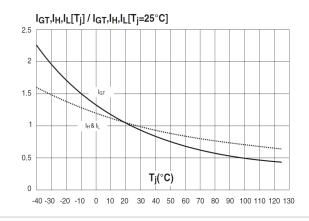
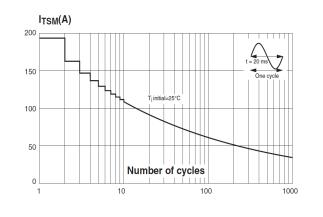


Figure 6. Non-repetitive surge peak on-state current versus number of cycles



DS7040 - Rev 4 page 4/10



Figure 7. Non-repetitive surge peak on-state current for a sinusoidal pulse and corresponding values of I²t

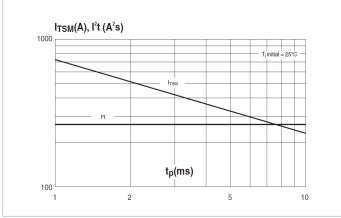


Figure 8. On-state characteristics (maximum values)

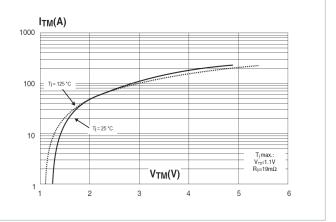
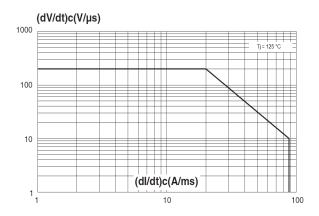


Figure 9. Safe turn-off operating area



DS7040 - Rev 4 page 5/10



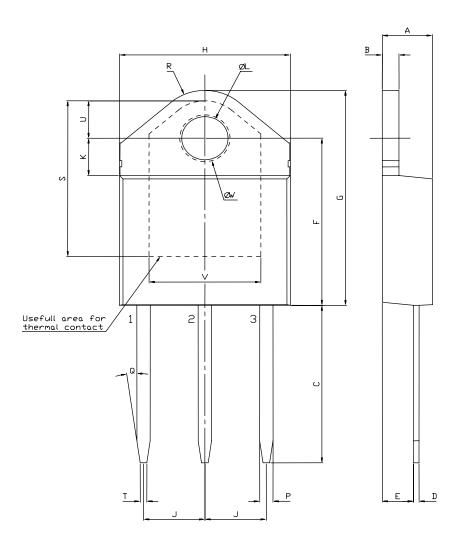
Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 Package information

- ECOPACK (lead-free plating and halogen free package compliance)
- · Lead-free package leads finishing
- Halogen-free molding compound resin meets UL94 standard level V0
- Recommended torque: 1.05 N·m (max. torque: 1.2 N·m)

Figure 10. Package outline



DS7040 - Rev 4 page 6/10



Table 5. Mechanical data

			I	Dimensions		
Ref.		mm			Inches ⁽¹⁾	
	Min.	Тур.	Max.	Min.	Тур.	Max.
А	4.40		4.60	0.1732		0.1811
В	1.45		1.55	0.0571		0.0610
С	14.35		15.60	0.5650		0.6142
D	0.50		0.70	0.0197		0.0276
E	2.70		2.90	0.1063		0.1142
F	15.80		16.50	0.6220		0.6496
G	20.40		21.10	0.8031		0.8307
Н	15.10		15.50	0.5945		0.6102
J	5.40		5.65	0.2126		0.2224
K	3.40		3.65	0.1339		0.1437
L	4.08		4.17	0.1606		0.1642
Р	1.10		1.30	0.0430		0.0510
R		4.60			0.1811	

^{1.} Inches given for reference only

DS7040 - Rev 4 page 7/10



3 Ordering information

Table 6. Ordering information

Order code	Marking	Package	Weight	Base qty.	Delivery mode
TPDV825RG	TPDV825				
TPDV1025RG	TPDV1025	TOP3 Ins.	4.5 g	30	Tube
TPDV1225RG	TPDV1225				

DS7040 - Rev 4 page 8/10



Revision history

Table 7. Document revision history

Date	Revision	Changes
30-Mar-2011	1	First issue.
13-Jan-2012	2	Updated dl/dt in Table 2 and added V_{to} and R_d to Table 3.
06-Oct-2023	3	Updated Section 2.1 Package information.
23-May-2024	4	Updated Table 2.

DS7040 - Rev 4 page 9/10



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DS7040 - Rev 4 page 10/10