UM0488
User manual

Evaluation board with STM32F103Zx MCU

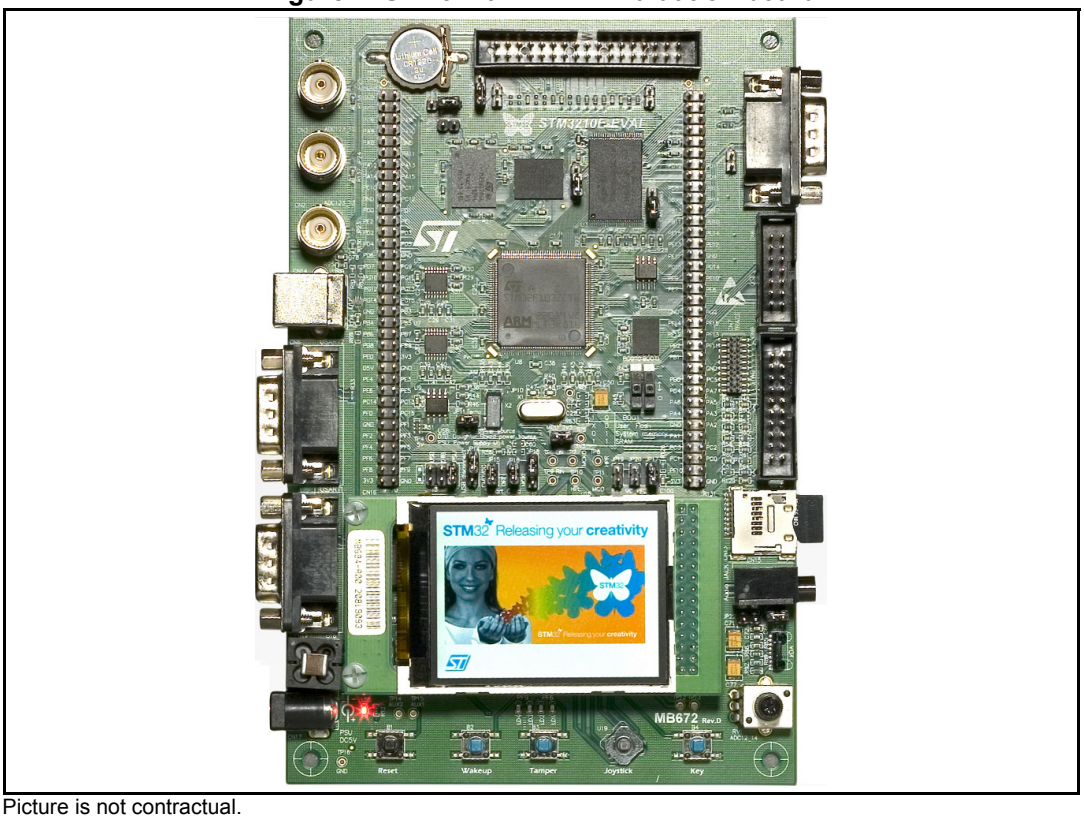
Introduction

The STM3210E-EVAL Evaluation board is a complete development platform for STMicroelectronics Arm® Cortex®-M3 core-based STM32F103ZGT6 microcontroller with full-speed USB 2.0, CAN 2.0 A/B compliant interface, two I^2S channels, two I^2C channels, five USART channels with smartcard support, three SPI channels, two DAC channels, FSMC interface, SDIO, internal 96-Kbyte SRAM and 1-Mbyte flash memory, and JTAG and SWD debug support.

The STM3210E-EVAL products delivered with the MB672 board versions D-03 or older are based on the STM32F103ZET6 instead of the STM32F103ZGT6 and include 64-Kbyte internal SRAM and 512-Kbyte flash memory. The board number and version are on a label on the bottom side of the board.

The full range of hardware features on the board helps the user to evaluate all peripherals (USB, motor control, CAN, microSD™ card, smartcard, USART, NOR and NAND flash memories, SRAM) and develop his applications. Extension headers make it easy to connect a daughterboard or wire-wrap board for his specific application.

Figure 1. STM3210E-EVAL Evaluation board



Picture is not contractual.

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1 Features

- STM32F103ZGT6 Arm®(a) Cortex®-M3 core-based microcontroller with 1 Mbyte of flash memory and 96 Kbytes of SRAM, in a 144-pin TQFP package
- 240 x 320.pixel TFT color LCD
- I^2S audio DAC, with stereo output
- Both A- and B-type smartcard support
- IrDA transceiver
- 512 Kx16 SRAM, 64- or 128-Mbit serial, 512-Mbit or 1-Gbit NAND, and 128-Mbit NOR flash memories
- I^2C/SMBus compatible serial interface with temperature sensor
- RTC with backup battery
- 4 color LEDs
- Reset, wakeup, tamper, and user push-buttons
- 4-way joystick with selection
- Board connectors:
  - 5V power jack
  - USB 2.0 FS Type-B
  - Two RS-232 channels with RTS/CTS handshake support on one channel
  - Stereo audio jack
  - Three ADC inputs
  - CAN 2.0 A/B compliant
  - Smartcard socket
  - microSD™ card holder with 128-Mbyte card
  - Coin-battery cell holder for power backup
  - JTAG and ETM trace debugger connector
  - Motor-control interface
  - Extension headers for daughterboard or wire-wrap board
- Three 5 V power supply options: power jack, USB connector, or daughterboard

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2 Ordering information

To order the STM3210E-EVAL Evaluation board, refer to *Table 1*. Additional information is available from the datasheet and reference manual of the target microcontroller.

Table 1. Ordering information

Order code	Board references	Target STM32
STM3210E-EVAL	MB672(1) MB895(2)	STM32F103ZET6(3)
		STM32F103ZGT6(4)

1. Mother board
2. LCD daughterboard
3. For MB672 mother board version D-03 and older
4. For MB672 mother board newer than version D-03

3 Development environment

3.1 System requirements

- Multi.OS support: Windows® 10, Linux® (a) 64-bit, or macOS® (b)
- USB Type-A or USB Type-C® to Type-B cable

3.2 Development toolchains

- IAR Systems - IAR Embedded Workbench® (c)
- Keil® - MDK-ARM(c)
- STMicroelectronics - STM32CubeIDE

4 Conventions

Table 2 defines some conventions used in the present document.

Table 2. ON/OFF conventions

Convention	Definition
Jumper JPx ON	Jumper fitted
Jumper JPx OFF	Jumper not fitted
Jumper JPx [1-2]	Jumper fitted between Pin 1 and Pin 2
Solder bridge SBx ON	SBx connections closed by 0 Ω resistor
Solder bridge SBx OFF	SBx connections left open
Resistor Rx ON	Resistor soldered
Resistor Rx OFF	Resistor not soldered
Capacitor Cx ON	Capacitor soldered
Capacitor Cx OFF	Capacitor not soldered

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c. On Windows® only.

5 Hardware layout and configuration

The STM3210E-EVAL Evaluation board is designed around the STM32F103ZGT6 microcontroller in a 144-pin TQFP package. The hardware block diagram in *Figure 2* illustrates the connections between the STM32F103ZGT6 and peripherals (LCD, SPI flash, USART, IrDA, USB, audio, CAN bus, smartcard, microSD™ card, NOR flash, NAND flash, SRAM, temperature sensor, audio DAC, and motor control) and *Figure 3* helps to locate these features on the actual Evaluation board.

Figure 2. Hardware block diagram

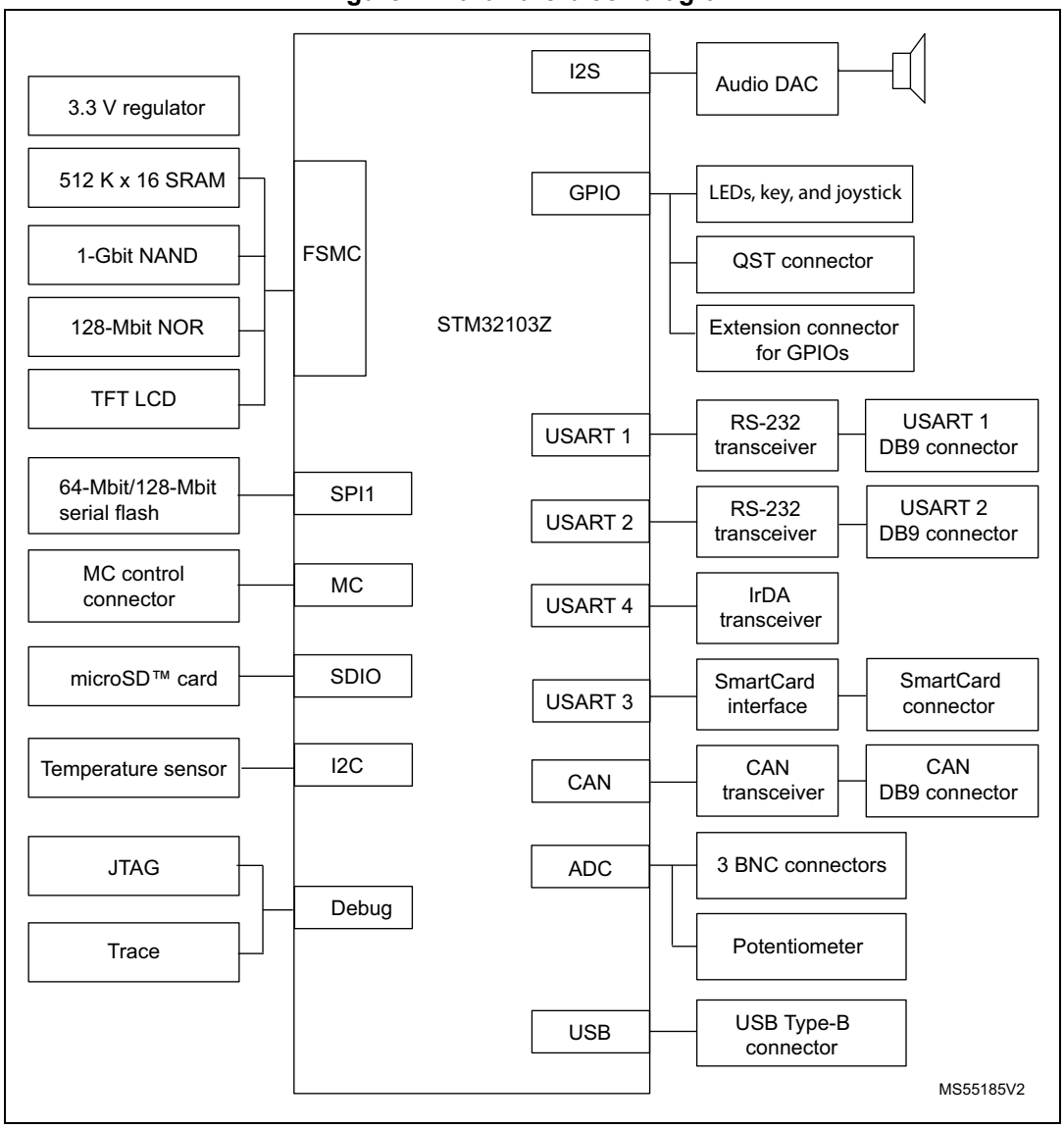
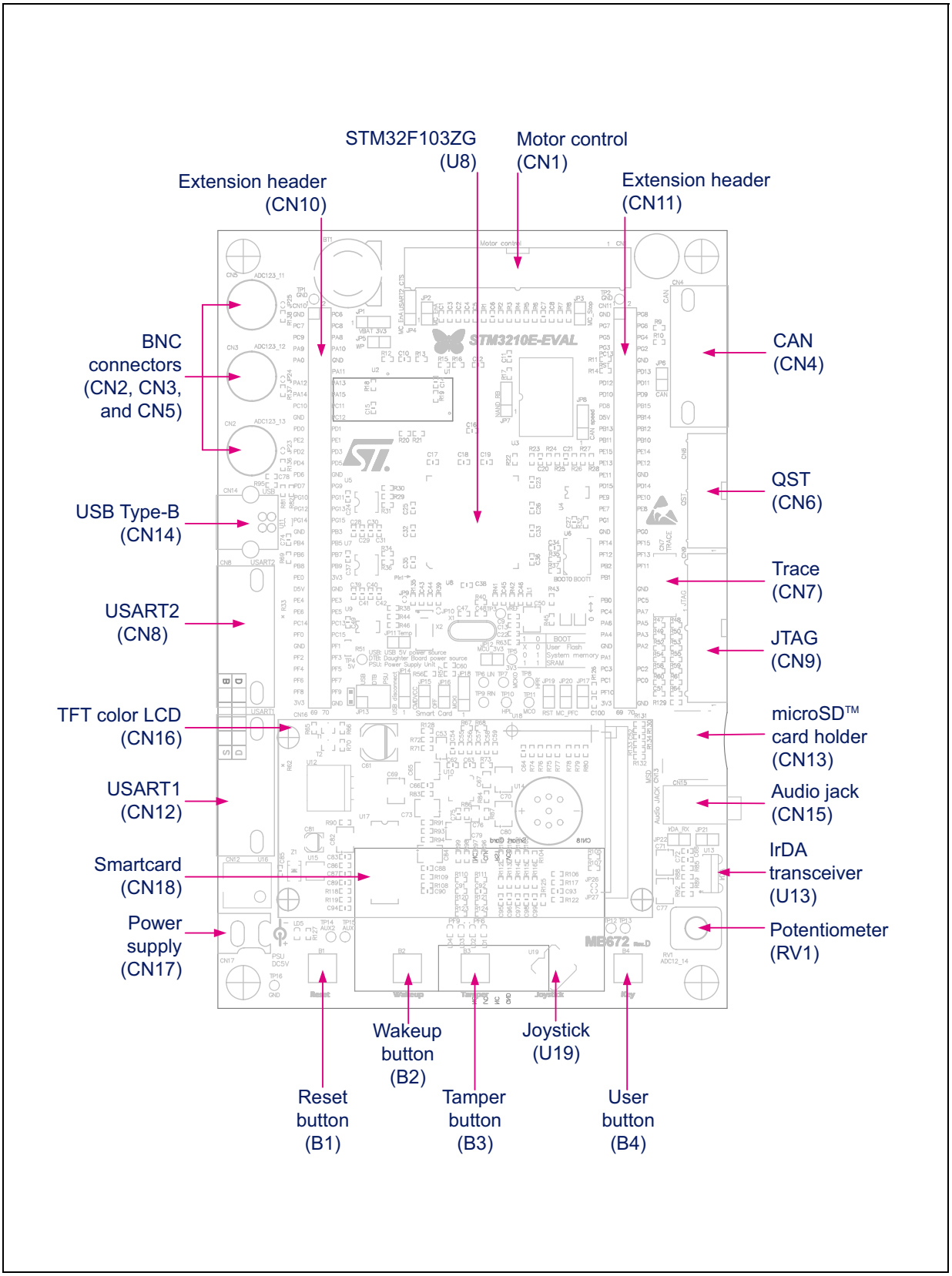


Figure 3. STM3210E-EVAL Evaluation board layout



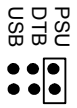
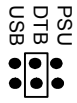
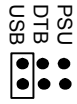
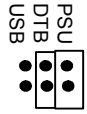
5.1 Power supply

The STM3210E-EVAL Evaluation board is designed to be powered by a 5 V DC power supply and to be protected by PolyZen (U15) in the event of a wrong power plug-in. It is possible to configure the Evaluation board to use any of the following three sources for the power supply:

- 5V DC power adapter connected to the power jack on the board (CN17 - PSU on silk screen for power supply unit).
- 5V DC power with 500 mA limitation from the USB Type-B connector (CN14 - USB on silkscreen).
- 5V DC power from the two extension headers for the daughterboard (CN10 and CN11 - DTB for daughterboard on the silkscreen).

The power supply is configured by setting the related jumpers (JP13, JP12, and JP1) as described in *Table 3*. The LED LD5 is lit when the STM3210E-EVAL Evaluation board is powered correctly.

Table 3. Power related jumpers

Jumper	Description	
JP13	**JP13 is used to select one of the three possible power supply resources. For the power supply jack (CN17) to the STM3210E-EVAL only, JP13 is set as shown (Default setting).**	
	For the power supply from the daughterboard connectors (CN10 and CN11) to STM3210E-EVAL only, JP13 is set as shown.	
	For the power supply from USB (CN14) to STM3210E-EVAL only, JP13 is set as shown.	
	For the power supply from the power supply jack (CN17) to both STM3210E-EVAL and daughterboard connected to CN10 and CN11, JP13 is set as shown (The daughterboard must not have its power supply connected).	
JP12	**Enables consumption measurements of both VDD and VDDA. The default setting is ON**	
JP1	**Vbat is connected to 3.3 V power when JP1 is set as shown (Default setting).**	
	Vbat is connected to the battery when JP1 is set as shown.	

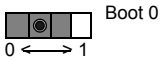
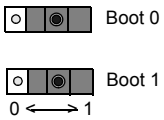
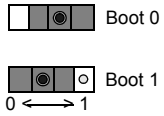
5.2 Boot option

The STM3210E-EVAL Evaluation board can boot from:

- Embedded user flash
- System memory with boot loader for ISP
- Embedded SRAM for debugging

The boot option is configured by setting BOOT0 and BOOT1 switches.

Table 4. Boot related switches (Boot0 and BOOT1)

Switch	Boot from	Switch configuration
BOOT0 BOOT1	STM3210E-EVAL boots from **User flash** when BOOT0 is set as shown to the right. BOOT1 is not required in this configuration. (Default setting)	
	STM3210E-EVAL boot from **Embedded SRAM** when BOOT0 and BOOT1 are set as shown to the right.	
	STM3210E-EVAL boot from **System Memory** when BOOT0 and BOOT1 are set as shown to the right.	

5.3 Clock source

Two clock sources are available on the STM3210E-EVAL Evaluation board for STM32F103 and RTC.

- X2, 32KHz crystal for embedded RTC.
- X1, 8MHz crystal with its socket for STM32F103ZGT6 microcontroller, it can be removed from the socket when the internal RC clock is used.

5.4 Reset source

The reset signal of the STM3210E-EVAL Evaluation board is active LOW and the reset sources include:

- Reset button B1
- Debugging tools from the JTAG (CN7) and trace (CN9) connectors
- Daughterboard from CN11

Table 5. Reset related jumper

Jumper	Description
JP19	Enables reset of the STM32F103ZGT6 embedded JTAG TAP controller each time a system reset occurs. JP19 connects the TRST signal from the JTAG connection with the system reset signal RESET#. **The default setting is OFF**.

5.5 Audio

The STM3210E-EVAL Evaluation board supports stereo audio play because it provides an audio DAC connected to both the I^2S port and two channels of DAC of the STM32F103ZGT6 microcontroller. Either external slave mode or PLL slave mode (BICK or LRCK reference clock) of audio DAC can be used by setting the JP18 jumper.

The I2S_MCK is multiplexed with smartcard and motor control and can be enabled by setting the JP15 jumper. Refer to *Section 5.9: Motor control* for details. Audio DAC is in power-down mode when the PDN pin is pulled down by PG11.

Table 6. Audio related jumpers

Jumper	Description	
JP18	**External slave mode (MCK from STM32F103ZGT6) is selected when JP18 is set as shown (Default setting)**.	
	PLL slave mode (BICK or LRCK reference clock) is selected when JP18 is set as shown.	

5.6 Serial flash

A 64 or 128 Mbit serial flash connected to SPI1 of STM32F103ZGT6 serial flash chip select is managed by IO-pin PB2. The SPI1_MISO is multiplexed with motor control, it can be enabled by setting the JP3 jumper. Refer to *Section 5.9: Motor control* for details.

5.7 CAN

The STM3210E-EVAL Evaluation board supports CAN 2.0 A/B compliant CAN-bus communication based on a 3.3 V CAN transceiver. High-speed mode, standby mode, and slope control mode are available and can be selected by setting the JP8 jumper.

Table 7. CAN related jumpers

Jumper	Description	
JP8	CAN transceiver works in standby mode when JP8 is set as shown.	
	CAN transceiver works in high-speed mode when JP8 is set as shown (Default setting).	
	CAN transceiver works in slope-control mode when JP8 is OFF.	
JP6	CAN terminal resistor is enabled when JP6 is ON. **The default setting is OFF.**	

5.8 RS-232 connectors

USART1 (CN12) and USART2 (CN8) D-type 9-pin connectors are available on the STM3210E-EVAL Evaluation board.

- The USART1 connector is connected to the U7 RS-232 transceiver.
- The USART2 connector with RTS/CTS handshake signal support is connected to the U5 RS-232 transceiver. The USART2_CTS is multiplexed with motor control, it can be enabled by setting the JP4 jumper. Refer to *Section 5.9: Motor control* for details.

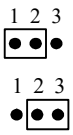
5.9 Motor control

The STM3210E-EVAL Evaluation board supports three-phase brushless motor control via the 34-pin connector (CN1), which provides all required control and feedback signals to and from the motor power driving board. Available signals on this connector include emergency stop, motor speed, three-phase motor current, bus voltage, heatsink temperature from the motor driving board, and 6 channels of PWM control signals going to the motor driving circuit.

The JP20 jumper selects one of the two synchronization methods for power factor correction (PFC).

The I/O pins used on the motor-control connector (CN1) are multiplexed with some peripherals on the board; either the motor-control connector or multiplexed peripherals can be enabled by setting the jumpers JP3, JP4, JP11, JP15, and JP16 as described in *Table 8*.

Table 8. Motor-control related jumpers

Jumper	Description	Multiplexed peripherals
JP20	JP20 allows to have a PFC synchronization signal redirected to the timer 3 input capture 1 pin, and additionally to the timer 3 external trigger input. JTAG debugging is disabled when JP20 is ON. **The default setting is OFF.**	
JP2	JP2 must be kept OFF when the encoder signal is input from pin 31 of CN1 while it must be kept ON when an analog signal is from pin 31 of CN1 for a special motor. **The default setting is OFF.**	
JP3	MC_EmergencySTOP is enabled when JP3 is ON. The pin PA6 is used as SPI1_MISO when JP3 is OFF. **The default setting is OFF.**	SPI1
JP4	**MC_EnA is enabled when JP4 is set as shown on the right (Default setting)**: USART2_CTS is enabled when JP4 is set as shown on the right: 	USART2
JP11	MC_PFCpwm is enabled when JP11 is OFF. The pin PB5 will be used as the interrupt input from the temperature sensor when JP11 is ON.	Temperature sensor
JP15	MC_UH or I2S_MCK are enabled when JP15 is OFF. The pin PC6 is used as Smartcard_CMDVCC when JP15 is ON.	I^2S and smartcard
JP16	MC_VH is enabled when JP16 is OFF. The pin PC7 is used as Smartcard_OFF when JP16 is ON.	Smartcard

5.10 Smartcard

The smartcard interface chip is used on the STM3210E-EVAL board for asynchronous 3 and 5 V smartcards. It performs all supply protection and control functions based on the connections with STM32F103ZGT6 listed in *Table 9*.
The Smartcard_CMDVCC and Smartcard_OFF are multiplexed with motor control. They can be enabled by setting JP15 and JP16 jumpers. Refer to *Section 5.9: Motor control on page 15* for details.

Table 9. Connection between the smartcard interface and STM32F103ZGT6

Smartcard interface signals	Description	Connect to STM32F10X
5V/3V	Smartcard power supply selection pin	PB0
I/OUC	MCU data I/O line	PB10
XTAL1	Crystal or external clock input	PB12
OFF	Detect presence of a card, send interrupt to MCU, and share the same pin with motor controller	PC7
RSTIN	Card reset input from MCU	PB11
CMDVCC	Start activation sequence input (Active LOW), share same pin with I^2S DAC and motor control	PC6

Table 10. Smartcard related jumpers (JP15 and JP16)

Jumper	Description
JP15	The CMDVCC is connected to PC6 when JP15 is ON. It must be kept OFF, or the SD card needs to be removed from the microSD™ card holder when PC6 is used by I^2S or the motor-control connector. **The default setting is ON**.
JP16	The OFF is connected to PC7 when JP16 is ON. It must be kept OFF when PC7 is used by the motor-control connector. **The default setting is ON**.

5.11 microSD™ card

The 128-Mbyte microSD™ card connected to the SDIO of STM32F103ZGT6 is available on the board. The microSD™ card detection is managed by standard IO port PF11.
The MicroSDcard_D3 signal is multiplexed with IrDA. It can be enabled by setting the JP22 jumper, as explained in *Section 5.14: IrDA on page 17*.
The MicroSDcard_D0 and microSD™ card CMD are multiplexed with the motor-control connector. They can be enabled by setting JP17 and JP20 jumpers.

Table 11. microSD™ card related jumpers (JP17 and JP20)

Jumper	Description
JP17	JP17 is used to enable microSD™ card data line D0 when JP17 is ON. JP17 must be kept OFF when the motor-control connector (CN1) is used. **The default setting is ON.**
JP20	JP20 is used by the motor control connector, refer to *Table 8* for details. JP20 must be kept OFF for microSD™ card operation. JTAG debugging is disabled when JP20 is ON.

5.12 Temperature sensor

One I^2C interface temperature sensor connected to the I^2C interface of STM32F103ZGT6 is available on the board.

5.13 Analog input

The three BNC connectors (CN2, CN3, and CN5) are respectively connected to PC3, PC2, and PC1 of the STM32F103ZGT6 as external analog inputs. The 50-Ω terminal resistor can be enabled by closing the solder bridges (JP23, JP24, and JP25) for each BNC connector. A low-pass filter can be implemented for each BNC connector (CN5, CN3, and CN2) by replacing R5 and C22, R4 and C13, and R3 and C9 with the right resistor and capacitor values, depending on the requirements of the application.

5.14 IrDA

IrDA communication is supported by the IrDA transceiver (U13) connected to USART3 of STM32F103ZGT6. The IrDA transceiver can be enabled or disabled by the JP21 jumper.

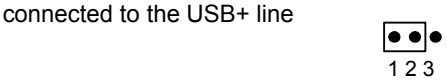
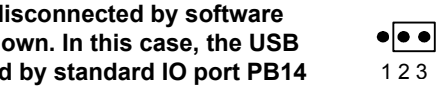
Table 12. IrDA related jumpers (JP21 and JP22)

Jumper	Description
JP21	Enables/disables the IrDA transceiver. **IrDA is enabled when JP21 is ON (Default setting).** IrDA is disabled when JP21 is OFF.
JP22	IrDA_RX is enabled when JP22 is ON. **I/O pin PC11 is data line 3 of the microSD™ card when JP22 is OFF (Default setting).**

5.15 USB

The STM3210E-EVAL Evaluation board supports USB 2.0 compliant full-speed communication via a USB Type-B connector (CN14). The Evaluation board can be powered by this USB connection at 5 V DC with a 500 mA current limitation. USB disconnection simulation can be implemented by disconnecting the 1.5 K pull-up resistor from the USB+ line. The USB disconnection simulation feature is enabled by setting the JP14 jumper.

Table 13. USB related jumper (JP14)

Jumper	Description	
JP14	The USB 1.5K pull-up resistor is always connected to the USB+ line when JP14 is set as shown.	 1 2 3
	The USB 1.5K pull-up resistor can be disconnected by software from USB+ line when JP14 is set as shown. In this case, the USB connect/disconnect feature is managed by standard IO port PB14 (Default setting).	 1 2 3

5.16 Development and debug support

The two debug connectors available on the STM3210E-EVAL Evaluation board are:

- The standard 20-pin JTAG interface connector (CN9), which is compliant with ARM7/9 debug tools.
- The 20-pin connector for both SWD and trace (CN7), which is compliant with Arm® CoreSight™ debug tools.

5.17 Display and input devices

The 240x320 TFT color LCD connected to bank1 NOR/PSRAM4 of the FSMC interface of the STM32F103ZGT6 and four general-purpose color LEDs (LD 1,2,3,4) are available as display devices. A 4-direction joystick with a selection key, general-purpose button (B4), wakeup button (B2) and tamper detection button (B3) are available as input devices. The JP4 jumper must be kept OFF to enable the wakeup button (B2) which shares the same I/O with USART2 and the motor-control connector.

The STM3210E-EVAL Evaluation board also supports a second optional 122x32 graphic LCD that can be mounted on the U18 connector. By default, the graphic LCD is not present.

Table 14. LCD modules

TFT LCD (CN16) (Default)			Graphic LCD (U18) (Optional)		
CN16 pin	**Description**	**Pin connection**	**U18 pin**	**Description**	**Pin connection**
1	CS	CS of Bank3 of FSMC	1	Vss	GND
2	RS	FSMC_A0	2	Vcc	3.3V
3	WR/SCL	FSMC_NWE	3	VO	-
4	RD	FSMC_NOE	4	CLK	PA5
5	RESET	RESET#	5	SID	PA7
6	PD1	FSMC_D0	6	CS	PF10
7	PD2	FSMC_D1	7	A	+5V
8	PD3	FSMC_D2	8	K	GND
9	PD4	FSMC_D3	-	-	-

Table 14. LCD modules (continued)

TFT LCD (CN16) (Default)			Graphic LCD (U18) (Optional)		
CN16 pin	Description	Pin connection	U18 pin	Description	Pin connection
10	PD5	FSMC_D4	-	-	-
11	PD6	FSMC_D5	-	-	-
12	PD7	FSMC_D6	-	-	-
13	PD8	FSMC_D7	-	-	-
14	PD10	FSMC_D8	-	-	-
15	PD11	FSMC_D9	-	-	-
16	PD12	FSMC_D10	-	-	-
17	PD13	FSMC_D11	-	-	-
18	PD14	FSMC_D12	-	-	-
19	PD15	FSMC_D13	-	-	-
20	PD16	FSMC_D14	-	-	-
21	PD17	FSMC_D15	-	-	-
22	BL_GND	GND	-	-	-
23	BL_control	3.3V	-	-	-
24	VDD	3.3V	-	-	-
25	VCI	3.3V	-	-	-
26	GND	GND	-	-	-
27	GND	GND	-	-	-
28	BL_VDD	3.3V	-	-	-
29	SDO	PA6 via JP26	-	-	-
30	SDI	PA7 via JP27	-	-	-

5.18 SRAM

512Kx16 SRAM is connected to bank1 NOR/PSRAM3 of the FSMC interface and both 8-bit and 16-bit access are allowed by BLN0 and BLN1 connected to BLE and BHE of SRAM respectively.

5.19 NAND flash

The 512 Mbit x8 or 1 Gbit x8 NAND flash is connected to bank2 of the FSMC interface. The ready/busy signal can be connected to either the WAIT signal or the FSMC_INT2 signal of the STM32F103ZGT6 depending on the setting of the JP7 jumper.

Table 15. NAND flash related jumper (JP7)

Jumper	Description
JP7	**The ready/busy signal is connected to the WAIT signal when JP7 is set as shown (Default setting)**  The ready/busy signal is connected to the FSMC_INT2 signal when JP7 is set as shown. 

5.20 NOR flash

128 Mbit NOR flash is connected to bank1 NOR/PSRAM2 of the FSMC interface. The 16-bit operation mode is selected by a pull-up resistor connected to the BYTE pin of the NOR flash. Write protection can be enabled or disabled by the JP5 jumper.

Table 16. NOR flash related jumper (JP5)

Jumper	Description
JP5	Write protection is enabled when JP5 is ON. **Write protection is disabled when JP5 is OFF (Default setting).**

Three different NOR 128-Mbit references can be present on the Evaluation board depending on component availability.

Table 17. NOR flash reference

Reference	Manufacturer	Status
M29W128GL70ZA6E	Micron (Numonyx)	Obsolete
M29W128GH70ZA6E	Micron (Numonyx)	Obsolete
S29GL128P90FFIR20	Spansion	Active

These three references are not identical in terms of ID code, speed, timing, or block protection. The demonstration firmware and the software library delivered with the board support these three NOR flash references. However, during the development of the application software, the user must verify which NOR reference is implemented on his board (The component referenced as U2 on silkscreen and schematic), and take its characteristics into account.

6 Connectors

6.1 Motor-control connector (CN1)

Figure 4. Motor-control connector (CN1) (Top view)

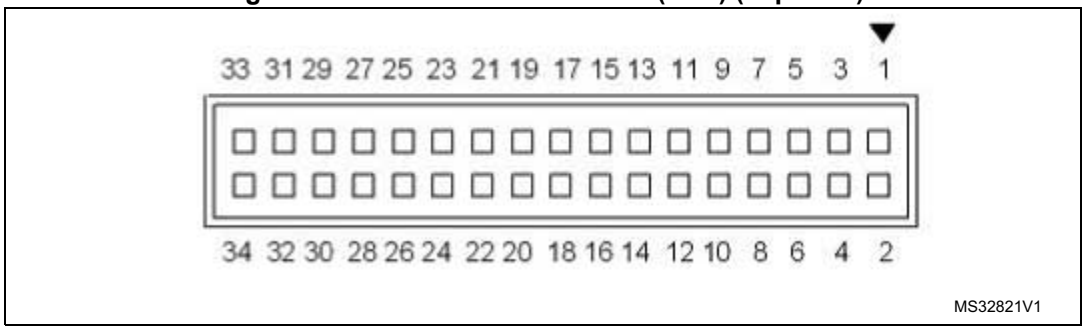


Table 18. Motor-control connector (CN1)

Description	STM32F103ZGT6 pin	CN1 pin#	CN1 pin#	STM32F103ZGT6 pin	Description
Emergency stop	PA6	1	2		GND
PWM-UH	PC6	3	4		GND
PWM-UL	PA7	5	6		GND
PWM-VH	PC7	7	8		GND
PWM-VL	PB0	9	10		GND
PWM-WH	PC8	11	12		GND
PWM-WL	PB1	13	14	PC0	Bus voltage
Phase A current	PC1	15	16		GND
Phase B current	PC2	17	18		GND
Phase C current	PC3	19	20		GND
NTC bypass relay	PB12	21	22		GND
Dissipative brake PWM	PA3 through 0-Ω resistor OFF	23	24		GND
+5V power	+5V	25	26	PC5	Heatsink temperature
PFC SYNC	PB4 and PD2	27	28		3.3V power
PFC PWM	PB5	29	30		GND
Encoder A	PA0	31	32		GND
Encoder B	PA1	33	34	PA2	Encoder index

6.2 Analog input connectors (CN2, CN3, and CN5)

Figure 5. Analog input connectors (CN2, CN3, and CN5) (Bottom view)

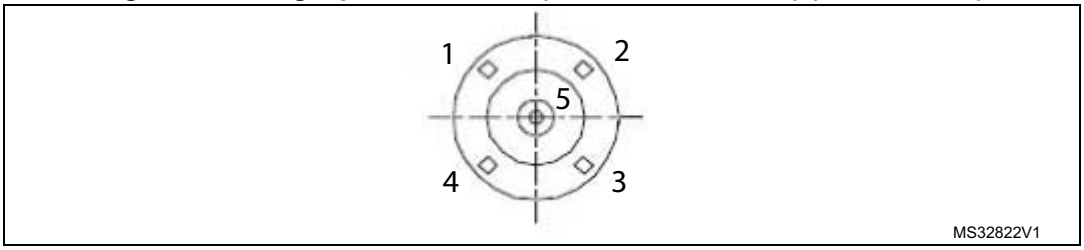


Table 19. Analog input connectors (CN2, CN3, and CN5)

Pin number	Description	Pin number	Description
1	GND	4	GND
2	GND	5	Analog input PC3, PC2, and PC1 for CN2, CN3, and CN5 respectively
3	GND		

6.3 CAN D-type 9-pin male connector (CN4)

Figure 6. CAN D-type 9-pin male connector (CN4) (Front view)

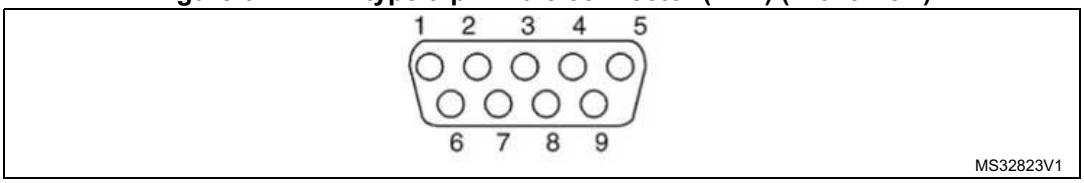


Table 20. CAN D-type 9-pins male connector (CN4)

Pin number	Description	Pin number	Description
1,4,8,9	NC	7	CANH
2	CANL	3,5,6	GND

6.4 QST connector (CN6)

The QST connector connects the STM3210E-EVAL to the QST Evaluation board to demonstrate the QST function.

Figure 7. QST connector (CN6) (Front view)

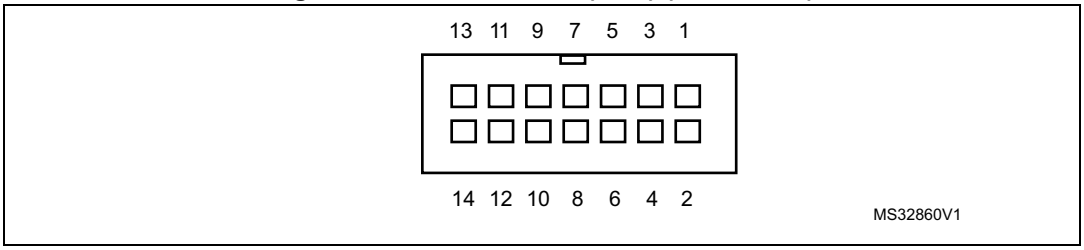


Table 21. QST connector (CN6)

Pin number	Description	Pin number	Description
1	+5V	2	+5V
3	PB6	4	PA5
5	PB7	6	PA7
7	PB1	8	PA6
9	PF11	10	PB5
11	PA8	12	-
13	GND	14	GND

6.5 Trace debugging connector (CN7)

Figure 8. ETM trace debugging connector (CN7) (Top view)

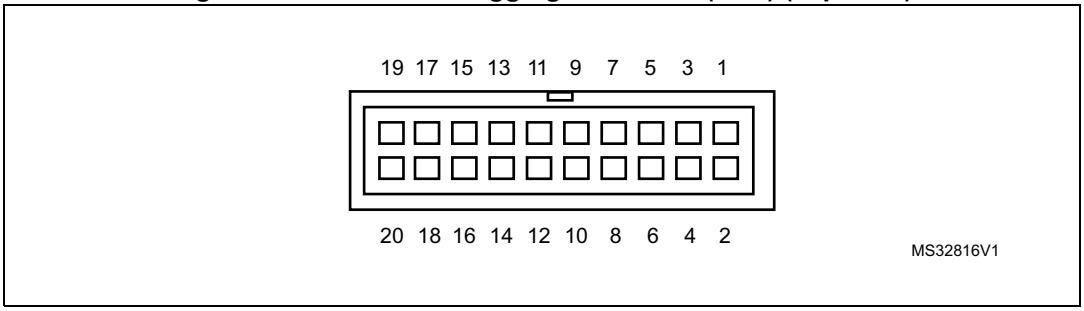


Table 22. ETM trace debugging connector (CN7)

Pin number	Description	Pin number	Description
1	3.3V power	2	TMS/PA13
3	GND	4	TCK/PA14
5	GND	6	TDO/PB3
7	KEY	8	TDI/PA15
9	GND	10	RESET#
11	GND	12	TraceCLK/PE2
13	GND	14	TraceD0/PE3 or SWO/PB3
15	GND	16	TraceD1/PE4 or nTRST/PB4
17	GND	18	TraceD2/PE5
19	GND	20	TraceD3/PE6

6.6 RS-232 connector with RTS/CTS handshake support (CN8)

Figure 9. RS-232 connector with RTS/CTS handshake support (CN8) (Front view)

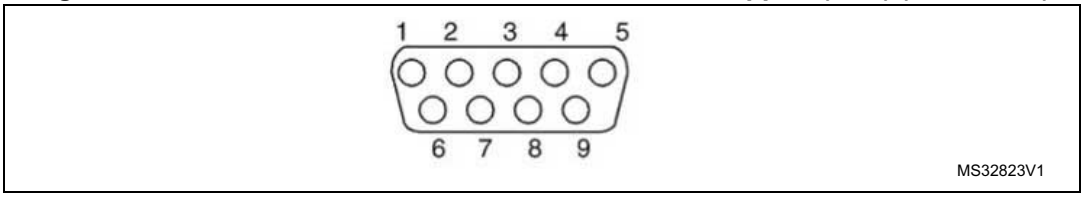


Table 23. RS-232 connector with RTS/CTS handshake support (CN8)

Pin number	Description	Pin number	Description
1	NC	6	Connect to Pin 4
2	USART2_PA3	7	USART2_PA1
3	USART2_PA2	8	USART2_PA0
4	Connect to Pin 6	9	NC
5	GND		

6.7 JTAG debugging connector (CN9)

Figure 10. JTAG debugging connector (CN9) (Top view)

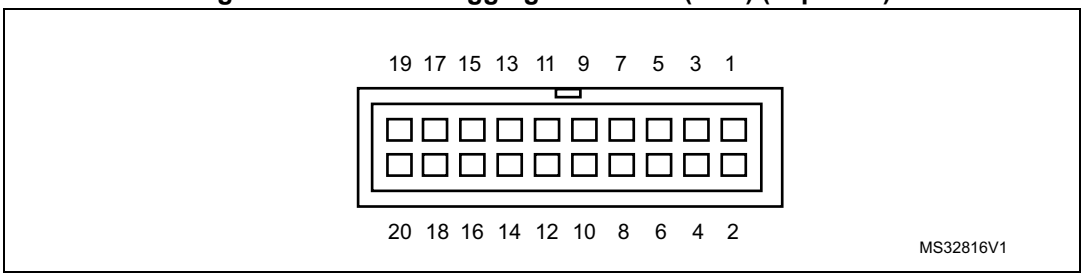


Table 24. JTAG debugging connector (CN9)

Pin number	Description	Pin number	Description
1	3.3V power	2	3.3V power
3	PB4	4	GND
5	PA15	6	GND
7	PA13	8	GND
9	PA14	10	GND
11	RTCK	12	GND
13	PB3	14	GND
15	RESET#	16	GND
17	DBGRQ	18	GND
19	DBGACK	20	GND

6.8 Daughterboard extension headers (CN10 and CN11)

Two 70-pin male headers (CN10 and CN11) can be used to connect a daughterboard or standard wrapping board to the STM3210E-EVAL Evaluation board. A total of 112 GPI/Os is available on it. The space between these two connectors and the position of power, GND and RESET pins (Marked in gray in *Table 25* and *Table 26*) are defined as a standard that allows the development of common daughterboards for several Evaluation boards. The standard width between CN10 pin1 and CN11 pin1 is 2700 mils (68.58 mm). This standard is implemented on the majority of Evaluation boards.

Each pin on CN10 and CN11 can be used by a daughterboard after disconnecting it from the corresponding function block on the STM3210E-EVAL Evaluation board, as described in *Table 25* and *Table 26*.

Table 25. Daughterboard extension header (CN10)

Pin #	Description	Alternative function	How to disconnect from function block on STM3210E-EVAL board
1	GND	-	-
3	PC7	MC/Smartcard	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Keep JP16 OFF.
5	PC9	microSD™ card	Remove the SD card from the microSD™ card holder.
7	PA9	UASRT1_TX	-
9	PA0	MC/Wakeup/USART2_CTS	Keep JP4 OFF.
11	-	-	-
13	PA12	USB_DP	Remove R82.
15	PA14	Debug_TCK	-
17	PC10	IrDA_TX/MicroSDcard_D2	Remove the SD card from the microSD™ card holder.
19	GND	-	-
21	PD0	FSMC_D2	-
23	PE2	Trace_CLK/FSMC_A23	-
25	PD2	MicroSDcard_CMD/MC	Disconnect the STM3210E-EVAL Evaluation board from motor-power drive board. Remove the SD card from the microSD™ card holder.
27	PD4	FSMC_OEN	-
29	PD6	FSMC_WAITN	-
31	PD7	FSMC_EBAR0	Remove R22.
33	PG10	FSMC_EBAR2	Remove R15.
35	PG12	FSMC_EBAR3	Remove R77.
37	PG14	Joystick_Left	Remove R102.
39	GND	-	-

Table 25. Daughterboard extension header (CN10) (continued)

Pin #	Description	Alternative function	How to disconnect from function block on STM3210E-EVAL board
41	PB4	Debug_TRST/MC	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Keep JP19 OFF.
43	PB6	I2C_SCL/QST	Disconnect the STM3210E-EVAL Evaluation board from the QST board.
45	PB8	CAN_RX	Remove R32.
47	PE0	FSMC_BLN0	-
49	D5V	-	-
51	PE4	Trace_D1/FSMC_A20	-
53	PE6	Trace_D3/FSMC_A22	-
55	PC14	OSC32_IN	Remove R135 and keep the JP9 jumper ON.
57	PF0	FSMC_A0	-
59	GND	-	-
61	PF2	FSMC_A2	-
63	PF4	FSMC_A4	-
65	PF6	LD2	Remove R96.
67	PF8	LD4	Remove R98.
69	+3V3	-	-
2	PC6	Smartcard/MC/I2S_MCK	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Keep JP15 OFF.
4	PC8	MicroSDcard_D0/MC	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Remove the SD card from the microSD™ card holder.
6	PA8	MCO/LCD_backlight/QST	Disconnect the STM3210E-EVAL Evaluation board from the QST board.
8	PA10	USART1_RX	Remove R36.
10	GND	-	-
12	PA11	USB_DM	Remove R81.
14	PA13	Debug TMS	-
16	PA15	Debug TDI	-
18	PC11	IrDA_RX/MicroSDcard_D2	Remove the SD card from the microSD™ card holder. Remove R89.
20	PC12	MicroSDcard_CLK	Remove the SD card from the microSD™ card holder.
22	PD1	FSMC_D3	-
24	PE1	FSMC_BLN1	-
26	PD3	Joystick_Down	Remove R100.

Table 25. Daughterboard extension header (CN10) (continued)

Pin #	Description	Alternative function	How to disconnect from function block on STM3210E-EVAL board
28	PD5	FSMC_WEN	-
30	GND	-	-
32	PG9	FSMC_EBAR1	Remove R21.
34	PG11	-	-
36	PG13	Joystick_Right	Remove R103.
38	PG15	Joystick_Up	Remove R104.
40	PB3	Debug_TDO	-
42	PB5	MC/QST/Temperature sensor	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive and QST boards. Remove R46.
44	PB7	I2C_SDA/QST	Disconnect the STM3210E-EVAL Evaluation board from the QST board.
46	PB9	CAN_TX	-
48	3V3	-	-
50	GND	-	-
52	PE3	Trace_D0/FSMC_A19	-
54	PE5	Trace_D2/FSMC_A21	-
56	PC13	Anti-tamper button	Remove R111.
58	PC15	OSC32_OUT	Remove R39 and keep the JP10 jumper ON.
60	PF1	FSMC_A1	-
62	PF3	FSMC_A3	-
64	PF5	FSMC_A5	-
66	PF7	LD3	Remove R97.
68	PF9	LD5	Remove R99.
70	GND	-	-

Table 26. Daughterboard extension header (CN11)

Pin #	Description	Alternative function	How to disconnect from function block on STM3210E-EVAL board
1	GND	-	-
3	PG7	Joystick_Select	Remove R101.
5	PG5	FSMC_A15	-
7	PG3	FSMC_A13	-
9	PC13 Button B3	-	-
11	RESET#	-	-
13	PD12	FSMC_A17	-
15	PD10	FSMC_D15	-
17	PD8	FSMC_D13	-
19	D5V	-	-
21	PB13	I2S_CLK	-
23	PB11	Smartcard_Reset	-
25	PE15	FSMC_D12	-
27	PE13	FSMC_D10	-
29	PE11	FSMC_D8	-
31	PD15	FSMC_D1	-
33	PE9	FSMC_D6	-
35	PE7	FSMC_D4	-
37	PG1	FSMC_A11	-
39	GND	-	-
41	PF14	FSMC_A8	-
43	PF12	FSMC_A6	-
45	PB2	BOOT1/SPI_NSS	-
47	PB1	MC/QST	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive and QST boards.
49	-	-	-
51	PB0	Smartcard_3/5V/MC	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board.
53	PC4	Potentiometer	Remove R126.
55	PA6	MC/SPI_MISO/QST	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive and QST boards. Remove R37.
57	PA4	Audio_RIN	Remove R67.
59	GND	-	-

Table 26. Daughterboard extension header (CN11) (continued)

Pin #	Description	Alternative function	How to disconnect from function block on STM3210E-EVAL board
61	PA1	MC/USART2_RTS	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board.
63	PC3	MC/BNC3	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Disconnect the analog signal from BNC3.
65	PC1	MC/BNC1	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Disconnect the analog signal from BNC1.
67	PF10	LCD_CS	-
69	+3V3	-	-
2	PG8	User button B4	Remove R106.
4	PG6	FSMC_INT2	Keep JP7 OFF.
6	PG4	FSMC_A14	-
8	PG2	FSMC_A12	-
10	GND	-	-
12	PD13	FSMC_A18	-
14	PD11	FSMC_A16	-
16	PD9	FSMC_A14	-
18	PB15	I2S_DIN	-
20	PB14	USB disconnect	Connect pin1 of JP14 to pin2.
22	PB12	Smartcard_CK/MC/I2S_CMD	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board.
24	PB10	Smartcard_IO	Remove R94.
26	PE14	FSMC_D11	-
28	PE12	FSMC_D9	-
30	GND	-	-
32	PD14	FSMC_D0	-
34	PE10	FSMC_D7	-
36	PE8	FSMC_D5	-
38	-	-	-
40	PG0	FSMC_A10	-
42	PF15	FSMC_A9	-
44	PF13	FSMC_A7	-
46	PF11	QST/microSD™ card detection	Disconnect the STM3210E-EVAL Evaluation board from the QST board. Remove the SD card from the card holder (CN13).
48	-	-	-

Table 26. Daughterboard extension header (CN11) (continued)

Pin #	Description	Alternative function	How to disconnect from function block on STM3210E-EVAL board
50	GND	-	-
52	PC5	MC	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board.
54	PA7	MC/SPI_MOSI/QST	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive and QST boards.
56	PA5	SPI_CLK/DAC_LIN/QST	Disconnect the STM3210E-EVAL Evaluation board from the QST board. Remove R68.
58	PA3	MC/USART2_RX	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Remove R29.
60	PA2	MC/USART2_TX	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board.
62	-	-	-
64	PC2	MC/BNC2	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Disconnect the analog signal from BNC2.
66	PC0	MC	Disconnect the STM3210E-EVAL Evaluation board from the motor-power drive board. Remove C7 and R63.
68	-	-	-
70	GND	-	-

6.9 RS-232 connector (CN12)

Figure 11. RS-232 connector (Front view) (CN12)

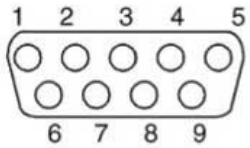


Table 27. RS-232 connector (CN12)

Pin number	Description	Pin number	Description
1	NC	6	Connect to Pin 4
2	USART1_PA10	7	Connect to Pin 8
3	USART1_PA9	8	Connect to Pin 7
4	Connect to Pin 6	9	NC
5	GND		

6.10 microSD™ card holder (CN13)

Figure 12. microSD™ card holder (CN13) (Front view)

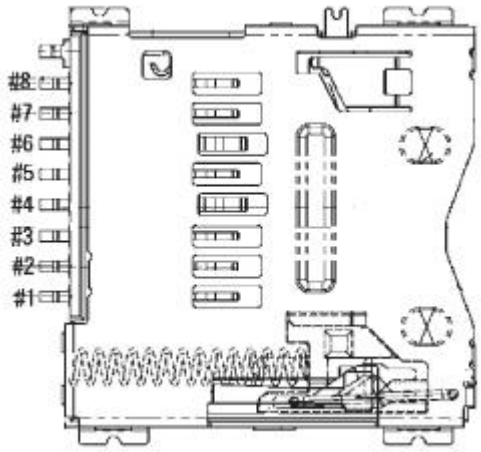


Table 28. microSD™ card holder (CN13)

Pin number	Description	Pin number	Description
1	MicroSDcard_D2 (PC10)	5	MicroSDcard_CLK (PC12)
2	MicroSDcard_D3 (PC11)	6	Vss/GND
3	MicroSDcard_CMD (PD2)	7	MicroSDcard_D0 (PC8)
4	+3V3	8	MicroSDcard_D1 (PC9)
-	-	9	MicroSDcard_detect (PF11)

6.11 USB Type-B connector (CN14)

Figure 13. USB Type-B connector (CN14) (Top view)

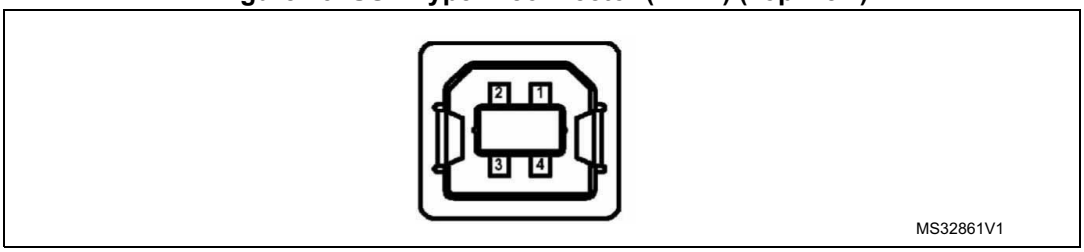


Table 29. USB Type-B connector (CN14)

Pin number	Description	Pin number	Description
1	VBUS (Power)	4	GND
2	PA11	5,6	Shield
3	PA12	-	-

6.12 Audio jack (CN15)

A 3.5 mm stereo audio jack (CN15) connected to the audio DAC is available on the STM3210E-EVAL board.

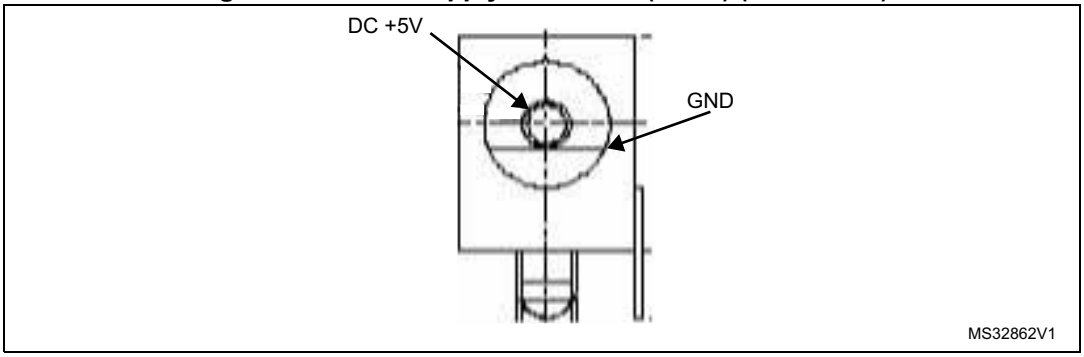
6.13 TFT LCD connector (CN16)

One 30-pin male header is available on the board to connect the LCD module board MB895 to the FSMC interface of the STM32F103ZGT6. Refer to *Section 5.17: Display and input devices on page 18* for details.

6.14 Power connector (CN17)

The STM3210E-EVAL board can be powered from a DC 5 V power supply via the external power supply jack (CN17) shown in *Figure 14*. The central pin of CN17 must be positive.

Figure 14. Power supply connector (CN17) (Front view)



6.15 Smartcard connector (CN18)

Figure 15. Smartcard connector (CN18) (Front view)

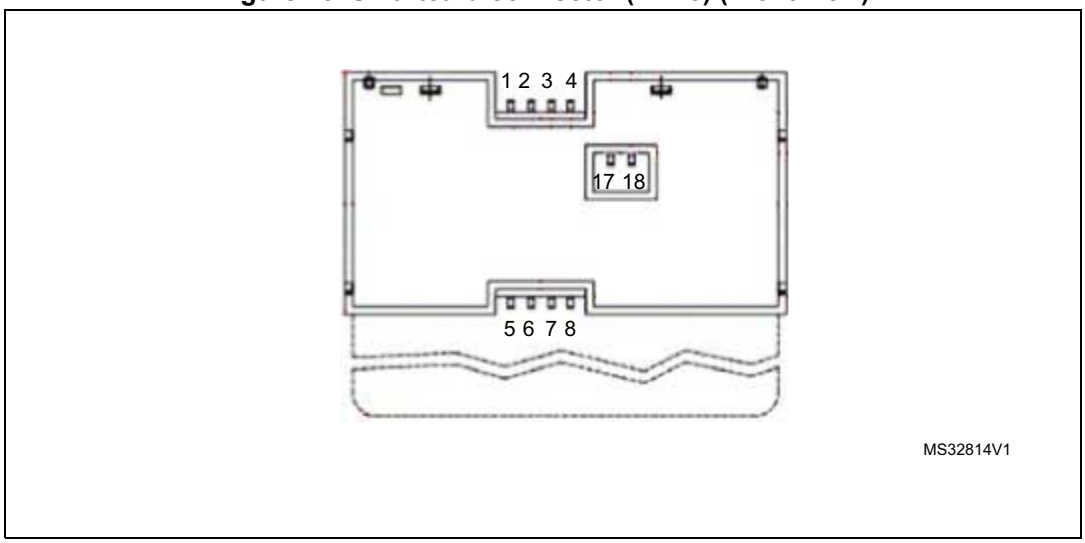


Table 30. Smartcard connector (CN18)

Pin number	Description	Pin number	Description
1	VCC	5	GND
2	RST	6	NC
3	CLK	7	I/O
4	NC	8	NC
17	Detection pin of card presence	18	Detection pin of card presence

7 STM3210E-EVAL I/O assignment

Table 31. STM3210E-EVAL I/O assignment

Pin #	Pin name	STM3210E-EVAL I/O assignment
1	PE2	Trace_CLK/FSMCA23
2	PE3	Trace_D0/FSMCA19
3	PE4	Trace_D1/FSMCA20
4	PE5	Trace_D2/FSMCA21
5	PE6	Trace_D3/FSMCA22
6	VBAT	+3V3 or battery
7	PC13-ANTI_TAMP	Anti-tamper button
8	PC14-OSC32_IN	32K OSC
9	PC15-OSC32_OUT	32K OSC
10	PF0	FSMCA0
11	PF1	FSMCA1
12	PF2	FSMCA2
13	PF3	FSMCA3
14	PF4	FSMCA4
15	PF5	FSMCA5
16	VSS_5	GND
17	VDD_5	+3V3
18	PF6	LD2
19	PF7	LD3
20	PF8	LD4
21	PF9	LD5
22	PF10	LCD_CS for graphic LCD (Optional)
23	OSC_IN	8MHz crystal X1
24	OSC_OUT	8MHz crystal X1
25	NRST	Reset button B1
26	PC0	MC_ADC_123_10 pin14 (Bus voltage)
27	PC1	MC_ADC11 pin 15/BNC1
28	PC2	MC_ADC12 pin 17/BNC2
29	PC3	MC_ADC13 pin 19/BNC3
30	VSSA	GND
31	VREF-	GND
32	VREF+	+3V3

Table 31. STM3210E-EVAL I/O assignment (continued)

Pin #	Pin name	STM3210E-EVAL I/O assignment
33	VDDA	+3V3
34	PA0-WKUP	MC_TIM2_CH1 pin 31(Ena)/WAKEUP/USART2 CTS
35	PA1	MC_TIM2_CH2 pin 33 (EnB)/USART2 RTS
36	PA2	MC_TIM2_CH3 pin34 (EnIndex)/USART2 TX
37	PA3	MC_TIM6_CH4 pin 23 (Dissipative brake)/USART2 RX
38	VSS_4	GND
39	VDD_4	+3V3
40	PA4	DAC1_Audio RIN
41	PA5	SPI_Flash_CLK/DAC2_Audio LIN/QST pin4
42	PA6	MC_STOP pin 1 (Emergency stop)/SPI_Flash_MISO/QST pin8
43	PA7	MC_TIM5_CH1N pin 5 (UL)/SPI_Flash_MOSI/QST pin6
44	PC4	Potentiometer
45	PC5	MC_ADC_12_15 pin 26 (Heatsink temperature)
46	PB0	MC_TIM5_CH2N pin 9 (VL)/SmartCard_3/5
47	PB1	MC1_TIM5_CH3N pin 13 (WL)/QST pin7
48	PB2	Boot1/NSS_SPI_Flash
49	PF11	QST pin9/microSD™ card detection
50	PF12	FSMCA6
51	VSS_6	GND
52	VDD_6	+3V3
53	PF13	FSMCA7
54	PF14	FSMCA8
55	PF15	FSMCA9
56	PG0	FSMCA10
57	PG1	FSMCA11
58	PE7	FSMCD4
59	PE8	FSMCD5
60	PE9	FSMCD6
61	VSS_7	GND
62	VDD_7	+3V3
63	PE10	FSMCD7
64	PE11	FSMCD8
65	PE12	FSMCD9
66	PE13	FSMCD10
67	PE14	FSMCD11

Table 31. STM3210E-EVAL I/O assignment (continued)

Pin #	Pin name	STM3210E-EVAL I/O assignment
68	PE15	FSMCD12
69	PB10	Smart_IO
70	PB11	Smart Reset
71	VSS_1	GND
72	VDD_1	+3V3
73	PB12	Smart_CK/MC_pin21 (NTC)/Audio I2S_CMD
74	PB13	Audio I2S_CK
75	PB14	USB Disconnect
76	PB15	Audio I2S_DIN
77	PD8	FSMCD13
78	PD9	FSMCD14
79	PD10	FSMCD15
80	PD11	FSMCA16
81	PD12	FSMCA17
82	PD13	FSMCA18
83	VSS_8	GND
84	VDD_8	+3V3
85	PD14	FSMCD0
86	PD15	FSMCD1
87	PG2	FSMCA12
88	PG3	FSMCA13
89	PG4	FSMCA14
90	PG5	FSMCA15
91	PG6	FSMC_INT2
92	PG7	JOY_Select
93	PG8	User Button B4
94	VSS_9	GND
95	VDD_9	+3V3
96	PC6	MC_TIM5_CH1 pin 3 (UH)/Smart_ CMD/VCC/I2S_MCK
97	PC7	MC_TIM5_CH2 pin 7(VH)/Smartcard_OFF
98	PC8	MC_TIM5_CH3 pin 11 (WH)/microSD™ card D0
99	PC9	microSD™ card D1
100	PA8	MCO/LCD backlight/QST pin11
101	PA9	USART1 TX
102	PA10	USART1 RX

Table 31. STM3210E-EVAL I/O assignment (continued)

Pin #	Pin name	STM3210E-EVAL I/O assignment
103	PA11	USB DM
104	PA12	USB DP
105	PA13	Debug TMS
106	NC	
107	VSS_2	GND
108	VDD_2	+3V3
109	PA14	Debug TCK
110	PA15	Debug TDI
111	PC10	IRDA TX/microSD™ card D2
112	PC11	IRDA RX/microSD™ card D3
113	PC12	microSD™ card CLK
114	PD0	FSMCD2
115	PD1	FSMCD3
116	PD2	microSD™ card CMD/MC1_TIM3_ETR pin 27 (PFCsync2)
117	PD3	JOY_Down
118	PD4	FSMCNOE
119	PD5	FSMCNWE
120	VSS_10	GND
121	VDD_10	+3V3
122	PD6	FSMCNWAIT
123	PD7	FSMCNE1
124	PG9	FSMCNE2
125	PG10	FSMCNE3
126	PG11	PDN of Audio DAC
127	PG12	FSMCEBAR3
128	PG13	JOY_Right
129	PG14	JOY_Left
130	VSS_11	GND
131	VDD_11	+3V3
132	PG15	JOY_Up
133	PB3	Debug TDO
134	PB4	Debug TRST/MC_TIM3_CH1 pin 27 (PFCsync1)
135	PB5	Temperature SMBIA/MC_TIM3_CH2 pin 29 (PFC PWM)/QST pin10
136	PB6	Audio I2C_SCL and temperature SCL/QST pin3
137	PB7	Audio_I2C_SDA and temperature SDA/QST pin5

Table 31. STM3210E-EVAL I/O assignment (continued)

Pin #	Pin name	STM3210E-EVAL I/O assignment
138	BOOT0	BOOT0
139	PB8	CAN RX
140	PB9	CAN TX
141	PE0	FSMCBLN0
142	PE1	FSMCBLN1
143	VSS_3	GND
144	VDD_3	+3V3

8 STM3210E-EVAL Evaluation board information

8.1 Product marking

The stickers located on the top or bottom side of the PCB provide product information:

- Product order code and product identification for the first sticker
- Board reference with revision, and serial number for the second sticker

On the first sticker, the first line provides the product order code, and the second line the product identification.

On the second sticker, the first line has the following format: "MBxxxx-Variant-yzz", where "MBxxxx" is the board reference, "Variant" (optional) identifies the mounting variant when several exist, "y" is the PCB revision and "zz" is the assembly revision, for example B01. The second line shows the board serial number used for traceability.

Evaluation tools marked as "ES" or "E" are not yet qualified and therefore not ready to be used as reference design or in production. Any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering sample tools as reference designs or in production.

"E" or "ES" marking examples of location:

- On the targeted STM32 that is soldered on the board (For an illustration of STM32 marking, refer to the STM32 datasheet "Package information" paragraph at the *www.st.com* website).
- Next to the evaluation tool ordering part number that is stuck or silk-screen printed on the board.

Some boards feature a specific STM32 device version, which allows the operation of any bundled commercial stack/library available. This STM32 device shows a "U" marking option at the end of the standard part number and is not available for sales.

To use the same commercial stack in their applications, the developers may need to purchase a part number specific to this stack/library. The price of those part numbers includes the stack/library royalties.

8.2 STM3210E-EVAL product history

8.2.1 Product identification VA3210E$AY1

This product identification is based on the MB672-F103ZGT6-D06 mother board.

It embeds the STM32F103ZGT6 microcontroller with silicon revision code "A" or "1". The limitations of this silicon revision are detailed in the errata sheet *STM32F101xF/G and STM32F103xF/G XL-density device limitations* (ES0346).

8.3 STM3210E-EVAL product limitations

8.3.1 Product identification VA3210E$AY1 limitations

No limitation identified for this product identification.

8.4 Board revision history

8.4.1 Board MB672 revision D-03

The revision D-03 of the MB672 board is the first official release with the STM32F103ZET6 microcontroller.

8.4.2 Board MB672 revision D-04

The revision D-04 of the MB672 board is the first official release with the STM32F103ZGT6 microcontroller.

8.4.3 Board MB672 revision D-05

The revision D-05 of the MB672 board corresponds to:

- NAND flash reference changed due to obsolescence.

8.4.4 Board MB672 revision D-06

The revision D-06 of the MB672 board corresponds to:

- Several part references updated due to obsolescence (Such as memory or others, refer to the bill of materials for details).

8.4.5 Board MB895 revision C-03

The revision C-03 of the MB895 board is the initial release.

8.4.6 Board MB895 revision C-04

The revision C-04 of the MB895 board corresponds to:

- Several part references updated due to obsolescence (Such as inductor or others, refer to the bill of materials for details).

8.5 Board known limitations

8.5.1 Board MB672 revision D-03 limitations

No limitation identified for this board revision.

8.5.2 Board MB672 revision D-04 limitations

No limitation identified for this board revision.

8.5.3 Board MB672 revision D-05 limitations

No limitation identified for this board revision.

8.5.4 Board MB672 revision D-06 limitations

No limitation identified for this board revision.

8.5.5 Board MB895 revision C-03 limitations

No limitation identified for this board revision.

8.5.6 Board MB895 revision C-04 limitations

No limitation identified for this board revision.

9 Federal Communications Commission (FCC) and Innovation, Science and Economic Development Canada (ISED) Compliance Statements

9.1 FCC Compliance Statement

9.1.1 Part 15.19

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

9.1.2 Part 15.21

Any changes or modifications to this equipment not expressly approved by STMicroelectronics may cause harmful interference and void the user's authority to operate this equipment.

9.1.3 Part 15.105

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Responsible party (in the USA)

Terry Blanchard
Americas Region Legal | Group Vice President and Regional Legal Counsel, The Americas
STMicroelectronics, Inc.
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9.2 ISED Compliance Statement

This device complies with FCC and ISED Canada RF radiation exposure limits set forth for general population for mobile application (uncontrolled exposure). This device must not be collocated or operating in conjunction with any other antenna or transmitter.

9.2.1 Compliance Statement

Notice: This device complies with ISED Canada licence-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

ISED Canada ICES-003 Compliance Label: CAN ICES-3 (A) / NMB-3 (A).

9.2.2 Déclaration de conformité

Avis: Le présent appareil est conforme aux CNR d'ISDE Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Étiquette de conformité à la NMB-003 d'ISDE Canada : CAN ICES-3 (A) / NMB-3 (A).

Revision history

Table 32. Document revision history

Date	Revision	Changes
5-May-2008	1	Initial release.
2-Jun-2008	2	Added information on NOR flash references in *Section 2.20*. Updated schematics in *Section 4*.
20-Nov-2008	3	Modified cover page. Inserted a new *Chapter 1*. Modified bank specified in *Section 2.17*, *Section 2.18*, *Section 2.19*, and *Section 2.20*.
21-Jan-2010	4	Modified bank specified in *Section 2.19*. Modified LCD in *Section 3.13* and *Figure 27*.
01-Jul-2010	5	Replaced STM32F103Z with STM32F103ZGT6. 64-Kbyte internal SRAM and 512-Kbyte flash replaced with 96-Kbyte internal SRAM and 1-Mbyte flash.
12-Aug-2013	6	Replaced schematics.
20-Apr-2022	7	Reshuffled document from *Introduction* to *Conventions* to align with the latest standards. Added: – *STM3210E-EVAL Evaluation board information* – *Federal Communications Commission (FCC) and Innovation, Science and Economic Development Canada (ISED) Compliance Statements* Removed *Schematic diagrams*.