AN2640
Application note

Intelligent multipower digital ballast for fluorescent lamps

Introduction

Fluorescent lamps are highly popular due to their luminous efficiency, long life and color rendering. These lamps need external circuitry to compensate for their negative resistance characteristic. This circuitry is called "ballast". The simplest ballast is a magnetic inductor connected in series at the lamp. The electronic ballast with respect to the magnetic one offers the following advantages:

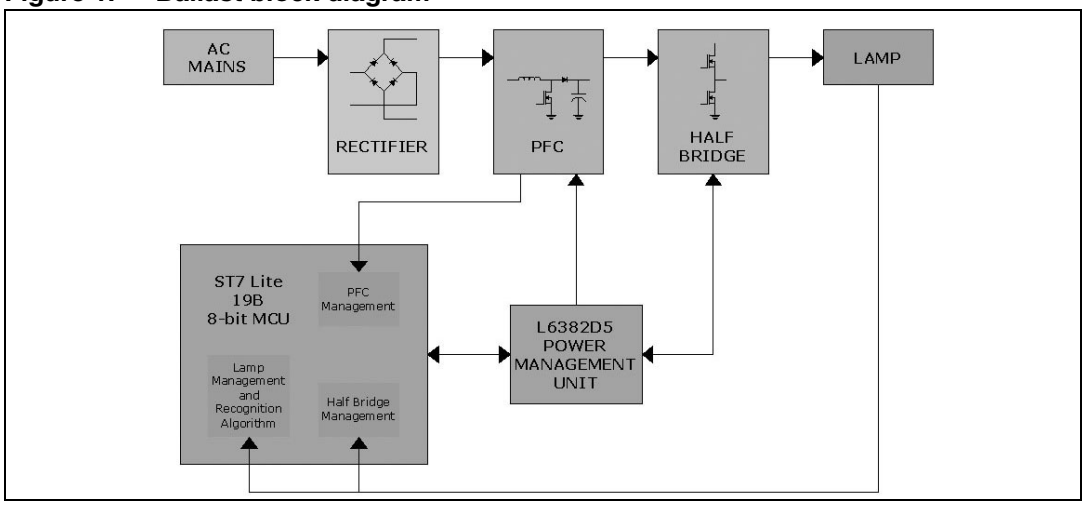
- Better efficiency
- Increased lamp life
- Lightweight with smaller dimensions
- Better lamp power control

For these reasons, in the last years there has been a shift in the market towards the use of electronic ballasts with dedicated drivers and controllers. Today, thanks to microcontrollers, it is possible to add intelligence into the circuit. Instead of having a dedicated circuit for each lamp with a single ballast it is possible to drive many different lamp groups. This application note describes an electronic ballast that is able to recognize lamps within the T5 fluorescent family such as 24 W, 39 W, 54 W and 80 W. It consists of two main blocks:

- A boost converter (Power Factor Controller PFC) working in transition mode (fixed T_{ON} and variable frequency)
- An inverter in half-bridge configuration working in zero voltage switching

Both ballast and PFC stages are controlled by the ST7FLIT19B that offers its entire signal to the L6382D5 which provides the right voltage and current levels for the Power MOSFET. This system after tube recognition sets the right parameter and drives the lamp correctly. *Figure 1* shows the ballast block diagram.

Figure 1. Ballast block diagram



Contents

List of figures

1 PFC section design criteria

1.1 Introduction

The following data are needed to calculate the input and output capacitors and the boost inductance:

- Mains range ($V_{irms(min)}$ and $V_{irms(max)}$)
- Regulated DC output voltage (V_o)
- Rated output power (P_o)
- Minimum switching frequency (f_{swmin})
- Maximum output voltage ripple (ΔV_o)
- Expected efficiency (η)
- Maximum mains RMS current (I_{rms})
- Rated output current I_o

Input capacitor

The input capacitor that has been chosen is 470 nF. Using this value good performances in terms of power factor and current distortion have been obtained with the lamps that can be driven.

Output capacitor

The output bulk capacitor (C_o) selection depends on the DC output voltage and the ripple on it. For lighting applications the ripple, $2*\Delta V_o$, is typically 5% of the output voltage.

The output bulk capacitor has been calculated using the following formula:

Equation 1

$$C_o \geq \frac{I_o}{4 \cdot \pi \cdot f \cdot \Delta V_o} = \frac{P_o}{4 \cdot \pi \cdot f \cdot V_o \cdot \Delta V_o}$$

Where:

- f= 50 Hz (mains frequency)
- V_o= is the output voltage (420V)
- ΔV_o= (½ ripple peak-to-peak value at 5%) is 10.5 V
- I_o= is the output peak current capacitor
- $P_{o(max)}$= (lamp specifications)

therefore

- Co ≥ 30.7 µF
- C_o was selected as 47 µF

1.2 Boost inductor

To define the PFC inductor several parameters are involved. The formula used to obtain the inductance value is:

Equation 2

$$L = \frac{V^2_{irms(min)} \cdot (V_o - \sqrt{2} \cdot V_{irms(min)})}{2 \cdot f_{sw(min)} \cdot P_i \cdot V_o}$$

Where

- $f_{sw(min)}$= 35 kHz
- $V_{irms(min)}$= 185 V
- $P_i = P_o/\eta$
- P_o is the lamp power
- η is the estimated efficiency (0.9)

For multipower ballast the inductance calculation must be performed adopting the maximum lamp power (85 W).

Using these parameters L = 1.95 mH.

An inductance value of 2 mH ± 5% is chosen.

The switching frequency of PFC power transistor can be obtained using the following formula:

Equation 3

$$f_{sw} = \frac{1}{2 \cdot L \cdot P_i} \cdot \frac{V^2_{irms} \cdot (V_o - \sqrt{2} \cdot V_{irms} \cdot \sin\Theta)}{V_o}$$

Notice that increasing the inductance value L decreases the PFC switching frequency.

1.3 PFC devices selection

The PFC is a step-up "Boost" regulator, therefore in normal operation the energy is fed from the inductor to the load and then stored in the output capacitor

Figure 2. The step-up "Boost" regulator

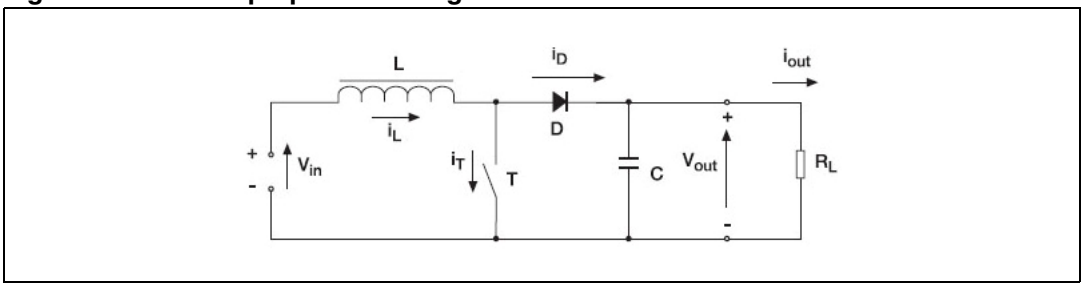
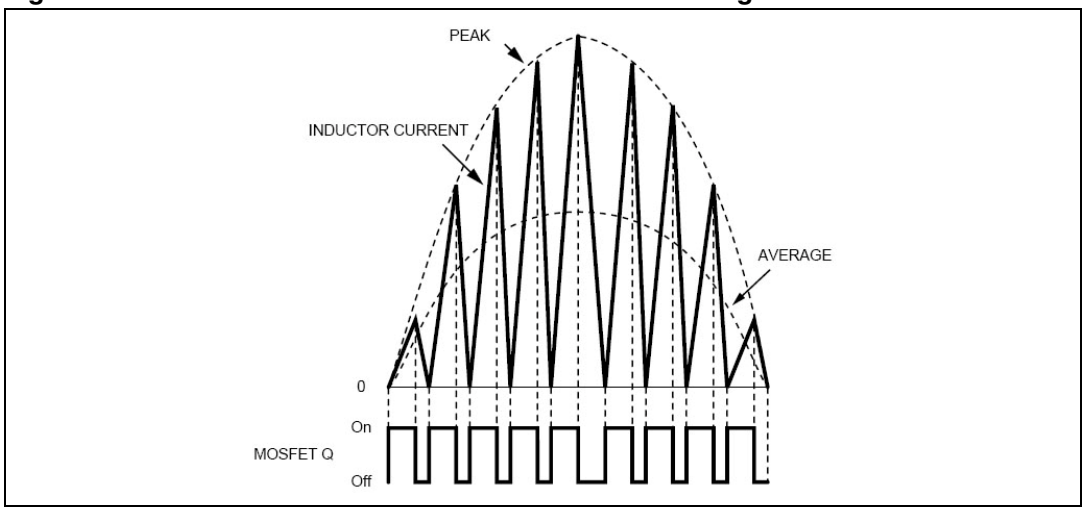


Figure 3. Inductor current waveform and MOSFET timing



1.3.1 Power switch

It must be:

- $V_{DSS} > V_{out}$
- $I_D > I_{T(pk)}$

Equation 4

$$V_{out} = 420\,V$$

Equation 5

$$P_{omax} = 85\,W$$

Equation 6

$$\eta = 0.9$$

Equation 7

$$P_{imax} = \frac{P_{omax}}{\eta} \cong 95\,W$$

Equation 8

$$V_{imin(rms)} = 185\,V$$

Equation 9

$$I_{Lmax(rms)} = \frac{P_{imax}}{V_{imin(rms)}} \cong 510\,mA$$

Equation 10

$$I_{L(pk)} = 2 \cdot \sqrt{2} \cdot I_{Lmax(rms)} \cong 1.5\,A$$

For safety reasons we must choose a device with:

- V_{RRM} 20% more V_{out}, that is, 504 V
- $I_{F(av)}$ 3 times more I_{out}, that is, 4.5 A (to be considered transient current)

The STP6NK60Z, a Zener-Protected SuperMESH™ MOSFET, satisfies these specifications.

Table 1. STP6NK60Z general features

V_{DSS}	$R_{DS(on)}$	I_D
600 V	< 1.2 Ω	6 A

1.3.2 Rectifier

It must be:

Equation 11

$$V_{RRM} > V_{out} = 420\ V$$

Equation 12

$$I_{F(av)} > I_{out} = \frac{P_{omax}}{V_{out}} \cong 200mA$$

For safety reasons we must choose a device with:

- V_{RRM} 20% more V_{out}, that is, 504 V
- $I_{F(av)}$ 3 times more I_{out}, that, is 600 mA

The STTH1L06, a turbo 2 ultrafast, high-voltage rectifier, was selected because it is especially suitable as a boost diode in discontinuous or critical mode power factor corrections.

Table 2. STTH1L06 general features

$I_{F(AV)}$	V_{RRM}	$V_{F(typ)}$	$t_{rr(max)}$
1 A	600 V	1.05 V	80 ns

2 Half-bridge design criteria

The design of the half-bridge section involves dimensioning the resonant components: ballast inductor and startup capacitor. The component design is not an easy matter and several parameters must be considered, especially when different lamps must be driven with the same resonant components. The main parameters to be considered are preheating current and voltage, maximum preheating voltage, maximum ignition voltage and run lamp voltage. For each lamp the transfer function was plotted in order to evaluate the operating point in terms of preheating and run frequency. The resonant inductor has been chosen as 1.2 mH and the startup capacitor has been chosen as 10 nF.

Figure 4. 24 W lamp power

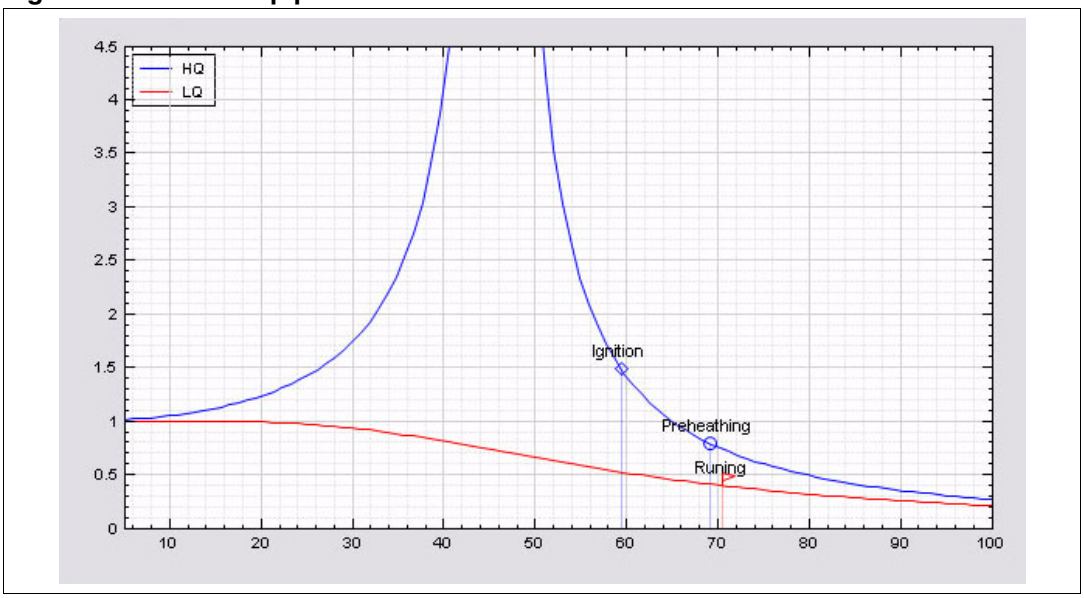


Figure 5. 39 W lamp power

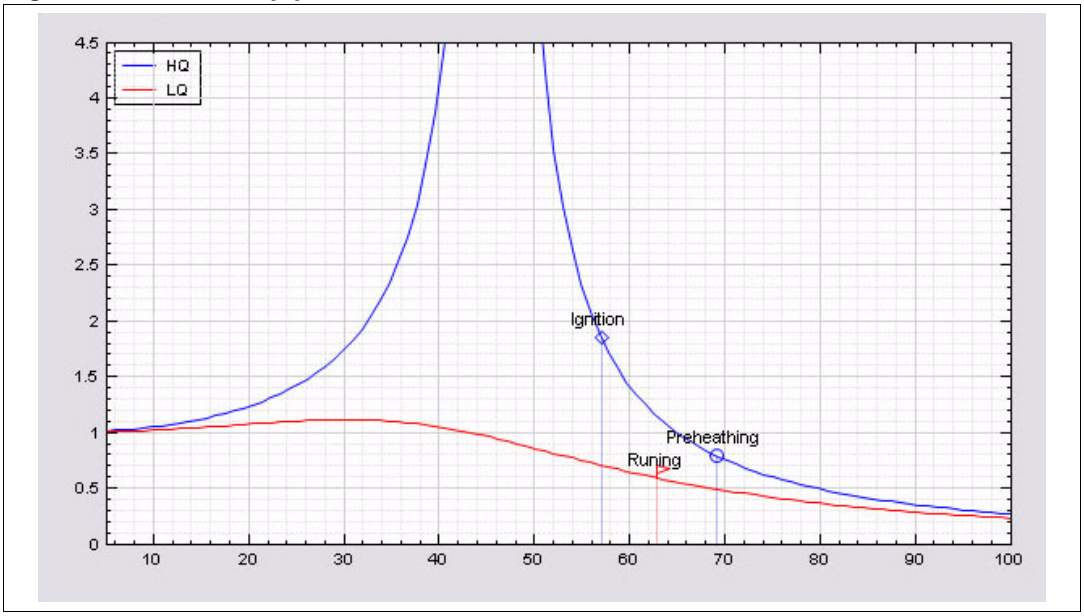


Figure 6. 54 W lamp power

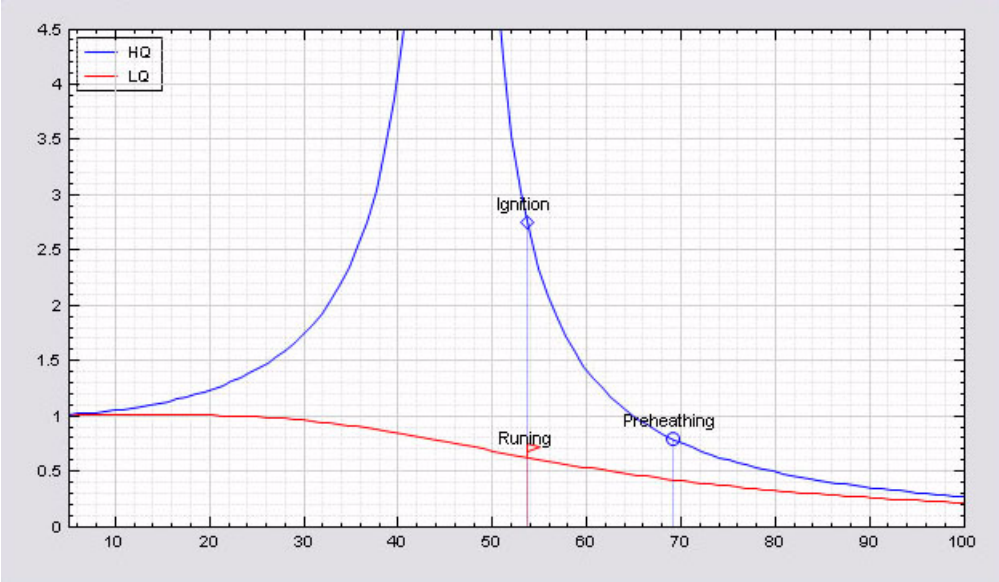
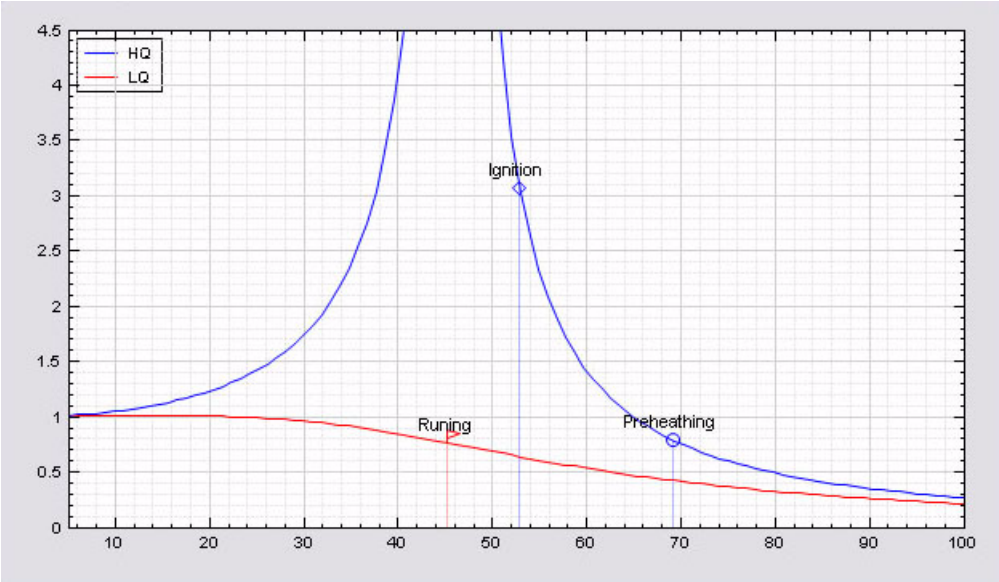


Figure 7. 80 W lamp power



During the preheating phase in this system the half-bridge works at fixed frequency and the selected preheating frequency is the best choice according to the selected lamp specifications.

This working frequency guarantees the right preheating current for all lamps that can be driven by this system.

After tube recognition the microcontroller sets the right run frequency for the connected lamp.

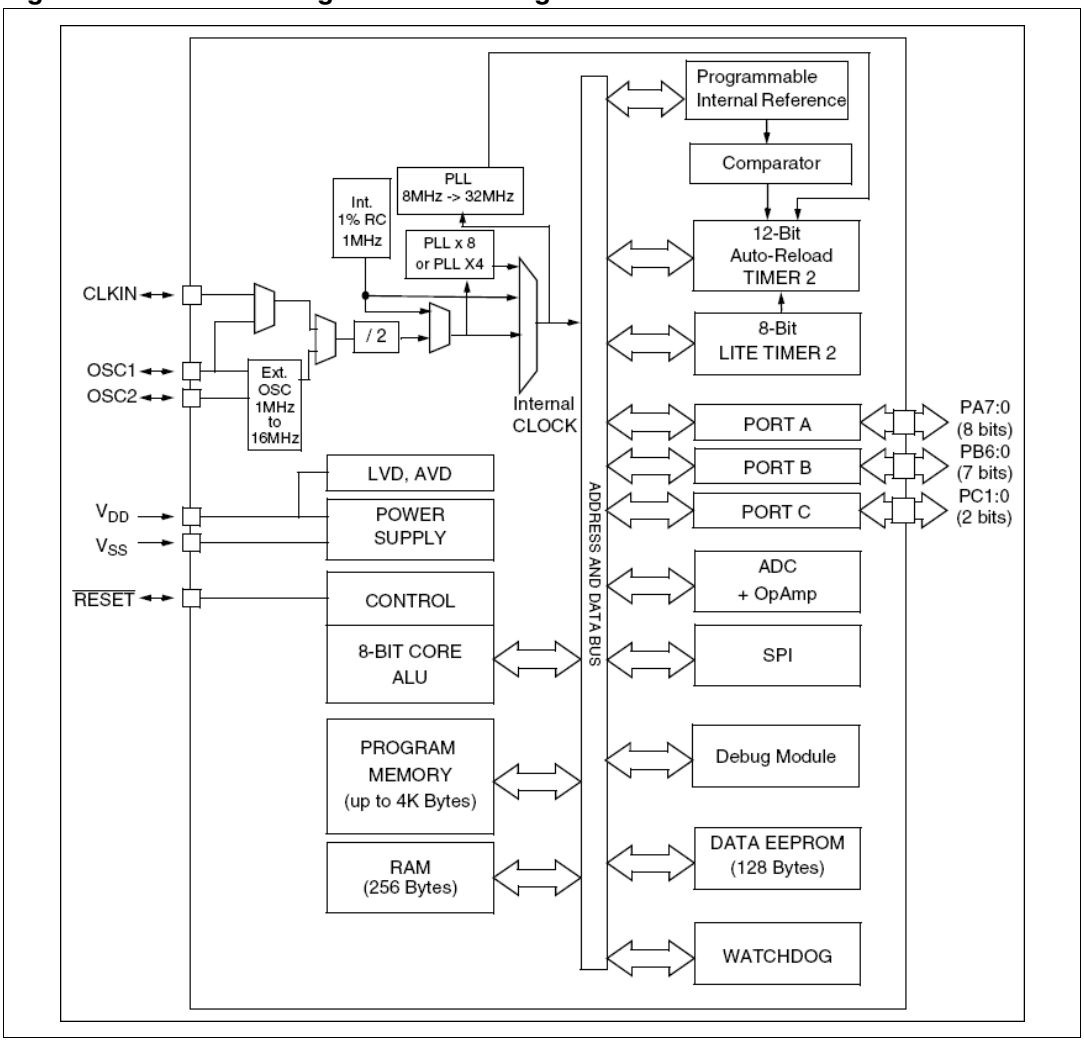
3 ST7LIT19BF1 - 8-bit MCU

3.1 Introduction

The ST7LIT19BF1 is a member of the ST7 microcontroller family.

All ST7 devices are based on a common industry-standard 8-bit core, featuring an enhanced instruction set.

Figure 8. ST7LITE1xB general block diagram

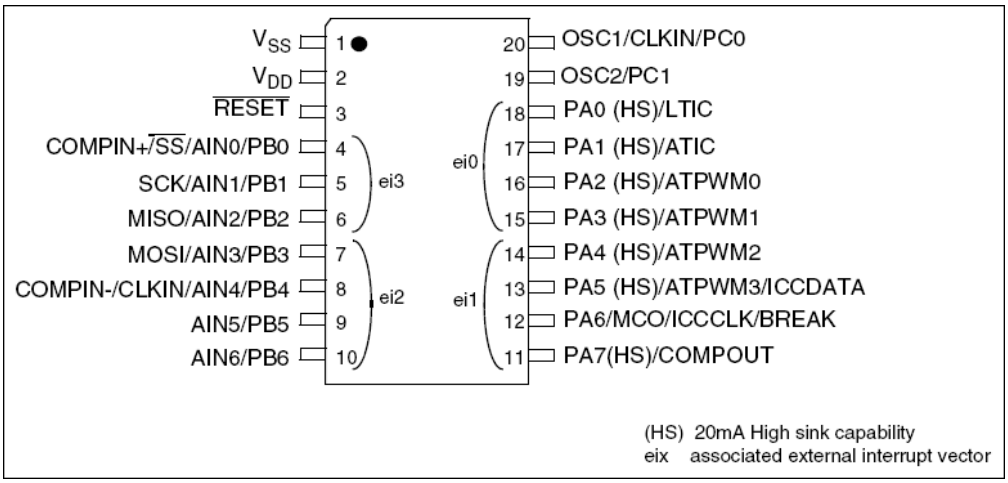


The ST7LIT19BF1, moreover, is a microcontroller designed for lighting applications.

The following are a few main features that make this microcontroller suitable for this scope:

- Internal RC oscillator with 1% precision at 8 MHz CPU frequency
- 32 MHz timer counter clock with two independent counters for half-bridge and PFC management
- Analog PFC zero-current detection and half-bridge dead time generation
- Analog comparator
- 10-bit A/D Converter with 7 channels and the possibility to use an amplifier (fixed gain 8) between the input and converter
- 2 timers with 1 ms or 2 ms time base to provide timing to the system management

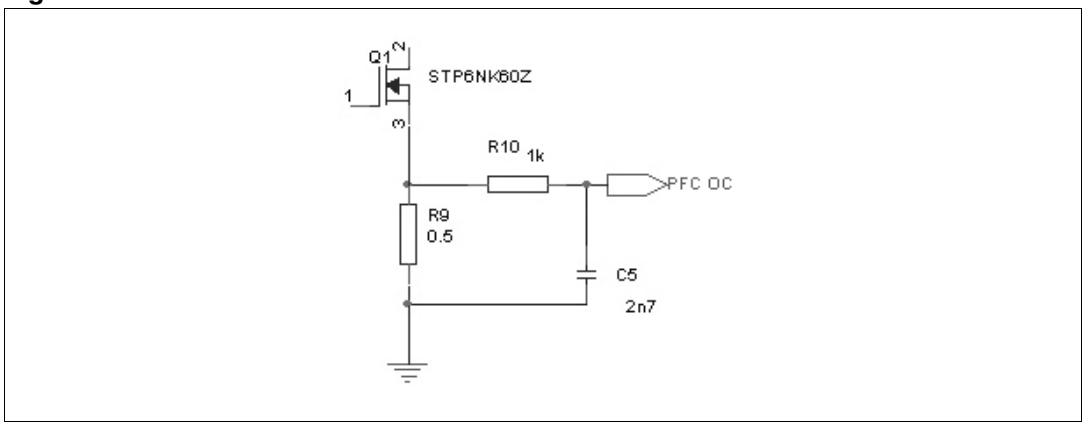
Figure 9. ST7LITE1xB 20-pin SO and DIP package pinout



3.2 Use of the pins

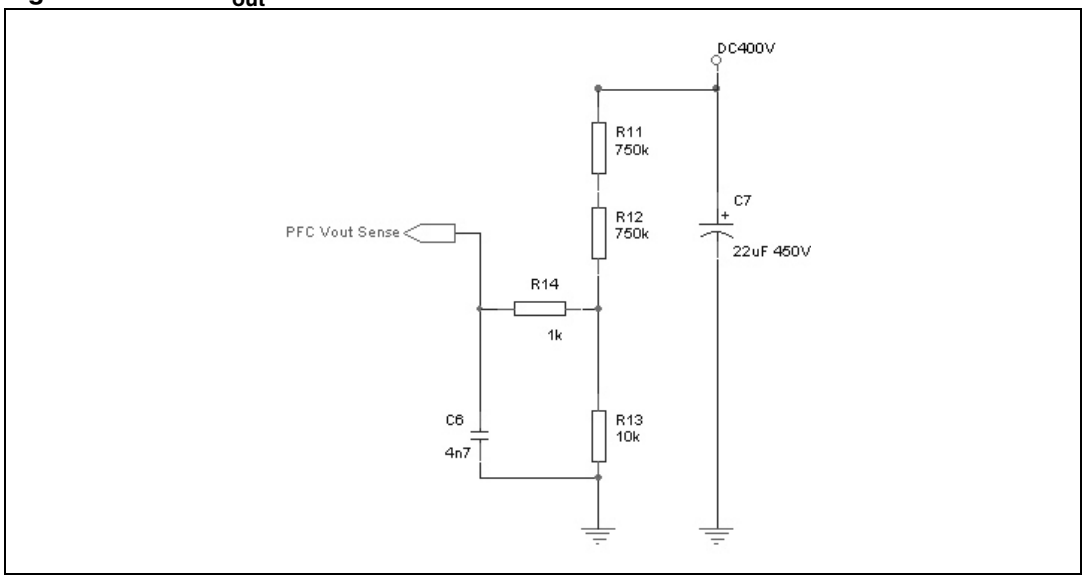
- Pin 1: GND
- Pin 2: V_{CC}. The microcontroller is supplied by means of this pin. The voltage is generated by the L6382D5 device. To prevent noise in this pin a 100 nF capacitor must be soldered as close as possible between this pin and GND.
- Pin 3: reset (not used). It is advisable to connect a small capacitor to avoid undesired reset of the micro between this pin and GND.
- Pin 4: COMPIN+. This pin is used to protect against overcurrent on the PFC Power MOSFET and inductor. When the current exceeds 2 A, the comparator inside the MCU stops the ballast without using the MCU core. *Figure 10* shows the detection circuit.

Figure 10. PFC overcurrent detection circuit



- Pin 5: AIN1 - PFC V_{out} sense. This pin is used to perform the PFC V_{out} voltage protection and regulation. *Figure 11* shows the circuit for the PFC V_{out} sense.

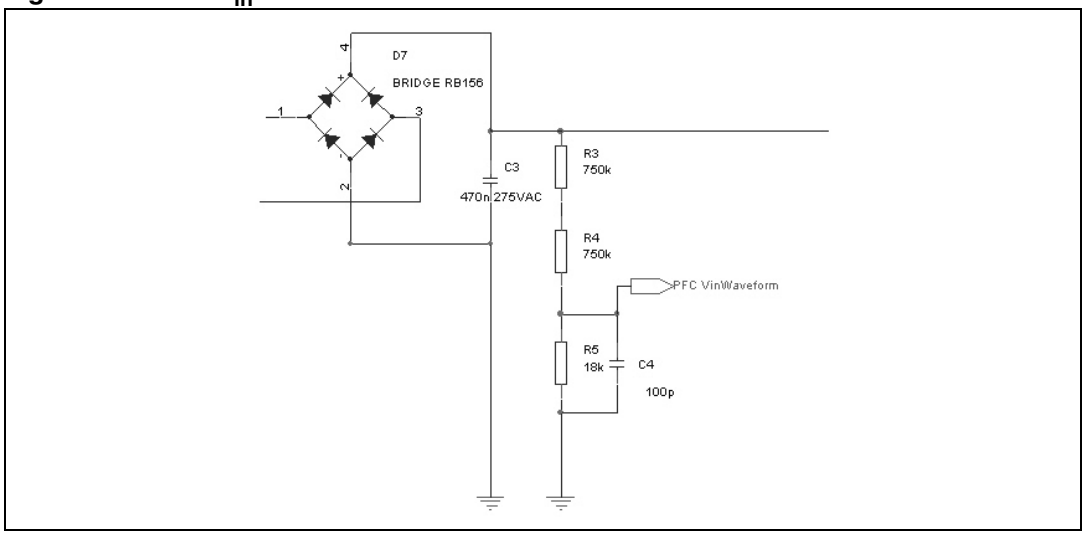
Figure 11. PFC V_{out} sense circuit



In this pin the MCU reads the voltage on the C6 capacitor and converts this value to a digital one which is proportional to the DC bus voltage.

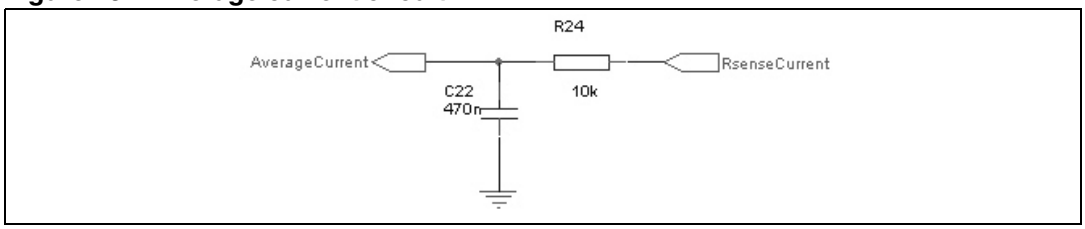
- Pin 6: AIN2 - PFC V_{in} waveform. The circuitry shown in *Figure 12* measures the input voltage and the voltage across R5-C4 is used by the MCU to understand the instantaneous main voltage.

Figure 12. PFC V_{in} waveform circuit



- Pin 7: AIN3 - average current. In the ballast during the run state the inductor current is controlled by monitoring the voltage across R_{sense}.

Figure 13. Average current circuit



The voltage across C22 is proportional to the current that flows in the Power MOSFET which is related to the discharge current in the tube.

When ballast frequency is changed, a current regulation is performed.

- Pin 8: AIN4 - lamp type detection. This circuit is used to distinguish between lamps having different cathode resistances. When the NPN transistor Q5 is in the cutoff region, the PNP transistor Q4 is also, producing a voltage close to zero at pin 8 "Lamp Type Detection". When the NPN transistor Q5 is in the saturation region, the PNP transistor Q4 is also, producing at pin 8 "Lamp Type Detection" a voltage that depends on the resistor of the lamp electrodes. Normally the NPN transistor Q5 is kept in the cutoff region so that the whole circuit is disabled. This circuit is enabled just to recognize the lamp family, after recognition, it is disabled.

Figure 14. Lamp type detection circuit (a)

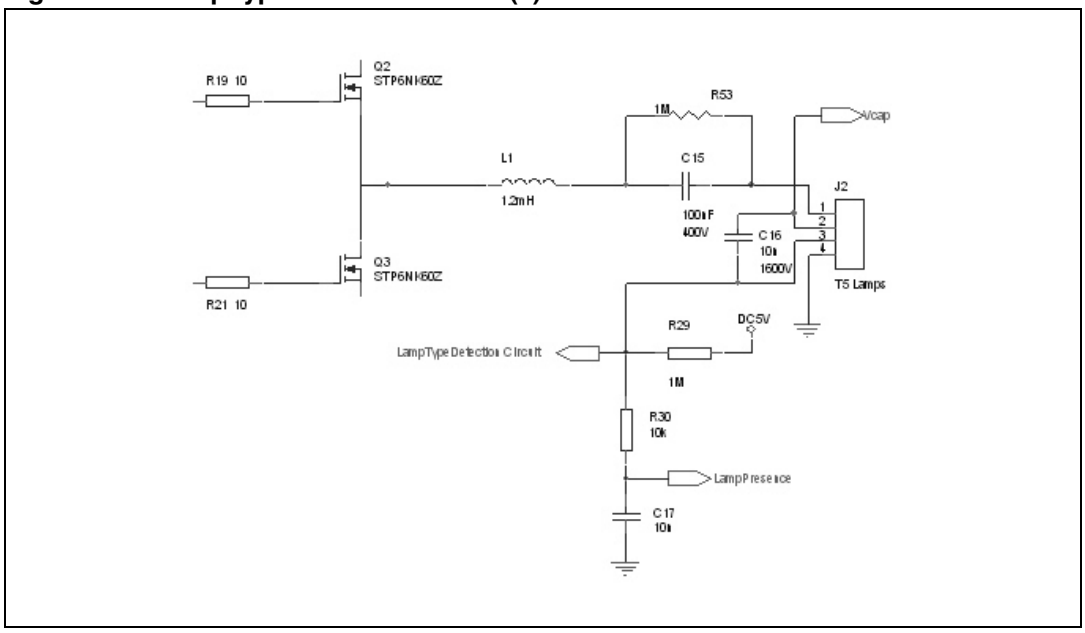
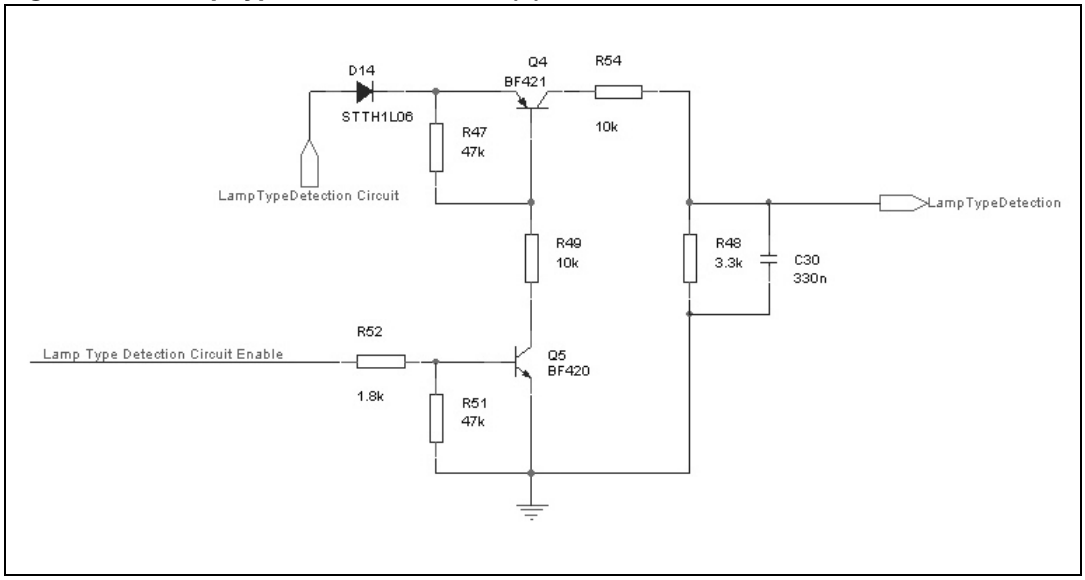
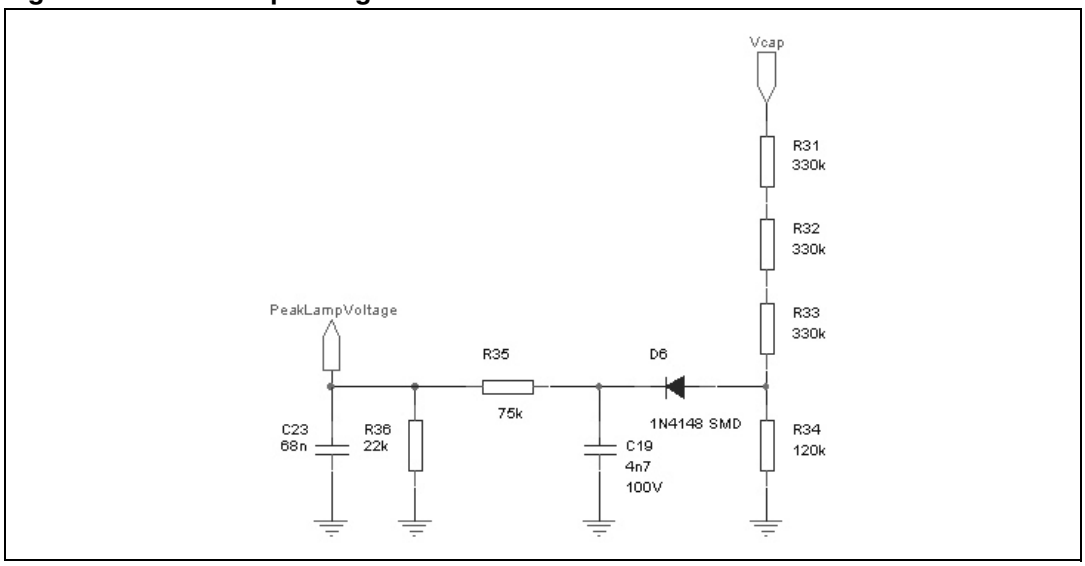


Figure 15. Lamp type detection circuit (b)



- Pin 9: AIN5 - peak lamp voltage. Using the circuit shown in *Figure 16*, it is possible to measure the voltage across the lamp.

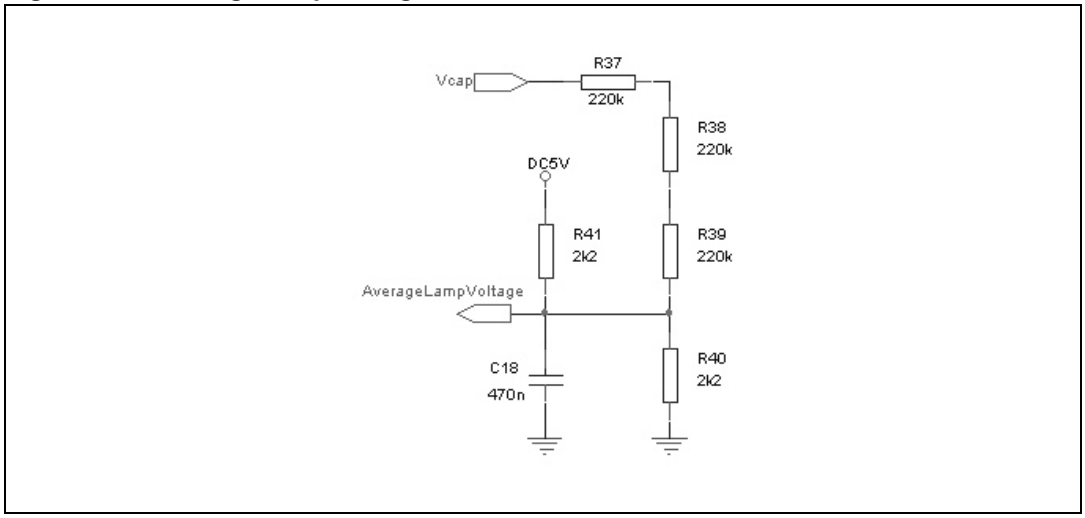
Figure 16. Peak lamp voltage circuit



The resistors R31 ÷ R34 form a voltage divider and the voltage across R36-C23 is used to control the voltage on the lamp during all lamp phases.

- Pin 10: AIN6 - average lamp voltage

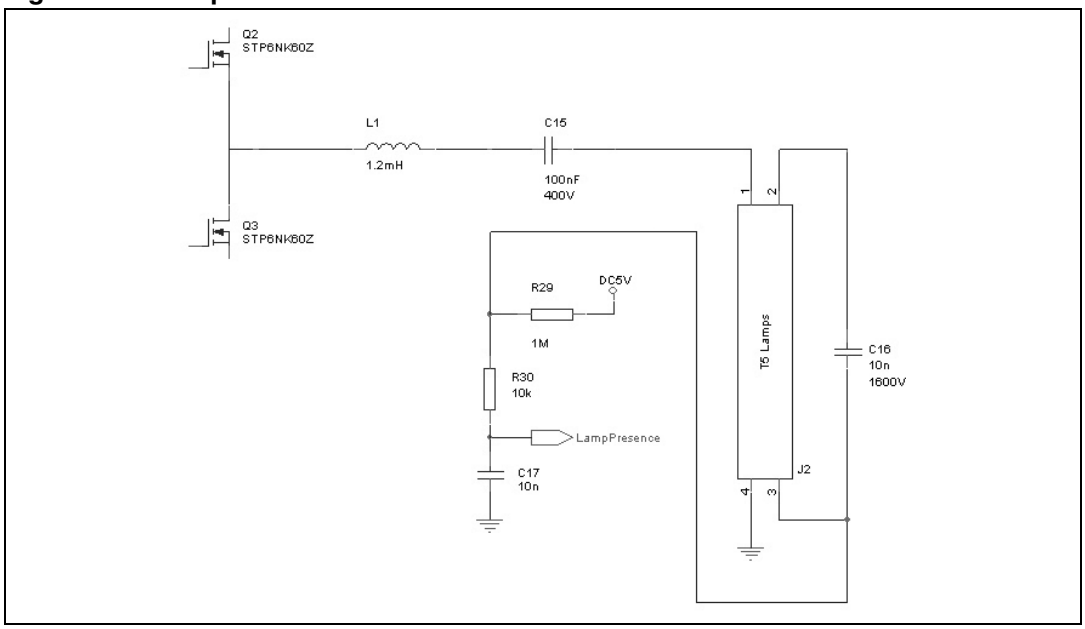
Figure 17. Average lamp voltage circuit



The circuit shown in *Figure 17* is used to detect asymmetrical lamp voltage when lamp rectification happens.

- Pin 11: PA7 - lamp detection

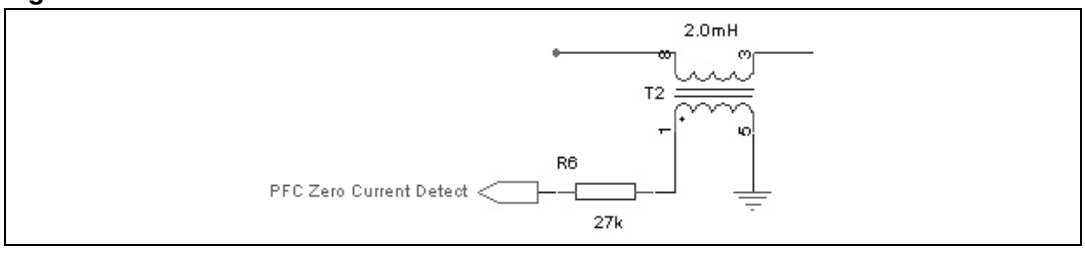
Figure 18. Lamp detection circuit



The circuit shown in *Figure 18* connected at this digital input is used to detect the lamp presence. If the lamp is present, the cathode is in parallel to R30 and C17 and the voltage across C17 is low. The low voltage is used by the micro to sense the lamp presence. If the lamp is not present or the cathode is broken, the voltage across C17 is high (5 V) and the MCU stops the ballast.

- Pin 12: PA6 (not used). This pin is connected at micro V_{CC} voltage by means of a 10 kΩ resistor because this pin is also used as ICCCLK and during normal operation it must be pulled up, internally or externally (external pull-up of 10 kΩ is mandatory in noisy environments).
- Pin 13: PWM3 - PFC gate driver. This pin is connected to the L6382 driver in order to control the PFC PMOS.
- Pin 14: PA4 (not used). This pin is connected to micro V_{CC} voltage by means of a 10 kΩ resistor because an unused pin must be kept at a fixed voltage. It can be left unconnected if it is configured as output (0 or 1) by the software.
- Pin 15: PWM1 - High side input. This pin is connected to the L6382 driver and the signal is used to drive the High side PMOS.
- Pin 16: PWM0 - Low side input. This pin is connected to the L6382 driver and the signal is used to drive the High side PMOS
- Pin 17: PA1 - CSO. This pin is connected to the CSO pin of the L6382 and can be used to lock the ballast when the CSI pin is high.
- Pin 18: LTIC - Zero-current detect

Figure 19. Zero-current detection circuit



The zero-current detection circuit switches the external MOSFET ON as soon as the voltage across the boost inductor reverses or the current through the boost inductor goes to zero. This feature allows the transition mode operation. The signal for ZCD is obtained with an auxiliary winding on the boost inductor. The secondary winding is connected to the LTIC pin by means of a resistor. The MCU detecting negative dv/dt gives the turn-on signal to the driver for the Power MOSFET commutation.

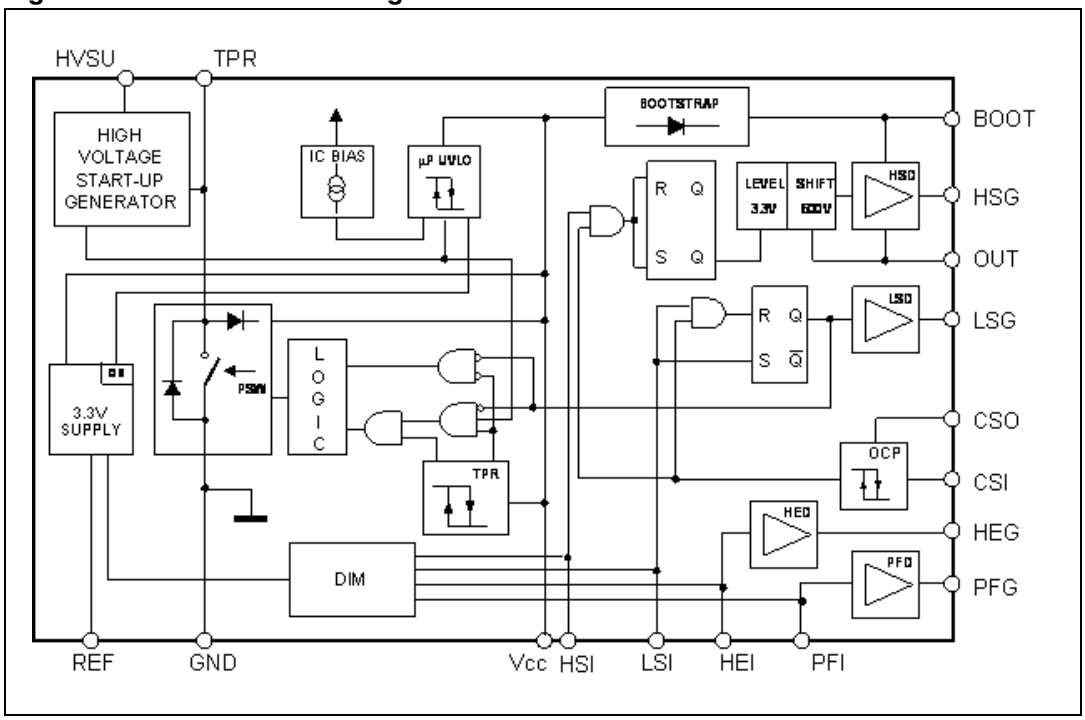
- Pin 19: PC1 (not used). This pin is connected to micro V_{CC} voltage by means of a 10 kΩ resistor because an unused pin must be kept at a fixed voltage. It can be left unconnected if it is configured as output (0 or 1) by the software.
- Pin 20: Lamp Type Detection Circuit Enable. This pin is used to enable the "Lamp Type Detection Circuit".

4 L6382D5 - power management units for microcontrolled ballast

4.1 Introduction

This driver allows powering efficiently all the ICs (PFC, microcontroller, driver) in all conditions and allows the microcontroller to drive the MOSFET (both half-bridge and PFC) without using numerous different drivers.

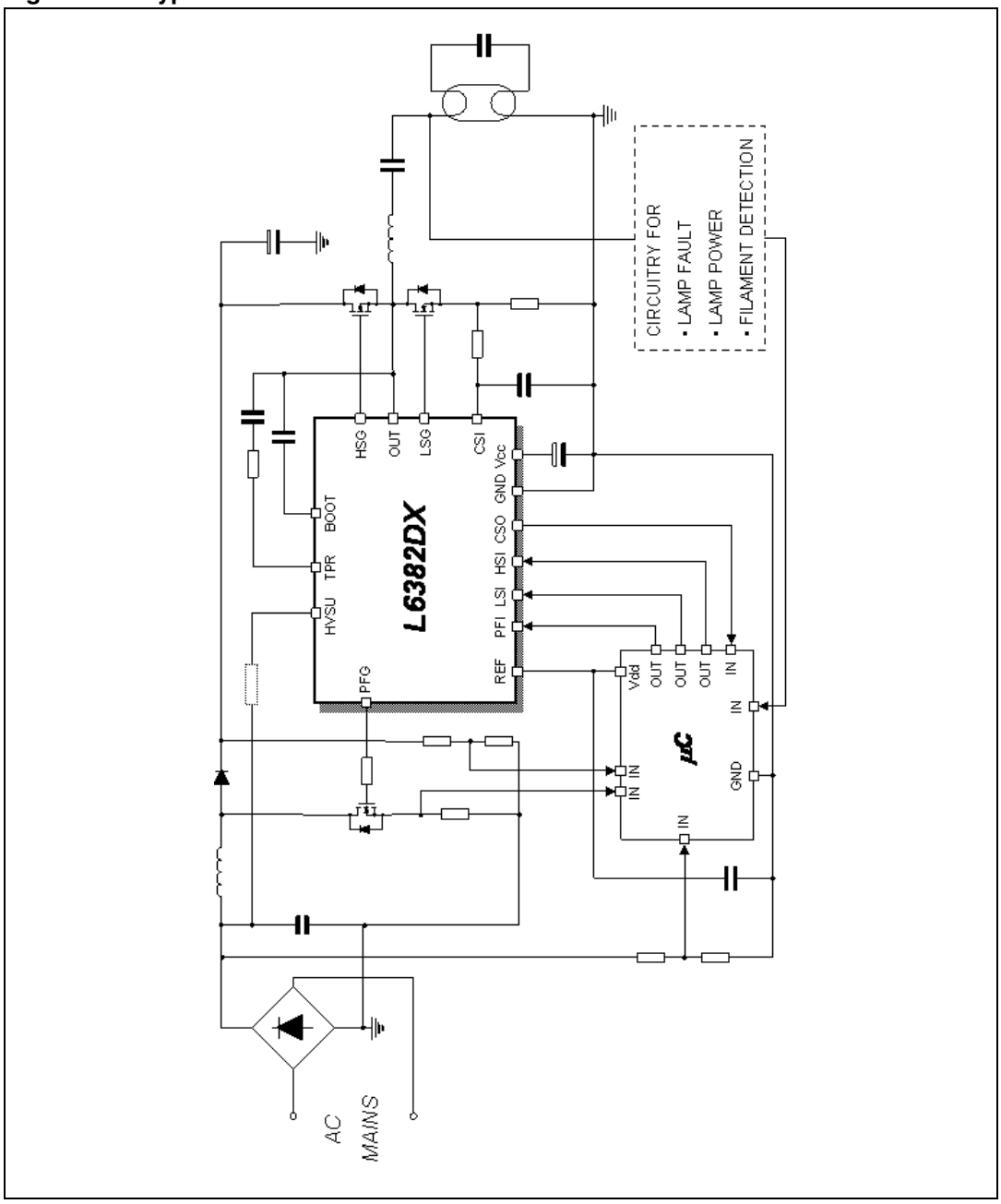
Figure 20. L6385Dx block diagram



The L6382D5 ICs (*Figure 20*) include 3 MOSFET driving stages (for PFC, for the half-bridge, for the preheating MOSFET) plus a power management unit (PMU) able to supply the microcontroller in any condition by means of a voltage reference available at a pin. It has a precise reference voltage (5VDC ±2%, overall temperature range) able to provide up to 30 mA to supply the microcontroller.

The L6382D5 also integrates a function that regulates the IC supply voltage without the need of any external charge pump and optimizes the current consumption (*Figure 21*). The L6382D5 reduces the application bill of materials because many different tasks (regarding drivers and power management) are performed by a single IC, which of course improves application reliability.

Figure 21. Typical L6385Dx use



Another feature of the driver is the internal interlocking that avoids cross-conduction in the half-bridge FET's. If by chance both HGI and LGI inputs are brought high at the same time, then LSG and HSG are forced low as long as this critical condition persists.

A current sense is also available in this driver. When the voltage on pin CSI overcomes the internal comparator reference (0.56 V, typ), the block latches the fault condition. In this state the OCP block forces both HSD and LSD signals low while CSO is forced high so that it can be sent to an input pin of the microcontroller that, based on its programming, starts the proper protection sequence. The CSO output remains latched high until LSI and HSI are simultaneously low (e.g. during dead time) and CSI is below 0.5 V. This function is suitable to implement an overcurrent protection or hard-switching detection by using an external

sense resistor. As the voltage on pin CSI can go negative, the current must be limited below 2 mA by external components.

4.2 Use of the pins

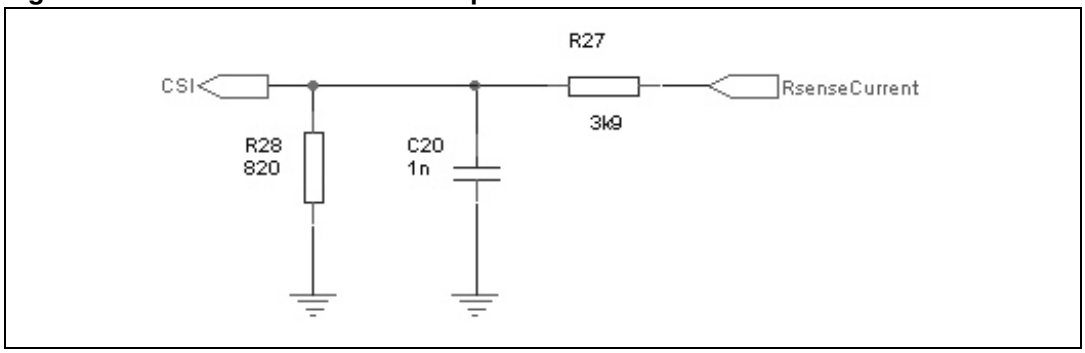
A short description of each pin function is given below.

- Pin 1: PFI. This pin receives a digital input signal from the ST7 micro to control the PFC gate driver. We advise connecting a capacitor for noise filtering between this pin and GND. In this application a 33pf capacitor is used.
- Pin 2: LSI. This pin receives digital input signal from the ST7 to control the low side switch in the ballast.
- Pin 3: HSI. This pin receives digital input signal from the ST7 to control the high side switch in the ballast.
- Pin 4: HEI (not used). This pin receives digital input signal from the ST7 to control the HEG driver.
- Pin 5: PFG. This pin is able to drive an external MOSFET with a sink current capability of 120 mA and a source current capability of 250 mA. A 10 Ω resistor is connected between this pin and the Power MOSFET gate to reduce the peak current.
- Pin 6: not connected
- Pin 7: TPR. This pin is connected by means of an RC net to the half-bridge midpoint in order to form a charge pump circuit charging the capacitor connected to the V_{CC} pin. In this application a capacitor of 1 nF at 630 V and a resistor of 44 Ω (2 x 22 Ω) have been mounted. The high voltage capacitor in this connection also performs the snubber function in the half-bridge section limiting the slope during the voltage variation.
- Pin 8: GND. On the GND traces it is better to keep separate power traces from the signal and a star connection of these tracks is advisable.
- Pin 9: LSG. This pin is connected to the Power MOSFET gate of the low side of the half-bridge. This pin has 120 mA as source and sink current capability. A 33 Ω resistor is connected between this pin and the MOSFET gate to limit the peak current. At turnoff a net composed of a diode and a 33 Ω resistor reduces the resistance which decreases the turnoff time.
- Pin 10: V_{CC}. This pin provides the supply voltage to the driver. A capacitor of 47 µF is connected between this pin and GND and in parallel another small capacitor is mounted.
- Pin 11: BOOT. This pin provides the supply voltage at the high side gate driver. A 100 nF capacitor is connected between this pin and the out pin of the driver. This

capacitor is supplied thanks to a patented structure that replaces an external diode connected between this capacitor and V_{CC}.

- Pin 12: HSG. The same as pin 9 but is able to drive the half-bridge high side Power MOSFET gate.
- Pin 13: OUT. This pin is the high side floating ground and it is connected at the midpoint of the half-bridge.
- Pin 14: not connected
- Pin 15: HVSU. This pin allows driver startup and two resistors of 10 Ω are connected at the DC bus according to the V_{ref} current requirement.
- Pin 16: not connected
- Pin 17: HEG (not used)
- Pin 18: CSO. This pin is the output of the current sense comparator. During normal operation this pin is forced low, but if the voltage on the CSI pin exceeds 0.55 V this pin is high with 5 V logic level.
- Pin 19: CSI. This is the input of the current sense comparator.The circuit that is connected at this pin is shown in *Figure 22*. During the operating mode if overcurrent occurs in the half-bridge, the voltage on the R28 resistor increases and when it exceeds 0.55 V, the L6382 forces both half-bridge drivers low. This condition remains until the input signals LGI and HGI are low simultaneously (dead time) or V_{cc} is below the undervoltage lockout.

Figure 22. Circuit connected at CSI pin



The capacitor C20 is used to filter the voltage on the CSI pin.

- Pin 20: V_{ref}. This pin provides a precise voltage reference of 5 V with a current capability up to 30 mA. This voltage is used to supply the ST7 microcontroller which avoids adding external components. To ensure voltage stability and prevent noise, a 220 nF capacitor is recommended between this pin and GND.

5 Recognition technique

To identify the connected lamp, the power must be evaluated by measuring both the lamp voltage and current.

In this way, by multiplying these measurements, it is possible to obtain the lamp power:

Equation 13

$$P_{lamp} = V_{lamp} \cdot I_{lamp}$$

With the evaluation board based on STMicroelectronics' ST7FLIT19BF1 MCU and L6382D5 driver, the lamp power measurements can be easily calculated. Our proposal is based on a patented method that evaluates the PFC T_{ON}. The PFC is a boost converter working in transition mode (TM). In the transition mode operation the boost converter works with a fixed switch conduction time, T_{ON}, and variable frequency.

To measure the lamp power the constant T_{ON} is evaluated and moreover the T_{ON} is proportional at the load power as shown in the following relationship:

Equation 14

$$T_{ON} = \frac{2 \cdot L \cdot P_o}{V^2_{inr}}$$

Where:

- T_{ON} is the PFC switch conduction time
- L is the PFC inductor value
- V_{inrms} is the RMS AC input voltage
- P_o is the load power, that is, the lamp power

This technique provides a key advantage of obtaining the lamp power information by directly reading the PFC conduction time without multiplier evaluations in the board.

When the mains is switched ON the microcontroller performs a measurement on the AC input voltage. After this phase it starts the half-bridge. The PFC is activated during this initial phase to distinguish the family type and a cathode resistance measurement is performed to select the lamp type.

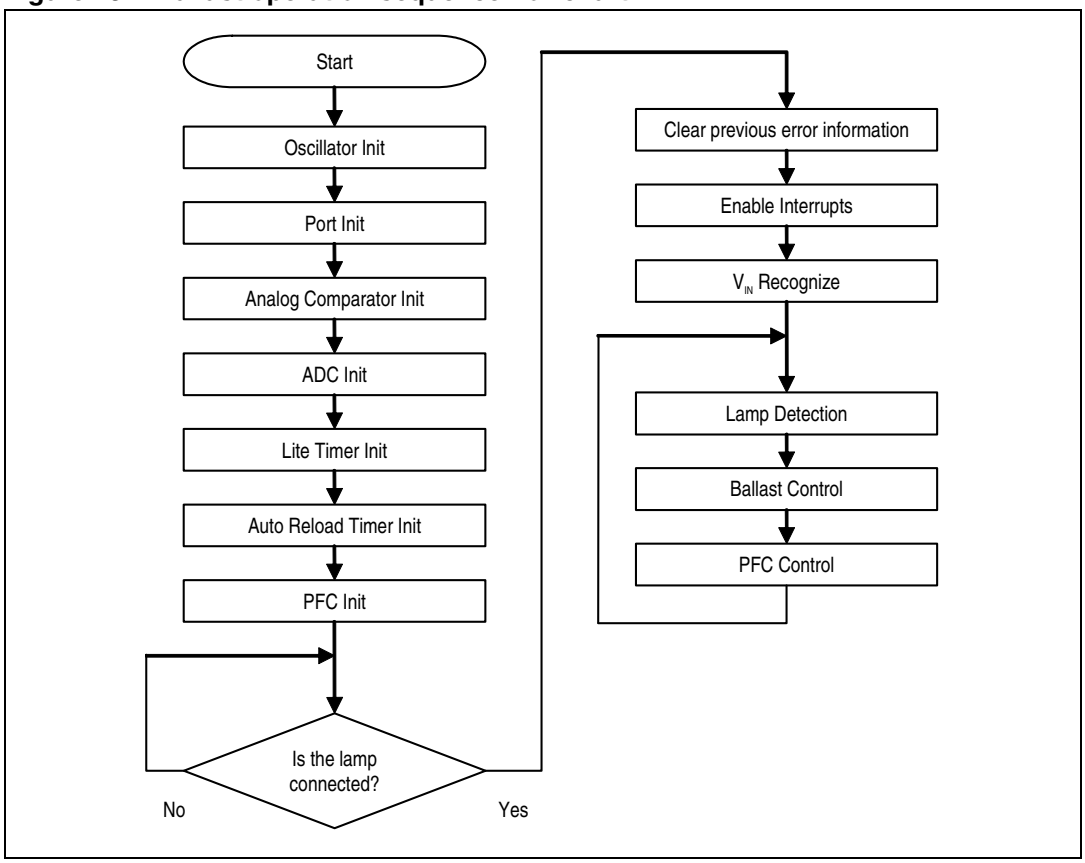
After this selection, the preheating phase is performed until the ignition phase turns the lamp on.

After the ignition the connected lamp is recognized and starts the run phase.

Using the described technique it is simple to calculate the lamp power. Experimental results have confirmed this data.

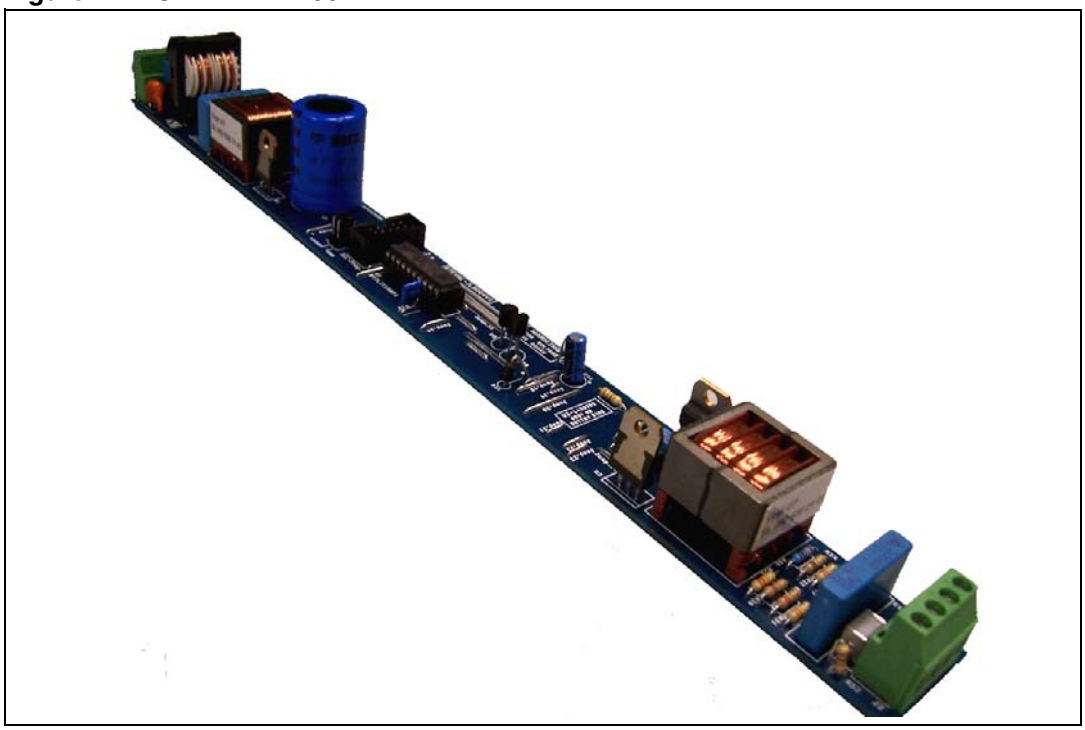
5.1 Code implementation on microcontroller

Figure 23. Ballast operation sequence flowchart



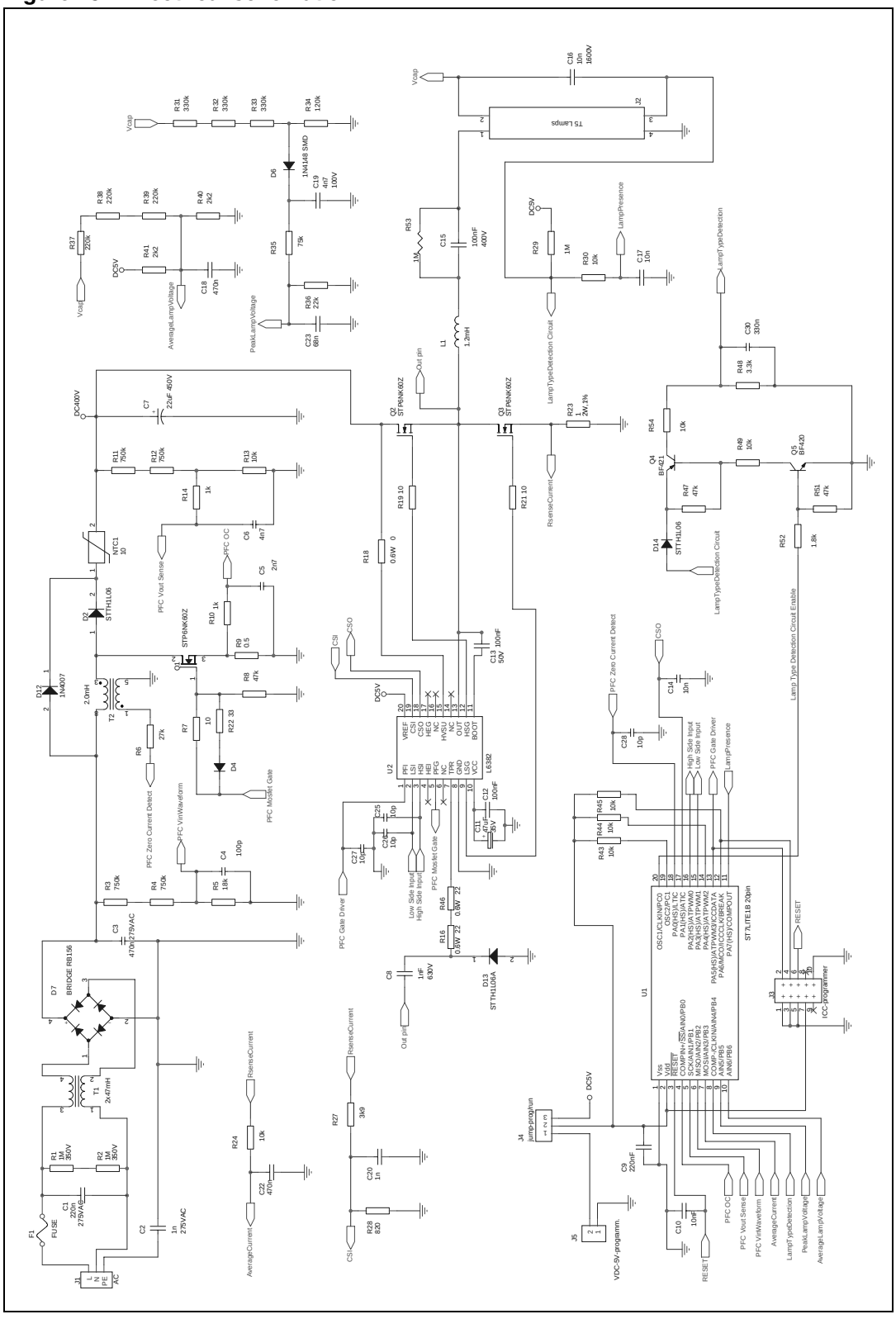
6 Board description

Figure 24. STEVAL-ILB004V1



6.1 Electrical schematic

Figure 25. Electrical schematic



6.2 Bill of materials

Table 3. BOM

Item	Qty	Reference	Part / value	Voltage Watt	Type
1	1	C1	220 nF	275 V_{ac}	EPCOS - order code B32922C3224K
2	1	C10, C14	10 F		Ceramic
3	1	C11	47 µF	35 V	Electrolytic
4	2	C12, C13	100 nF	50V	Ceramic
5	2	C16	10 nF	1600 V	EPCOS - order code B32653A1103J
6	1	C15	100 nF	400 V	Polyester
7	1	C17	10 nF	50 V	Ceramic
8	2	C18, C22	470 nF	50 V	Ceramic
9	1	C19	4.7 nF	100 V	Ceramic
10	1	C2	1 nF	275 V_{ac}	Y2 capacitor
11	1	C20	1 nF	50 V	Ceramic
12	1	C23	68 nF	50 V	Ceramic
13	3	C25, C26, C28	10 pF	50 V	Ceramic
14	1	C27	10 pF	50 V	Ceramic
15	1	C3	470 nF	275 V_{ac}	Polyester
16	1	C30	330 nF	50 V	Ceramic
17	1	C4	100 pF	50 V	Ceramic
18	1	C5	2.7 nF	50 V	Ceramic
19	1	C6	4.7 nF	50 V	Ceramic
20	1	C7	47 µF	450 V	Electrolytic
21	1	C8	1 nF	630 V_{dc}	Polyester
22	1	C9	220 nF	50 V	Ceramic
23	1	D12	1N4007	1 A 1000 V	General purpose rectifier
24	3	D2, D13, D14	STTH1L06A	1 A 600 V	ST Microelectronics turbo 2 ultrafast high-voltage rectifier
25	2	D4, D6	1N4148	200 mA 100 V	Small signal diode
26	1	D7	BRIDGE RB156		Bridge rectifier
27	1	F1	Fuse 2 A, 250 V	250 V	
28	1	L1	1.2 mH ± 5%		VOGT PFC choke EVD25 Part nr. SL0606302101
29	1	NTC1	10		
30	3	Q1, Q2, Q3	STP6NK60Z	1 Ω/ 6 A 600 V	STMicroelectronics Zener-protected SuperMESH™ MOSFET

Table 3. BOM (continued)

Item	Qty	Reference	Part / value	Voltage Watt	Type
31	1	Q4	BF421	500 mA 300 V	Small signal PNP transistor
32	1	Q5	BF420	500 mA 300 V	Small signal NPN transistor
33	3	R1, R2, R29	1 MΩ		
34	2	R10, R14	1 kΩ - 1%		
35	5	R13, R24, R30, R49, R54	10 kΩ - 1%		
36	2	R16, R46	22 Ω		
37	1	R18	0 Ω	0.6 W	
38	1	R22	33 Ω		
39	1	R23	1 Ω - 1%	1 W	
40	1	R27	3.9 kΩ - 1%		
41	1	R28	820 Ω - 1%		
42	4	R3, R4, R11, R12	750 kΩ - 1%		
43	3	R31, R32, R33	330 kΩ - 1%	0.25 W	
44	1	R34	120 kΩ - 1%	0.2 5W	
45	1	R35	75 Ω - 1%	0.25 W	
46	1	R36	22 kΩ - 1%		
47	3	R37, R38, R39	220 kΩ - 1%	0.25 W	
48	1	R40	2.2 kΩ	0.25 W	
49	1	R41	2.2 kΩ - 1%		
50	3	R43, R44, R45	10 kΩ		
51	1	R48	3.3 kΩ		
52	1	R5	18 kΩ - 1%		
53	1	R52	1.8 kΩ		
54	1	R53	1 MΩ		
55	1	R6	27 kΩ		
56	3	R7, R19, R21	10 Ω		
57	3	R8, R47, R51	47 kΩ		
58	1	R9	0.5 Ω - 1%	1 W	
59	1	T1	2x47 mH at 0.5 A		EPCOS Current-compensated D core choke Or. code B82731-M2501-A30
60	1	T2	2 mH ± 5%		VOGT PFC choke EVD25 Part nr. SL0606301101

Table 3. BOM (continued)

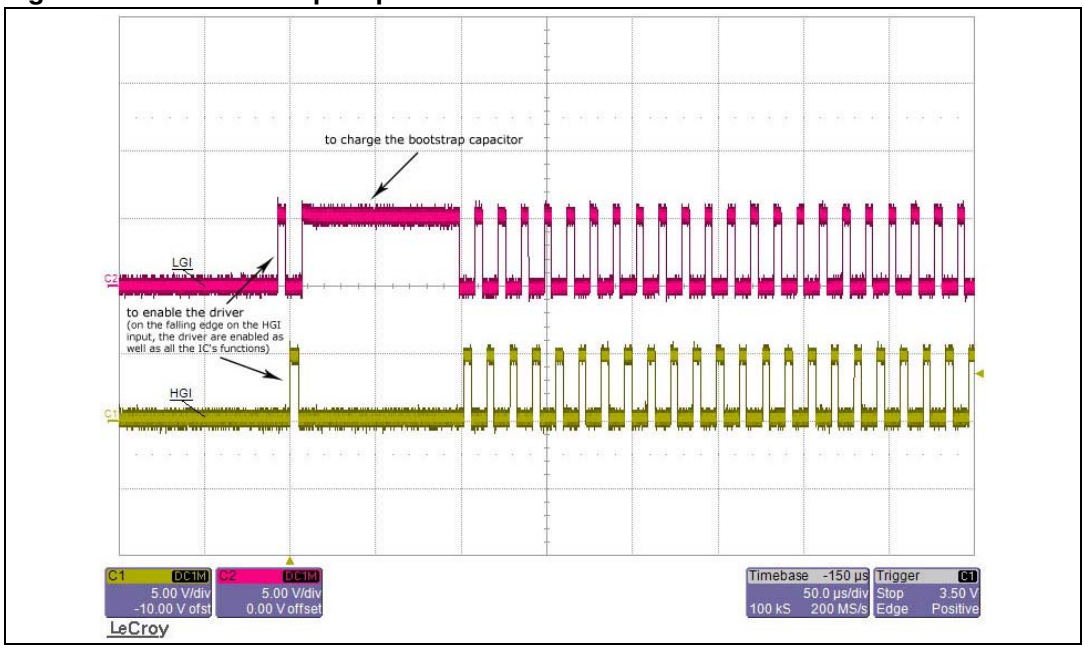
Item	Qty	Reference	Part / value	Voltage Watt	Type
61	1	U1	ST7FLIT19BF1B6		STMicroelectronics 8-bit MCU
62	1	U2	L6382D5		STMicroelectronics power management unit for microcontrolled ballast

6.3 Experimental results

6.3.1 From system switch on to ballast run

The identification tests have been performed using T5 tubes having 24, 39, 54 and 80 W lamp power ratings. Tests have been performed across the entire European mains (185 V ÷ 230 V / 50 Hz) input range.

Figure 26. L6382 startup sequence and ballast start



The following results have been obtained with 230 V at 50 Hz as mains.

Figure 27. 24 W lamp power

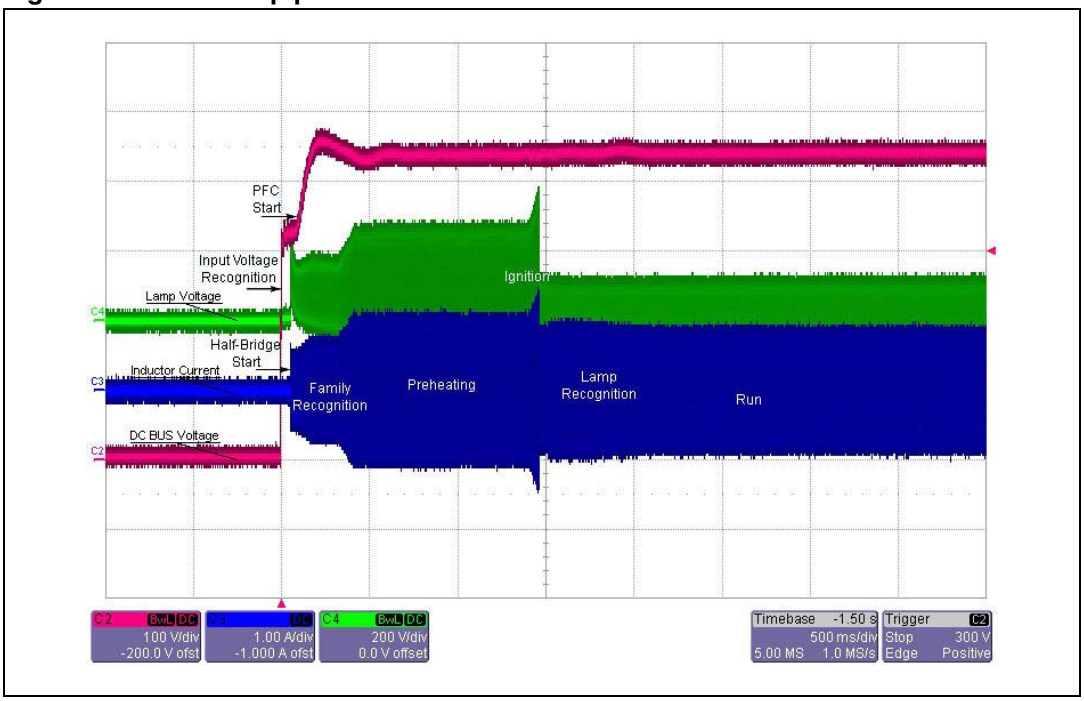


Figure 28. 39 W lamp power

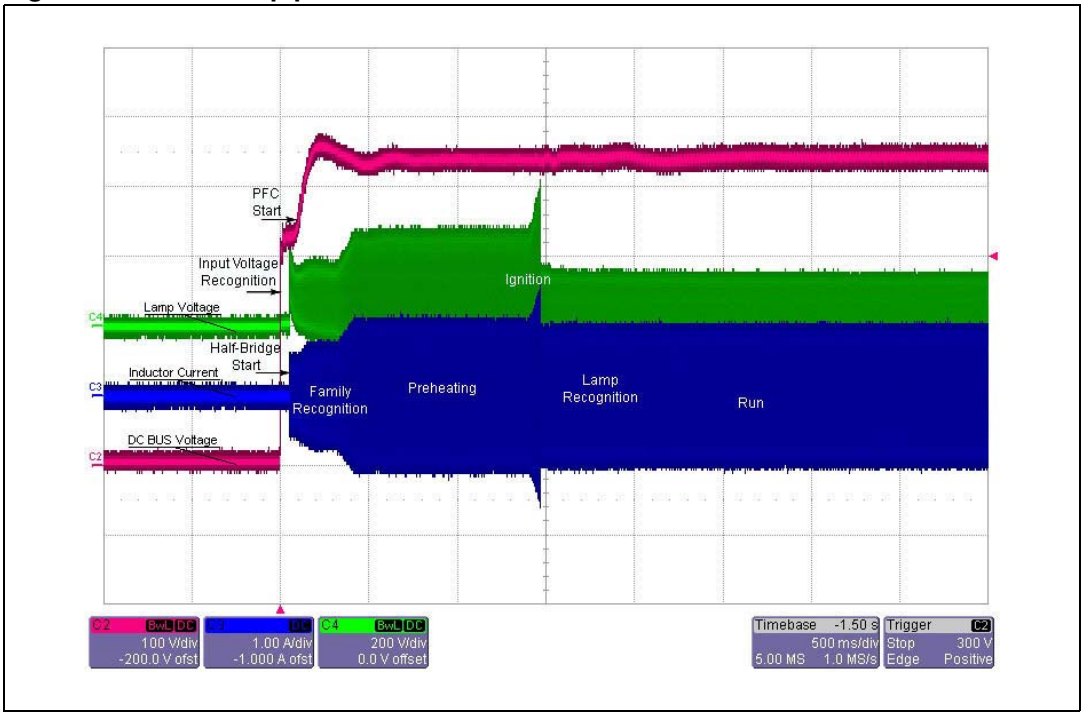


Figure 29. 54 W lamp power

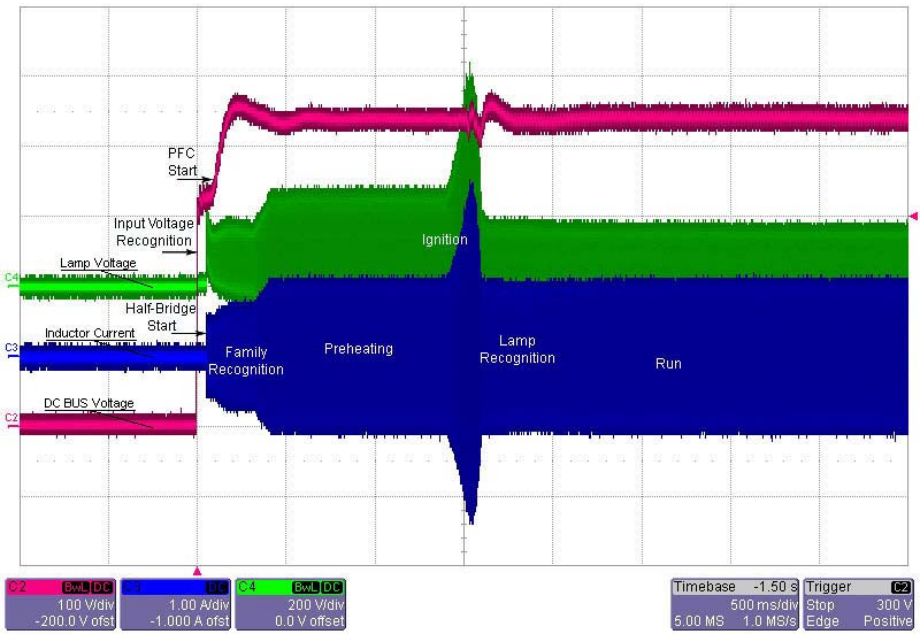
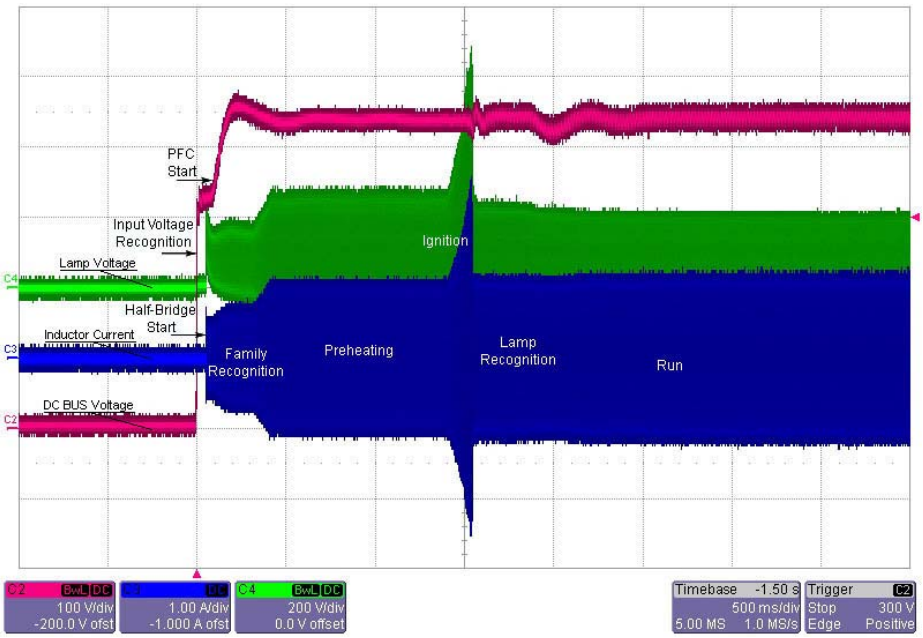


Figure 30. 80 W lamp power



In *Figure 27*, *28*, *29*, and *30* it can be seen that the ballast identifies each lamp and that after the recognition phase it adjusts and regulates the half-bridge working frequency to supply the correct current to the lamp.

6.3.2 PF, THD and ballast efficiency

The power factor, total harmonic distortion of current and ballast efficiency are measured and the results are shown in *Table 4*, *5*, *6*, and *7*.

Table 4. 24 W lamp power

Mains	PF	THD	η %
185 V at 50 Hz	0.968	17.6	88.2
230 V at 50 Hz	0.949	20.0	89.3
265 V at 50 Hz	0.923	22.0	89.9

Table 5. 39 W lamp power

Mains	PF	THD	η %
185 V at 50 Hz	0.983	13.5	90.4
230 V at 50 Hz	0.970	15.7	90.6
265 V at 50 Hz	0.956	17.4	90.6

Table 6. 54 W lamp power

Mains	PF	THD	η %
185 V at 50 Hz	0.989	11.3	94.1
230 V at 50 Hz	0.982	13.0	94.4
265 V at 50 Hz	0.972	14.4	94.6

Table 7. 80 W lamp power

Mains	PF	THD	η %
185 V at 50 Hz	0.992	10.9	97.6
230 V at 50 Hz	0.988	11.1	98.0
265 V at 50 Hz	0.980	14.6	98.2

6.3.3 Electromagnetic compatibility

The EMC tests have been performed according to the EN55015 standard (Limits and methods of measurement of radio disturbance characteristics of electrical lighting and similar equipment).

The Agilent E7401A EMC Analyzer has been used as test equipment.

Figure 31. Test equipment

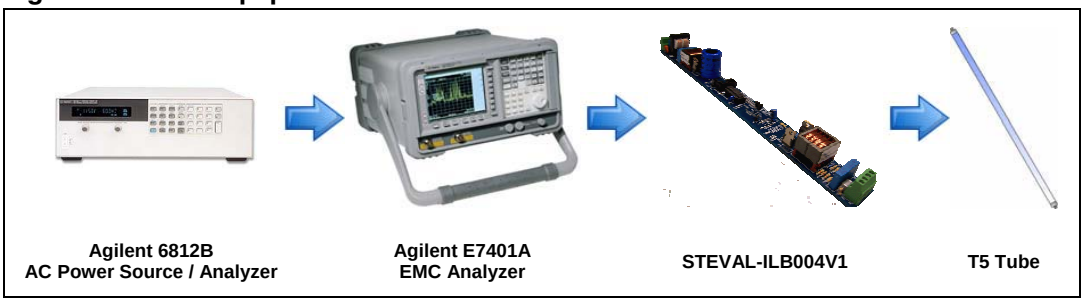


Figure 32, *33*, *34*, and *35* show the results.

Figure 32. 24 W

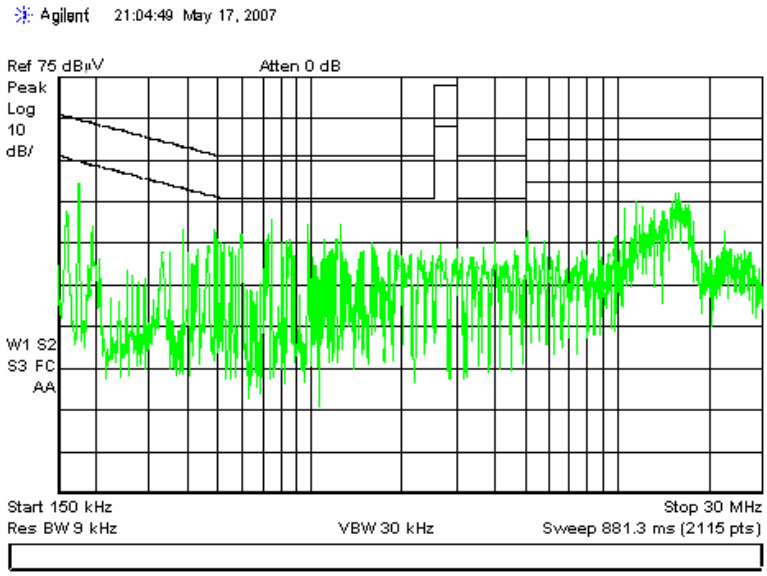


Figure 33. 39 W

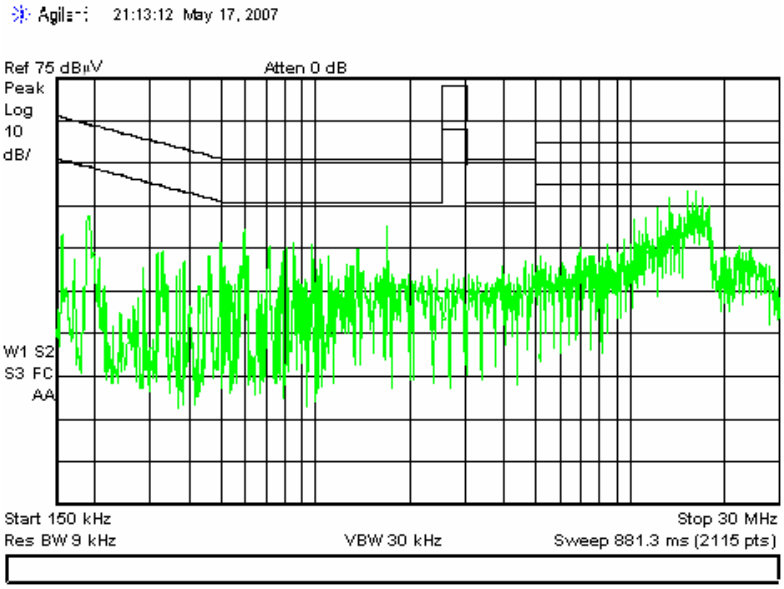


Figure 34. 54 W

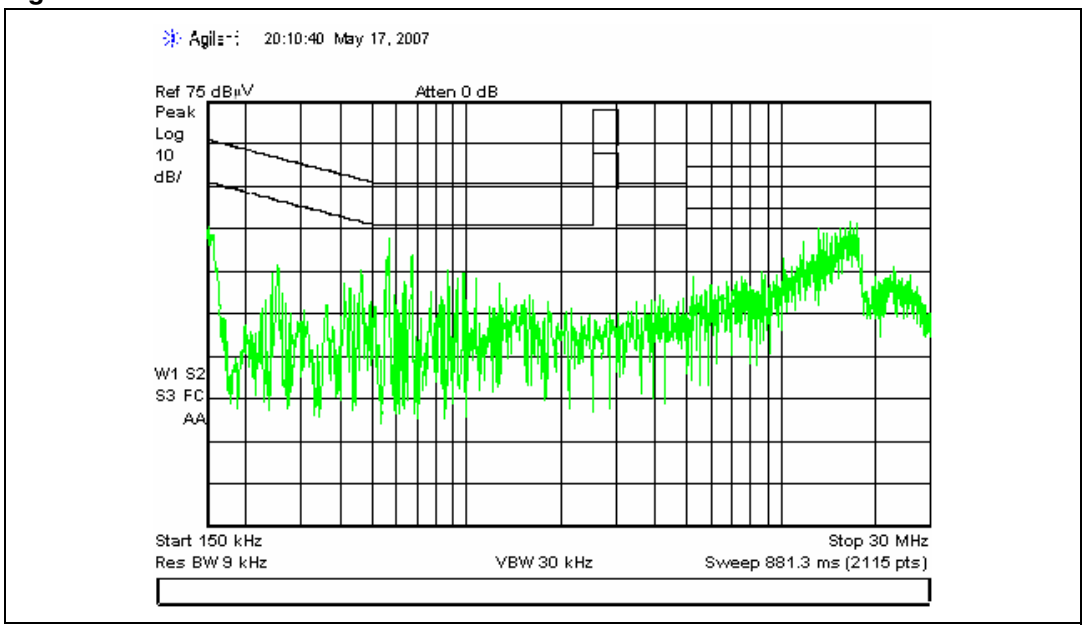
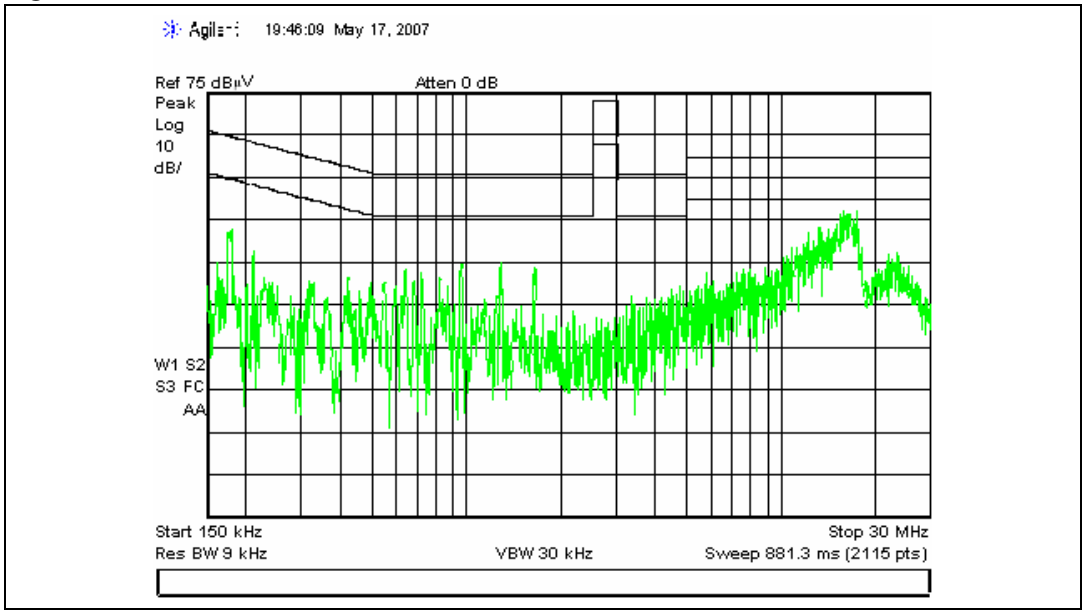


Figure 35. 80 W



7 Conclusion

The proposed microcontrolled multipower ballast has several advantages. Design and production cost are reduced as there is no need for different circuits to drive different lamps. Moreover, by using the microcontroller, the systems' present flexibility from a design point of view respects that of an analog circuit. With the use of STMicroelectronics' Power MOSFET and diodes, the circuit shows good overall efficiency results.

8 References

1. AN966: L6561, Enhanced Transition Mode Power Factor Corrector
2. STMicroelectronics ST7LITE1xB (8-BIT MCU with single voltage flash memory, data EEPROM, ADC, 5 Timers, SPI) datasheet
3. STMicroelectronics L6382D5 (Power management unit for microcontrolled ballast) datasheet

9 Revision history

Table 8. Document revision history

Date	Revision	Changes
28-Jan-2008	1	Initial release