AN2738
Application note

L6390 half-bridge gate driver

Introduction

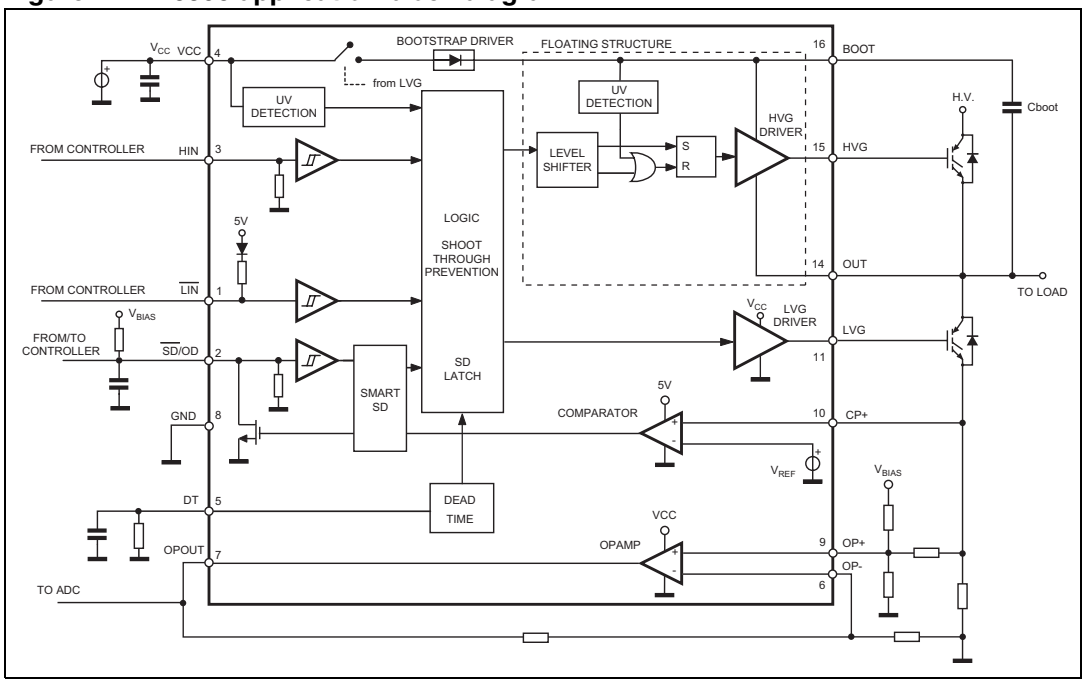
The L6390 is a versatile high voltage gate driver IC which is particularly suited for field oriented control (FOC) motor driving applications. It simplifies the design of control systems for a wide range of motor applications such as home appliances, industrial drives, DC motors and fans.

Designed using BCD off-line technology, this device is capable of operating with voltage rails up to 600 V. The gate driver provides all the functions and current capability necessary for high side and low side power MOSFET and IGBT driving.

The L639x series are high voltage half-bridge gate drivers. These devices can be used in all applications where high voltage shifted control is necessary. The devices have a driver current capability best suited for home appliance motor driving ratings, and they are also equipped with patented internal circuitry which replaces the external bootstrap diode. This feature is achieved by means of a high voltage DMOS synchronously driven with the low side gate driver.

The L6390 is a half-bridge driver with several functions such as externally adjustable dead-time, interlocking, smart shutdown (patented), fault comparator and a dedicated high performance op-amp for advanced current sensing. The outputs can be driven by two dedicated logic signals or, alternatively, only one logic signal by connecting the two inputs together. The device is available in the DIP16 or SO16 packages.

Figure 1. L6390 application block diagram



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1 Pin description

Table 1. Pin description

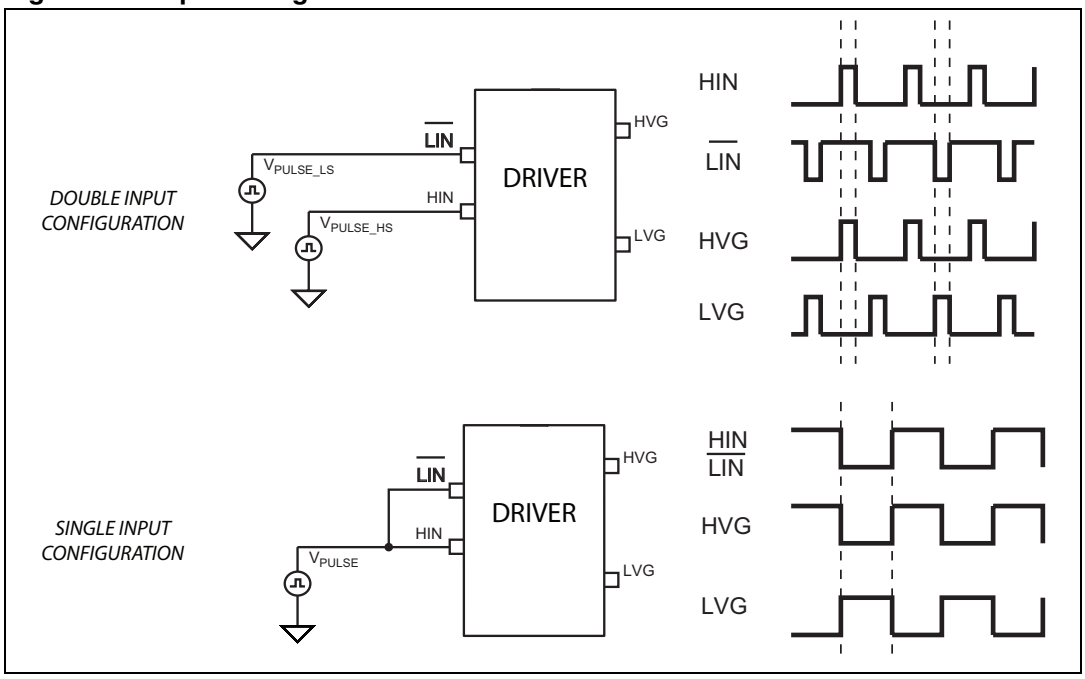
Pin n°	Pin name	Type	Function
1	$\overline{LIN}$	I	Low side driver logic input (active low)
2	$\overline{SD}$/OD(1)	I/O	Shutdown logic input (active low)/open drain (comparator output)
3	HIN	I	High side driver logic input (active high)
4	VCC	P	Lower section supply voltage
5	DT	I	Dead time setting
6	OP-	I	Op-amp inverting input
7	OPOUT	O	Op-amp output
8	GND	P	Ground
9	OP+	I	Op-amp non inverting input
10	CP+	I	Comparator input
11	LVG(1)	O	Low side driver output
12,13	NC		Not connected
14	OUT	P	High side (floating) common voltage
15	HVG(1)	O	High side driver output
16	BOOT	P	Floating section (bootstrap) supply voltage

1. The circuit provides less than 1 V on the LVG and HVG pins (@ I_{sink} = 10 mA), with VCC > 3 V. This allows the omission of the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low. The gate driver ensures low impedance in SD conditions also. See *Section 4*.

2 Logic inputs

The L6390 has two logic inputs, HIN and $\overline{\text{LIN}}$, to separately control the high side and low side outputs, HVG and LVG. HIN is in phase with HVG, while $\overline{\text{LIN}}$ is out of phase with LVG. The signal inversion on the low side input allows control of the half-bridge output with only one control signal (see *Figure 2*).

Figure 2. Input configuration



Note that by connecting the two logic input signals together, the resulting dead time is defined by the resistor connected between pin 5 and ground. The dead time can be set to a wide range of values from hundreds of nanoseconds to a few microseconds (see *Figure 5* or the L6390 datasheet). All the logic inputs are provided with hysteresis (~1 V) for low noise sensitivity and are TTL//CMOS 3.3 V compatible. Thanks to this low voltage interface logic compatibility, the L6390 can be used with any kind of high performance controller, such as microcontrollers, DSPs or FPGAs.

As shown in the block diagram in *Figure 1*, the logic inputs have internal pull-down (or pull-up) resistors. The purpose of these resistors is to set a proper logic level in case, for example, there is an interruption in the logic lines or the controller outputs are in tri-state conditions. If logic inputs are left floating, the gate driver outputs LVG and HVG are set to low level. The internal resistors are:

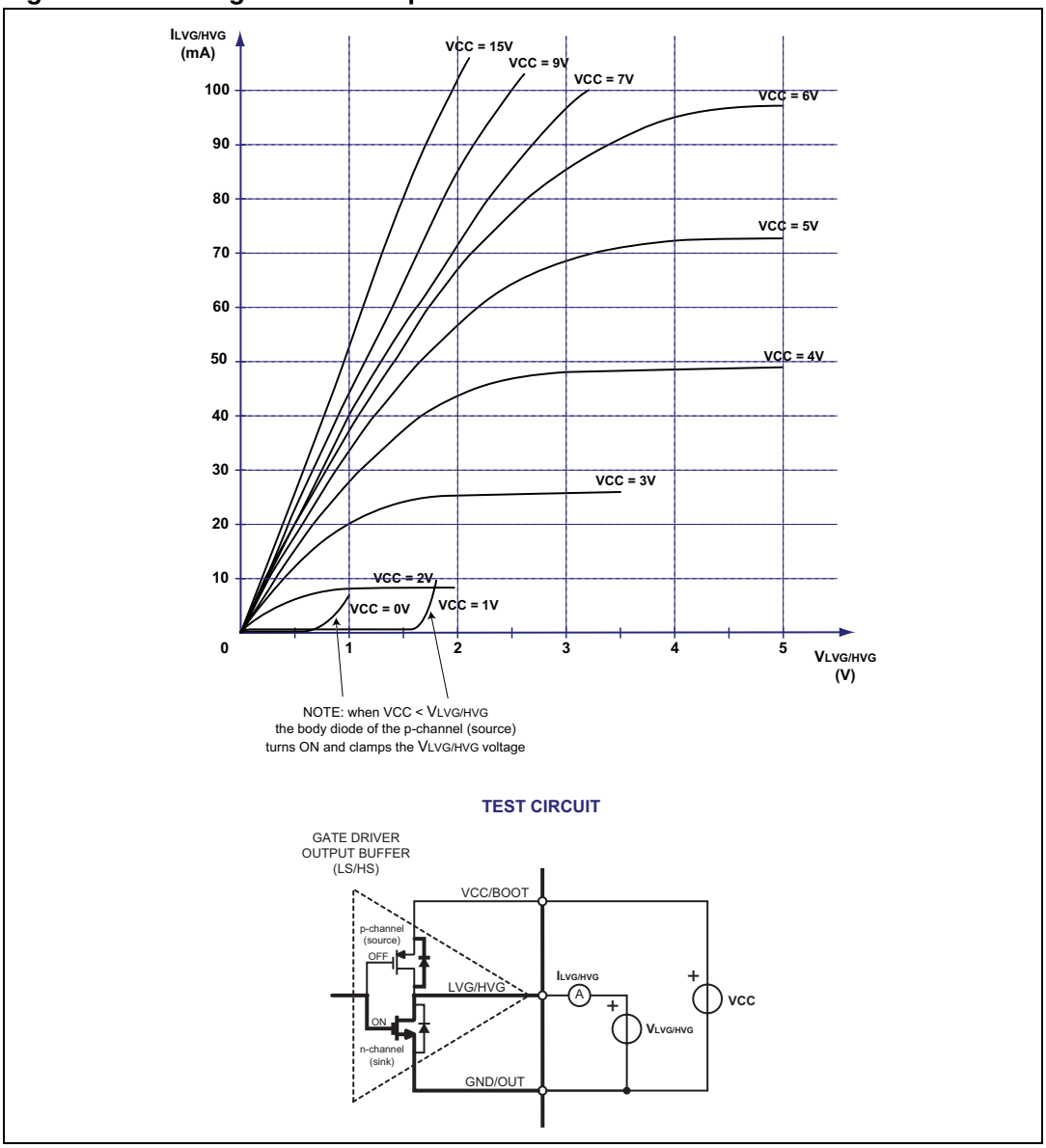
- HIN logic input: 85 kΩ (typ.) pull-down
- $\overline{\text{LIN}}$ logic input: 720 kΩ (typ.) pull-up connected to an internal 5 V regulator through a diode
- $\overline{\text{SD}}$ logic input: 375 kΩ (typ.) pull-down

If the logic inputs are connected together as in the single input configuration (*Figure 2*) and they are left floating, the internal pull-down and pull-up resistors form a resistive divider providing a voltage value (about 460 mV) which keeps the HVG off and LVG on, thus turning on the low side power switch.

3 UVLO function

The L6390 supply voltage VCC is continuously monitored by an under-voltage lockout (UVLO) circuitry which turns off the IC outputs when the supply voltage goes below the V_{CC_thOFF} threshold (see L6390 datasheet for values) and turns on the device when the supply voltage goes above the V_{CC_thON} voltage. A hysteresis of about 1.5 V is provided for noise rejection purpose. The high voltage floating supply VBOOT is provided with a similar under-voltage lockout circuitry also. When the L6390 is in UVLO condition, both gate driver outputs are set to low level, setting the half-bridge power stage output to high impedance. *Figure 3* below shows the I-V characteristics of the output buffers at different VCC values.

Figure 3. L6390 gate driver outputs in UVLO condition



4 Dead time and interlocking function management

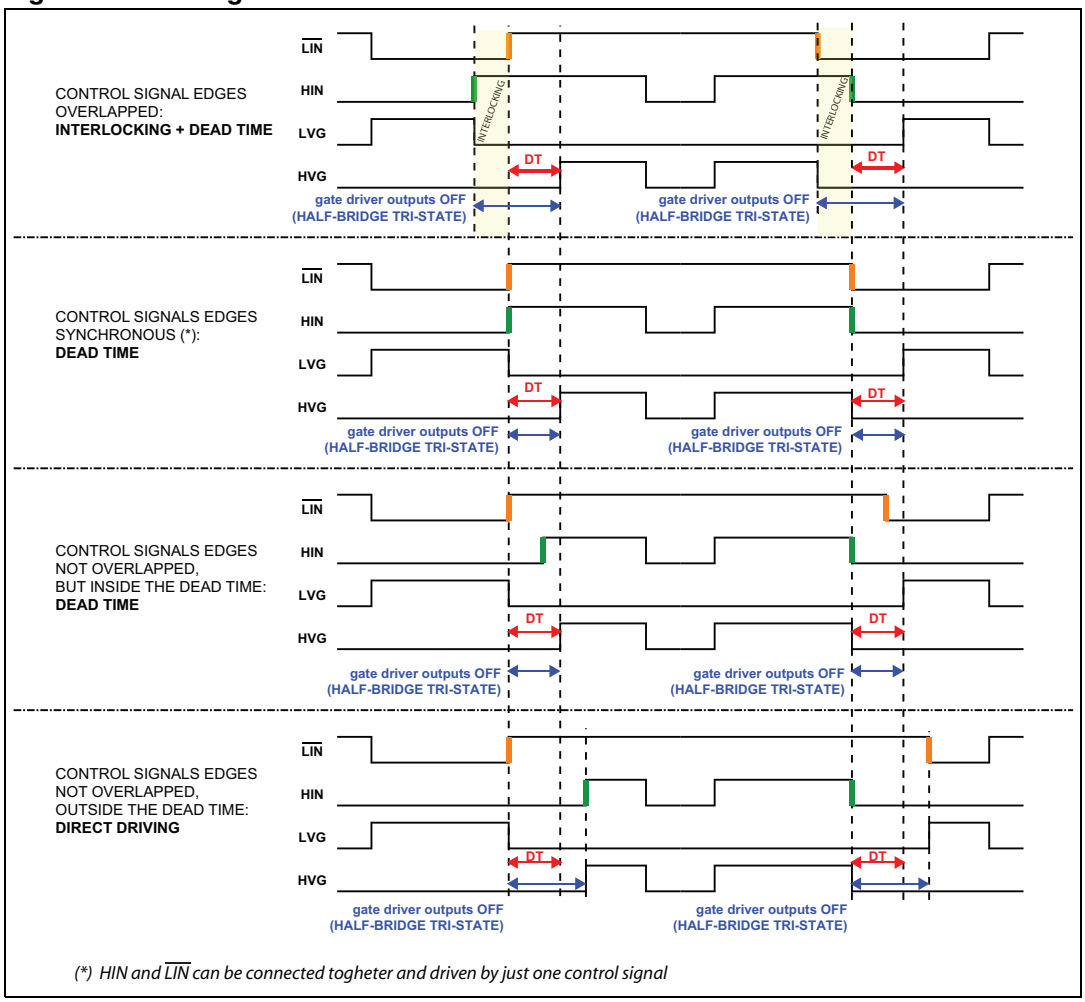
In order to avoid any possible cross-conduction between the power MOSFETs/IGBTs of the half-bridge, the L6390 provides both the dead time and the interlocking functions. The interlocking function is a logic operation which sets both the outputs to low level when the inputs are simultaneously active (HIN to high level and $\overline{\text{LIN}}$ to low level). The dead time function is a safety time introduced by the device between the falling edge transition of one driver output and the rising edge of the other output. If the rising edge set externally by the user occurs before the end of this dead time, it is ignored and results delayed until the end of the dead time. The dead time can be adjusted externally through the value of the DT resistor connected between pin 5 and pin 8 (see *Figure 5*). A 100 nF ceramic capacitor in parallel with this resistor is recommended for noise immunity. In *Figure 4* the details of dead time and interlocking function management are described.

Table 2. L6390 truth table

Inputs			Outputs	
$\overline{\text{SD}}$	$\overline{\text{LIN}}$	HIN	LVG	HVG
L	X(1)	X(1)	L	L
H	H	L	L	L
H	L	H	L	L
H	L	L	H	L
H	H	H	L	H

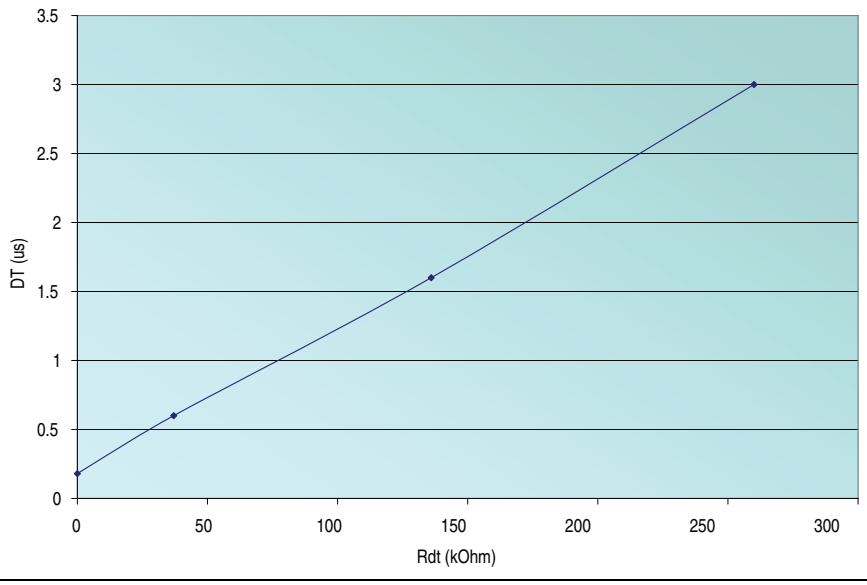
1. Don't care

Figure 4. Timing waveforms



(*) HIN and $\overline{LIN}$ can be connected togheter and driven by just one control signal

Figure 5. Typical dead time vs. DT resistor value

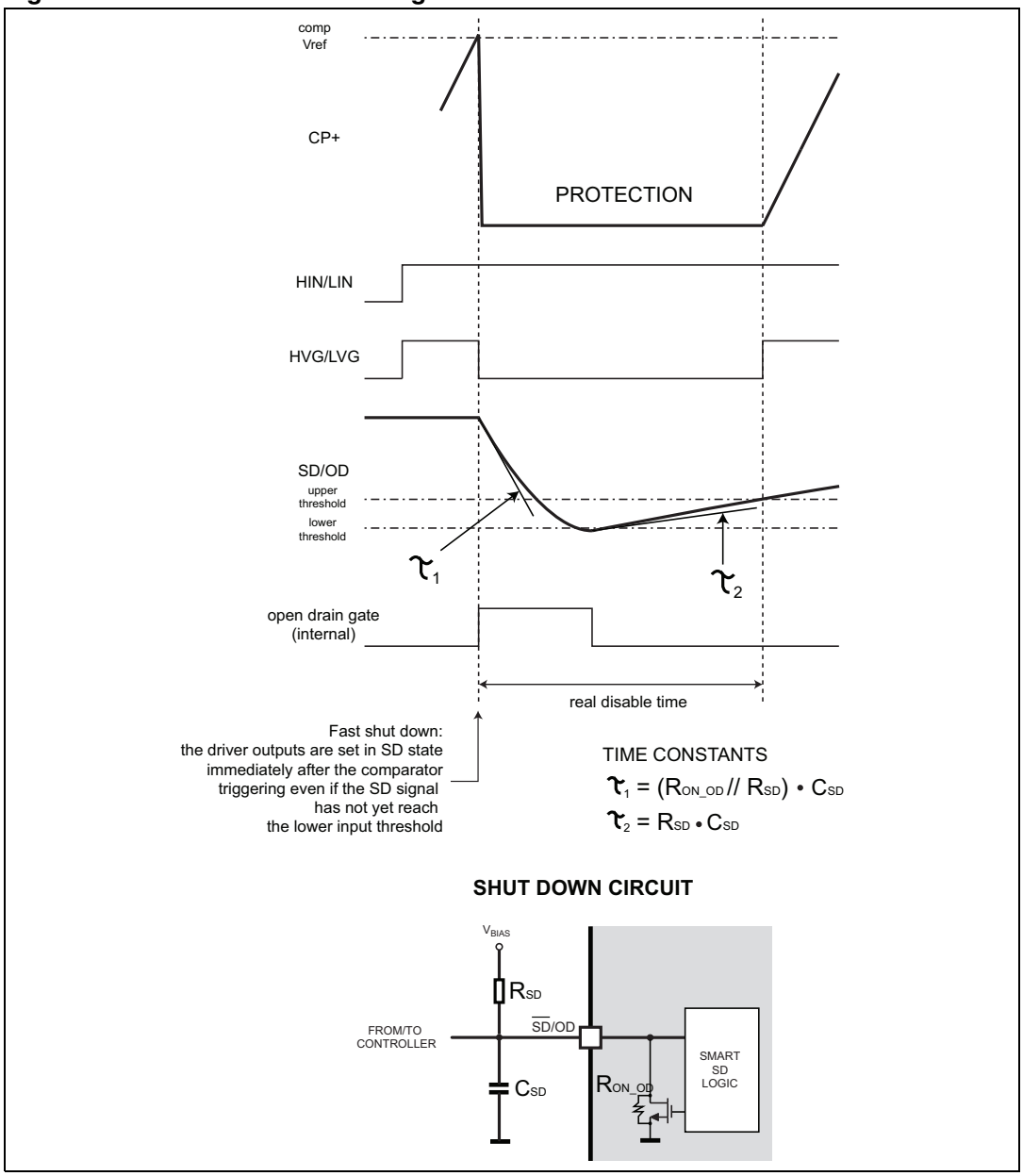


5 Smart shutdown function

The L6390 integrates a comparator for fault sensing purposes. The comparator has an internal reference voltage V_{ref} on its inverting input (see L6390 datasheet), while the non-inverting input is available on pin 10. The comparator input can be connected to an external shunt resistor in order to implement a simple over-current detection function. The output signal of the comparator is fed to an integrated MOSFET with the open drain available on pin 2, shared with the $\overline{SD}$ input.

When the comparator triggers, the device is set in shutdown state and both its outputs are set to low level leading the half-bridge in tri-state.

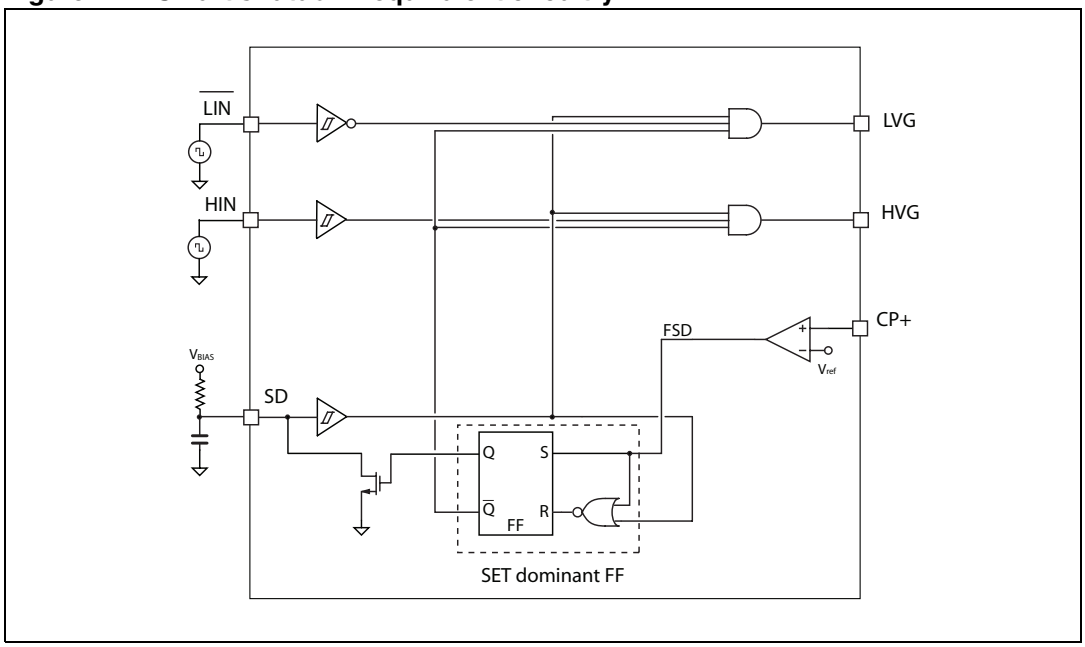
Figure 6. Smart shutdown timing waveforms



In common over-current protection architectures the comparator output is usually connected to the $\overline{SD}$ input and an RC network is connected to this $\overline{SD}$/OD line in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Unlike common fault detection systems, the L6390 smart shutdown architecture allows to immediately turn-off the output gate driver in case of fault, by minimizing the propagation delay between the fault detection event and the actual outputs switch-off. In fact the time delay between the fault and the outputs turn-off is no more dependent on the RC value of the external network connected to the pin. In the smart shutdown circuitry, the fault signal has a preferential path which directly switches off the outputs after the comparator triggering. At the same time the internal logic turns on the open drain output and holds it on until the SD voltage goes below the SD logic input lower threshold. The smart SD system provides the possibility to increase the time constant of the external RC network (that is the disable time after the fault event) without increasing the delay time of the protection. Any external signal provided to the SD pin is not latched and can be used as control signal in order to perform, for instance, PWM chopping through this pin. In fact when a PWM signal is applied to the SD input and the logic inputs of the gate driver are stable, the outputs switch from the low level to the state defined by the logic inputs and vice-versa.

A block diagram of the smart shutdown architecture is depicted in *Figure 7*.

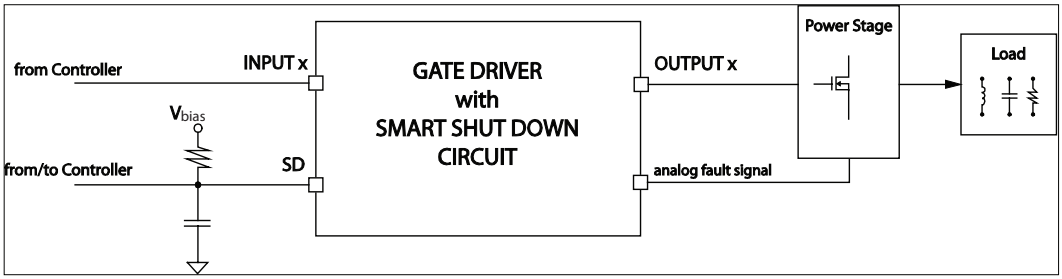
Figure 7. Smart shutdown equivalent circuitry



In normal operation the outputs follow the commands received from respective input signals. When a fault detection event occurs the fault signal (FSD) is set to high by the fault detection circuit output (LVG, HVG) and the FF receives a SET input signal. Consequently the FF outputs set output signals to low level and, at the same time, turn-on the open drain MOSFET which works as active pull-down for the SD signal. Note that the gate driver outputs stay at low level until the $\overline{SD}$ pin has experienced both a falling edge and a rising edge, although the fault signal could be returned to low level immediately after the fault sensing. In fact even if the FF is reset by the falling edge of the $\overline{SD}$ input, the SD signal also works as enable for the outputs, thanks to the two AND ports. Moreover once the internal open-drain transistor has been activated, due to the latch, it cannot be turned-off until the $\overline{SD}$ pin voltage reaches the low logic level. Note that, since the FF is SET dominant,

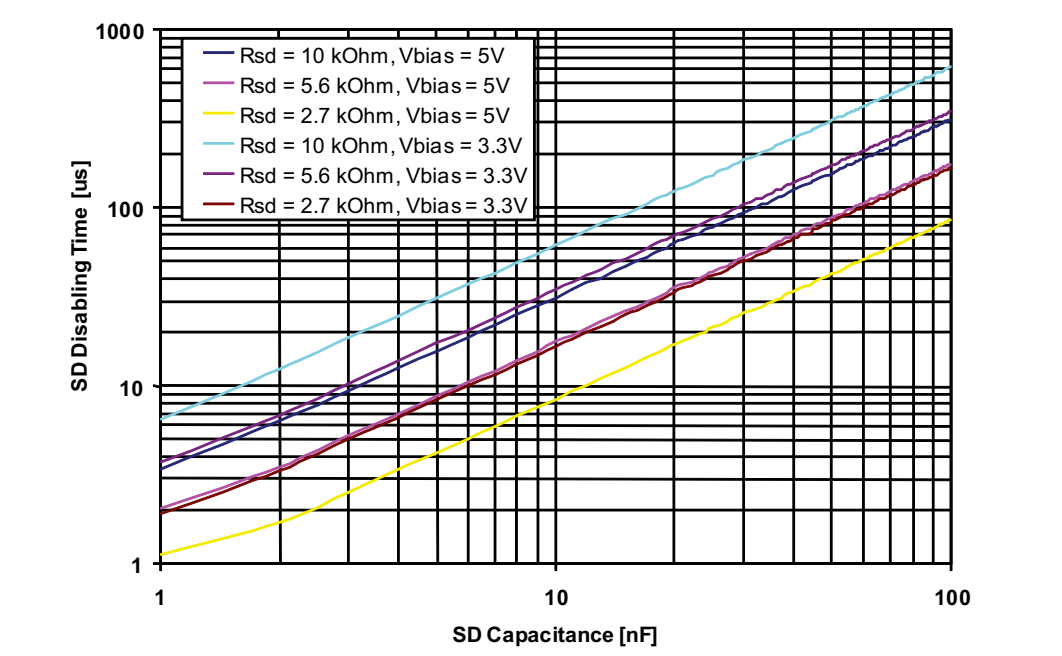
oscillations of the $\overline{SD}$ pin are avoided if the fault signal remains steady at high level. The block diagram of a power system using the gate driver with the smart shutdown architecture is shown in *Figure 8*. An RC network is used to implement the disable time after a fault detection event.

Figure 8. Protection scheme



In *Figure 9* the typical duration of the disable time vs. the SD capacitance with different R_{sd} values and V_{bias} values is shown.

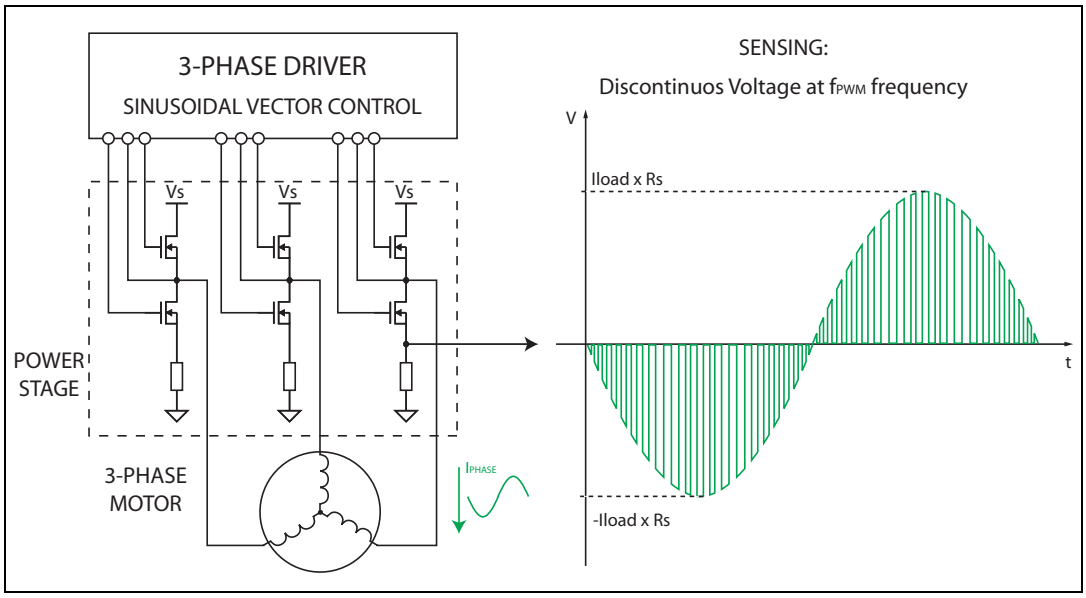
Figure 9. Disable time vs. SD capacitance (typical values)



6 L6390 op-amp

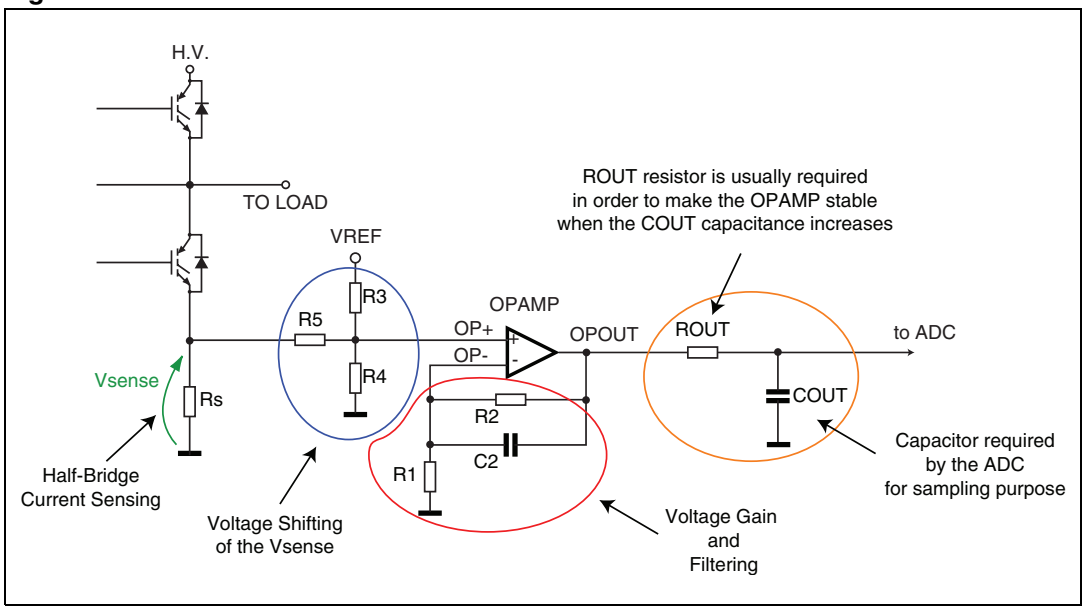
The L6390 integrates an operational amplifier optimized for field oriented control (FOC) applications. In a typical FOC application a tri-phase power bridge is used and the currents in the three half-bridges are sensed using a shunt resistor on the source of each low side power switch. The analog current information is transformed in a discontinuous sense voltage signal, available only when the current is flowing in the low side path and having the same frequency of the PWM signal driving the bridge. The sense voltage is a bipolar analog signal, which sign depends on the direction of the current (see *Figure 10*):

Figure 10. 3-phase system



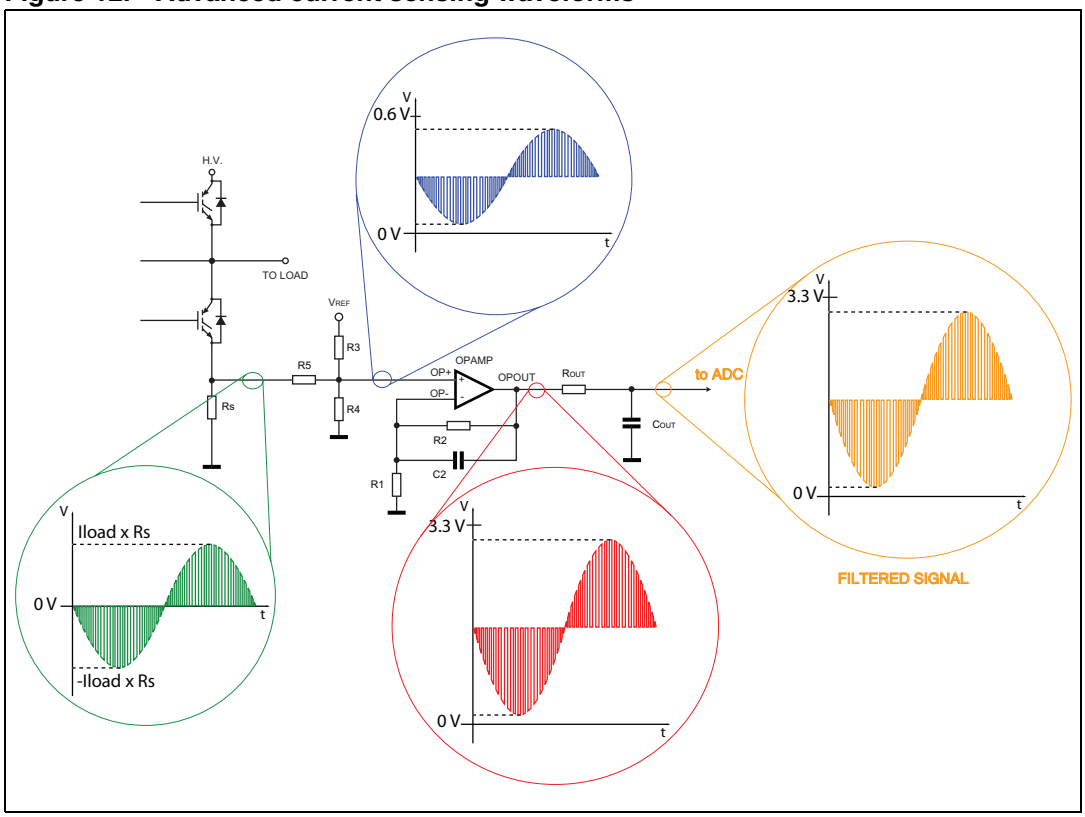
PWM frequency in a typical home appliance motor driver application is in the range of 5-20 kHz. The sense voltage signals must be provided to an A/D converter in order to perform the matrix calculation related to a certain control technique. Those sense signals are usually shifted and amplified by dedicated op-amps in order to exploit the full range of the A/D converter. The typical scheme shown in *Figure 11* is used.

Figure 11. General advanced current sense scheme



Principle waveforms corresponding to the above scheme are provided in *Figure 12*:

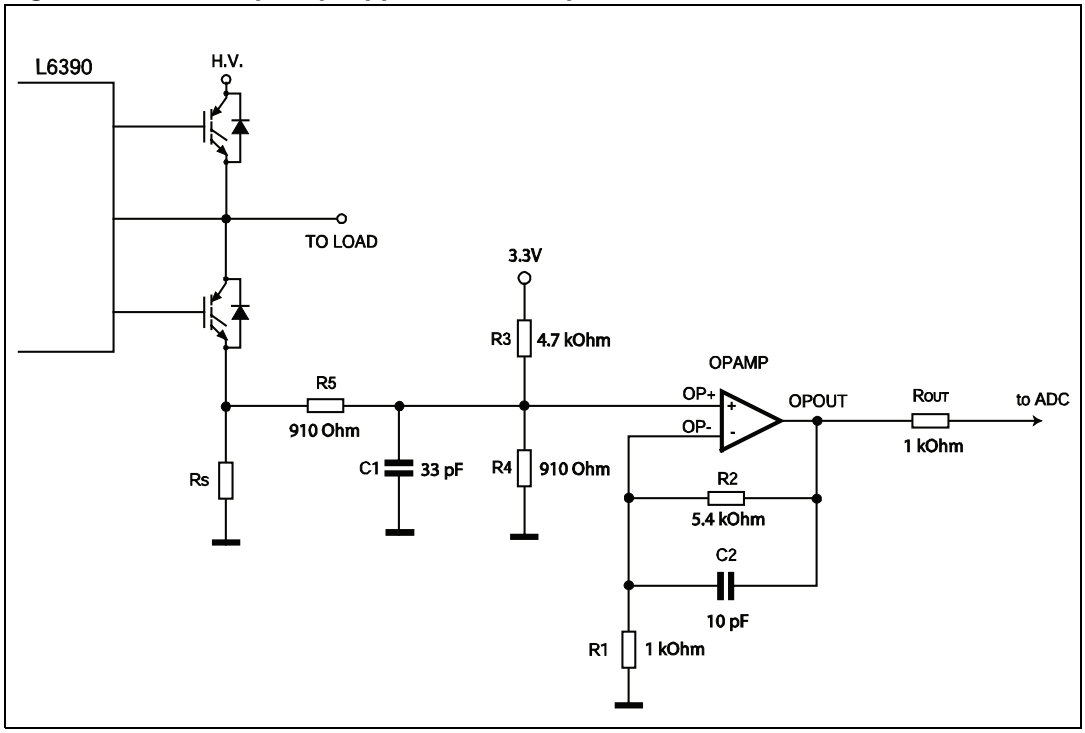
Figure 12. Advanced current sensing waveforms



ADCs used in vector control applications have a typical FSR of about 3.3 V. The sense signals have to be shifted and centered on FSR/2 voltage (about 1.65 V) and amplified with a gain which provides the matching between the maximum value of the sensed signal and

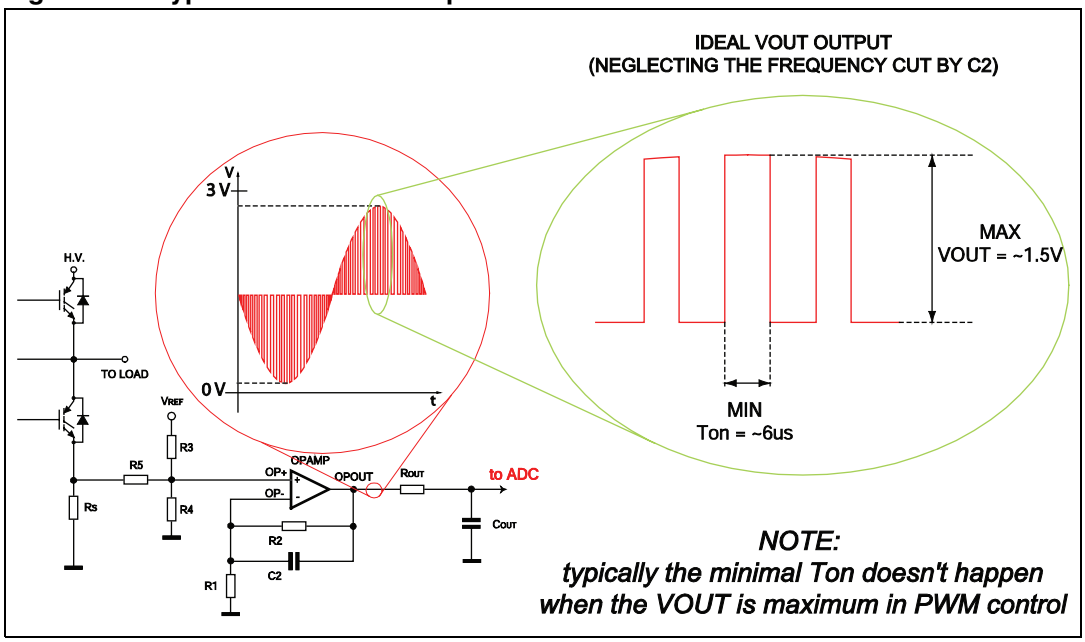
the FSR of the ADC. In *Figure 13* an application circuit of the op-amp with typical passive components values is shown.

Figure 13. L6390 op-amp, application example



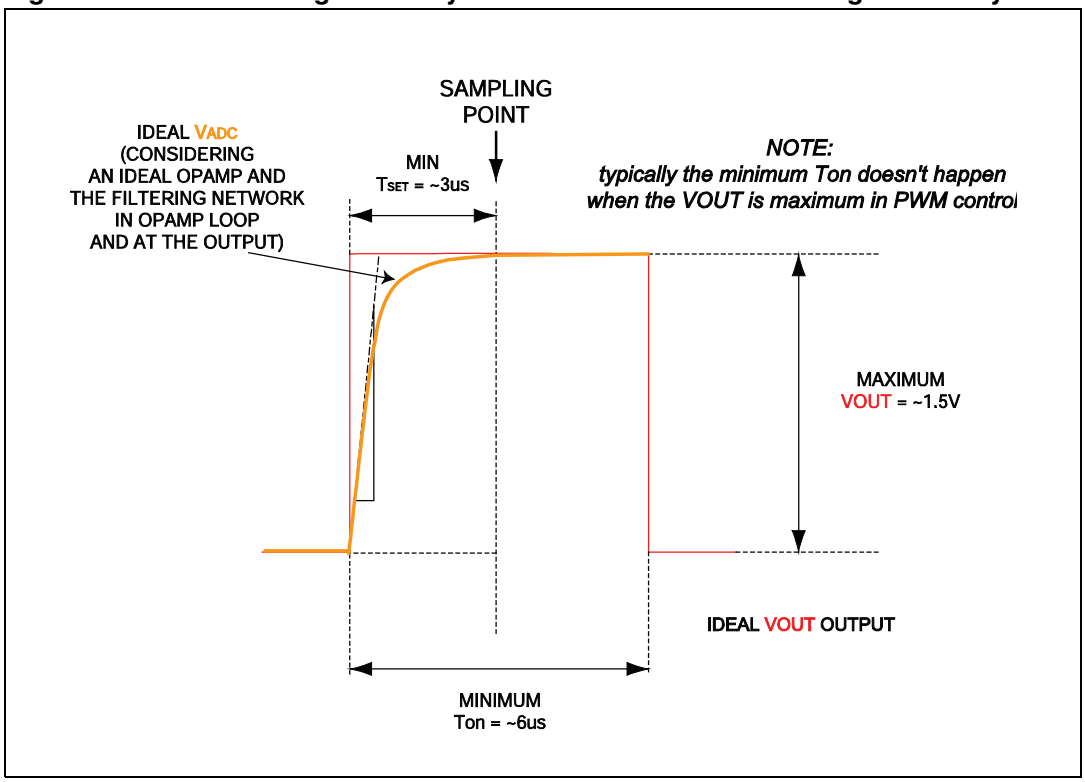
Following *Figure 14* shows the output voltage waveform of the L6390 op-amp considering the voltage level shifting and the gain amplification provided by the amplifier configuration of the op-amp, neglecting the low-pass filtering action of the feedback network. In particular the waveform is zoomed on the maximum amplitude of PWM sinusoidal voltage signal which represents the extreme condition for the external slew rate of the op-amp. The required external slew rate increases proportionally to the voltage excursion and reverse proportionally to the ON time of PWM output.

Figure 14. Typical L6390 ideal output



Typically the maximum voltage variation on op-amp output is FSR/2 (about 1.65 V) and the ON time usually does not show its minimum value where the PWM voltage amplitude is higher. In fact the duty cycle of each half-bridge of the 3-phase power stage is proportional to the average voltage applied to each 3-phase terminal which normally is not in phase with the output current of the same bridge, due to the load angle and the BEMF of the running motor. The ADC front-end usually samples the op-amp output voltage in the middle of the ON time, so the output must approach its final value as much as possible within one half of the ON-time. Considering a minimum ON time of about 6 µs, the op-amp output settling time must be lower than 3 µs. If the maximum output voltage variation is 1.5 V and the maximum time needed to reach the desired value is 3 µs, the minimum SR requirement for proper operation would be 1.5 V/ 3 µs = 0.5 V/µs (see *Figure 15*).

Figure 15. Detail on single PWM cycle in advanced current sensing for FOC systems



7 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 16* a). In the L6390 a patented integrated structure replaces the external diode. It is realized with a high voltage DMOS driven synchronously with the low side driver (LVG), with a diode in series, as shown in *Figure 16* b. An internal charge pump (*Figure 16*.b) provides the DMOS driving voltage.

7.1 C_{BOOT} selection and charging

To choose the proper C_{BOOT} value the external MOSFET can be seen as an equivalent capacitor. This capacitor C_{EXT} is related to the MOSFET total gate charge:

Equation 1

$$C_{EXT} = \frac{Q_{GATE}}{V_{GATE}}$$

The ratio between the capacitors C_{EXT} and C_{BOOT} is proportional to the cyclical voltage loss. It has to be:

Equation 2

$$C_{BOOT} \gg C_{EXT}$$

For example: if Q_{GATE} is 30 nC and V_{GATE} is 10 V, C_{EXT} is 3 nF. With C_{BOOT} = 100 nF the drop would be 300 mV.

If HVG has to be supplied for a long time, the C_{BOOT} selection has to take into account also the leakage and quiescent losses.

For example: since the HVG steady state consumption is lower than 200 µA, if HVG T_{ON} is 5 ms then CBOOT has to supply 1 µC to C_{EXT}. This charge on a 1 µF capacitor means a voltage drop of 1 V.

The internal bootstrap driver gives a great advantage: the external fast recovery high voltage diode can be avoided (it usually has great leakage current). This structure works if V_{OUT} is close to GND (or lower) and in the meanwhile the LVG is on. The charging time (T_{charge}) of C_{BOOT} is the time in which both conditions are fulfilled and it has to be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS $R_{DS(on)}$. At low frequency of operation this drop can be neglected, but if the frequency is increased the drop must be taken into account.

The following equation is useful to compute the drop on the bootstrap DMOS:

Equation 3

$$V_{DROP} = I_{CHARGE} \cdot R_{DS(on)} \rightarrow V_{DROP} = \frac{Q_{GATE}}{T_{CHARGE}} \cdot R_{DS(on)}$$

where Q_{GATE} is the gate charge of the external power MOSFET, $R_{DS(on)}$ is the on resistance of the bootstrap DMOS and T_{CHARGE} is the charging time of the bootstrap capacitor.

For example: given the typical value of 120 Ω for $R_{DS(on)}$ and using a power MOS with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V if the T_{CHARGE} is 5 µs. In fact:

Equation 4

$$V_{DROP} = \frac{30nc}{5\mu s} \cdot 120\Omega \approx 0.7V$$

V_{DROP} has to be considered when the voltage drop on C_{BOOT} is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

Working at very low frequencies the high side driver on-time can be very long. So C_{BOOT} voltage can drop because of HVG steady state consumption. To avoid extremely large capacitor (> 1-2 µF) an external charge pump can be added (see *Figure 17* as example). It is mandatory for the diodes to have a low parasitic capacitance, because C1 and C2 should be greater than diodes capacitance. The oscillator has to work in order to balance the high voltage side consumption, and the minimum frequency is fixed by C1 and C2 values (with C1 = C2 = 33 pF then f > 250 - 300 kHz).

Figure 16. Bootstrap driver

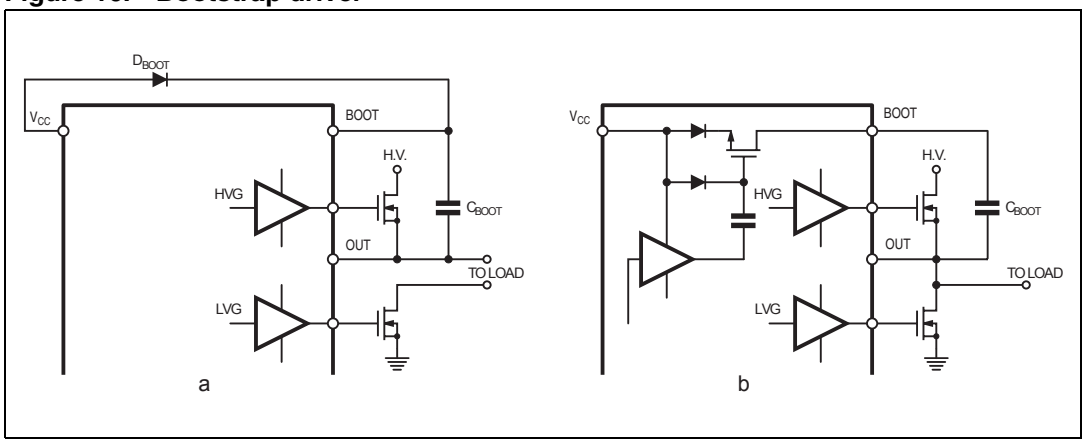
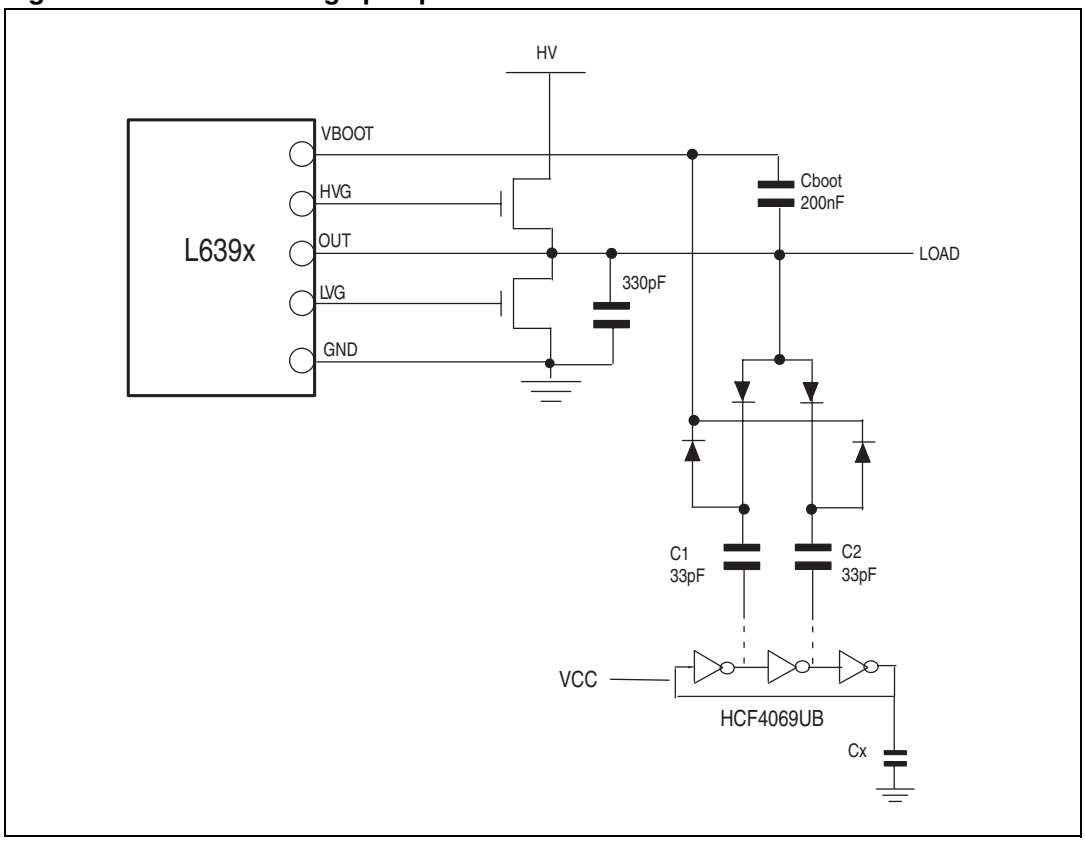


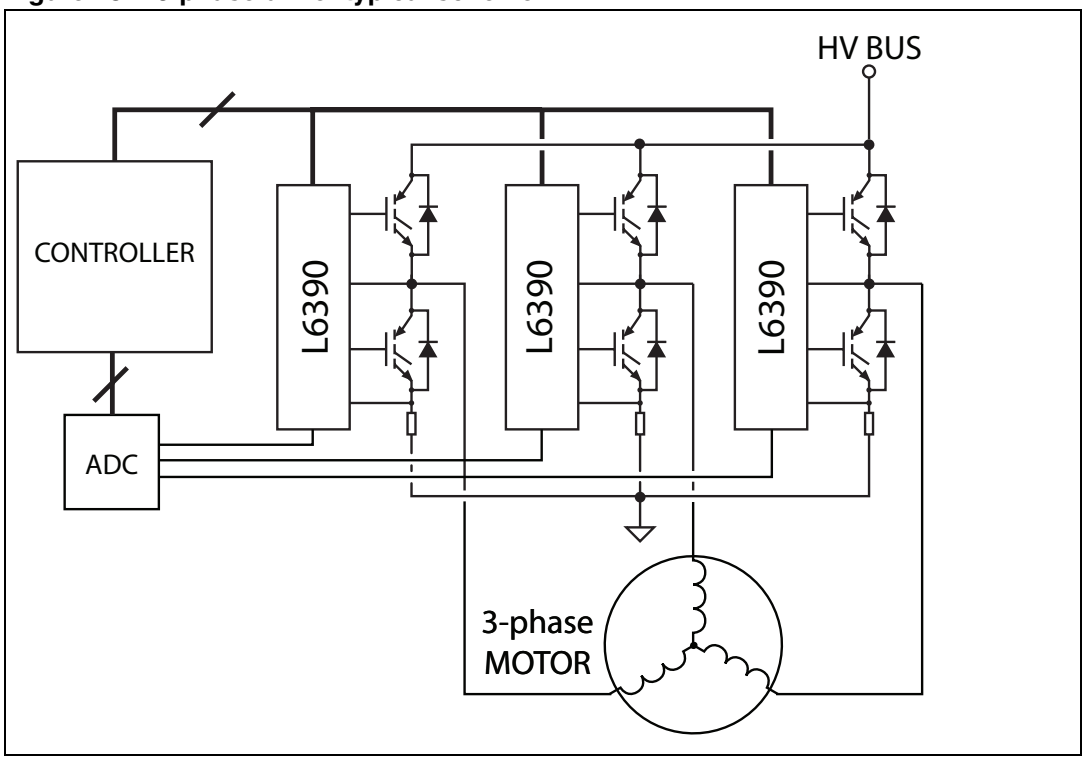
Figure 17. External charge pump



8 Application example

A typical scheme for a 3-phase inverter application is shown in *Figure 18*. In order to drive a 3-phase load as for example a BLDC or Induction AC motor, three L6390 ICs can be used.

Figure 18. 3-phase drive- typical scheme

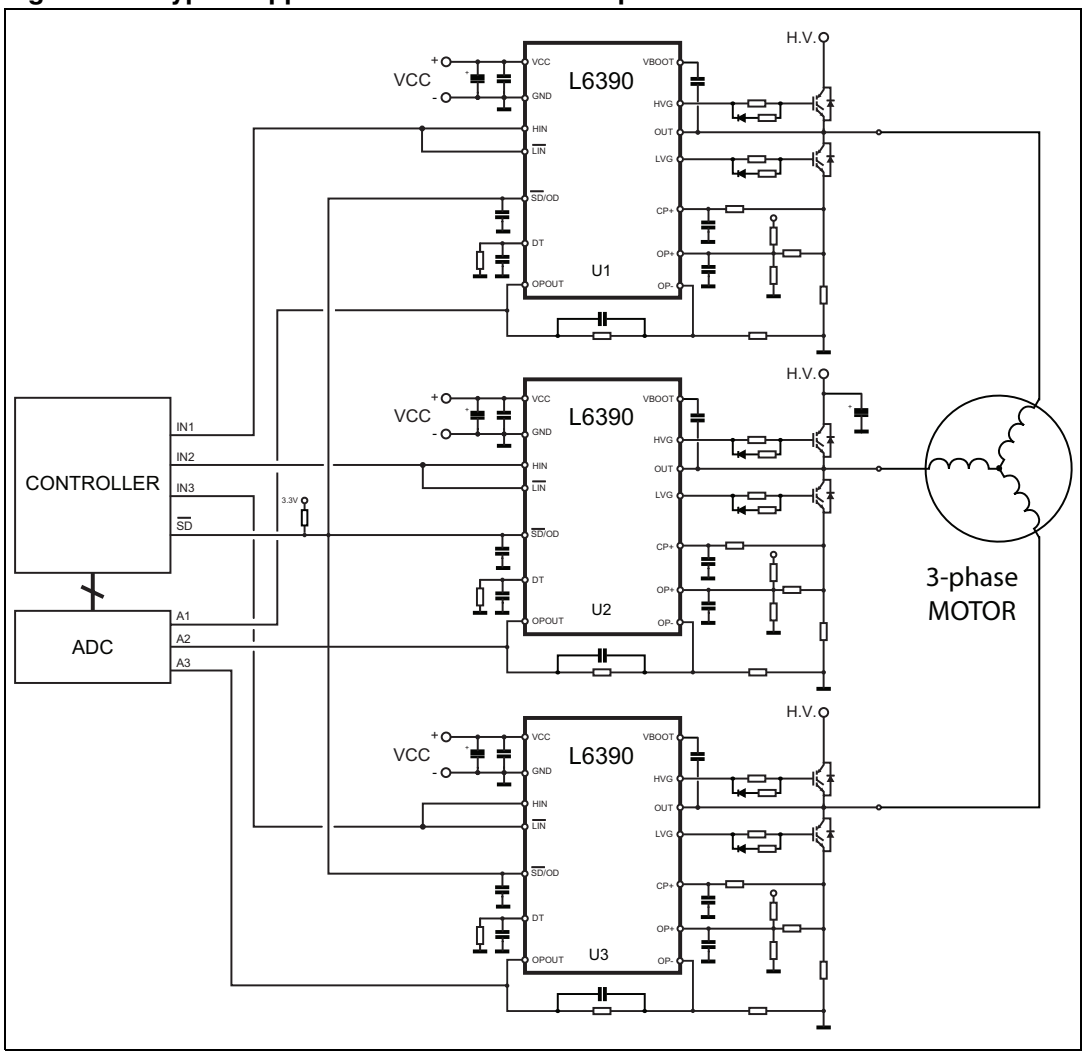


Each L6390 IC drives one half-bridge of the 3-phase power stage. The three gate drivers are driven by the controller and the sensing signals coming from the power stage are managed directly by the L6390 analog blocks (comparators and op-amps) which provide the proper feedback signals to the ADC and the system controller. Each half-bridge comprises two power switches such as IGBTs (or MOSFETs), one high side and one low side. When the high side switch is ON, it brings the output voltage of the half-bridge to the HV bus voltage, which can be a high DC voltage power supply with large power availability, while the low side switch shorts the output to power ground voltage when it is ON. Thanks to the internal floating structure for the high side switch driving, n-type IGBTs (or N-channel MOSFETs) can be used. The gate drivers work exactly as digital/analog-power interface between the controller and the power stage. A shunt resistor can be placed between each low side switch and the power ground, to sense the current on each low side. The information contained in each current sense signal can be conditioned by the L6390 op-amp as described in *Section 6*.

In *Figure 19* a more detailed schematic of a 3-phase power stage topology is shown. Note that usually is recommended (not mandatory) to have some gate resistances between each power switch gate and the correspondent gate driver output, in order to limit the current during the gate charge. Then some filtering and/or level shifting RC networks should be added between the shunt resistors and the correspondent comparator and op-amp input pins of each gate driver. A unique RC network can be used for the $\overline{SD}$ pin even if it is strongly recommended to split the capacitor in three equal components in parallel in order to

place each one very close to the $\overline{SD}$ input pin of each IC. This capacitance and, in general, each capacitance indicated in the schematic must be placed as close as possible to the IC in order to guarantee a good noise filtering action.

Figure 19. Typical application schematic of a 3-phase FOC



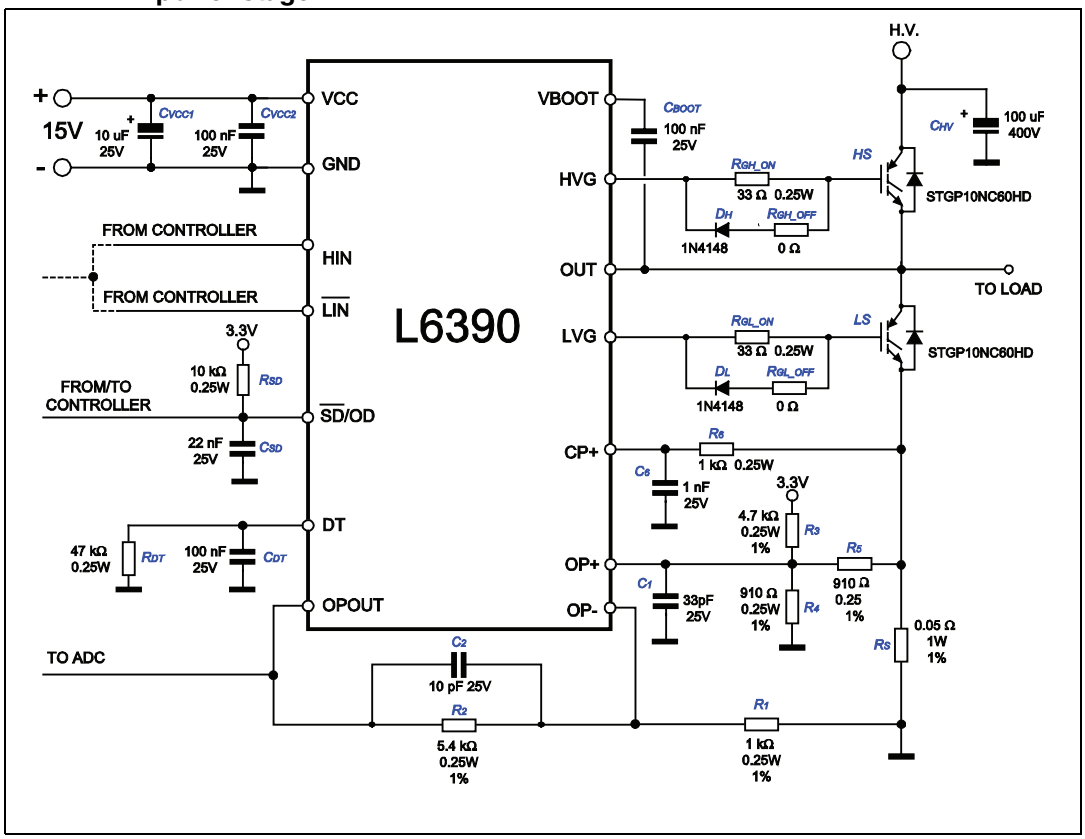
In the example of *Figure 19* the logic inputs HIN and $\overline{LIN}$ are connected together, using just one single signal to drive each L6390.

In *Figure 20* a special focus on a single gate driver circuit of the 3-phase L6390 scheme is provided.

8.1 VCC supply pin

Regarding the VCC pin, a local filtering of the supply voltage very close to the L6390 IC is recommended. Generally the suggestion is to use two capacitors, one electrolytic with greater value (C_{VCC1} = 10 µF, for example) which has a great energy capability but also a not negligible ESR (so is quite slow in providing the current) and a second smaller ceramic capacitor (C_{VCC2} = 100 nF) which has a lower ESR value but a lower energy capability. The first capacitor works mainly as bulk energy storage while the second one is able to supply the dynamic current spikes required by the commutations of the device, so is better for high frequency decoupling of the IC supply voltage. On the other hand, the selection of the proper value for the CBOOT capacitor is already described in *Section 7*.

Figure 20. Ex. of an application circuit for one of the three half-bridges of a 3-phase power stage



In the example a VCC supply voltage of 15 V is used. This voltage is approximately the same voltage provided to the gate of the power switches.

8.2 BOOT (floating) supply pin

The bootstrap capacitor to supply the high-side floating section of the gate driver must be placed between the BOOT pin 16 and the OUT pin 14. For a deep description of the proper dimensioning of the bootstrap capacitor please refer to *Section 7 on page 18*. The capacitor must be placed as close as possible to the related IC pins. The bootstrap diode required for the charge of the bootstrap capacitor is integrated inside the L6390 device.

8.3 Logic input pins

The logic input pins can be connected directly to the controller with the suggestions provided in *Section 2 on page 6*. If the application environment is very noisy and the logic input voltage is low (e.g. 3.3 V), it can be useful to place some small RC network (not showed in *Figure 20*) in series with the logic input lines, in order to avoid false input triggering due external noise.

8.4 Shutdown pin

Dimensioning of the SD network (R_{SD} and C_{SD}) is provided in *Section 5*.

8.5 Dead time pin

The resistance value on the DT pin must be selected following the indications in *Section 4* and in *Figure 5*. It is recommended to connect between DT and GND pins a capacitor with a value of at least 100 nF, as close as possible to the IC and with short PCB tracks.

8.6 Op-amp

As explained in the previous paragraphs, the L6390 op-amp is completely uncommitted so a large amount of amplifier configurations can be implemented by the application designer. An example of amplifying network is provided in *Section 6*. Typically low tolerance resistors are used, if high accuracy is required in the conditioning of analog signals.

8.7 Comparator input

No particular external circuits are required apart some noise filtering network useful to avoid false triggering of the comparator due to voltage spikes on sense resistor. In the example of *Figure 20* a common RC network is implemented (time constant ~1 µs).

8.8 Sense resistor

The value of the sense resistor must be chosen considering mainly the current rating of the application and the amplitude of the sense voltage desired. The power rating of the sense resistor must be large enough to withstand the maximum current of the application. More resistors in parallel are often used in order to withstand higher power requirements and to obtain low resistance values with low parasitic inductance, which must be as low as possible in order to reduce the dynamic below-ground voltage on the OUT pin of the gate driver.

8.9 Gate driver outputs: gate lines

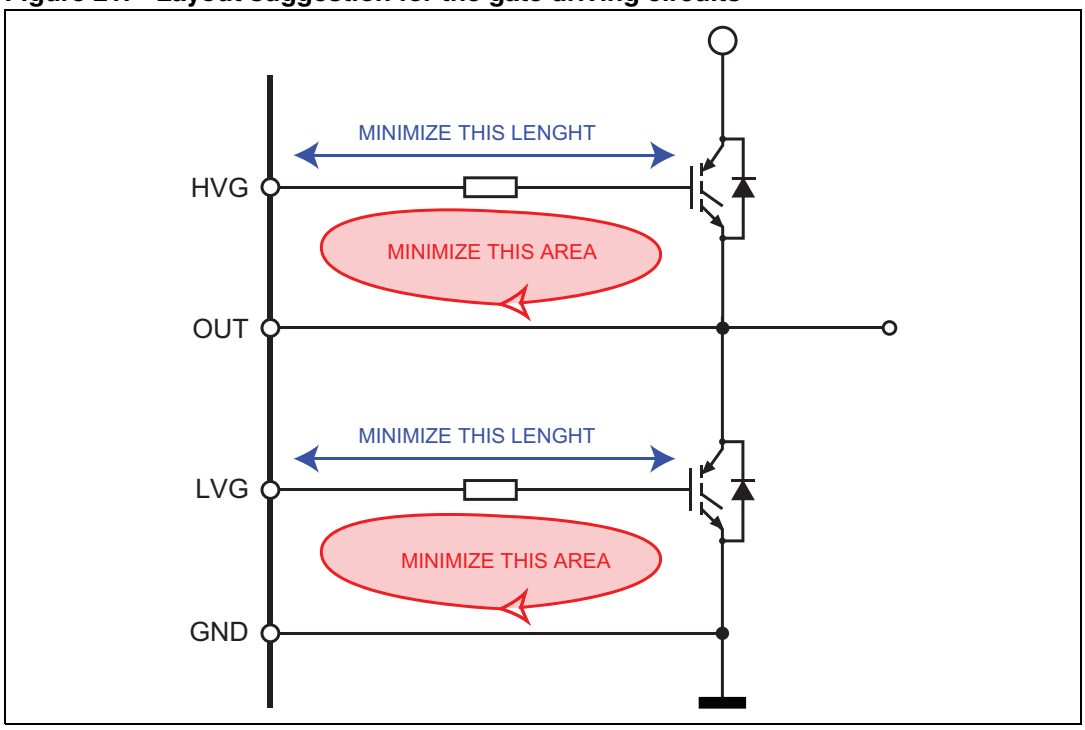
The gates of the power switches and the gate driver outputs can be connected directly, but usually some gate resistors are placed in series on the gate lines in order to limit the gate current during commutations. The final target is to control the dV_{OUT}/dt of each half-bridge output and then reducing the EMI. A more detailed explanation of the mechanisms behind the dV_{OUT}/dt control through the gate resistors is provided in the next sub-paragraph.

Consider that all the following considerations should be considered as approximated analyses of the gate charge phenomenon, so for a proper sizing of the gate resistor is always strongly recommended to evaluate the resulting power bridge transitions in bench analyses.

As shown in *Figure 20*, the gate line is split into separated paths, one for the turn-on (with, in the example, a gate resistor of 33 Ω) and the other one for the turn-off, using a small signal diode as path selector the equivalent turn OFF resistance is in a first approximation the parallel of the turn OFF and the turn ON resistances (neglecting the diode drop). In the example the turn-off resistance is set to 0 Ω to provide the lowest resistance path for the turn-off of the IGBT. In fact, as explained in the two following paragraphs, low impedance on the gate driver turn-off helps in reducing the induced turn-on phenomena.

Regarding the layout of such gate lines, it is always strongly recommended to place the power IGBT (or MOSFETs) very close to the gate driver. It is important to reduce as much as possible the lengths of such line paths as well the areas included in the gate circuits, because these can act as weak antennas and could catch noise from the surrounding environment. The larger these areas, the higher the gain of such undesired antenna circuits.

Figure 21. Layout suggestion for the gate driving circuits



8.10 Gate driving: principle of working with inductive load

In this paragraph a deeper description of the power IGBT (or MOSFET) gate driving, in case of inductive load, will be provided. The following explanations and calculations are just intended to provide a general understanding of physical principles lying behind the phenomenon of the dV_{OUT}/dt control through the gate current limitation performed by the gate resistors. The target is to help the application designer which uses L6390 ICs to be aware of the various contributes that different parameters of the gate driver system have on the power transitions and also to distinguish the main effects on which he should focus on.

Calculations and formulae should be considered as qualitative indications and not for an accurate quantitative use since, as explained in the above paragraph, they are the result of a first approximation study. The experimental verification of the design choices is always recommended.

The description distinguishes and explores the two main actors of the gate driver system: by one side the inner structure of the gate driver output buffers is described and on the other side the switching mechanism of a generic IGBT (or MOSFET) is analyzed in detail. In *Figure 22* a simplified view of the L6390 gate driver output buffers is provided. Each one can be considered as a CMOS push-pull stage where a P-channel MOSFET works as source driver while an N-channel MOSFET works as sink driver. The structure is similar both for the low side and for the high side and the behavior can be considered the same. In fact the high side driver can be thought as a floating buffer having as supply the VBOOT voltage and as reference the OUT pin. The C_{BOOT} capacitor represents the floating supply voltage source of the high side driver. During the charge of the power switch gate, each source/sink MOSFET can be considered (in first approximation, for simplicity) as if it would be in the ohmic region, so it can be represented as an equivalent resistor with a value equal to its $R_{DS(on)}$. Thanks to this approximation it is possible to use a simplified equivalent circuit for the turn-on and the turn-off commutation (see *Figure 22* and *23*). Regarding the turn-on, this gate charge circuit has two resistors in series (R_{GATE_ON} and $R_{DS(on)\_SOURCE}$) and a supply voltage which is VCC for the low side and VBOOT-OUT for the high side. Regarding the turn-off the equivalent circuit is composed just by two resistors (R_{GATE_OFF} and $R_{DS(on)\_SINK}$) connected to the source of the power switch.

Gate driver output buffers: equivalent circuit

Figure 22. Gate driver output: equivalent circuit for turn-on

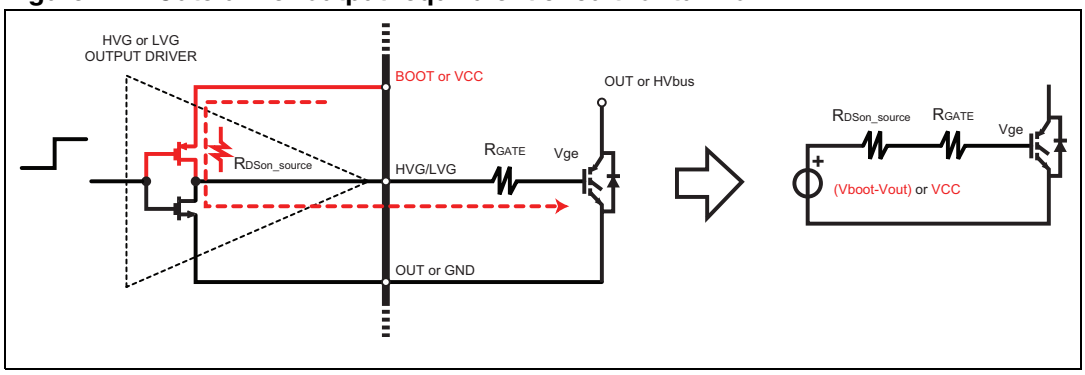
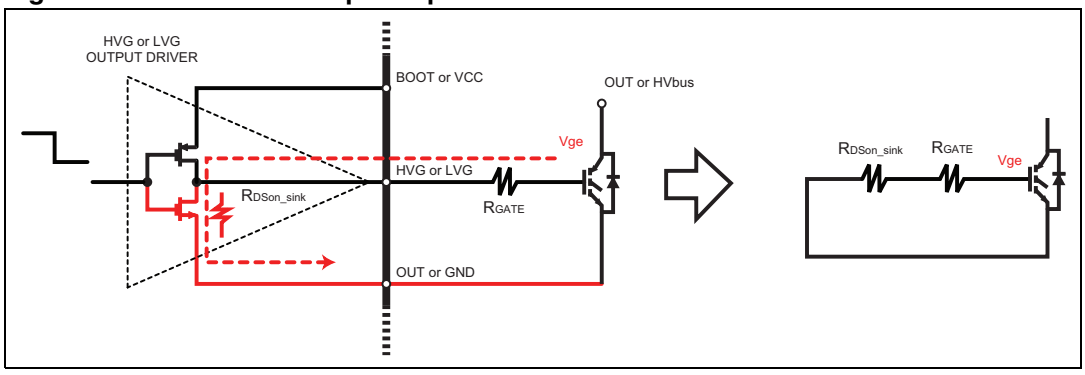


Figure 23. Gate driver output: equivalent circuit for turn-off



This first simplification is related to the inner structure of the gate driver circuitry. Let now focus for a while on the side of the power bridge and its commutations. In a common half-bridge composed by a high side and a low side switch the transitions of the power IGBTs (or MOSFETs) are not all similar, but they can be distinguished in two main types: soft switching and hard switching (see *Figure 24* and *25*). The main element playing a key role in the dynamic of transitions is the direction of the current flowing in the power IGBT (or MOSFET) under evaluation which depends on the direction of the load current respect to the half-bridge. Mainly if the current has the same direction of the power switch the commutation is hard. If it is in opposite direction the commutation is soft.

Figure 24. Hard switching

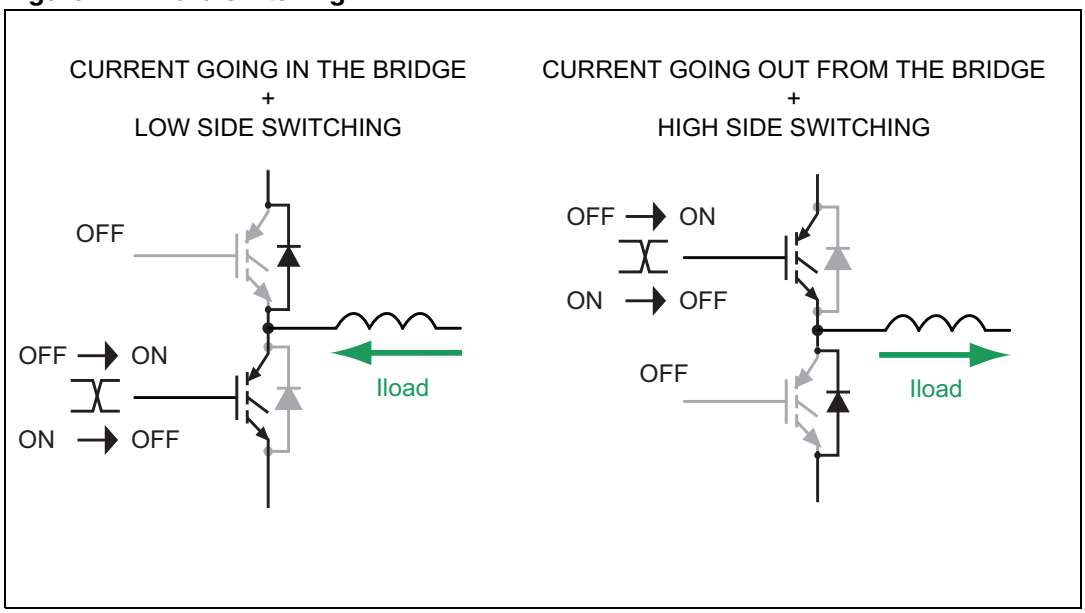
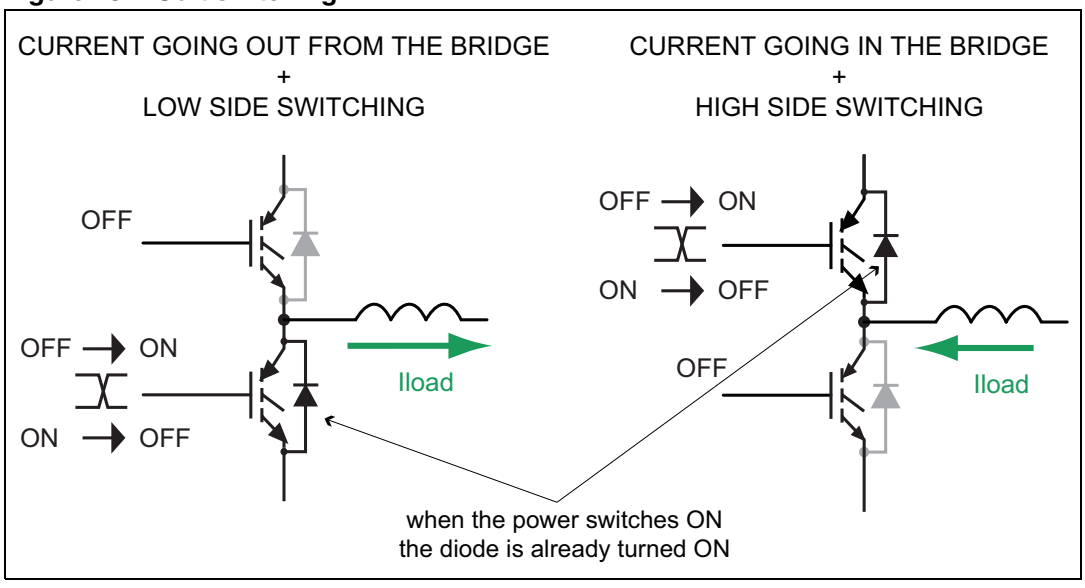


Figure 25. Soft switching



As shown in *Figure 24* and *25*, there is hard switching when the high side is commutating and the load current is exiting the bridge or when the low side is commutating and the load

current is entering the bridge. This type of transition is called “hard” because the power switch turns on when the related V_{CE} (V_{DS}) is at maximum; V_{CE} (V_{DS}) goes back to maximum during turn-off (V_{CE} is close to zero while the switch is steadily ON). The transition is completely managed by the switch that, during the commutation, dissipates some energy. On the other hand, if the switch turns on when its V_{CE} is already closed to zero or V_{CE} remains close to zero after turn-off, the transition is soft and, during the commutation, the switch dissipates almost no energy. This last condition happens when the free-wheeling diode of the switch is bringing the current because the diode is in the same direction of the load current. As a general rule, consider that the dynamic of the transition (dV_{OUT}/dt, V_{CE} rise/fall time etc.) is always managed and controlled by the power switch in hard switching, while its companion switch is necessarily in soft switching because it is in the opposite direction of the load current. Considering this, in order to understand the power IGBT (MOSFET) transition, the hard switching transition will be further investigated. Note that all of the descriptions that follow consider an inductive load connected to the half-bridge stage output.

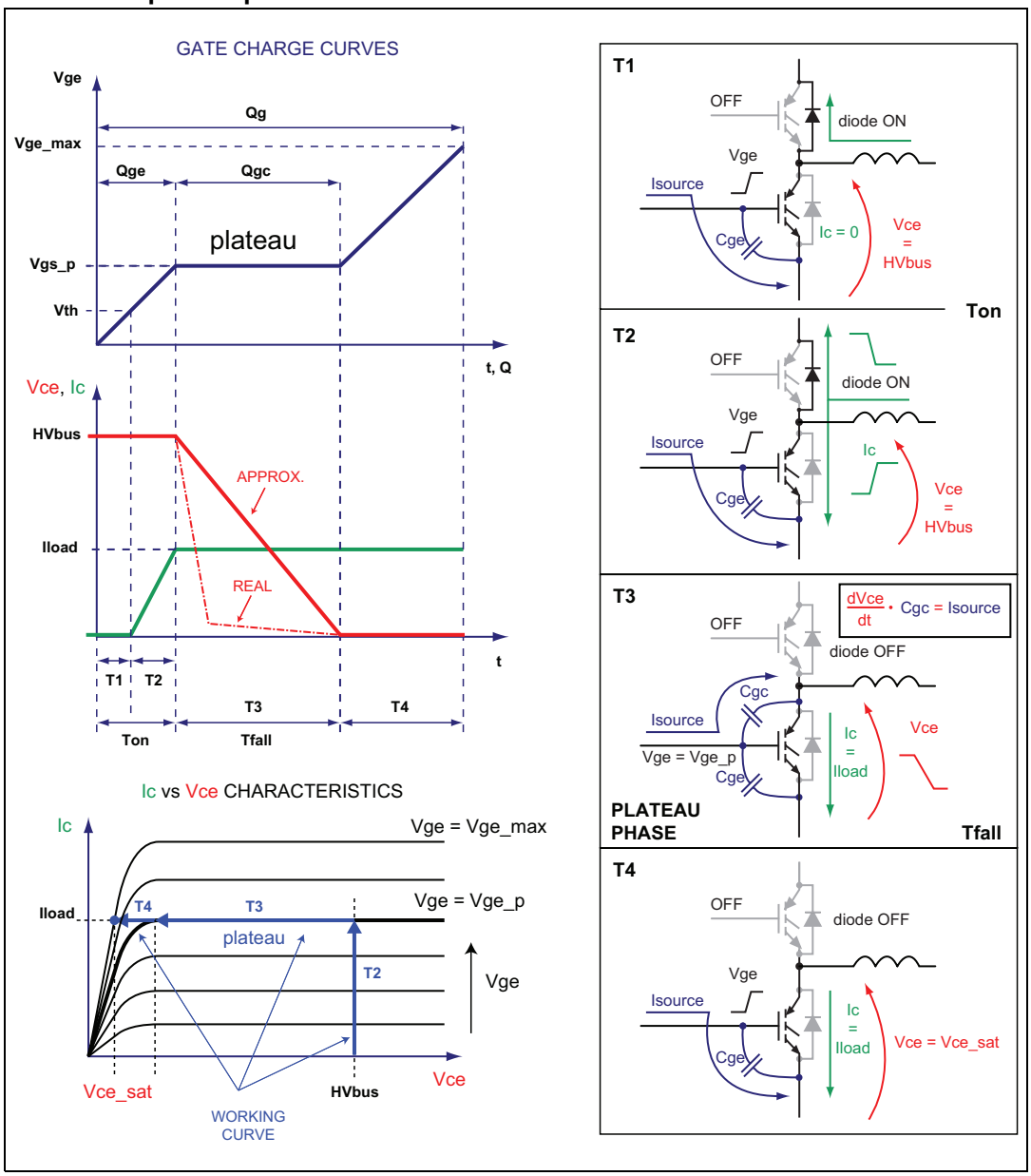
In *Figure 26*, the dynamics of the hard switching for the turn-on transition are described. The first graph is related to the gate charge curves of the power IGBTs (or MOSFETs). This is a typical graph which is also available in the datasheets for the IGBT or MOSFET and describes the dependence of the amount of charge required by the IGBT gate on the voltage drop between the gate and the emitter (or source). In the second graph the collector current (I_C) and V_{CE} voltage versus time are shown. The third graph shows the working point of the IGBT traced on the various Ic vs. V_{CE} characteristic curves for different V_{GE} voltages. For a single turn-on transition, four main phases related to the power IGBT (MOSFET) commutation can be distinguished. On the left side of *Figure 26*, the IGBT conditions for each phase are described. During phase T1 the gate begins to be charged, but the power IGBT still is not conducting because V_{GE} is below the threshold of the IGBT. In this state, the IGBT current is zero and its V_{CE} is at maximum, while V_{GE} is gradually increasing. In phase T2 the V_{GE} voltage goes above to the IGBT threshold and the IGBT starts to bring part of the load current. V_{CE} remains fixed at maximum level because the free-wheeling diode of the companion IGBT is still bringing the rest of the load current and is still conducting, thereby clamping the V_{CE} voltage. Both in T1 and T2 phases, the gate current contributes to charge the equivalent V_{GE} parasitic capacitance of the IGBT. In the Ic vs. V_{CE} characteristic plot the T2 phase is the vertical section of the working curve trace, because the IGBT is moving on its own characteristic with a constant V_{CE} and an increasing current, while its V_{GE} is increasing also. When the amount of current flowing in the IGBT is equal to the load current, the diode turns off and the V_{CE} voltage starts to decrease because it is no longer clamped by the free-wheeling diode of the other IGBT. The working point on Ic vs. V_{CE} curve reaches the load value and starts to move horizontally on the Ic constant curve in the direction of decreasing V_{CE} voltages. This is the T3 phase, usually called the “plateau” phase. This name derives from the fact that the gate charge curve is horizontal for the entire T3 phase, until V_{CE} reaches the V_{CE_sat} value corresponding to the load current. Note that the V_{GE} voltage is constant, although the gate current flowing in the IGBT gate is not zero. The reason for this is that the whole gate current is used to charge the C_{GC} (Miller) parasitic capacitance which then experiences a dV/dt on its terminals because the V_{CE} voltage is decreasing after the diode turn-off. As a first approximation, if C_{GC} was constant (currently it is not), the dV_{OUT}/dt could be calculated as follows:

Equation 5

$$\left(\frac{dV_{OUT}}{dt}\right)_{FALL} = \frac{I_{SOURCE}}{C_{GC}}$$

The formula above shows how the source current coming from the gate driver can directly control the dV_{OUT}/dt of the power half-bridge. This calculation is just a first approximation, since typically the C_{GC} Miller capacitance value is not constant but depends on the V_{CE} voltage, C_{GC} is not linear. The main result of the abrupt variation of the C_{GC} is that the actual slope of the OUT transition is composed of two different dV_{OUT}/dt slopes, one faster and the other slower compared to the value obtained by the above formula (see *Figure 26*). In this document only the first approximation approach will be used.

Figure 26. Turn-on hard switching details with induction load: gate charge and plateau phase



Due to C_{GC} non-linearity, the IGBT (or MOSFET) datasheet also reports the equivalent total amount of charge required during the different gate charge phases: the total gate charge Q_g required for turning on the IGBT (or MOSFET) completely, the Q_{GE} required for increasing

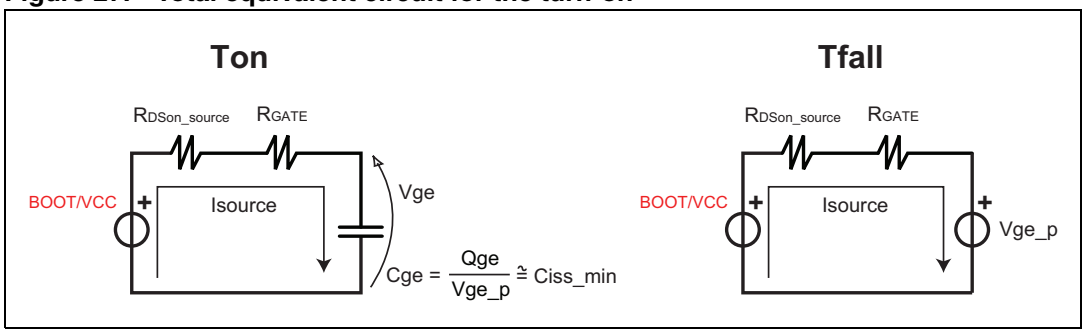
the V_{GE} up to the plateau voltage and the Q_{GC} required during the whole plateau phase. This last amount of charge is also called the plateau charge. The time required to provide the complete plateau charge is the T_{fall} time, and this is the same time necessary for completing the V_{CE} transition. For Ton time is intended the time delay between the beginning of the gate charge and the full conduction of the IGBT (or MOSFET), when the power switch current equals the full load current. So T_{fall} can be calculated as follows:

Equation 6

$$T_{fall} = \frac{Q_{GC}}{I_{SOURCE}}$$

It is now possible to merge the equivalent gate driver output circuit reported in figures *24* and *25* and the considerations regarding the different gate charge phases in the total equivalent circuit reported in *Figure 27*.

Figure 27. Total equivalent circuit for the turn-on



From the above circuit the value of the transition times could be calculated (the following formulae are related to the low side transition, but the same are suitable also for the high side by exchanging “VCC” with “VBOOT-VOUT”):

Equation 7

$$T_{ON} = (R_{DS(on)} + R_{GATE}) \cdot C_{ISSmin} \cdot \ln\left(\frac{VCC}{VCC - V_{GEP}}\right)$$

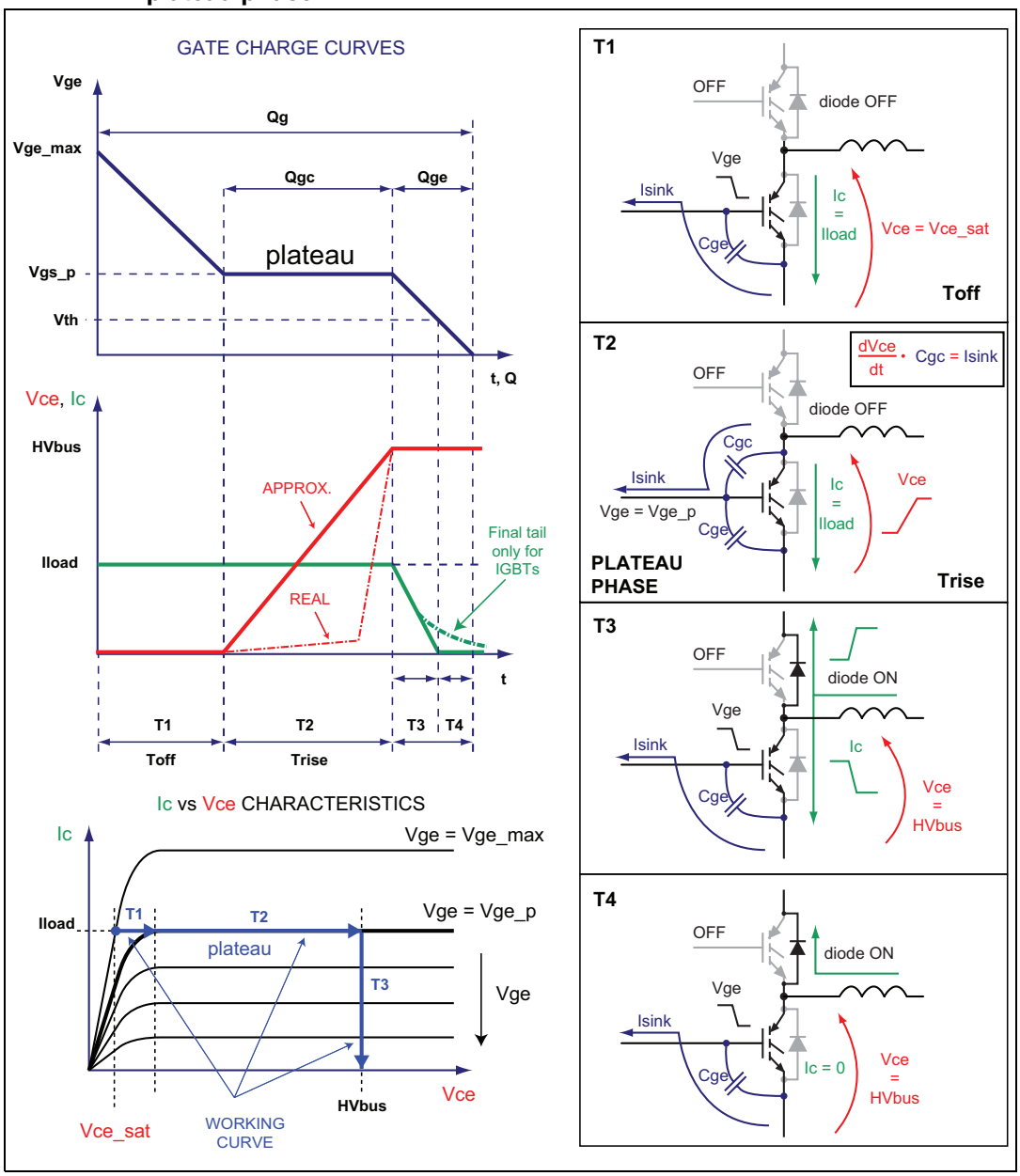
Equation 8

$$T_{FALL} = \frac{Q_{GC}}{I_{SOURCE}} = Q_{GC} \cdot \frac{(R_{DS(on)} + R_{GATE})}{VCC - V_{GEP}}$$

C_{ISS_min} is used because when the V_{CE} (or V_{DS}) of the power IGBT (or MOSFET) is maximum (equal to HV_{bus}), C_{ISS} (which depends on the V_{CE}) shows its minimum value.

During the turn-off of the power IGBT (or MOSFET), the behavior is the same as the turn-on, but in reversed time order. In *Figure 28*, the gate charge characteristics and V_{CE} vs. I_C curves are provided. The time required to sink the complete plateau charge is the T_{rise} time, while for T_{off} time is intended the time delay between the beginning of the gate charge and the increase of Vce (or Vds) voltage.

Figure 28. Turn-off hard switching details with induction load: gate charge and plateau phase



The rising dV_{OUT}/dt and T_{rise} can be calculated as follows:

Equation 9

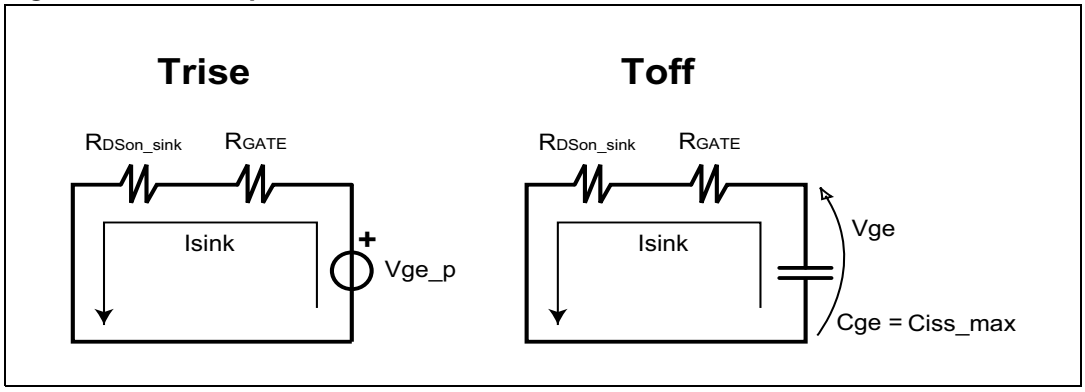
$$\left(\frac{dV_{OUT}}{dt}\right)_{RISE} = \frac{I_{SINK}}{C_{GC}}$$

Equation 10

$$T_{RISE} = \frac{Q_{GC}}{I_{SINK}}$$

As discussed above, the equivalent gate driver output circuit can be represented as in *Figure 29*:

Figure 29. Total equivalent circuit for the turn-off



Given the equivalent circuits in *Figure 29* and the approximations of the power IGBT (MOSFET) switching behavior, the timing equations are as follows:

Equation 11

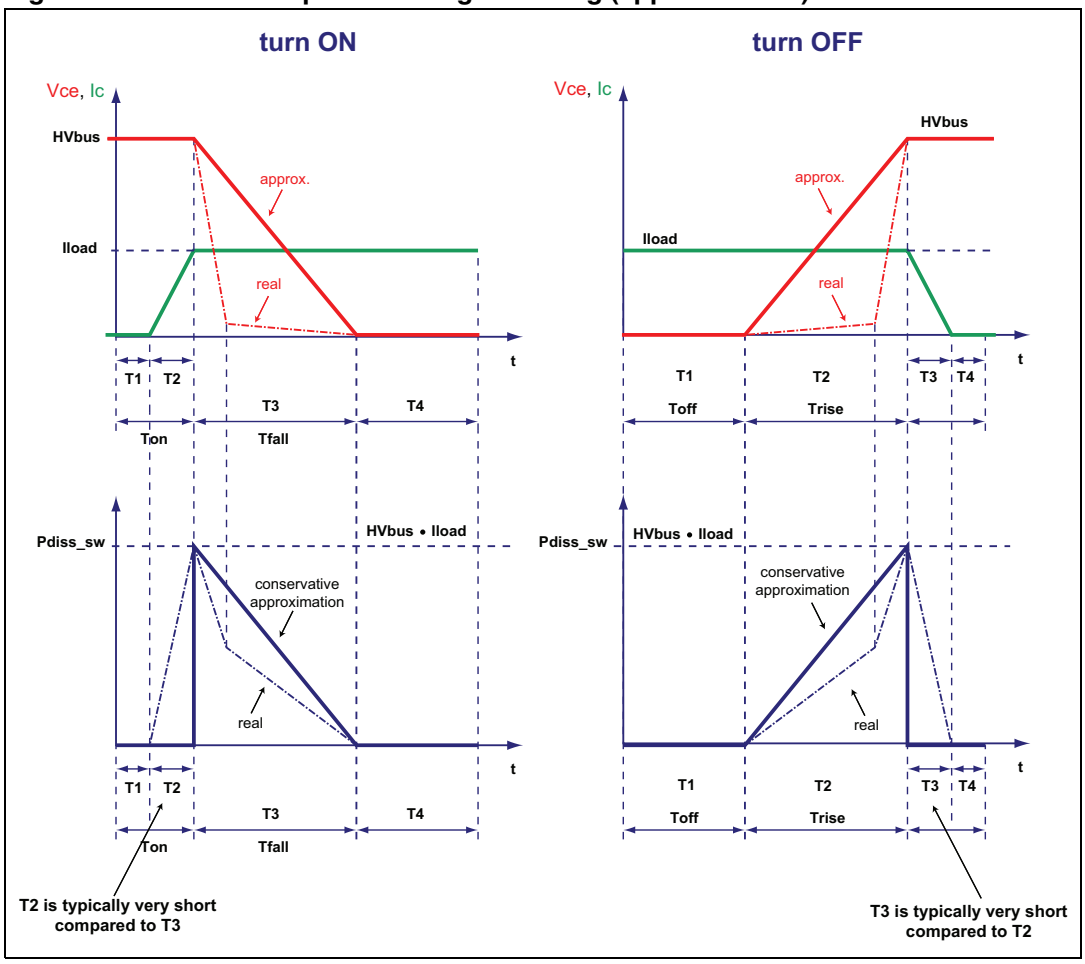
$$T_{OFF} = (R_{DS(on)} + R_{GATE}) \cdot C_{ISSmax} \cdot \ln \cdot \left(\frac{V_{GE\_MAX}}{V_{GEP}}\right)$$

Equation 12

$$T_{RISE} = \frac{Q_{GC}}{I_{SINK}} = Q_{GC} \cdot \frac{(R_{DS(on)SINK} + R_{GATE})}{V_{GEP}}$$

As above, C_{ISS_max} is used because when the V_{CE} (or V_{DS}) of the power IGBT (or MOSFET) is minimum (equal to V_{CE_sat}) the C_{ISS} (which depends on the V_{CE}) shows its maximum value. Even if they are just approximations, the T_{fall} and T_{rise} are very important values to be estimated because they provide an indication of the power dissipation during the switching of the power IGBT (or MOSFET), which can be approximated as indicated in *Figure 30*.

Figure 30. Power dissipation during switching (approximation)



Since the T2 time for the turn-on and T3 time for the turn-OFF are much shorter compared to T_{fall} and T_{rise}, respectively, the approximated instantaneous amount of energy dissipated during the commutation can be calculated as the triangular area having as its base the T_{fall}, or T_{rise} time and as its height the product of the maximum V_{CE} voltage (equal to HV_{bus}) and the load current value:

Equation 13

$$E_{DISS-SW} \cong \frac{(HV_{bus} \cdot I_{LOAD}) \cdot (T_{fall} + T_{rise})}{2}$$

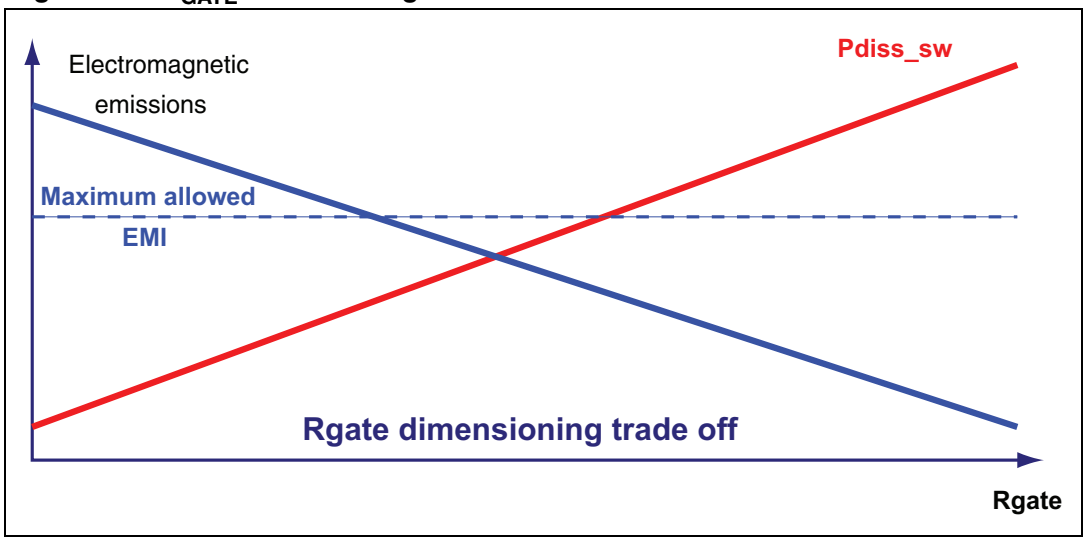
Equation 14

$$P_{DISS-SW} \cong \frac{(HV_{bus} \cdot I_{LOAD}) \cdot (T_{fall} + T_{rise}) \cdot f_{SW}}{2}$$

The term f_{SW} represents the switching frequency of the power IGBT (or MOSFET).

Based the results obtained by these approximate calculations, it should be clear that the main consideration when dimensioning the gate resistor values is the trade-off between electromagnetic emission and the power dissipated during power IGBT (or MOSFET) switching, as shown in *Figure 31*.

Figure 31. R_{GATE} dimensioning criteria

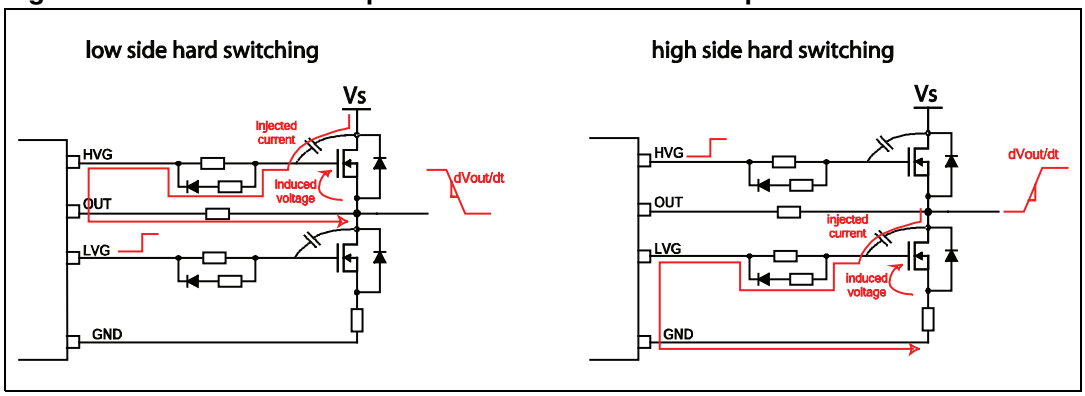


R_{GATE} influences the power dissipation on one side and the EMI effects on the other. Therefore, the best trade-off must be determined during the application design-in phase.

9 Induced turn-on phenomenon

One possible phenomenon to be analyzed is the induced turn-on that could occur on a turned-off power IGBT (or MOSFET) when its companion on the same half-bridge is switching on. This phenomenon is due to the current injected on the gate by the Miller parasitic capacitance (C_{GC}) which causes an undesired voltage increase on the gate of the power IGBT (or MOSFET) which should be kept well turned off. Induced gate voltage depends on the absolute value of the parasitic capacitance C_{GC}, its relative ratio with C_{GE}, the value of the dV_{OUT}/dt of the half-bridge and the value of the equivalent (turn-off) resistance between the emitter (or the source) and the gate. *Figure 32* illustrates this phenomenon.

Figure 32. Induced turn-on phenomenon - circuital description



Note: Typically the induced turn-on phenomenon does not cause a complete turn-on of the power MOSFET, so it is rare to have destructive cross-conduction on the half-bridge during commutations. Nevertheless, weak conduction of the opened power switch could increase the power dissipation of the power stage, increasing the overall temperature of the power MOSFETs and reducing the efficiency. This is why this phenomenon deserves particular attention also in terms of thermal performance of the power application.

Some strategies to reduce this phenomenon are:

a) **Reducing resistance path between gate and emitter (source).** Reducing as much as possible the gate resistance in which the injected current flows, the voltage drop on the gate becomes lower. The drawback is a possible increase of the dV_{OUT}/dt during turn-off of the power IGBT (or MOSFET) which commutates in hard switching, and then an increase of electrical noise and EMI issues (as explained in the previous paragraph, the power IGBT or MOSFET in hard-switching is always the one which has the channel in the same direction as the current). On the other hand, usually the dV_{OUT}/dt during turn-off is lower than during turn-on, because the plateau voltage is closer to the source voltage than the supply voltage of the driver. This results in a lower gate current for the discharge of the gate charge.

b) **Reducing the maximum dV_{OUT}/dt**. This reduction can be achieved by increasing the gate resistor value which limits the gate current for the turn-on of the power MOSFET. The drawback is a consequent increase of the switching time which means dissipating more power during commutations.

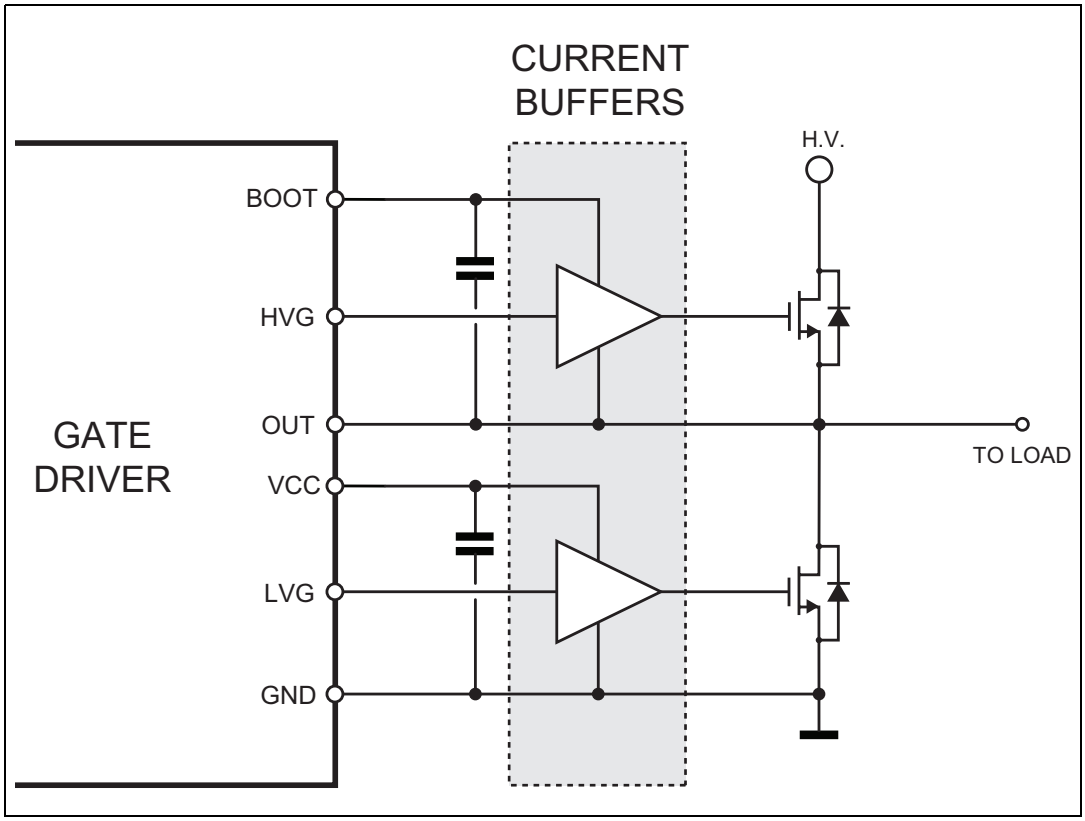
c) **Using a MOSFET with lower C_{GD}/C_{GS} (or C_{GC}/C_{GE} for IGBTs) ratio.** This solution is not always the simplest, but it could be the best strategy where the induced turn-on phenomenon is dominant.

10 How to increase the gate driver output current capability

In some cases, certain applications may require more gate driver output current capability. This requirement could be found in systems having a power rating higher than about 1 kW. In those applications, in fact, typically the power MOSFET/IGBTs have a large gate charge which contributes to a slowing down of the power switch transition (the dV_{OUT}/dt), increasing the power dissipation during each commutation. Note that also in applications with power rating higher than 1 kW, the output current capability of the L6390 could be enough if the power dissipation for commutation is acceptable (the power dissipation due to $R_{DS(on)}$ or V_{CESAT} is not dependent on the gate current). But if the limitation of this power contribution is a constraint, the dV_{OUT}/dt of each transition must be increased by enhancing the current capability of the gate driver.

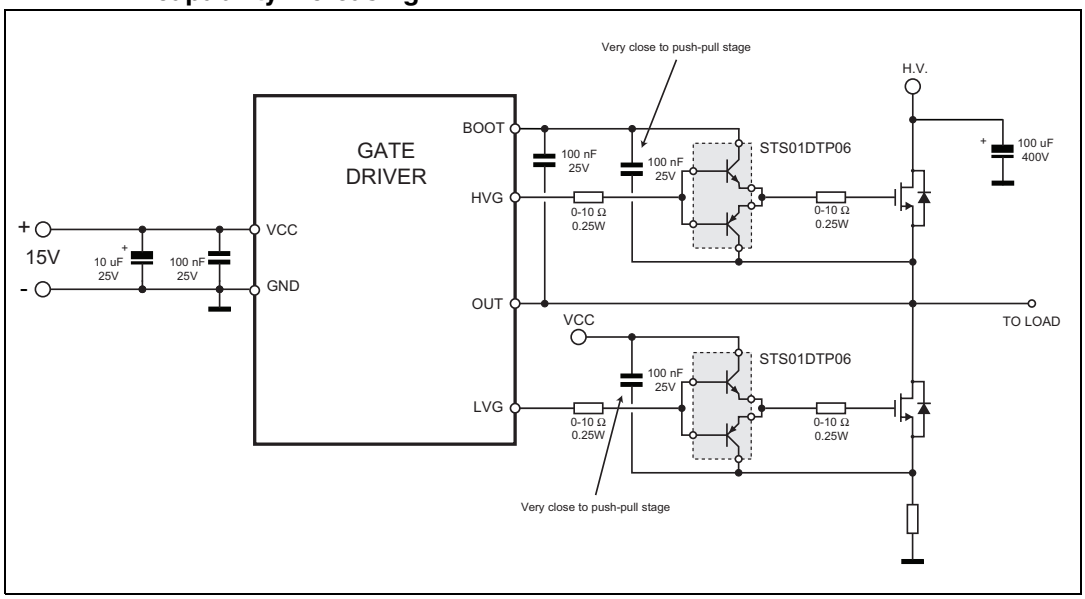
A simple way to increase the current capability of the gate driver outputs is to insert, in series with the two gate lines of one half-bridge gate driver IC, two external current buffers (*Figure 33*).

Figure 33. Block diagram of output current capability enhancement using external current buffers



Typically the current buffers are implemented using bipolar NPN-PNP push-pull non-inverting (emitter follower configuration) structures. In *Figure 34*, a typical circuit using a gate driver with bipolar push-pull current buffers is shown.

Figure 34. Example of a gate driving circuit with current buffers for current capability increasing



In the example above, the STMicroelectronics devices STS01DTP06 are dual NPN-PNP complementary bipolar transistors rated for 1 A of current and available in the small SO-8 package. The two push-pull structures are placed on each gate driving path and must be provided with a decoupling capacitor very close to device pins (see *Figure 34*).

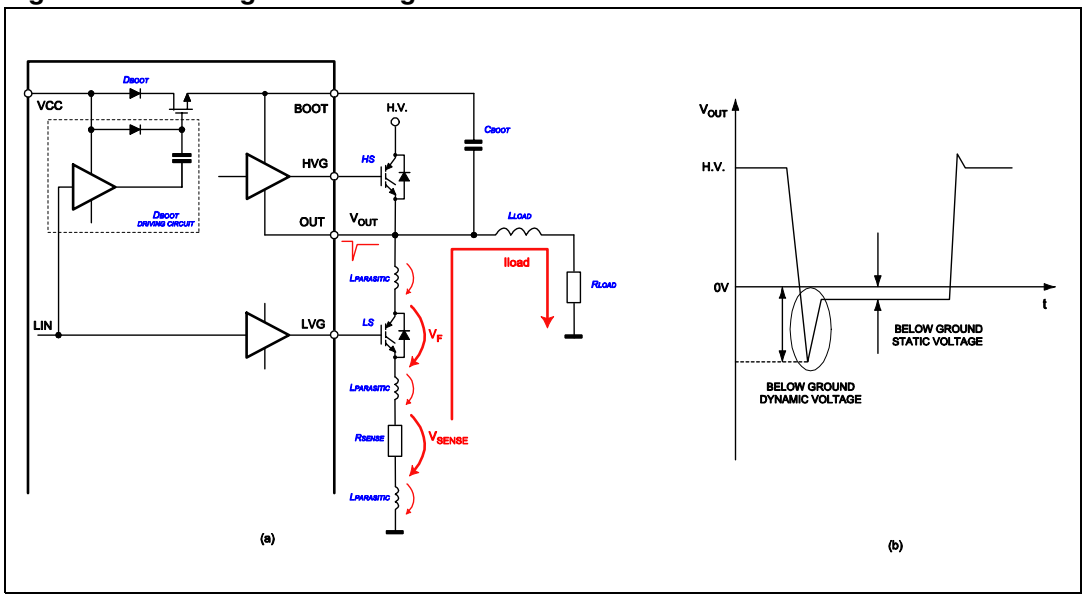
11 The below-ground voltage on the OUT pin

A typical phenomenon found in a great number of power applications is the below-ground voltage experienced by the OUT pin, which sometimes can be very high. Contrary to common opinion, the real problem of the below-ground voltage is not in the maximum absolute value of the OUT pin, but rather the voltage on BOOT pin and the over-charging of the bootstrap capacitance. In the paragraph that follows the root causes of the below-ground voltages will be explained in detail, and the description of the real issues which could result from the phenomenon will be provided.

11.1 The below-ground voltage phenomenon

In power applications using half-bridge topologies and typically driving loads with a significant inductive component, the output of the power half-bridge experiences, systematically, a below-ground voltage transition, which can be distinct in a dynamic contribution consisting of a greater undershoot spike and in a static contribution, which is a below-ground static voltage with lower absolute value (*Figure 35*b). This phenomenon occurs when the bridge carries out a so-called hard switching transition towards a low voltage level and the load current is outgoing (from the bridge to the load). When the high side switch turns off, the output current tends to remain quite constant due to the inductive component of the load, and then has to flow through the low side freewheeling diode, which turns on going from a high voltage reverse condition to a forward condition. It is evident that until the output bridge voltage has reached the “zero” value, the diode is turned off, so the output transition is dominated by the high side turn-off commutation. After the output voltage reaches the zero-voltage level, the diode can turn on and it begins to bring the entire load current in a very brief time, so the high dI_F/dt causes the well-known forward peak voltage, which is the main contribution to the undershoot spikes. Other contributions to dynamic below-ground voltage are the spikes due to the high dI/dt experienced by the parasitic inductances in series with the free-wheeling diode located along the turn-off current path of the half-bridge (*Figure 35*).

Figure 35. below-ground voltages in L6390



The overall below-ground voltage on the OUT pin can be calculated as follows:

Equation 15

$$V_{OUTmin\ \ static} = -(R_{SENSE} \cdot I_{LOAD} + V_F)$$

Equation 16

$$V_{BGV\_spike} = \underbrace{V_{FPK} + L_{PARASITIC} \cdot \frac{dI_F}{dt}}_{\text{dynamic contribution}} + \underbrace{V_{OUTmin\_static}}_{\text{static contribution}}$$

where:

- V_{FPK} is the free-wheeling diode transient peak forward voltage, which depends mainly on the device technology and on the dI_F/dt of the current in the diode. Typical values could be from a few volts to more than 10 V. In *Figure 36*, VFP vs. dIF/dt of the STTH1L06 diode is shown.
- the dI_F/dt is the current slope in the low side IGBT/MOSFET and could have a value from a few tens to several hundreds of A/µs. The value depends mainly on the power switch characteristics and in part on the driving current.
- $L_{PARASITIC}$ represents the sum of all parasitic inductances on the current path and mainly depends on the PCB layout. Generally, during the design of the power application it is important to pay attention to the layout of the power bridges in order to limit this parameter. Typical values of a good layout are in the order of some tens of nH. Note that it is useful also to use R_{SENSE} resistors with low parasitic inductances for the same reason.
- R_{SENSE} * I_{LOAD} product is the value of the V_{SENSE} voltage and typically is less than 1 V, also for thermal dissipation issues on the same resistor.
- V_F is the forward voltage of the free-wheeling diode and it is usually less than 2 V.

11.2 How to reduce the below ground spike voltage

In order to reduce the below ground spike, the following action should be taken:

- Reduce the parasitic inductances (see *Figure 35*).
- Reduce the dI_F/dt by slowing down the turn-off of the high side IGBT/MOSFET.

In most of application the two previous strategies result to be enough to reduce properly the below ground spike voltage, increasing the robustness of power system and then the margin for safe operation of the application. On the other hand in some cases, where the below ground spike voltage is significantly higher, the above suggestions may be not sufficient to limit that value and then it could be useful to add some external components to improve further the noise robustness of the power stage section:

- Add a small resistor (2÷10 Ω typically) in series to the OUT line (see *Figure 37*). The series resistor has the positive effect of limiting the spike voltage on the BOOT pin, thanks to the filtering effect of such resistor coupled with the bootstrap capacitor. Note that, in order to obtain an effective filtering effect, the OUT resistor must be placed between the minus terminal of bootstrap capacitor and the output of the power stage, as indicated in *Figure 37*.

Figure 36. Transient peak forward voltage vs. dI_F/dt of STTH1L06 diode

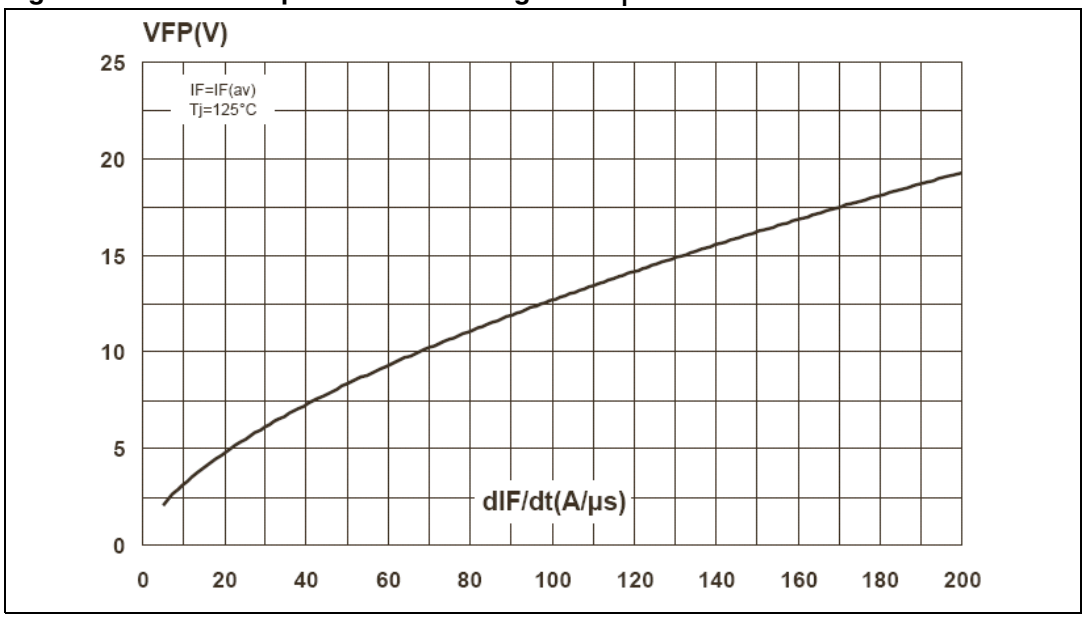
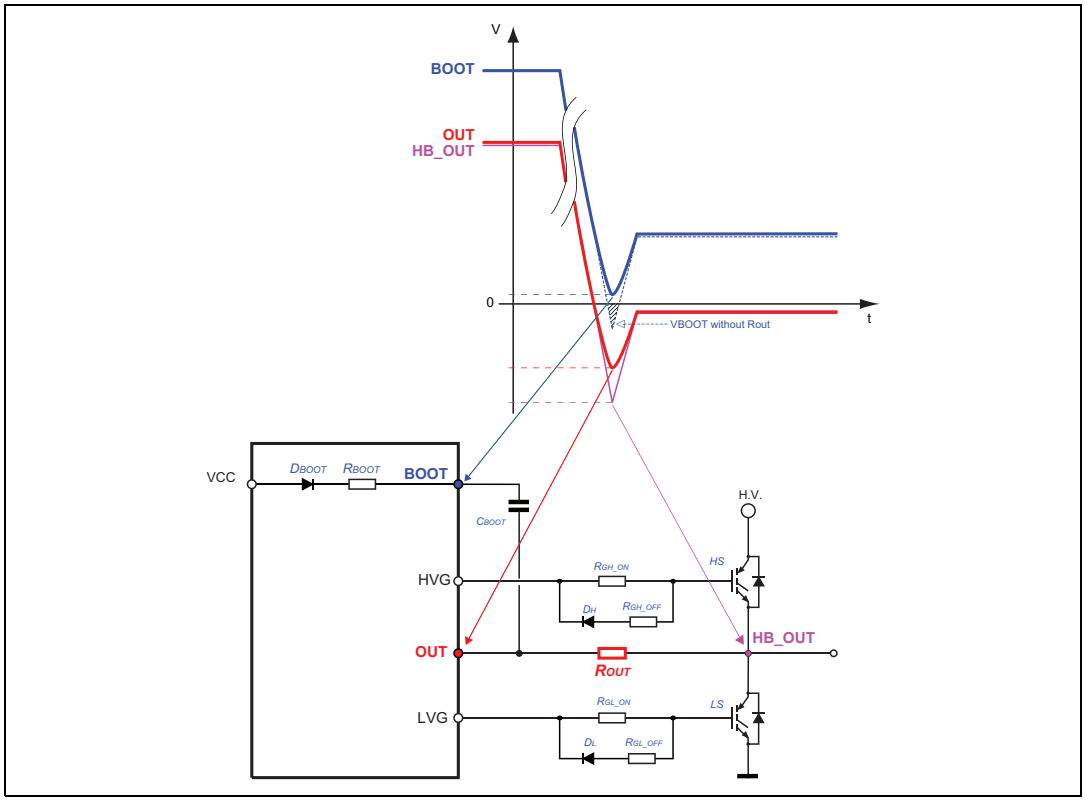


Figure 37. Use of OUT resistor to limit the below ground voltage spike on OUT pin

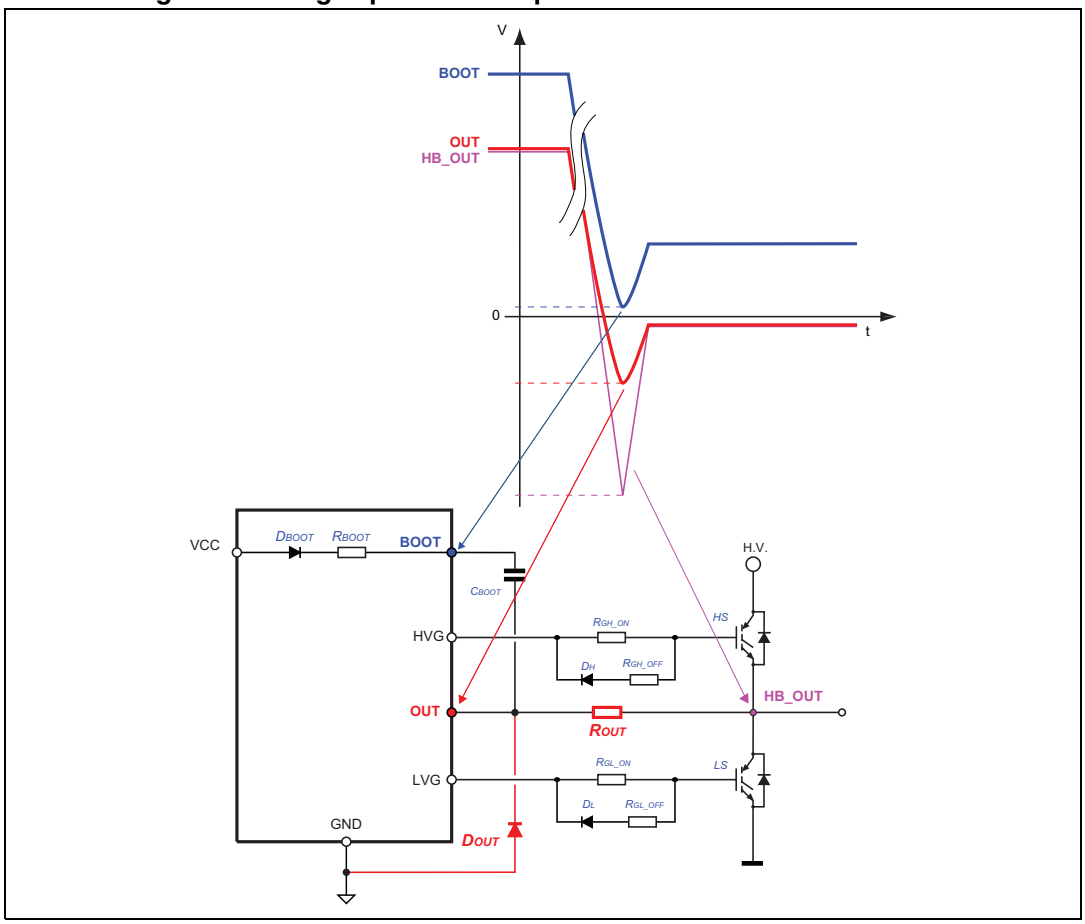


Note that this resistor is in series with both the turn ON and the turn OFF path, so it must be considered in the sizing of overall turn-ON and turn-OFF resistance.

In case neither the OUT resistor would not be enough to limit the below ground voltage, the following final resolving action could be taken:

- Add a high voltage fast diode (e.g. STTH1L06) between the GND pin and the OUT pin (very close to the device pins) in order to clamp directly on the gate driver OUT pin the below ground voltage spike. Note that, in any case, this diode must be used together with the OUT resistance suggested in the previous tip, because it must be avoided that the diode brings the very large load current during low side recirculation, in order to increase the clamping action of the diode itself (see following *Figure 38*).

Figure 38. Use of combination of OUT resistor and OUT diode to limit the below ground voltage spike on OUT pin



Note that R_{OUT} resistor is also in series with the charging path of the bootstrap capacitor. Its effects may be more evident during the first charge of the bootstrap capacitor, when it is completely discharged and a significant charging current may flow into the R_{OUT} resistor, producing an additional voltage drop between ground and OUT pin. Because during the bootstrap charging the HVG pin is set to low level, the OUT pin and the HVG pin are shorted together and have the same voltage, so the voltage drop due to ROUT results directly transferred to the V_{GE} (or V_{GS}) of the high side IGBT (or MOSFET). Then the risk is that a weak turn ON of the high side power switch, when the low side power switch is already ON, could cause a cross-conduction in the power half bridge. Actually in most of cases this doesn't represent an issue for the proper working of the application, because the typical intrinsic resistance R_{BOOT} (~120 Ω) in series to the internal bootstrap diode is much higher than the R_{OUT} commonly used and the voltage drop on R_{OUT} is negligible.

11.3 Issues related to the below-ground voltage phenomenon

Contrary to common belief, the issues resulting from significant below-ground voltages on the OUT pin are not related to the maximum absolute voltage values that the OUT pin is able to withstand, but are instead related mainly to the voltage value of BOOT pin, which is indirectly bound to the OUT pin voltage. There are two main issues to be taken into consideration, all related to the absolute maximum ratings of the IC:

- VBOOT absolute minimum voltage
- VBOOT-VOUT absolute maximum voltage

11.3.1 V_{BOOT} voltage safe operating condition

Electrically, the OUT pin could safely tolerate even many volts below ground without problems, but the BOOT pin cannot. The absolute value of the VBOOT voltage must not go steadily below -0.3 V, in order to avoid the turn-on of the built-in junction between BOOT pin and the IC gate driver substrate (connected to GND), which is normally in reverse condition. The turn-on of this junction could, in fact, cause a current large enough to damage the device.

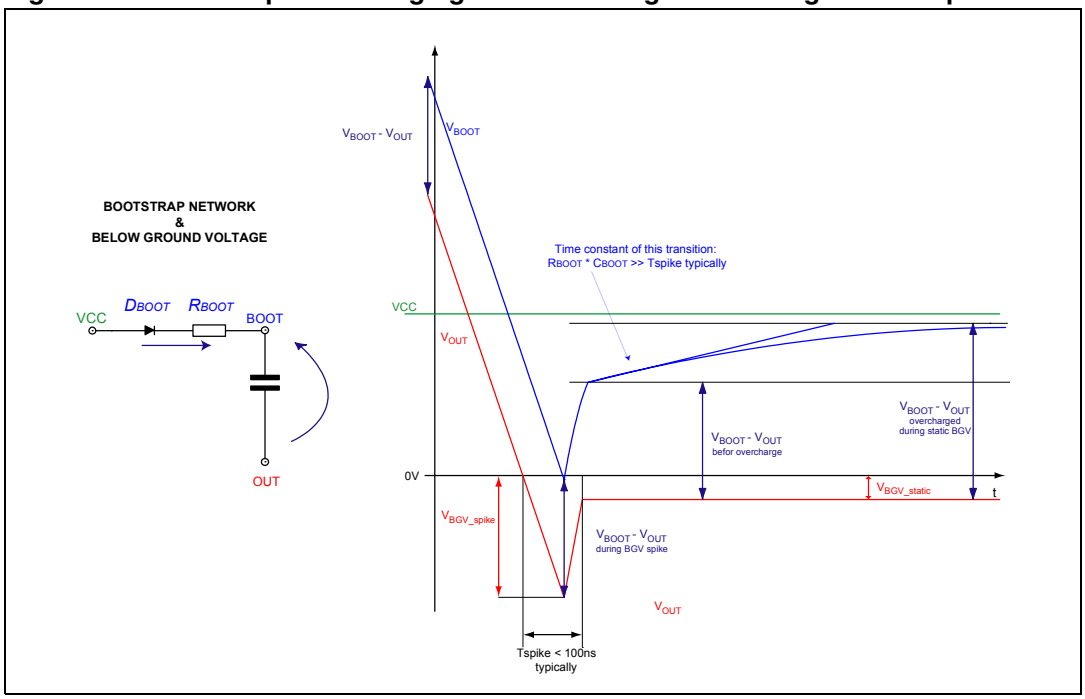
11.3.2 Bootstrap capacitor over-charging

Another very important consideration is bootstrap capacitor over-charging. Actually, even before the OUT pin approaches the zero voltage value, the bootstrap diode (internal or external) tends to tie V_{BOOT} close to the VCC supply voltage. Since the OUT pin is below ground, the bootstrap capacitor is overcharged through the current coming from the bootstrap diode, and the V_{BOOT} - V_{OUT} voltage increases. It is very important that the bootstrap over-charge does not exceed the recommended maximum value for the V_{BOOT} - V_{OUT} voltage (see the relevant datasheet), as the high side floating section of the gate driver could be damaged.

Note that a significant over-charging of the bootstrap capacitor is only possible through the static contribution of the below-ground voltage, because the dynamic below-ground voltage is very brief and the over-charging transition is limited by the time constant RC of the bootstrap capacitor and by the overall resistance in series with the bootstrap diode.

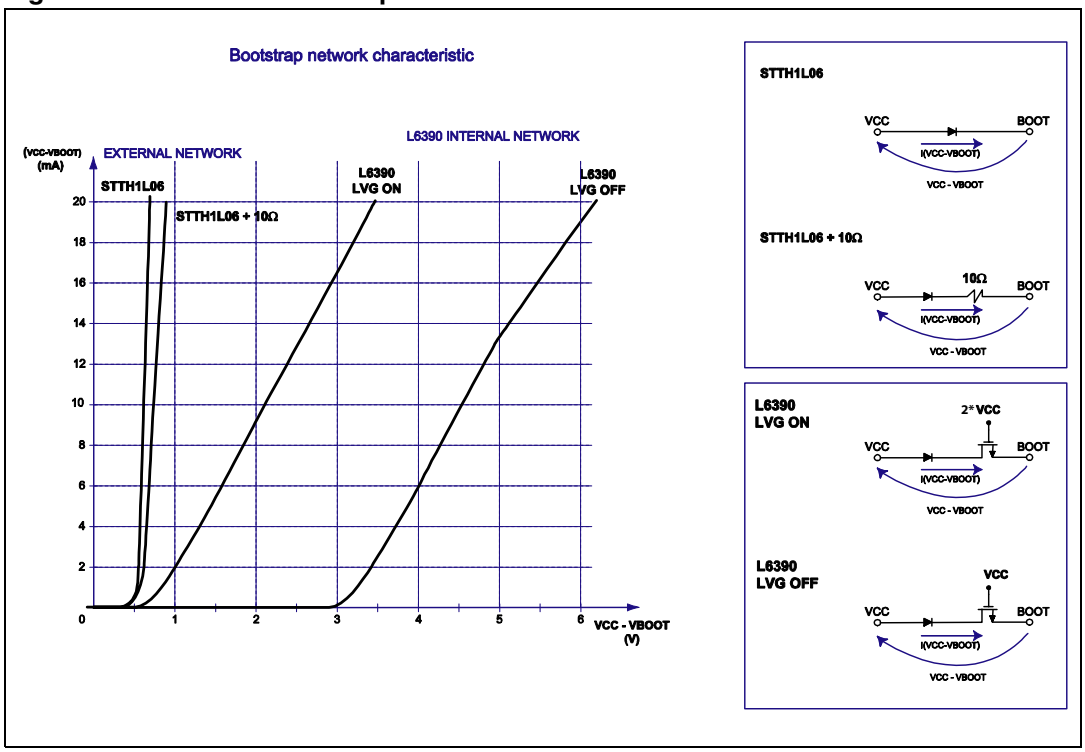
In *Figure 39*, the over-charging phenomenon is illustrated in detail.

Figure 39. Bootstrap over-charging due to below-ground voltage on OUT pin



Note that in the L6390 IC gate driver the internal DMOS in series with the integrated bootstrap diode is fully turned on only when LVG is ON. In fact, when the LVG is OFF, the gate of the bootstrap DMOS is biased at VCC voltage. This means that if the V_{BOOT} is pulled down by the bootstrap capacitor (due to below-ground voltage on OUT pin) at about 3 V (typ) below VCC voltage, the DMOS turns on again. *Figure 40* shows some characteristics of different (internal and external) bootstrap networks.

Figure 40. Different bootstrap network characteristics

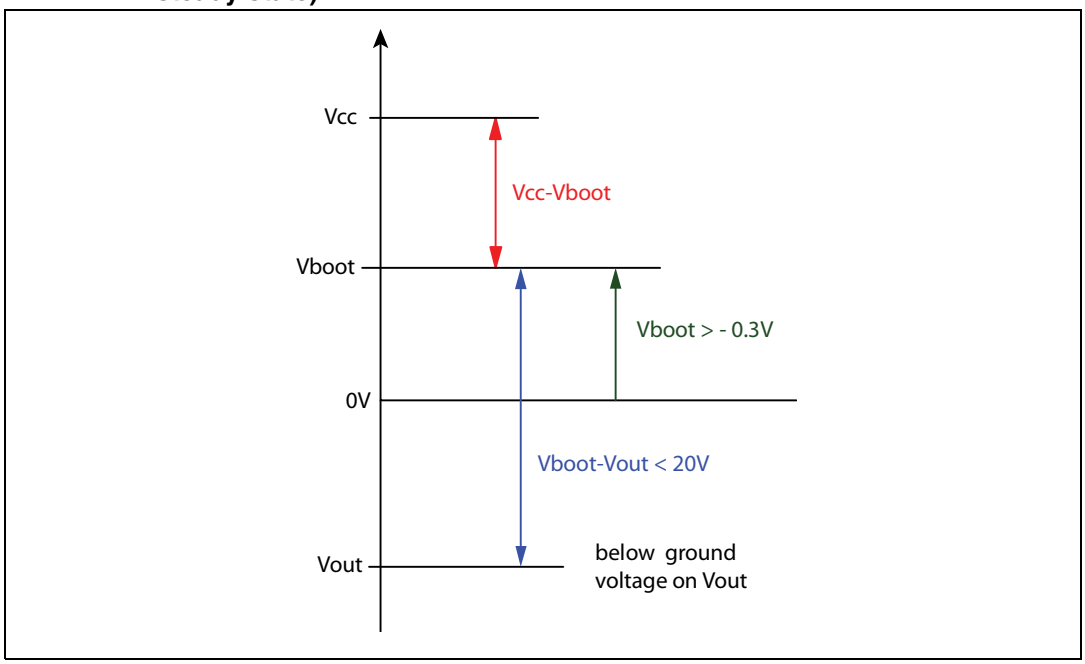


Regarding the below-ground voltage spike, typically this undershoot voltage has a very brief duration (less than 100 ns) and is not enough to further over-charge the bootstrap capacitor, because the charging time constant of the bootstrap is equal to the product of the C_{BOOT} and the R_{BOOT} resistance in series with the diode. Moreover, the higher this resistance, the lower the risk of bootstrap over-charging during BVG spikes.

For example, with a R_{BOOT} of 120 Ω and a C_{BOOT} of 100 nF, the associated time constant would be about 12 µs, much higher than typical below-ground voltage spike duration. Using an internal bootstrap diode it is very difficult to over-charge the floating section up to dangerous voltage levels with the very short duration of the undershoot spike. More attention should be given to the below-ground voltage of the V_{BOOT} during this spike because, as explained previously, the internal junction V_{BOOT} -to-substrate could turn on; typically for very short time (a few tenths of nanoseconds), this is not a problem.

In *Figure 41*, the main conditions to avoid issues related to the below-ground voltage phenomenon in steady-state are resumed. As explained in paragraph *11.1*, typically the static below-ground voltage is hardly higher than 2 V, so these constraints are usually not a limitation for most applications.

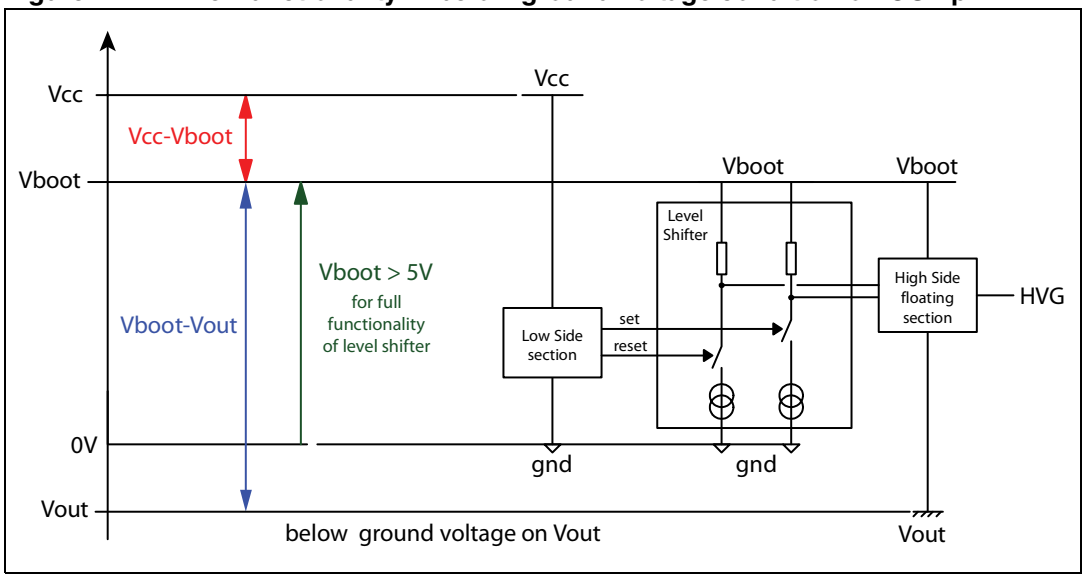
Figure 41. L6390 safe operating range when the OUT pin is below ground voltage (in steady state)



11.4 Functionality of L6390 outputs in below-ground condition

The L6390 IC gate driver makes use of a level shifter to send the set-reset information to the high side floating section. The level shifter, shown in *Figure 42*, is mainly composed of two high voltage switches, for set/reset signals, driven by the low voltage section and linked to two pull-up resistors connected to the BOOT pin.

Figure 42. Driver functionality in below-ground voltage condition on OUT pin



The two level-shifted signals are then fed into a logic latch in the high side floating section, providing the logic state for the high side gate driver (HVG output). The L6390 IC provides

full functionality of the switching operation of the high side section until the level shifter is operating. Because the two pull-up resistors are connected to the floating supply V_{BOOT} of the high side floating section, the driver still functions properly if the OUT voltage begins to go below ground. This means that the operating limit for the level shifter structure must be referred to the absolute value of the BOOT voltage relative to ground. In fact, the BOOT voltage can be considered the supply of the level shifter block. The minimum operating value of the level shifter supply is 5 V, so the V_{BOOT} value must be at least 5 V. The V_{BOOT} - V_{OUT} voltage can be any value in the 12.4 V to 20 V range. If the BOOT voltage is between 0 V and 5 V, the functionality of the level shifter is not guaranteed, but internal structures should not be damaged. Some examples are given in the following section.

11.4.1 Steady state (DC) conditions

When the LVG is off, the bootstrap diode turns on only when the BOOT voltage is about 2 V below the VCC (worst case: minimum voltage drop value), so it could over-charge the bootstrap capacitor up to a maximum voltage of about VCC - 2 V - V_{OUT}. To avoid exceeding the value of 20 V on V_{BOOT} - V_{OUT} voltage, the OUT pin could be forced permanently to the value of VCC - 2 V- 20 V with the L6390 IC still operating safely, making the HVG output switching as the HIN logic input (see the table below).

Table 3. Minimum V_{OUT} in DC condition providing safe and full operation of the high side section

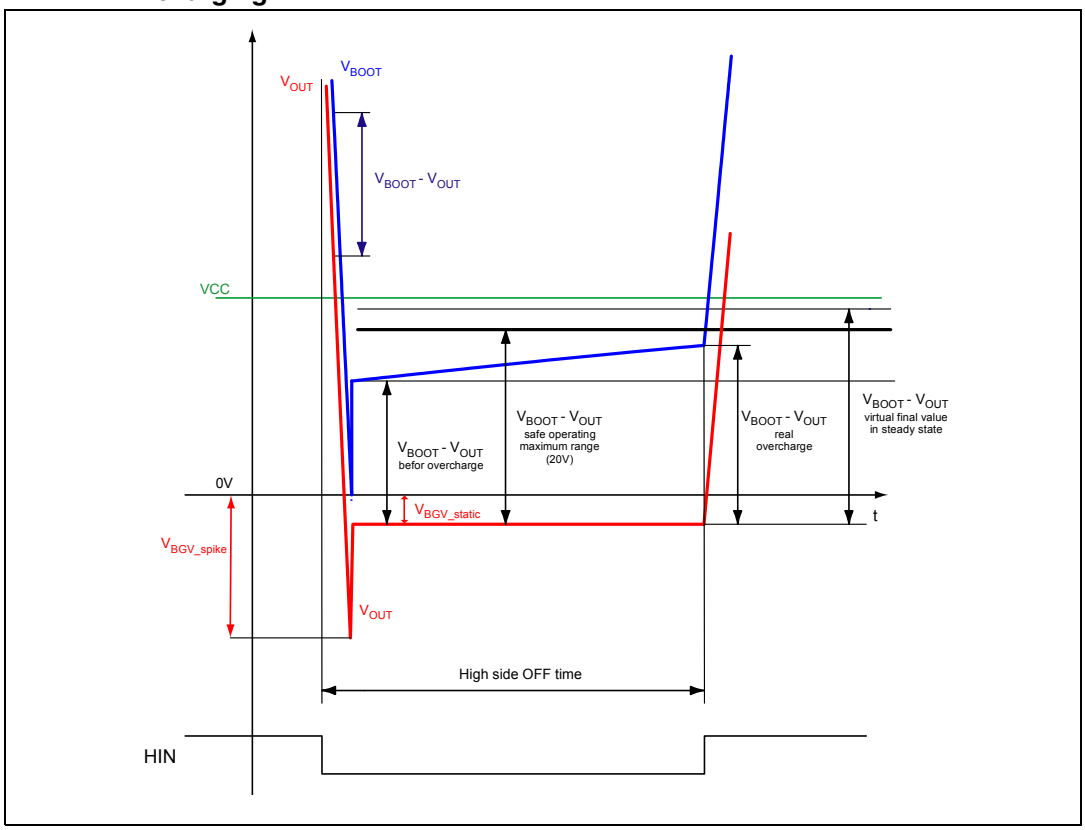
	Example 1	Example 2	Example 3
VCC	12.5	15	17
V_{BOOT}	10.5	13	15
V_{OUT} (min)	-9.5	-7	-5
V_{BOOT} - V_{OUT} (max)	20	20	20

It must be emphasized, as explained in the previous paragraph, how in most applications the static below-ground voltage of the OUT pin is very rarely lower than about - 2 V.

11.4.2 Transient conditions

If the time that the OUT pin goes below ground is limited, the bootstrap over-charge probably will not exceed the safe operating range (20 V) of V_{BOOT} - $V_{OUT,}$ even if the V_{OUT} voltage is lower than the limit of VCC - 2 V - 20 V. In this case the gate driver and the high side section are fully operational if the V_{BOOT} voltage remains above 5 V, as explained previously, for proper functioning of the high side level shifter. The logic state is anyway held if the V_{BOOT} remains above ground.

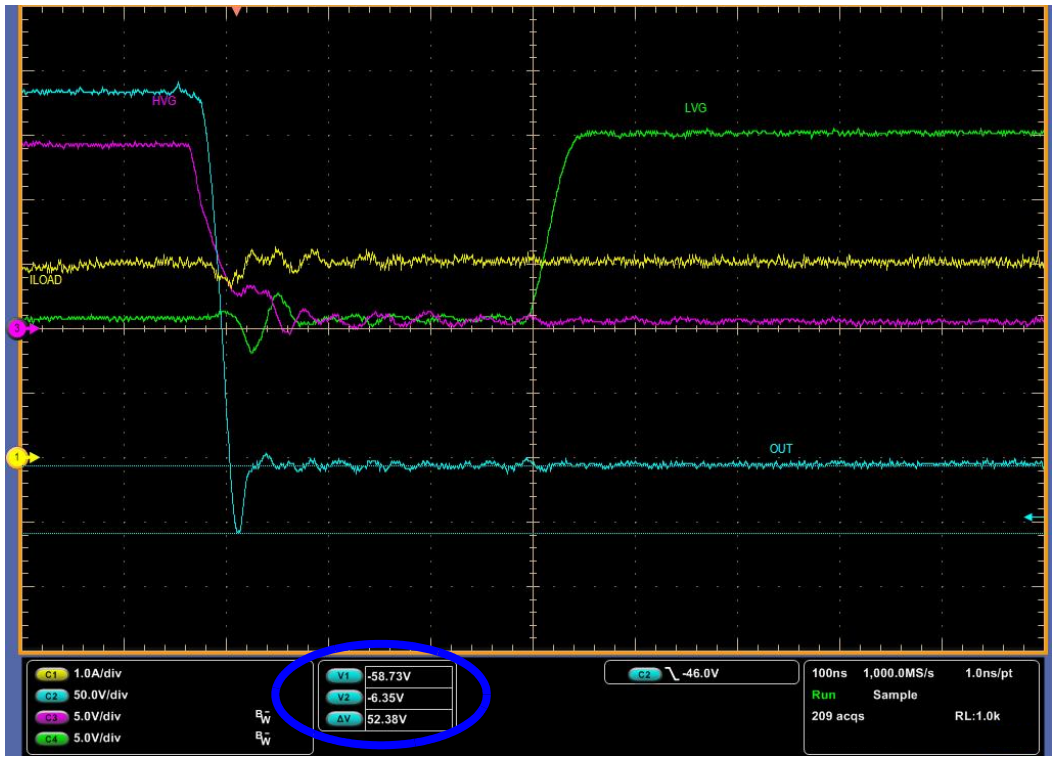
Figure 43. OUT below-ground voltage in transient conditions: limited boot over-charging



11.4.3 Below-ground voltage spikes

As previously stated, the duration of the dynamic contribution of the below-ground voltage on the OUT pin is not enough to over-charge the bootstrap capacitor. This fact usually removes the risk of exceeding the recommended maximum value of 20 V for V_{BOOT} -V_{OUT} voltage, but it increases the danger of pulling down the BOOT pin below ground, thus violating its absolute minimum rating. As mentioned above, this phenomenon should be avoided for safe IC gate driver operation. However, note that applicative bench tests have shown the L6390 proper operation even with below-ground spikes on the OUT pin well above - 50 V (see *Figure 44*).

Figure 44. Example of below-ground voltage spike



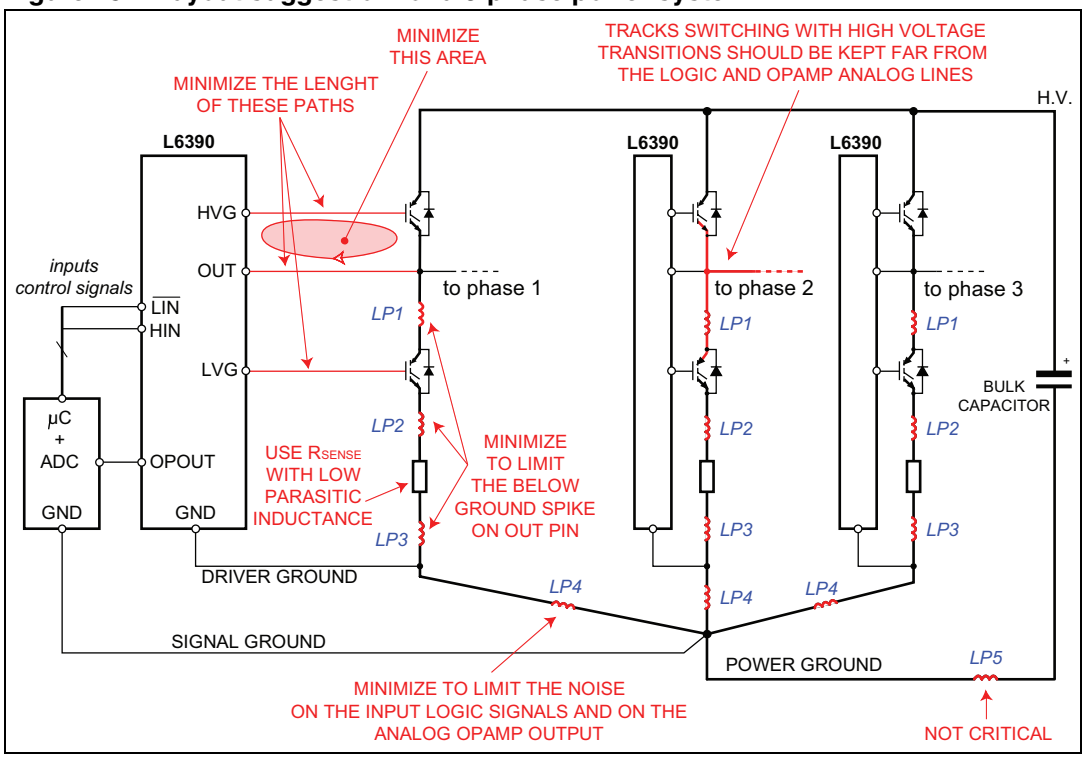
12 Layout suggestions

Typically, for power applications using high voltages and large load currents, the board layout of all circuits related to the power stage is important. Board layout includes several aspects, such as track dimensions (length and width), circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements and power sources in the PCB area.

Reasons to give particular attention to the PCB layout include EMI issues (both induced and perceived by the application) and over-voltage spikes due to parasitic inductances along the PCB traces, the proper connection of the sense blocks, the logic inputs and the analog outputs of the L6390 device. In fact, the L6390 IC not only has the function of driving the power stage, but also embeds analog sensing blocks such as comparator and op-amps. For example, especially regarding multi-phase power stages, it is important to keep the current reading, performed through the integrated op-amp, from ground noise.

In *Figure 45* some layout guidelines and suggestions for a 3-phase application are provided.

Figure 45. Layout suggestion for a 3-phase power system



As explained in *Section 8.9*, the gate driving PCB traces should be designed to be as short as possible and the area of the circuits should be minimized to avoid the sensitivity of such structures to the surrounding noise. Typically, a good power system layout keeps the power IGBTs (or MOSFETs) of each half-bridge as close as possible to the related gate driver.

In *Figure 45* a set of parasitic inductances related to the different circuit tracks is shown. The various groups of inductances may have undesired effects which should be limited as much as possible. Moreover, note that *Figure 45* emphasizes parasitic inductances located on the lines usually managing high voltages and fast current transitions, which are very noisy.

The group of LP1, LP2 and LP3 parasitic inductances is located along the low side path of each half-bridge, between the OUT pin and the ground of the related driver and provides an undesired contribution to the issue of below-ground voltage spike on each OUT pin of the L6390 device (as described in *Section 11.1*). In fact, at the beginning of the current recirculation on the low side switches, the current may experience a high dI/dt which may produce, on those parasitic inductances, significant voltage spikes. These spikes are summed with the voltage drop of the low side diode and with the R_{SENSE} and have a negative sign, so the overall voltage drop between OUT and GND may be significant. The recommendation is to limit as much as possible each contribution to this phenomenon by limiting the length of tracks LP1, LP2 and LP3 and using an R_{SENSE} resistor with low intrinsic inductance. More specifically, LP1 may be reduced by connecting the OUT line directly to the collector (or drain) of the low side IGBT (or MOSFET). LP2 may be reduced by placing the R_{SENSE} resistor as close as possible to the emitter (or source) of the low side IGBT (or MOSFET). The LP3 may be minimized by connecting the ground line (also called driver ground) of the related gate driver directly on the R_{SENSE} resistor.

LP4 represents the parasitic inductance located between the ground connections of each gate driver (driver ground) and the ground connection of the application controller (also called signal ground). Due to its location, this parasitic inductance introduces noise which is experienced by the input logic signals and the op-amp output analog signals. In fact, each phase of the bridge causes high currents (with high dI/dt) to flow on these paths, resulting in voltage noise which drops between the gate driver ground and the controller ground. This noise between the two grounds is directly added to all logic and analog voltage signals between the gate driver and the microcontroller included the input logic signals and the analog output of the related gate driver op-amp. It is recommended to minimize this noise by reducing the distance between the signal ground and the driver ground (for each gate driver in the system) as much as possible. Generally, it is recommended to connect the signal ground to the three driver grounds through a star connection, in order to improve the balancing and symmetry of the 3-phase driving topology.

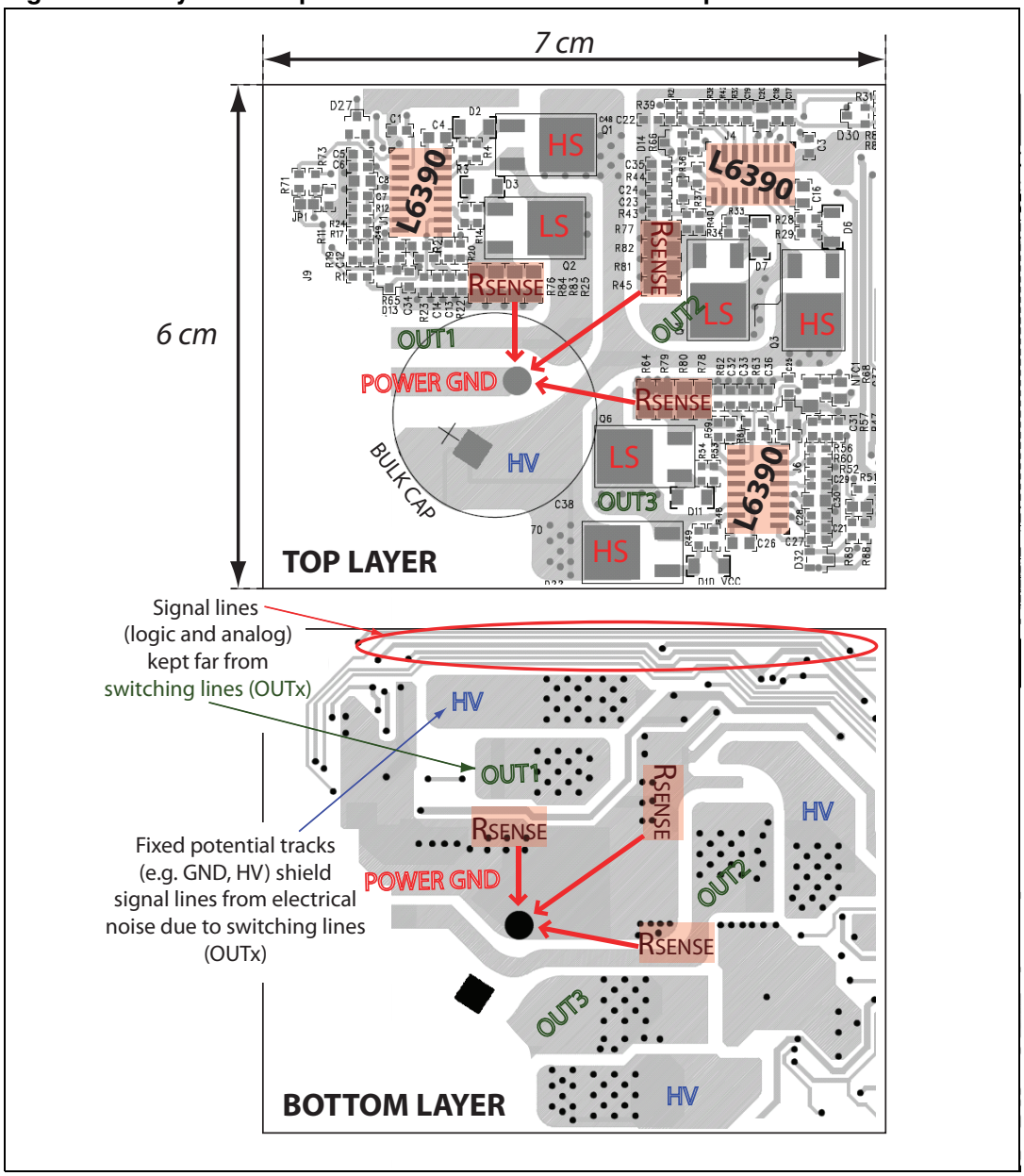
Note: It is very important to avoid any ground loop; only a single path must connect two different ground nodes.

The LP5 parasitic inductance is usually not critical, because it stands between the negative terminal of the bulk capacitor and the signal/power ground.The spikes on this parasitic element minimally influence other nodes of the system.

Another useful suggestion is to ensure some distance between the lines switching with high voltage transitions, and the signal lines sensitive to electrical noise. Specifically, the tracks of each OUT phase bringing significant currents and high voltages should be separated from the logic lines and analog sensing circuits of op-amps and comparators.

In *Figure 46* a practical example of the layout is provided. The example represents the 3-phase power stage section of the STEVAL-IHM021V1 demonstration board. It includes the L6390 gate drivers, the six IGBTs (or MOSFETs) in the DPAK package and the bulk capacitor. The layout suggestions described in this paragraph are implemented in the layout example in *Figure 46*. As described in *Figure 46*, the fixed voltage tracks, such as GND or HV lines, can be used to shield the logic and analog lines from the electrical noise produced by the switching lines (e.g. OUT1, OUT2 and OUT3). Each half-bridge ground is connected in a star configuration and the three R_{SENSE} resistors are very close to each other and to the power ground. Note also that the suggested 3-phase configuration occupies a modest amount of surface area (7 cm x 6 cm), and thanks to the SMD packages and board vias, no heat sinks are required.

Figure 46. Layout example from the STEVAL-IHM021V1 3-phase board



13 Revision history

Table 4. Document revision history

Date	Revision	Changes
02-Oct-2008	1	Initial release
03-Aug-2009	2	Removed chapter 11 The use of the resistor on the OUT line and added *Section 11.2: How to reduce the below ground spike voltage on page 40*.