AN3139
Application note

Migration and compatibility guidelines for STM8L microcontroller applications

Introduction

For designers of STM8L microcontroller applications, it is important to be able to replace easily one microcontroller type by another one in the same product family. Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on the memory size and on the number of I/Os.

However, to achieve cost reduction objectives, the user may need to switch to smaller components and to shrink the PCB area. This application note aims at analyzing the steps required to migrate from an existing STM8L-based design to any one of the other microcontroller types in the fast-growing STM8L family.

This application note groups all the most important information and provides a list of the fundamental aspects.

The information included in this document can also be extremely useful in a first STM8 design. Studying the issues in this phase can allow the user to adapt from the beginning his design to any future requirement.

To benefit fully from the information in this application note, the user should be familiar with the STM8L microcontroller family. The STM8L family reference manuals (RM0013 and RM0031), the STM8L datasheets, and the STM8L Flash program memory / data EEPROM programming manual (PM0054) are available from www.st.com.

This application note is divided into four main sections:

- **Section 1: STM8L family compatibility**: This section presents a first-level view of the different aspects of the STM8L family architecture that must be taken into account for a new design or migration. The microcontroller blocks and peripherals are grouped and identified either as “compatible” or “compatible with minor limitations”.
- **Section 2: Planning for migration:** This section gives an overview of common migration cases. It provides a checklist of items which are potentially impacted by each case to allow the user to quickly analyze which subjects have to be anticipated.
- **Section 3**: **Block-by-block compatibility**: This section focuses on the migration between different packages and details the pin-to-pin compatibility between all STM8L sub-families.
- **Section 4: Peripheral pinout through all STM8L sub-families**. This section shows the differences in the pinout for each peripheral.

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1 STM8L family compatibility

1.1 Family concept

The STM8L family is one of a growing number of different STM8 microcontroller families.

All these STM8 microcontroller families are based on a common robust and low-cost 8-bit high performance core with a rich set of enhanced peripherals. This ensures a high level of compatibility within the STM8L 'world', especially in terms of software development, compilers, debugging environment, programming tools and driver libraries.

The STM8L product family offers a wide choice of memory sizes and package types to fit different application requirements as closely as possible. Consequently, when there are new requirements on the application side, it can make sense to switch to another STM8L type with different memory capacity or package size.

The STM8L family includes a product line divided into two main sub-families:

- **STM8L15x/STM8L16x** sub-family of microcontrollers with different memory densities, packages and peripherals.
  - **The low density STM8L15x** devices are the STM8L151C2/K2/G2/F2, STM8L151C3/K3/G3/F3 microcontrollers with a 4-Kbyte or 8-Kbyte Flash memory density.
  - **The medium density STM8L15x** devices are the STM8L151C4/K4/G4, STM8L151C6/K6/G6, STM8L152C4/K4/G4 and STM8L152C6/K6/G6 microcontrollers with a 16-Kbyte or 32-Kbyte Flash memory density.
  - **The medium+ density STM8L15x** devices are the STM8L151R6 and STM8L152R6 microcontrollers with a 32-Kbyte Flash memory density. They offer a wider range of peripherals than the medium density devices.
  - **The high density STM8L15x** devices are the STM8L151x8 and STM8L152x8 microcontrollers with a Flash memory density equal to 64 Kbytes. They offer the same peripheral set as medium+ density devices.
  - **The high density STM8L162x** devices are the STM8L162x8 microcontrollers where the Flash memory density is equal to 64 Kbytes. They offer the same peripheral set as high density STM8L152 devices plus the AES hardware accelerator.
- **STM8L10x low density** sub-family where the Flash memory density ranges between 4 and 8 Kbytes. The STM8L10x MCUs are ideal for cost-sensitive applications with low code density.

Both sub-families provide a complete set of essential peripherals. STM8L10x devices target applications requiring reduced cost, lower memory capacity, fewer GPIOs and less advanced features.

The wide range of available pin-counts and package sizes is discussed in *Chapter 3.1: Package pinout*.

All STM8L family microcontrollers use the same application development tools:

- Embedded single wire interface module (SWIM)
- Software integrated development environment (IDE) tools including assembler, simulator, debugger, programmer:
  - ST Visual Develop (ST)
  - Ride (Raisonance)
  - IAR
- In-circuit debugging and programming tools
  - STIce from ST (full hardware emulator)
  - ST-Link from ST
  - RLink from Raisonance (low cost debug/programming tool)
- Starter kits and evaluation boards
- C compiler and assembler tool chains (Cosmic, Raisonance, IAR)
- Firmware libraries (peripheral control examples, MISRA or class B compliance, touch sensing)
- Application notes

By using a common development environment, you significantly reduce code maintenance effort and shorten the time-to-market, especially in cases when an application has to be migrated from one STM8 microcontroller to another.

By using the drivers provided in the STM8L firmware library to interface with the hardware, it becomes reasonably straightforward to move the application firmware from one STM8L product to another. The principle job is analyzing the details on the hardware side, taking care of the placement and availability of the peripheral I/O functions in the pinout. More details can be obtained in the STM8L datasheet and further in this document in *Section 3.1: Package pinout*.

Figure 1: STM8L family block diagram gives an overview of the STM8L blocks and their compatibility level, as discussed in the next sections.

Table 1. Overview of STM8L family peripherals

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	**Low density STM8L15x**	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
RAM	Up to 1.5 Kbytes	Up to 2 Kbytes	Up to 2 Kbytes	Up to 4 Kbytes
Flash Program memory	Up to 8 Kbytes	From 4 to 8 Kbytes	From 16 to 32 Kbytes	32 Kbytes in medium+ density devices 64 Kbytes in high density devices (STM8L15x/16x)

Table 1. Overview of STM8L family peripherals (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	**Low density STM8L15x**	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
Data EEPROM	Up to 2 Kbytes in Flash program memory Size configurable by option byte	Up to 1 Kbytes in separate memory array; Fixed size	Up to 1 Kbytes in separate memory array; Fixed size	Up to 2 Kbytes in separate memory array; Fixed size
Interrupt	Up to 26 Peripheral interrupt vectors	Up to 32 Peripheral interrupt vectors	Up to 32 Peripheral interrupt vectors	Up to 32 Peripheral interrupt vectors
CLK	Yes	Yes	Yes	Yes
AWU	Yes	Not available	Not available	Not available
RTC	Not available	Yes	Yes	Yes
Beep	Yes	Yes	Yes	Yes
IWDG	Yes	Yes	Yes	Yes
WWDG	Not available	Yes	Yes	Yes
COMP	Yes	Yes	Yes	Yes
RI & SYSCFG	Not available	Yes	Yes	Yes
GPIO	Up to 30I/Os (GPIOA..D)	Up to 41 I/Os (GPIOA..F)	Up to 41 I/Os (GPIOA..F)	Up to 68 I/Os (GPIOA..F) in high density devices
EXTI	Up to 29 external interrupt lines	Up to 40 external interrupt lines	Up to 40 external interrupt lines	Up to 67 external interrupt lines
DMA	Not available	DMA1 with 4 channels	DMA1 with 4 channels	DMA1 with 4 channels
ADC	Not available	ADC1	ADC1	ADC1
DAC	Not available	DAC1 channel	DAC 1 channels	DAC 2channels
TIM	Basic TIM4 General-purpose TIM2/3	Basic TIM4 General-purpose TIM2/3	Basic TIM4 General-purpose TIM2/3 Advanced-control TIM1	Basic TIM4 General-purpose TIM2/3/5 Advanced-control TIM1
Infrared Interface IRTIM	Yes	Yes	Yes	Yes
I2C	I2C	I2C1	I2C1	I2C1

Table 1. Overview of STM8L family peripherals (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
SPI	SPI	SPI1	SPI1	SPI1/SPI2
USART	USART	USART1	USART1	USART1/USART2/USART3
LCD	Not available	Yes	Yes	Yes
AES	Not available	Not available	Not available	Yes(1)

1. Available on high-density STM8L16x devices only.

1.2 Fully compatible blocks

The STM8L family embeds a set of system blocks which are by definition common to all products. Those blocks are identical, so they have the same structure, registers and control bits. There is no need to perform any software change to keep the same functionality at the application level after migration. When external components are needed (e.g. Vcap capacitor) no change is required from one product to another. All the features and behaviors remain the same. These blocks are shown in *Figure 1: STM8L family block diagram*.

Fully compatible parts and peripherals are:

- STM8 core
- Debug / SWIM module
- Power-on reset (POR)
- Voltage regulator
- Low speed internal RC (LSI)
- High speed internal RC (HSI)
- Independent watchdog
- Timers (TIM2, TIM3 and TIM4)
- IR (infrared interface)

1.3 Blocks that are compatible with minor exceptions

Some of the peripherals or functional blocks can have differences in their electrical parameters, structure, registers, control bits or other minor aspects but not in their main functionality.

Note: The RTC, ADC, DAC, DMA, WWDG, LCD, SPI2, USART2, USART3 and BootROM peripherals are not available in STM8L10x devices.

SPI2, USART2 and USART3 are not available in low and medium density STM8L15x devices.

The AES peripheral is available only in high density STM8L16x devices.

The AWU peripheral is not available in STM8L15x devices and is replaced by the RTC, so this aspect can also be considered as an incompatibility.

The following functional blocks can be considered as compatible with only a few negligible differences:

- GPIO (I/O capabilities)
- Interrupt management (interrupt vectors)
- Power control (wakeup from low power mode)
- I2C1 (true open drain)
- SPI1
- USART1
- Internal memories (Flash, SRAM, EEPROM)

You can find more details about these blocks in *Chapter 3: Block-by-block compatibility analysis*. You can also refer to *Figure 1: STM8L family block diagram*.

1.4 Blocks that are compatible with significant exceptions

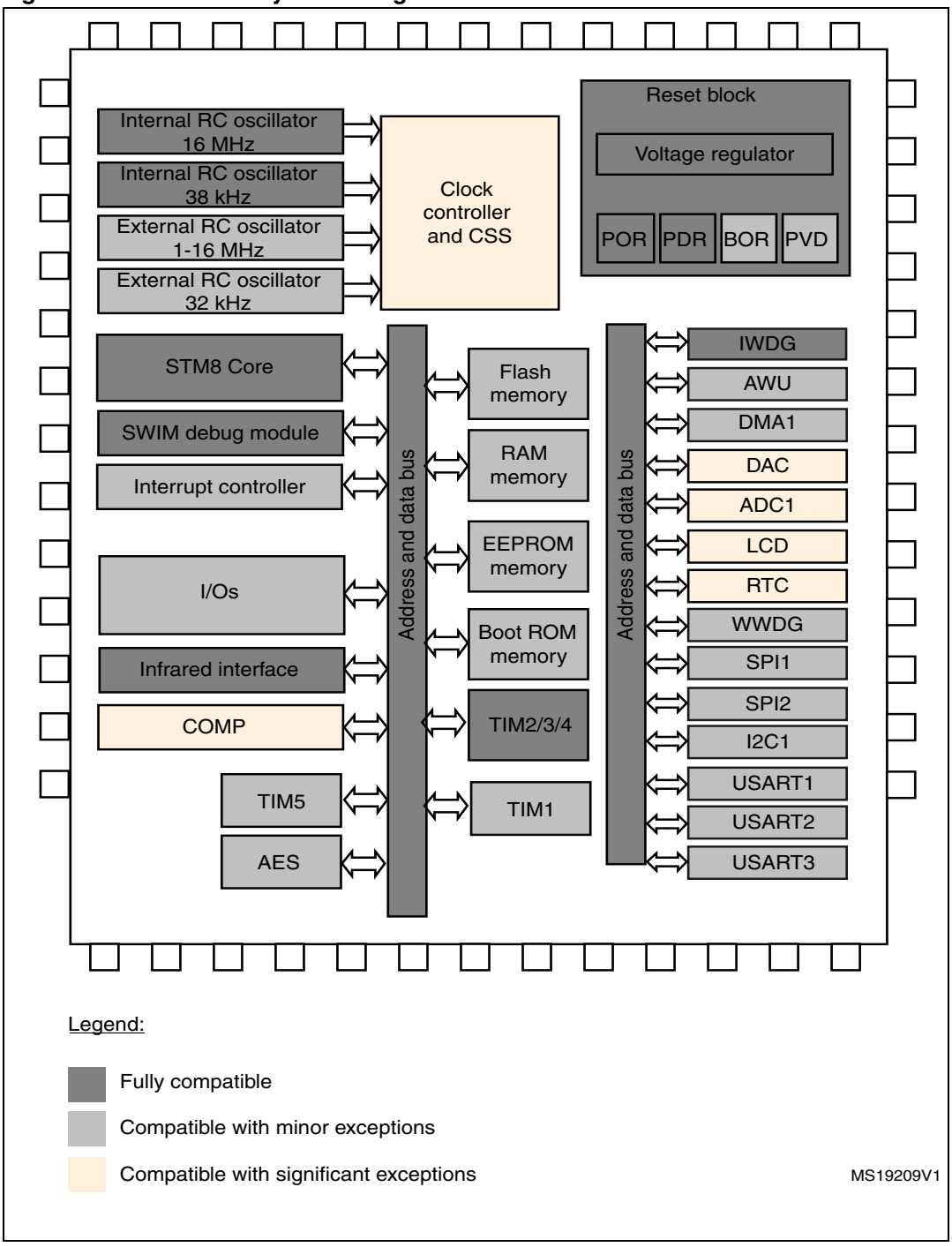
A few peripherals have additional features or less important functionalities compared to the same peripheral in another STM8L sub-family. For these particular peripherals you have to adapt the software drivers and check all possible hardware dependencies.

The peripheral and functional blocks in the following list are compatible with significant exceptions. The package pinout is high on the list as this aspect requires special attention:

- Package pinout
- CLK
- COMP
- ADC
- DAC
- LCD
- RTC

You can find more details in *Section 3: Block-by-block compatibility analysis*. You can also refer to *Figure 1: STM8L family block diagram*.

Figure 1. STM8L family block diagram



1. LCD, ADC1, WWDG, RTC, DAC, DMA, Boot ROM and AWU are fully compatible but not present in all STM8L devices.

1.5 Firmware library

The peripheral compatibility throughout STM8L MCU families promotes platform design and eases significantly the migration from one product line to the other. The software support is

however essential during development time. Extensive software libraries are available for both STM8L10x, STM8L15x and STM8L16x devices, providing the user with a hardware abstraction layer (HAL) for all MCU resources. Moreover, there is not a single control/status bit that is not covered by a C function or an API.

The software library covers three abstraction levels, and it includes:

1. A complete register address map with all bits, bit fields and registers declared in C. By providing this map, the software library makes the designers' task much lighter and, even more importantly so, it gives all the benefits of a bug-free reference mapping file, thus speeding up the early project phase.
2. A collection of routines and data structures in API form, that covers all peripheral functions. This collection can directly be used as a reference framework, since it also includes macros for supporting core-related intrinsic features and common constant and data type definition. Moreover, it is compiler agnostic and can therefore be used with any existing or future toolchain. It was developed using the MISRA C automotive standard.
3. A set of examples covering all available peripherals (35 examples so far for the STM8L10x sub-family, 35 for the STM8L15x sub-family), with template projects for the most common development toolchains. With the appropriate hardware evaluation board, only a few hours are needed to get started with a brand new microcontroller. It is then up to you to choose how to use the library. You can either pick up the files useful for the design, use examples to get trained or quickly evaluate the product. You can also use the API to save development time.

Let us now have a look at the few key files and concepts. Two separate libraries support the STM8L10x and STM8L15x devices. In the file names below, you simply need to replace the "*stm8l1xx_*" prefix by "*stm8l10x*" or "*stm8l15x*" depending on the chosen product.

- **stm8l1xx_.h**

This file is the only header file that must be included in the C source code, usually in *main.c*. This file contains:

  – data structures and address mapping for all peripherals
  – macros to access peripheral register hardware (for bit manipulation for instance), plus STM8 core intrinsics
  – a configuration section used to select the device implemented in the target application. You also have the choice to use or not the peripheral drivers in the application code (that is code based on direct access to registers rather than through API drivers)

- **stm8l1xx_conf.h**

This is the peripheral driver configuration file, where you specify the peripherals you want to use in your application, plus a few application-specific parameters such as the crystal frequency.

- **stm8l1xxx_it.c**

This file contains the template IRQ handler to be filled, but this is already the first development step.

Once you have understood the above operating principle and file organization, for simple applications, you could virtually switch from one product to the other without referring to the reference manual. *Figure 2: STM8L10x code example* and *Figure 3: STM8L15x code example* show the initialization code (using the firmware library) for STM8L10x and STM8L15x products, respectively.

Figure 2. STM8L10x code example

```
/* SPI configuration */
SPI_Init(SPI_FirstBit_MSB,
         SPI_BaudRatePrescaler_2,
         SPI_Mode_Master,
         SPI_CPOL_High,
         SPI_CPHA_2Edge,
         SPI_Direction_2Lines_FullDuplex,
         SPI_NSS_Soft);

/* Enable SPI */
SPI_Cmd(ENABLE);
```

Figure 3. STM8L15x code example

```
/* SPI configuration */
SPI_Init(SPI1,
         SPI_FirstBit_MSB,
         SPI_BaudRatePrescaler_2,
         SPI_Mode_Master,
         SPI_CPOL_High,
         SPI_CPHA_2Edge,
         SPI_Direction_2Lines_FullDuplex,
         SPI_NSS_Soft,
         0x07);
/* Enable SPI  */
SPI_Cmd(SPI1, ENABLE);
```

All parameters are identical, and the procedure is similar with two function calls for both configuration and startup.

The main difference is the additional peripherals of the same type that are added in the STM8L15x sub-family:

- when migrating from STM8L10x sub-family to STM8L15x sub-family, the additional peripheral must be added in every firmware library function as the first parameter (refer to *Figure 3*)
- when migrating from STM8L15x sub-family to STM8L10x sub-family, the additional peripheral given as the first parameter in every firmware library function must be removed (refer to *Figure 2*)

Another difference in the SPI peripheral is the CRC capability which is supported only in the STM8L15x devices. In the above example (*Figure 3.*), the CRC polynomial “0x07” is explicitly defined. This CRC polynomial parameter must be removed from the “init” function in the case of a migration from the STM8L15x sub-family to the STM8L10x sub-family.

The following table shows an overview of the firmware library compatibility between the two sub-families STM8L10x and STM8L15x/STM8L16x and between the different peripherals of the STM8L15x/STM8L16x sub-family. It describes the differences in terms of:

1. **New features** like the IrDA, Smartcard, Halfduplex and DAC dual channel features
2. **Common features** but with different implementations, like the comparator and CLK initialization.

To migrate from the STM8L10x sub-family to the STM8L15x/STM8L16x sub-family when using the communication peripherals (SPI, I2C or USART), you have to add the additional peripheral of the same type as the first parameter in every function used from the firmware library. A full compatibility, in terms of function parameter names, is guaranteed for all common features.

Table 2. STM8L firmware library compatibility

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x

Flash	`Same API`	`"/* New functions */`
		`1/ void FLASH_ProgramOptionByte(uint16_t Address, uint8_t Data);`
		`2/ void FLASH_EraseOptionByte(uint16_t Address);`
		`3/ void FLASH_PowerWaitModeConfig(FLASH_Power_TypeDef FLASH_Power);`
		`4/ void FLASH_PowerRunModeConfig(FLASH_Power_TypeDef FLASH_Power);`
		`5/ FLASH_PowerStatus_TypeDef FLASH_GetPowerStatus(void);`
		`"`
			`"/* New functions */`
			`1/ void FLASH_ProgramOptionByte(uint16_t Address, uint8_t Data);`
			`2/ void FLASH_EraseOptionByte(uint16_t Address);`
			`3/ void FLASH_PowerWaitModeConfig(FLASH_Power_TypeDef FLASH_Power);`
			`4/ void FLASH_PowerRunModeConfig(FLASH_Power_TypeDef FLASH_Power);`
			`5/ FLASH_PowerStatus_TypeDef FLASH_GetPowerStatus(void);`
			`"`
				`"/* New functions */`
				`1/ void FLASH_ProgramOptionByte(uint16_t Address, uint8_t Data);`
				`2/ void FLASH_EraseOptionByte(uint16_t Address);`
				`3/ void FLASH_PowerWaitModeConfig(FLASH_Power_TypeDef FLASH_Power);`
				`4/ void FLASH_PowerRunModeConfig(FLASH_Power_TypeDef FLASH_Power);`
				`5/ FLASH_PowerStatus_TypeDef FLASH_GetPowerStatus(void);`
				`"`

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
CLK	"/* New functions */ 1/ void CLK_CCOCmd(FunctionalState NewState); 2/ void CLK_PeripheralClockConfig(CLK_Peripheral_TypeDef CLK_Peripheral, FunctionalState NewState); 3/ void CLK_MasterPrescalerConfig(CLK_MasterPrescaler_TypeDef CLK_MasterPrescaler); 4/void CLK_CCOConfig(CLK_Output_TypeDef CLK_Output); "	"/* New functions */ 1/ void CLK_HSICmd(FunctionalState NewState); 2/ void CLK_AdjustHSICalibrationValue(uint8_t CLK_HSICalibrationValue); 3/ void CLK_LSICmd(FunctionalState NewState); 4/ void CLK_HSEConfig(CLK_HSE_TypeDef CLK_HSE); 5/ void CLK_LSEConfig(CLK_LSE_TypeDef CLK_LSE); 6/ void CLK_SYSCLKSourceConfig(CLK_SYSCLKSource_TypeDef CLK_SYSCLKSource); 7/ void CLK_SYSCLKDivConfig(CLK_SYSCLKDiv_TypeDef CLK_SYSCLKDiv); 8/ void CLK_SYSCLKSourceSwitchCmd(FunctionalState NewState); 9/ CLK_SYSCLKSource_TypeDef CLK_GetSYSCLKSource(void); 10/ void CLK_ClockSecuritySystemEnable(void);CLK_BEEPCLKSource); 11/ void CLK_ITConfig(CLK_IT_TypeDef CLK_IT, FunctionalState NewState);	"/* New functions */ 1/ void CLK_HSICmd(FunctionalState NewState); 2/ void CLK_AdjustHSICalibrationValue(uint8_t CLK_HSICalibrationValue); 3/ void CLK_LSICmd(FunctionalState NewState); 4/ void CLK_HSEConfig(CLK_HSE_TypeDef CLK_HSE); 5/ void CLK_LSEConfig(CLK_LSE_TypeDef CLK_LSE); 6/ void CLK_SYSCLKSourceConfig(CLK_SYSCLKSource_TypeDef CLK_SYSCLKSource); 7/ void CLK_SYSCLKDivConfig(CLK_SYSCLKDiv_TypeDef CLK_SYSCLKDiv); 8/ void CLK_SYSCLKSourceSwitchCmd(FunctionalState NewState); 9/ CLK_SYSCLKSource_TypeDef CLK_GetSYSCLKSource(void); 10/ void CLK_ClockSecuritySystemEnable(void); 11/ void CLK_ITConfig(CLK_IT_TypeDef CLK_IT, FunctionalState NewState);	"/* New functions */ 1/ void CLK_HSICmd(FunctionalState NewState); 2/ void CLK_AdjustHSICalibrationValue(uint8_t CLK_HSICalibrationValue); 3/ void CLK_LSICmd(FunctionalState NewState); 4/ void CLK_HSEConfig(CLK_HSE_TypeDef CLK_HSE); 5/ void CLK_LSEConfig(CLK_LSE_TypeDef CLK_LSE); 6/ void CLK_SYSCLKSourceConfig(CLK_SYSCLKSource_TypeDef CLK_SYSCLKSource); 7/ void CLK_SYSCLKDivConfig(CLK_SYSCLKDiv_TypeDef CLK_SYSCLKDiv); 8/ void CLK_SYSCLKSourceSwitchCmd(FunctionalState NewState); 9/ CLK_SYSCLKSource_TypeDef CLK_GetSYSCLKSource(void); 10/ void CLK_ClockSecuritySystemEnable(void); 11/ void CLK_ITConfig(CLK_IT_TypeDef CLK_IT, FunctionalState NewState); "	"/* New functions */ 1/ void CLK_HSICmd(FunctionalState NewState); 2/ void CLK_AdjustHSICalibrationValue(uint8_t CLK_HSICalibrationValue); 3/ void CLK_LSICmd(FunctionalState NewState); 4/ void CLK_HSEConfig(CLK_HSE_TypeDef CLK_HSE); 5/ void CLK_LSEConfig(CLK_LSE_TypeDef CLK_LSE); 6/ void CLK_SYSCLKSourceConfig(CLK_SYSCLKSource_TypeDef CLK_SYSCLKSource); 7/ void CLK_SYSCLKDivConfig(CLK_SYSCLKDiv_TypeDef CLK_SYSCLKDiv); 8/ void CLK_SYSCLKSourceSwitchCmd(FunctionalState NewState); 9/ CLK_SYSCLKSource_TypeDef CLK_GetSYSCLKSource(void); 10/ void CLK_ClockSecuritySystemEnable(void); 11/ void CLK_ITConfig(CLK_IT_TypeDef CLK_IT, FunctionalState NewState); "

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
CLK		12/ void CLK_CCOConfig(CLK_CCOSource_TypeDef CLK_CCOSource, CLK_CCODiv_TypeDef CLK_CCODiv); 13/ void CLK_RTCClockConfig(CLK_RTCCLKSource_TypeDef CLK_RTCCLKSource, CLK_RTCCLKDiv_TypeDef CLK_RTCCLKDiv); 14/ void CLK_BEEPClockConfig(CLK_BEEPCLKSource_TypeDef 15/ void CLK_PeripheralClockConfig(CLK_Peripheral_TypeDef CLK_Peripheral, FunctionalState NewState); 16/ void CLK_LSEClockSecuritySystemEnable(void); 17/ void CLK_RTCCLKSwitchOnLSEFailureEnable(void);"	12/ void CLK_CCOConfig(CLK_CCOSource_TypeDef CLK_CCOSource, CLK_CCODiv_TypeDef CLK_CCODiv); 13/ void CLK_RTCClockConfig(CLK_RTCCLKSource_TypeDef CLK_RTCCLKSource, CLK_RTCCLKDiv_TypeDef CLK_RTCCLKDiv); 14/ void CLK_BEEPClockConfig(CLK_BEEPCLKSource_TypeDef CLK_BEEPCLKSource); 15/ void CLK_PeripheralClockConfig(CLK_Peripheral_TypeDef CLK_Peripheral, FunctionalState NewState); "	12/ void CLK_CCOConfig(CLK_CCOSource_TypeDef CLK_CCOSource, CLK_CCODiv_TypeDef CLK_CCODiv); 13/ void CLK_RTCClockConfig(CLK_RTCCLKSource_TypeDef CLK_RTCCLKSource, CLK_RTCCLKDiv_TypeDef CLK_RTCCLKDiv); 14/ void CLK_BEEPClockConfig(CLK_BEEPCLKSource_TypeDef CLK_BEEPCLKSource); 15/ void CLK_PeripheralClockConfig(CLK_Peripheral_TypeDef CLK_Peripheral, FunctionalState NewState); 16/ void CLK_LSEClockSecuritySystemEnable(void); 17/ void CLK_RTCCLKSwitchOnLSEFailureEnable(void);

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
COMP	"/*Updated functions*/ 1/ void COMP_Init(COMP_Selection_TypeDef COMP_Selection, COMP_Reference_TypeDef COMP_Reference, COMP_Polarity_TypeDef COMP_Polarity); 2/ void COMP_Cmd(FunctionalState NewState); 3/ void COMP_SelectionConfig(COMP_Selection_TypeDef COMP_Selection, FunctionalState NewState); 4/ void COMP_ITConfig(COMP_IT_TypeDef COMP_IT, FunctionalState NewState); 5/ void COMP_TIM2Config(COMP_TIM2Config_TypeDef COMP_TIM2Config); 6/ void COMP_SwitchConfig(COMP_Switch_TypeDef COMP_Switch, FunctionalState NewState);	"/*Updated functions*/ 1/ void COMP_Init(COMP_InvertingInput_Typedef COMP_InvertingInput, COMP_OutputSelect_Typedef COMP_OutputSelect, COMP_Speed_TypeDef COMP_Speed); 2/ void COMP_VrefintToCOMP1Connect(FunctionalState NewState); 3/ void COMP_EdgeConfig(COMP_Selection_TypeDef COMP_Selection, COMP_Edge_TypeDef COMP_Edge); 4/ COMP_OutputLevel_TypeDef COMP_GetOutputLevel(COMP_Selection_TypeDef COMP_Selection); 5/ void COMP_WindowCmd(FunctionalState NewState); 6/ void COMP_ITConfig(COMP_Selection_TypeDef COMP_Selection, FunctionalState NewState);	"/*Updated functions*/ 1/ void COMP_Init(COMP_InvertingInput_Typedef COMP_InvertingInput, COMP_OutputSelect_Typedef COMP_OutputSelect, COMP_Speed_TypeDef COMP_Speed); 2/ void COMP_VrefintToCOMP1Connect(FunctionalState NewState); 3/ void COMP_EdgeConfig(COMP_Selection_TypeDef COMP_Selection, COMP_Edge_TypeDef COMP_Edge); 4/ COMP_OutputLevel_TypeDef COMP_GetOutputLevel(COMP_Selection_TypeDef COMP_Selection); 5/ void COMP_WindowCmd(FunctionalState NewState); 6/ void COMP_ITConfig(COMP_Selection_TypeDef COMP_Selection, FunctionalState NewState);	"/*Updated functions*/ 1/ void COMP_Init(COMP_InvertingInput_Typedef COMP_InvertingInput, COMP_OutputSelect_Typedef COMP_OutputSelect, COMP_Speed_TypeDef COMP_Speed); 2/ void COMP_VrefintToCOMP1Connect(FunctionalState NewState); 3/ void COMP_EdgeConfig(COMP_Selection_TypeDef COMP_Selection, COMP_Edge_TypeDef COMP_Edge); 4/ COMP_OutputLevel_TypeDef COMP_GetOutputLevel(COMP_Selection_TypeDef COMP_Selection); 5/ void COMP_WindowCmd(FunctionalState NewState); 6/ void COMP_ITConfig(COMP_Selection_TypeDef COMP_Selection, FunctionalState NewState);

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
COMP	7/ void COMP_TIMConnect(COMP_TimersConnection_TypeDef COMP_TIMConnection); 8/ void COMP_SelectPolarity(COMP_Polarity_TypeDef COMP_Polarity); 9/ void COMP_SetReference(COMP_Reference_TypeDef COMP_Reference); 10/ FlagStatus COMP_GetOutputStatus(COMP_Output_TypeDef COMP_Output); 11/ FlagStatus COMP_GetFlagStatus(COMP_FLAG_TypeDef COMP_Flag);"	7/ void COMP_TriggerConfig(COMP_TriggerGroup_TypeDef COMP_TriggerGroup, COMP_TriggerPin_TypeDef COMP_TriggerPin, FunctionalState NewState); 8/ void COMP_VrefintOutputCmd(FunctionalState NewState); 9/ void COMP_SchmittTriggerCmd(FunctionalState NewState); 10/ FlagStatus COMP_GetFlagStatus(COMP_Selection_TypeDef COMP_Selection); 11/ void COMP_ClearFlag(COMP_Selection_TypeDef COMP_Selection); 12/ ITStatus COMP_GetITStatus(COMP_Selection_TypeDef COMP_Selection); 13/ void COMP_ClearITPendingBit(COMP_Selection_TypeDef COMP_Selection);"	7/ void COMP_TriggerConfig(COMP_TriggerGroup_TypeDef COMP_TriggerGroup, COMP_TriggerPin_TypeDef COMP_TriggerPin, FunctionalState NewState); 8/ void COMP_VrefintOutputCmd(FunctionalState NewState); 9/ void COMP_SchmittTriggerCmd(FunctionalState NewState); 10/ FlagStatus COMP_GetFlagStatus(COMP_Selection_TypeDef COMP_Selection); 11/ void COMP_ClearFlag(COMP_Selection_TypeDef COMP_Selection); 12/ ITStatus COMP_GetITStatus(COMP_Selection_TypeDef COMP_Selection); 13/ void COMP_ClearITPendingBit(COMP_Selection_TypeDef COMP_Selection);"	7/ void COMP_TriggerConfig(COMP_TriggerGroup_TypeDef COMP_TriggerGroup, COMP_TriggerPin_TypeDef COMP_TriggerPin, FunctionalState NewState); 8/ void COMP_VrefintOutputCmd(FunctionalState NewState); 9/ void COMP_SchmittTriggerCmd(FunctionalState NewState); 10/ FlagStatus COMP_GetFlagStatus(COMP_Selection_TypeDef COMP_Selection); 11/ void COMP_ClearFlag(COMP_Selection_TypeDef COMP_Selection); 12/ ITStatus COMP_GetITStatus(COMP_Selection_TypeDef COMP_Selection); 13/ void COMP_ClearITPendingBit(COMP_Selection_TypeDef COMP_Selection);"

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
I2C1	Same API	/* New functions */ 1/ void I2C_DMACmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 2/ void I2C_DMALastTransferCmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 3/ void I2C_ARPCmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 4/ void I2C_SMBusAlertConfig(I2C_TypeDef * I2Cx, I2C_SMBusAlert_TypeDef I2C_SMBusAlert); 5/ void I2C_PECPositionConfig(I2C_TypeDef* I2Cx, I2C_PECPosition_TypeDef I2C_PECPosition); 6/ void I2C_TransmitPEC(I2C_TypeDef* I2Cx, FunctionalState NewState); 7/ void I2C_CalculatePEC(I2C_TypeDef* I2Cx, FunctionalState NewState); . . .	/* New functions */ 1/ void I2C_DMACmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 2/ void I2C_DMALastTransferCmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 3/ void I2C_ARPCmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 4/ void I2C_SMBusAlertConfig(I2C_TypeDef * I2Cx, I2C_SMBusAlert_TypeDef I2C_SMBusAlert); 5/ void I2C_PECPositionConfig(I2C_TypeDef* I2Cx, I2C_PECPosition_TypeDef I2C_PECPosition); 6/ void I2C_TransmitPEC(I2C_TypeDef* I2Cx, FunctionalState NewState); 7/ void I2C_CalculatePEC(I2C_TypeDef* I2Cx, FunctionalState NewState); . . .	/* New functions */ 1/ void I2C_DMACmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 2/ void I2C_DMALastTransferCmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 3/ void I2C_ARPCmd(I2C_TypeDef* I2Cx, FunctionalState NewState); 4/ void I2C_SMBusAlertConfig(I2C_TypeDef * I2Cx, I2C_SMBusAlert_TypeDef I2C_SMBusAlert); 5/ void I2C_PECPositionConfig(I2C_TypeDef* I2Cx, I2C_PECPosition_TypeDef I2C_PECPosition); 6/ void I2C_TransmitPEC(I2C_TypeDef* I2Cx, FunctionalState NewState); 7/ void I2C_CalculatePEC(I2C_TypeDef* I2Cx, FunctionalState NewState); . . .

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
SPIx	"/*Updated functions*/ 1/ void SPI_Init(SPI_FirstBit_TypeDef SPI_FirstBit, SPI_BaudRatePrescaler_TypeDef SPI_BaudRatePrescaler, SPI_Mode_TypeDef SPI_Mode, SPI_CPOL_TypeDef SPI_CPOL, SPI_CPHA_TypeDef SPI_CPHA, SPI_DirectionMode_TypeDef SPI_Data_Direction, SPI_NSS_TypeDef SPI_Slave_Management);"	"/* New functions */ 1/ void SPI_TransmitCRC(SPI_TypeDef* SPIx); 2/ void SPI_CalculateCRCCmd(SPI_TypeDef* SPIx, FunctionalState NewState); 3/ uint8_t SPI_GetCRC(SPI_TypeDef* SPIx, SPI_CRC_TypeDef SPI_CRC); 4/ void SPI_ResetCRC(SPI_TypeDef* SPIx); 5/ uint8_t SPI_GetCRCPolynomial(SPI_TypeDef * SPIx); 6/ void SPI_DMACmd(SPI_TypeDef* SPIx, SPI_DMAReq_TypeDef SPI_DMAReq, FunctionalState NewState);	"/* New functions */ 1/ void SPI_TransmitCRC(SPI_TypeDef* SPIx); 2/ void SPI_CalculateCRCCmd(SPI_TypeDef* SPIx, FunctionalState NewState); 3/ uint8_t SPI_GetCRC(SPI_TypeDef* SPIx, SPI_CRC_TypeDef SPI_CRC); 4/ void SPI_ResetCRC(SPI_TypeDef* SPIx); 5/ uint8_t SPI_GetCRCPolynomial(SPI_TypeDef * SPIx); 6/ void SPI_DMACmd(SPI_TypeDef* SPIx, SPI_DMAReq_TypeDef SPI_DMAReq, FunctionalState NewState);	"/* New functions */ 1/ void SPI_TransmitCRC(SPI_TypeDef* SPIx); 2/ void SPI_CalculateCRCCmd(SPI_TypeDef* SPIx, FunctionalState NewState); 3/ uint8_t SPI_GetCRC(SPI_TypeDef* SPIx, SPI_CRC_TypeDef SPI_CRC); 4/ void SPI_ResetCRC(SPI_TypeDef* SPIx); 5/ uint8_t SPI_GetCRCPolynomial(SPI_TypeDef * SPIx); 6/ void SPI_DMACmd(SPI_TypeDef* SPIx, SPI_DMAReq_TypeDef SPI_DMAReq, FunctionalState NewState);

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
		/*Updated functions*/ 1/ void SPI_Init(SPI_TypeDef* SPIx, SPI_FirstBit_TypeDef SPI_FirstBit, SPI_BaudRatePrescaler_TypeDef SPI_BaudRatePrescaler, SPI_Mode_TypeDef SPI_Mode, SPI_CPOL_TypeDef SPI_CPOL, SPI_CPHA_TypeDef SPI_CPHA, SPI_DirectionMode_TypeDef SPI_Data_Direction, SPI_NSS_TypeDef SPI_Slave_Management, uint8_t CRCPolynomial);"	/*Updated functions*/ 1/ void SPI_Init(SPI_TypeDef* SPIx, SPI_FirstBit_TypeDef SPI_FirstBit, SPI_BaudRatePrescaler_TypeDef SPI_BaudRatePrescaler, SPI_Mode_TypeDef SPI_Mode, SPI_CPOL_TypeDef SPI_CPOL, SPI_CPHA_TypeDef SPI_CPHA, SPI_DirectionMode_TypeDef SPI_Data_Direction, SPI_NSS_TypeDef SPI_Slave_Management, uint8_t CRCPolynomial);"	/*Updated functions*/ 1/ void SPI_Init(SPI_TypeDef* SPIx, SPI_FirstBit_TypeDef SPI_FirstBit, SPI_BaudRatePrescaler_TypeDef SPI_BaudRatePrescaler, SPI_Mode_TypeDef SPI_Mode, SPI_CPOL_TypeDef SPI_CPOL, SPI_CPHA_TypeDef SPI_CPHA, SPI_DirectionMode_TypeDef SPI_Data_Direction, SPI_NSS_TypeDef SPI_Slave_Management, uint8_t CRCPolynomial);"

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
USARTx		"/* New functions */ 1/ void USART_HalfDuplexCmd(USART_TypeDef* USARTx, FunctionalState NewState); 2/ void USART_IrDAConfig(USART_TypeDef* USARTx, USART_IrDAMode_TypeDef USART_IrDAMode); 3/ void USART_IrDACmd(USART_TypeDef* USARTx, FunctionalState NewState); 4/ void USART_SmartCardCmd(USART_TypeDef * USARTx, FunctionalState NewState); 5/ void USART_SmartCardNACKCmd(USART_TypeDef* USARTx, FunctionalState NewState); 6/ void USART_SetGuardTime(USART_TypeDef * USARTx, uint8_t USART_GuardTime); 7/ void USART_SetPrescaler(USART_TypeDef * USARTx, uint8_t USART_Prescaler);"	"/* New functions */ 1/ void USART_HalfDuplexCmd(USART_TypeDef* USARTx, FunctionalState NewState); 2/ void USART_IrDAConfig(USART_TypeDef* USARTx, USART_IrDAMode_TypeDef USART_IrDAMode); 3/ void USART_IrDACmd(USART_TypeDef* USARTx, FunctionalState NewState); 4/ void USART_SmartCardCmd(USART_TypeDef * USARTx, FunctionalState NewState); 5/ void USART_SmartCardNACKCmd(USART_TypeDef* USARTx, FunctionalState NewState); 6/ void USART_SetGuardTime(USART_TypeDef * USARTx, uint8_t USART_GuardTime); 7/ void USART_SetPrescaler(USART_TypeDef * USARTx, uint8_t USART_Prescaler);"	"/* New functions */ 1/ void USART_HalfDuplexCmd(USART_TypeDef* USARTx, FunctionalState NewState); 2/ void USART_IrDAConfig(USART_TypeDef* USARTx, USART_IrDAMode_TypeDef USART_IrDAMode); 3/ void USART_IrDACmd(USART_TypeDef* USARTx, FunctionalState NewState); 4/ void USART_SmartCardCmd(USART_TypeDef * USARTx, FunctionalState NewState); 5/ void USART_SmartCardNACKCmd(USART_TypeDef* USARTx, FunctionalState NewState); 6/ void USART_SetGuardTime(USART_TypeDef * USARTx, uint8_t USART_GuardTime); 7/ void USART_SetPrescaler(USART_TypeDef * USARTx, uint8_t USART_Prescaler);"
ITC	Same API	Same API	Same API	Same API
PWR	Not available	Same API	Same API	Same API
WFE	Same API	Same API	Same API	Same API
RST	Same API	Same API	Same API	Same API
GPIO	Same API	Same API	Same API	Same API
EXTI	Same API	Same API	Same API	Same API
DMA1	Not available	Same API	Same API	Same API

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
ADC1	Not available	Same API	Same API	Same API
DAC	Not available	Same API	Same API	"/* New functions */ 1/ void DAC_DualSoftwareTriggerCmd(FunctionalState NewState); 2/ void DAC_WaveGenerationCmd(DAC_Channel_TypeDef DAC_Channel, DAC_Wave_TypeDef DAC_Wave, FunctionalState NewState); 3/ void DAC_SetNoiseWaveLFSR(DAC_Channel_TypeDef DAC_Channel, DAC_LFSRUnmask_TypeDef DAC_LFSRUnmask); 4/ void DAC_SetTriangleWaveAmplitude(DAC_Channel_TypeDef DAC_Channel, DAC_TriangleAmplitude_TypeDef DAC_TriangleAmplitude); 5/ void DAC_SetChannel2Data(DAC_Align_TypeDef DAC_Align, uint16_t DAC_Data); 6/ void DAC_SetDualChannelData(DAC_Align_TypeDef DAC_Align, uint16_t DAC_Data2, uint16_t DAC_Data1);"
IRTIM	Same API	Same API	Same Peripheral	Same API
TIM1	Not available	Not available	Same Peripheral	Same API
TIM2/3/4	Same API	Same API	Same Peripheral	Same API
TIM5	Not available	Not available	Not available	New Peripheral
AWU	Same API	Not available	Not available	Not available
RTC	Not available	Please refer to the AN3133 application note (Using the STM8L15x/STM8L16x real time clock).		
BEEP	Same API	Same API	Same API	Same API

Table 2. STM8L firmware library compatibility (continued)

Peripheral	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
WWDG	Not available	Same API	Same API	Same API
IWDG	Same API	Same API	Same API	Same API
SYSCFG	Not available	Same API	Same API	Same API
AES	Not available	Not available	Not available	New Peripheral

2 Planning for migration

To migrate your application from one sub-family to another, you have to analyze the hardware migration as well as the application resources and firmware migration.

2.1 Hardware migration

If you use the same package and the same pin numbers, you can use the same PCB without any modification. All sub-families are pin-to-pin compatible.

2.2 Application resources and firmware migration

You have to analyze the compatibility level of your peripherals between the initial sub-family and the new sub-family in the following cases:

- If you use the same resources and peripherals of the same type
  - you do not have to modify anything in your code except the clock configuration (Example: TIMx)
- If you use the same resources and different peripherals of the same type
  - If one peripheral of the same type is not present any more, you can change the reference to this peripheral and all related features (pin, clock and interrupt configuration).
- If you use new resources and/or new peripherals of the same type
  - If you need to migrate the application from STM8L10x devices to STM815x devices without using the new peripherals, the user software can be kept as is without any modification except the clock configuration. Using the standard Peripherals library has several advantages: it saves coding time while simultaneously reducing application development and integration costs.

The following table explains how to migrate from one sub-family to another and from one package to another.

The table is intended to be used as follows:

- Sub-families or devices within the family are listed in rows. Moving between the rows means changing the sub-family or changing the device.
- Available package sizes are listed in columns. Moving between columns means changing the pin-count.
- The gray fields represent the migration between each column or row and give the impacted features.

The impact of moves between two subfamilies is common for all available package pairs. Therefore all gray cells in rows are merged into common fields. The text in these common fields is as follows:

- When migrating downwards: the row between both sub-families lists the features that are lost due to the migration.
- When migrating upwards, the row between both sub-families lists the features that are added due to the migration.

A move to the right towards smaller packages mainly leads to a loss of I/O pins. So the content of these cells is a simple list of impacted items only.

This section mainly discusses cases of migration between neighboring pairs. However, your project may be a migration over several rows or columns in *Table 3* or even in a diagonal direction. In this case, you should check the differences indicated in each step passed by the vertical and horizontal moves through the following table.

Table 3. STM8L family migration products

		Pin-count →										
			20	28			32		48		64		80
Functionality	STM8L10x	Low-density		Pin-to-pin compatible		Pin-to-pin compatible							
	STM8L15x/STM8L16x				Pin-to-pin compatible RTC +ADC +COMP		Pin-to-pin compatible RTC +ADC +COMP						
		Low-density				Pin-to-pin compatible		Pin-to-pin compatible					
					Pin-to-pin compatible + TIM1		Pin-to-pin compatible + TIM1+ LCD		Pin-to-pin compatible + TIM1+LCD				
		Medium-density				Pin-to-pin compatible + LCD		Pin-to-pin compatible					
									Pin-to-pin compatible +TIM5, SPI2, USART2, USART3, AES				
		Medium+ and High density								Pin-to-pin compatible		Pin-to-pin compatible	

3 Block-by-block compatibility analysis

3.1 Package pinout

The following table gives an overview of the available packages in each STM8L family

Table 4. Overview of STM8L family packages

Package	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
LQFP80	Not available	Not available	Not available	x
LQFP64	Not available	Not available	Not available	x
UFQFPN48	Not available	Not available	Not available	x
LQFP48	Not available	x	x	x
LQFP32	x	Not available	x	Not available
VFQFPN48	Not available	Not available	x	Not available
WFQFPN32	Not available	Not available	x	Not available
WFQFPN28	Not available	Not available	x	Not available
UFQFPN28	Not available	x	x	Not available
UFQFPN32	x	x	Not available	Not available
UFQFPN28	x	x	Not available	Not available
UFQFPN28	x	x	Not available	Not available
UFQFPN20	x	x	Not available	Not available
UFQFPN20	Not available	x	Not available	Not available

3.1.1 Digital power supply

The digital power supply design includes two supply sources. The purpose is to distribute the current flowing through the I/O logic separately from the rest of the digital microcontroller

circuits. Up to two V_{DDIO} / V_{SSIO} pin pairs are used as well as the main V_{DD} / V_{SS} digital supply pair, depending on the pin-count:

- Both V_{DDIO} pairs are present in the 48-pin package in the STM8L15x/STM8L16x sub-family.
- Only one V_{DDIO} pin is available to supply power to the I/Os in the STM8L10x and STM8L15x/STM8L16x sub-families from 32-pin packages to 20-pin packages.

The total output current is limited by the number of supply pins. The total output current capability declines for smaller packages, regardless of the number of I/Os with high-sink capability.

In the medium, medium+ and high density STM8L15x/STM8L16x devices,, the V_{LCD} pin for connecting the external voltage source for the LCD is present on the 48-pin and 32-pin packages when the LCD is available.

3.1.2 ADC power supply and voltage reference

The analog power supply design includes an extra power supply for the analog parts of the microcontroller and an external reference voltage connected via an extra pin pair.

- The V_{DDA}/V_{SSA} and the V_{REF+}/V_{REF-} analog supply pin pair are present on the 28-pin and 48-pin packages in the STM8L15x/STM8L16x sub-family. Without these pins, it is not possible to use the ADC zooming function feature (see *Section 3.4: ADC modes* for more details).
- For the rest of the STM8L15x/STM8L16x sub-family (32-pin package) the ADC reference is taken from the main analog supply V_{DDA}.

Note: As the ADC is not present in the STM8L10x family, V_{DDA}/V_{SSA} and V_{REF+}/V_{REF} analog supply pins are not available on packages for this family.

3.1.3 Alternate functions

The main purpose of the alternate feature concept is to keep the microcontroller configurable for different user and application needs. This is especially important and useful in low pin-count packages.

Default alternate functions can be enabled on dedicated pins by settings in the peripheral registers.

In the STM8L15x/STM8L16x sub-family, a large number of alternate functions can be remapped to other pins by programming the system configuration controller registers. Consequently, many functions that would otherwise be lost by migrating to a smaller package size are preserved by remapping alternate functions to the remaining pins. For more details on pinout and packages, please refer to the related datasheet.

3.2 GPIO and peripheral registers

3.2.1 Mapping overview

The space for the GPIO and peripheral registers is mapped in the memory area between addresses 0x5000 and 0x57FF. The register blocks for each peripheral available in the sub-family have the same start addresses and the same register names.

The STM8L15x/STM8L16x sub-family, family has some peripherals that are not supported in the STM8L10x sub-family. In addition, some peripherals are not fully compatible between the two families, which explains why two firmware libraries are developed: one for the STM8L10x sub-family and the other for the STM8L15x/STM8L16x sub-family. To avoid any confusion for the user, when a peripheral feature is available in more than one sub-family, this feature has the same function name.

The following tables *Table 5: Overview of STM8L family memory addresses* and *Table 6: Overview of STM8L family peripheral addresses* give an overview of the mapping in the STM8L family.

Table 5. Overview of STM8L family memory addresses

Memory	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
RAM including stack	0x00 0000 - 0x00 5FF	0x00 0000 - 0x00 7FF	0x00 0000 - 0x00 7FF	0x00 0000 - 0x00 7FF
reserved	NA	0x00 0800 - 0x00 0FFF	0x00 0800 - 0x00 0FFF	0x00 0800 - 0x00 0FFF
Data EEPROM		0x00 1000 - 0x00 10FF	0x00 1000 - 0x00 13FF	0x00 1000 - 0x00 17FF
reserved	0x00 600 - 0x00 47FF	0x00 1100 - 0x00 47FF	0x00 1400 - 0x00 47FF	0x00 1800 - 0x00 47FF
Option bytes	0x00 4800 - 0x00 48FF	0x00 4800 - 0x00 48FF	0x00 4800 - 0x00 48FF	0x00 4800 - 0x00 48FF
reserved	0x00 4900 - 0x00 49FF	0x00 4900 - 0x00 49FF	0x00 4900 - 0x00 49FF	0x00 4900 - 0x00 49FF
GPIO and Peripheral register	0x00 5000 - 0x00 57FF	0x00 5000 - 0x00 57FF	0x00 5000 - 0x00 57FF	0x00 5000 - 0x00 57FF
reserved	NA	0x00 5800 - 0x00 59FF	0x00 5800 - 0x00 59FF	0x00 5800 - 0x00 59FF
Boot ROM		0x00 6000 - 0x00 67FF	0x00 6000 - 0x00 67FF	0x00 6000 - 0x00 67FF
reserved	0x00 5800 - 0x00 7EFF	0x00 6800 - 0x00 7EFF	0x00 6800 - 0x00 7EFF	0x00 6800 - 0x00 7EFF
CPU/SWIM/ Debug/ITC Registers	0X00 7F00 - 0x00 7FFF	0X00 7F00 - 0x00 7FFF	0X00 7F00 - 0x00 7FFF	0X00 7F00 - 0x00 7FFF
Flash program memory	0X00 8000 - 0x00 9FFF	0X00 8000 - 0x00 9FFF	0X00 8000 - 0x00 FFFF	0X00 8000 - 0x01 7FFF

Note: The gray cells show that the memory type is not present.

Table 6. Overview of STM8L family peripheral addresses

Bus	STM8L10x		STM8L15x/STM8L16x		
	Peripheral	**Low density STM8L10x**	**Low density STM8L15x**	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
Address data bus	GPIO	0x00 5000 - 0x00 5013	0x00 5000 - 0x00 501D	0x00 5000 - 0x00 501D	0x00 5000 - 0x00 502C
	Reserved	0x00 5014 - 0x00 5049	0x00 501E - 0x00 5049	0x00 501E - 0x00 5049	0x00 502D - 0x00 5049
	Flash	0x00 5050 - 0x00 5054	0x00 5050 - 0x00 5054	0x00 5050 - 0x00 5054	0x00 5050 - 0x00 5054
	Reserved		0x00 5055 - 0x00 506F	0x00 5055 - 0x00 506F	0x00 5055 - 0x00 506F
	DMA1		0x00 5070 - 0x00 509A	0x00 5070 - 0x00 509A	0x00 5070 - 0x00 509A
	Reserved	0x00 5055 - 0x00 509F	0x00 509B - 0x00 509D	0x00 509B - 0x00 509D	0x00 509B - 0x00 509C
	SYSCFG		0x00 509E - 0x00 509F	0x00 509E - 0x00 509F	0x00 509D - 0x00 509F
	ITC-EXTI	0x00 50A0 - 0x00 50A5	0x00 50A0 - 0x00 50A5	0x00 50A0 - 0x00 50A5	0x00 50A0 - 0x00 50A5
	WFE	0x00 50A6 - 0x00 50A7	0x00 50A6 - 0x00 50A8	0x00 50A6 - 0x00 50A8	0x00 50A6 - 0x00 50A8
	Reserved	0x00 50A8 - 0x00 50AF	0x00 50A9 - 0x00 50AF	0x00 50A9 - 0x00 50AF	0x00 50A9 - 0x00 50AF
	RST	0x00 50B0 - 0x00 50B1	0x00 50B0 - 0x00 50B1	0x00 50B0 - 0x00 50B1	0x00 50B0 - 0x00 50B1
	PWR		0x00 50B2 - 0x00 50B3	0x00 50B2 - 0x00 50B3	0x00 50B2 - 0x00 50B3
	Reserved	0x00 50B2 - 0x00 50BF	0x00 50B4 - 0x00 50BF	0x00 50B4 - 0x00 50BF	0x00 50B4 - 0x00 50BF
	CLK	0x00 50C0 - 0x00 50C5	0x00 50C0 - 0x00 50CF	0x00 50C0 - 0x00 50CF	0x00 50C0 - 0x00 50CF
	Reserved	0x00 50C6 - 0x00 50DF	0x00 50D0 - 0x00 50D2	0x00 50D0 - 0x00 50D2	0x00 50D0 - 0x00 50D2
	WWDG		0x00 50D3 - 0x00 50D4	0x00 50D3 - 0x00 50D4	0x00 50D3 - 0x00 50D4
	Reserved	0x00 50C6 - 0x00 50DF	0x00 50D5 - 0x00 50DF	0x00 50D5 - 0x00 50DF	0x00 50D5 - 0x00 50DF
	IWDG	0x00 50E0 - 0x00 50E2	0x00 50E0 - 0x00 50E2	0x00 50E0 - 0x00 50E2	0x00 50E0 - 0x00 50E2
	Reserved	0x00 50E3 - 0x00 50EF	0x00 50E3 - 0x00 50EF	0x00 50E3 - 0x00 50EF	0x00 50E3 - 0x00 50EF

Table 6. Overview of STM8L family peripheral addresses (continued)

Bus	STM8L10x		STM8L15x/STM8L16x		
	Peripheral	**Low density STM8L10x**	**Low density STM8L15x**	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
Address data bus	BEEP/ AWU	0x00 50F0 - 0x00 50F3	0x00 50F0 - 0x00 50F3	0x00 50F0 - 0x00 50F3	0x00 50F0 - 0x00 50F3
	Reserved		0x00 50F4 - 0x00 513F	0x00 50F4 - 0x00 513F	0x00 50F4 - 0x00 513F
	RTC		0x00 5140 - 0x00 515F	0x00 5140 - 0x00 515F	0x00 5140 - 0x00 515F
	Reserved	0x00 50F4 - 0x00 51FF	0x00 5160 - 0x00 51FF	0x00 5160 - 0x00 51FF	0x00 5160 - 0x00 51FF
	SPI1	0x00 5200 - 0x00 5204	0x00 5200 - 0x00 5207	0x00 5200 - 0x00 5207	0x00 5200 - 0x00 5207
	Reserved	0x00 5205 - 0x00 520F	0x00 5208 - 0x00 520F	0x00 5208 - 0x00 520F	0x00 5208 - 0x00 520F
	I2C1	0x00 5210 - 0x00 521D	0x00 5210 - 0x00 521E	0x00 5210 - 0x00 521E	0x00 5210 - 0x00 521E
	Reserved	0x00 521E - 0x00 522F	0x00 521F - 0x00 522F	0x00 521F - 0x00 522F	0x00 521F - 0x00 522F
	USART1	0x00 5230 - 0x00 5237	0x00 5230 - 0x00 523A	0x00 5230 - 0x00 523A	0x00 5230 - 0x00 523A
	Reserved	0x00 5238 - 0x00 524F	0x00 523B - 0x00 524F	0x00 523B - 0x00 524F	0x00 523B - 0x00 524F
	TIM2	0x00 5250 - 0x00 5265	0x00 5250 - 0x00 5266	0x00 5250 - 0x00 5266	0x00 5250 - 0x00 5266
	Reserved	0x00 5266 - 0x00 527F	0x00 5267 - 0x00 527F	0x00 5267 - 0x00 527F	0x00 5267 - 0x00 527F
	TIM3	0x00 5280 - 0x00 5295	0x00 5280 - 0x00 5296	0x00 5280 - 0x00 5296	0x00 5280 - 0x00 5296
	Reserved			0x00 5297 - 0x00 52AF	0x00 5297 - 0x00 52AF
	TIM1			0x00 52B0 - 0x00 52D3	0x00 52B0 - 0x00 52D3
	Reserved	0x00 5296 - 0x00 52DF	0x00 5297 - 0x00 52DF	0x00 52D4 - 0x00 52DF	0x00 52D4 - 0x00 52DF
	TIM4	0x00 52E0 - 0x00 52E8	0x00 52E0 - 0x00 52E9	0x00 52E0 - 0x00 52E9	0x00 52E0 - 0x00 52E9
	Reserved	0x00 52EA - 0x00 52FE	0x00 52EA - 0x00 52FE	0x00 52EA - 0x00 52FE	0x00 52EA - 0x00 52FE
	IRTIM	0x00 52FF	0x00 52FF	0x00 52FF	0x00 52FF

Table 6. Overview of STM8L family peripheral addresses (continued)

Bus	STM8L10x		STM8L15x/STM8L16x		
	Peripheral	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
Address data bus	TIM5				0x00 5300 - 0x00 5316
	Reserved		0x00 5300 - 0x00 533F	0x00 5300 - 0x00 533F	0x00 5317 - 0x00 533F
	ADC1		0x00 5340 - 0x00 5351	0x00 5340 - 0x00 5351	0x00 5340 - 0x00 5351
	Reserved		0x00 5352 - 0x00 537F	0x00 5352 - 0x00 537F	0x00 5352 - 0x00 537F
	DAC		0x00 5380 - 0x00 53AD	0x00 5380 - 0x00 53AD	0x00 5380 - 0x00 53B1
	Reserved				0x00 53B2 - 0x00 53BF
	SPI2				0x00 53C0 - 0x00 53C7
	Reserved				0x00 53C8 - 0x00 53CF
	AES(1)				0x00 53D0 - 0x00 53D3
	Reserved				0x00 53D4 - 0x00 53D9
	USART2				0x00 53E0 - 0x00 53EA
	Reserved				0x00 53EB - 0x00 53EF
	USART3				0x00 53F0 - 0x00 53FA
	Reserved		0x00 53AE - 0x00 53FF	0x00 53AE - 0x00 53FF	0x00 53FB - 0x00 53FF
	LCD		0x00 5400 - 0x00 5419	0x00 5400 - 0x00 5419	0x00 5400 - 0x00 5419
	Reserved		0x00 541A - 0x00 542F	0x00 541A - 0x00 542F	0x00 541A - 0x00 542F
	RI		0x00 5430 - 0x00 543F	0x00 5430 - 0x00 543F	0x00 5430 - 0x00 543F
	COMP1/COMP2	0x00 5300 - 0x00 5302	0x00 5440 - 0x00 5444	0x00 5440 - 0x00 5444	0x00 5440 - 0x00 5444
	Reserved		0x00 5445 - 0x00 544F		
	RI		0x00 5450 - 0x00 5457		

1. Not available on high density devices.

Note: The gray cells show that the peripheral is not present.

3.2.2 GPIO

All STM8L sub-families share the same GPIO architecture with a different number of ports used in each sub-family and package. All products are pin-to-pin compatible.

The following table presents the number of ports and pins used in each superset of each sub-family. For more details on pinout and packages, please refer to the related datasheet.

Table 7. STM8L family GPIOs overview

Ports	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
Port A	PA0 - PA6	PA0 - PA7	PA0 - PA7	PA0 - PA7
Port B	PB0 - PB7	PB0 - PB7	PB0 - PB7	PB0 - PB7
Port C	PC0 - PC6	PC0 - PC7	PC0 - PC7	PC0 - PC7
Port D	PD0 - PD7	PD0 - PD7	PD0 - PD7	PD0 - PD7
Port E		PE0 - PE7	PE0 - PE7	PE0 - PE7
Port F		PF0	PF0	PF0 - PF7
Port G				PG0 - PG7
Port H				PH0 - PH7

Note: All I/Os available in the package are mapped on external interrupt vectors.

3.3 Advanced, general purpose and basic timers

All STM8L sub-families are equipped with the following timers:

- TIM2 general purpose timer (3x16-bit Cap/Com channels)
- TIM3 general purpose timers (2x16-bit Cap/Com channels)
- TIM4 basic timer: (1x8bit, no Cap/Com channel, no output)

Note: In the STM815x/STM8L16x sub-family, the basic timer is especially used to trigger the DAC.

In addition to these timers, the medium+ and high density STM8L15x/STM8L16x devices are also equipped with the following timers:

- TIM1 advanced control timer: 16-bit up/down auto-reload counter with 16-bit prescaler, wide range of modes, 4x16-bit Cap/Com channels, 3 of them have a complementary output.
- TIM5 general purpose timers (2x16-bit Cap/Com channels).

The TIM1 is available also in medium density STM8L15x/STM8L16x devices.

All these timers are identical in all products. They are based on the same architecture and are pin-to-pin compatible. On the software side, in all products, they use the same fully compatible driver. The difference lies in the DMA capability feature that is supported only on the STM8L15x/STM8L16x sub-family. The differences are shown in the following table.

The only difference between all products is the number of peripherals of the same type. In addition, if a timer is not present in a product, the related trigger is also absent.

Table 8. Features of advanced, general purpose and basic timers

Timer	Counter type	Prescaler	Cap. Comp. Channels	Complem. outputs	Repet. Counter	Ext. trigger / break inputs	Interrupt sources	DMA requests
TIM1 16-bit advanced control timer	up/down	from 1 to 65536 (Any integer)	3+1*	3	Yes	Yes	Break Trigger Commutation Capture/ Compare Update event	Commutation Capture/ Compare I Update event
TIM2/TIM3 & TIM5 16-bit general purpose timers	up/down	from 1 to 128 (Any power of 2)	2	No	No	Yes	Break Trigger Capture/ Compare Update event	Capture/ Compare I Update event
TIM4 8-bit basic timer	Up	from 1 to 32768 (Any power of 2)	0	No	No	No	Trigger Update event	Update event

The following table shows the availability of timers in all products.

Table 9. STM8L family timers overview

Timer type	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
Advanced	Not available	Not available	TIM1	TIM1
General purpose	TIM2 TIM3	TIM2 TIM3	TIM2 TIM3	TIM2 TIM3 TIM5
Basic	TIM4	TIM4	TIM4	TIM4

The following table shows the internal triggers available for timer synchronisation.

Table 10. Overview of STM8L family timer internal trigger

Timers Internal Trigger		STM8L10x	STM8L15x/STM8L16x		
		Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
TIM1	ITR0			TIM4	TIM4
	ITR1				TIM5
	ITR2			TIM3	TIM3
	ITR3			TIM2	TIM2
TIM2	ITR0	TIM4	TIM4	TIM4	TIM4
	ITR1			TIM1	TIM1
	ITR2	TIM3	TIM3	TIM3	TIM3
	ITR3				TIM5
TIM3	ITR0	TIM4	TIM4	TIM4	TIM4
	ITR1			TIM1	TIM1
	ITR2				TIM5
	ITR3	TIM2	TIM2	TIM2	TIM2

Table 10. Overview of STM8L family timer internal trigger (continued)

Timers Internal Trigger		STM8L10x	STM8L15x/STM8L16x		
		Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
TIM4	ITR0				TIM5
	ITR1			TIM1	TIM1
	ITR2	TIM3	TIM3	TIM3	TIM3
	ITR3	TIM2	TIM2	TIM2	TIM2
TIM5	ITR0				TIM4
	ITR1				TIM1
	ITR2				TIM3
	ITR3				TIM2

3.4 ADC modes

This peripheral is only available in the STM8L15x sub-family. The table below presents the pinout of the ADC in this sub-family.

Table 11. Overview of STM8L family ADC channels

Channels	ADC1 (1)			
	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
AIN0		PA6	PA6	PA6
AIN1		PA5	PA5	PA5
AIN2		PA4	PA4	PA4
AIN3		PC7	PC7	PC7
AIN4		PC4	PC4	PC4
AIN5		PC3	PC3	PC3
AIN6		PC2	PC2	PC2
AIN7		PD7	PD7	PD7
AIN8		PD6	PD6	PD6
AIN9		PD5	PD5	PD5
AIN10		PD4	PD4	PD4

Table 11. Overview of STM8L family ADC channels

Channels	ADC1 (1) (continued)			
	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
AIN11		PB7	PB7	PB7
AIN12		PB6	PB6	PB6
AIN13		PB5	PB5	PB5
AIN14		PB4	PB4	PB4
AIN15		PB3	PB3	PB3
AIN16		PB2	PB2	PB2
AIN17		PB1	PB1	PB1
AIN18		PB0	PB0	PB0
AIN19		PD3	PD3	PD3
AIN20		PD2	PD2	PD2
AIN21		PD1	PD1	PD1
AIN22		PD0	PD0	PD0
AIN23		PE5	PE5	PE5
AIN24		PF0	PF0	PF0
AIN25		PE7		PF1
AIN26		PE3		PF2
AIN27		PE4		PF3

1. No AIN channel available in the STM8L10x devices.

The table below lists all TIMx internal triggers that can be used with ADC for the STM8L15x/STM8L16x sub-family:

Table 12. TIMx internal triggers(1)

ADC1 TIMx trigger	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
TIM1			TIM1_TRGO event	TIM1_TRGO event
TIM2		TIM2_TRGO event	TIM2_TRGO event	TIM2_TRGO event
TIM3				
TIM4				
TIM5				

1. No ADC TIMx trigger available in the STM8L10x devices.

3.5 DAC peripheral

This peripheral is only available in the STM8L15x/STM8L16x sub-family.

The DAC has one output channel in the medium density STM8L15x/STM8L16x devices and two output channels in medium+ and high density STM8L15x/STM8L16x devices. The dual DAC channel mode feature is available on medium+ and high density STM8L15x/STM8L16x devices.

All TIMx internal triggers that can be used with DAC for this sub-family are given in the following table:

Table 13. Overview of STM8L family DACTIMx triggers (1)

DAC TIMx trigger	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
TIM1-TRGO				
TIM2-TRGO				
TIM3-TRGO				
TIM4-TRGO		x	x	x
TIM5-TRGO				x

1. No DAC TIMx trigger available in the STM8L10x devices.

3.6 COMP peripherals

The STM8L products feature two zero-crossing comparators COMP1 and COMP2 that share the same current bias. For the STM8L10x sub-family, the COMP1 and COMP2 share also the reference voltage.

Each comparator has two inputs: inverting and non inverting inputs. The STM8L15x/STM8L16x sub-family offers more capabilities than the STM8L10x sub-family in terms of number and configuration of these inputs.

The following table shows the availability of the COMPx inverting and non inverting inputs in both sub-families.

Table 14. Overview of comparator inputs

		STM8L10x	STM8L15x/STM8L16x		
	Comparator Input	**Low density STM8L10x**	**Low density STM8L15x**	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
COMP1	Non Inverting Input	PB0	PA6	PA6	PA6
		PB1	PA5	PA5	PA5
		PD0	PA4	PA4	PA4
		PD1	PC7	PC7	PC7
			PC4	PC4	PC4
			PC3	PC3	PC3
			PC2	PC2	PC2
			PD7	PD7	PD7
			PD6	PD6	PD6
			PD5	PD5	PD5
			PD4	PD4	PD4
			PB7	PB7	PB7
			PB6	PB6	PB6
			PB5	PB5	PB5
			PB4	PB4	PB4
			PB3	PB3	PB3
			PB2	PB2	PB2
			PB1	PB1	PB1
			PB0	PB0	PB0
			PD3	PD3	PD3
			PD2	PD2	PD2

Table 14. Overview of comparator inputs (continued)

		STM8L10x	STM8L15x/STM8L16x		
	Comparator Input	**Low density STM8L10x**	**Low density STM8L15x**	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
COMP1	Non Inverting Input		PD1	PD1	PD1
			PD0	PD0	PD0
			PE5	PE5	PE5
			PF0	PF0	PF0
			PA7		
			PE7		
			PE3		
			PE4		
					PF1
					PF2
					PF3
	Inverting Input	PA6			
		VSS	V_{REFINT}	V_{REFINT}	V_{REFINT}
COMP2	Non Inverting Input	PB2	PD1	PD1	PD1
		PB3	PD0	PD0	PD0
		PD2	PE5	PE5	PE5
		PD3	PE4		

Table 14. Overview of comparator inputs (continued)

		STM8L10x	STM8L15x/STM8L16x		
	Comparator Input	**Low density STM8L10x**	**Low density STM8L15x**	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
COMP2	Inverting Input	PA6	PC7	PC7	PC7
		VSS	PC4	PC4	PC4
			PC3	PC3	PC3
			PE7		
			DAC1 Output	DAC1 Output	DAC1 Output
					DAC2 Output
			V_{REFINT}	V_{REFINT}	V_{REFINT}
			$3/4V_{REFINT}$	$3/4V_{REFINT}$	$3/4V_{REFINT}$
			$1/2V_{REFINT}$	$1/2V_{REFINT}$	$1/2V_{REFINT}$
			$1/4V_{REFINT}$	$1/4V_{REFINT}$	$1/4V_{REFINT}$

3.7 LCD peripheral

This peripheral is available in the medium, medium+ and high density STM8L15x/STM8L16x devices.

- In medium+ and high density STM8L15x/STM8L16x devices, it can interface with 8 common terminals and up to 44 segment terminals to drive up to 320 picture elements (pixels).
- In medium density STM8L15x/STM8L16x devices, it can interface with 4 common terminals and up to 28 segment terminals to drive up to 112 picture elements (pixels).

The table below gives the pinout of the LCD in the STM8L15x/STM8L16x sub-family.

Table 15. Overview of STM8L family LCD pins

Channels	**LCD (1)**			
	STM8L10x	**STM8L15x/STM8L16x**		
	Low density STM8L10x	**Low density STM8L15x**	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
COM0			PA4	PA4
COM1			PA5	PA5
COM2			PA6	PA6
COM3			PD1	PD1

Table 15. Overview of STM8L family LCD pins (continued) (continued)

Channels	LCD (1)			
	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
COM4				PF4
COM5				PF5
COM6				PF6
COM7				PF7
SEG0			PA7	PA7
SEG1			PE0	PE0
SEG2			PE1	PE1
SEG3			PE2	PE2
SEG4			PE3	PE3
SEG5			PE4	PE4
SEG6			PE5	PE5
SEG7			PD0	PD0
SEG8			PD2	PD2
SEG9			PD3	PD3
SEG10			PB0	PB0
SEG11			PB1	PB1
SEG12			PB2	PB2
SEG13			PB3	PB3
SEG14			PB4	PB4
SEG15			PB5	PB5
SEG16			PB6	PB6
SEG17			PB7	PB7
SEG18			PD4	PD4
SEG19			PD5	PD5
SEG20			PD6	PD6
SEG21			PD7	PD7
SEG22			PC2	PC2
SEG23			PC3	PC3
SEG24			PC4	PC4
SEG25			PC7	PC7

Table 15. Overview of STM8L family LCD pins (continued) (continued)

Channels	LCD (1)			
	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
SEG26			PE6	PE6
SEG27			PE7	PE7
SEG28				PG0
SEG29				PG1
SEG30				PG2
SEG31				PG3
SEG32				PG4
SEG33				PG5
SEG34				PG6
SEG35				PG7
SEG36				PH0
SEG37				PH1
SEG38				PH2
SEG39				PH3
SEG40				PF4
SEG41				PF5
SEG42				PF6
SEG43				PF7

1. LCD COMx and SEGx not available in the STM8L10x devices.

3.8 Communication peripherals

3.8.1 SPI

This peripheral is available in all STM8L sub-families. The differences are the supported features:

- DMA capability not supported in the STM8L10x sub-family
- Hardware CRC feature for reliable communication not supported in the STM8L10x sub-family.

When migrating from the STM8L10x sub-family to the STM8L15x sub-family, you have to add the additional peripheral of the same type as first parameter in every function used from the firmware library. You also have to add the CRC polynomial parameter in the *SPI_Init()* function. A full compatibility, in terms of function parameter names, is guaranteed for all common features.

Additional peripheral instances are available in the high/medium+ density STM8L15x/STM8L16x devices (refer to *Section 4.2: SPI on page 59*).

3.8.2 I2C

This peripheral is available in all STM8L sub-families.

Note: If true open drain lines are required, make sure that the default mapping is kept for SDA & SCL functions as these functions are generally mapped to pins with true open drain capabilities (which is not the case when SDA & SCL are remapped to other pins).

The differences are in the supported features:

- DMA capability not supported in the STM8L10x sub-family
- SMBUS 2.0/ PMBus not supported in the STM8L10x sub-family.
- Dual addressing mode not supported in the STM8L10x sub-family

When migrating from the STM8L10x sub-family to the STM8L15x sub-family, you have to add the additional peripheral of the same type as first parameter in every function used from the firmware library. For the common features, a full compatibility, in terms of function parameter names, is guaranteed.

Note: I/Os with true open drain capabilities are available for I2C in all STM8L sub-families.

3.8.3 USART

This peripheral is present in the whole STM8L family. The differences lie in the supported features. The following table gives an overview of the supported features for each family.

When migrating from the STM8L10x sub-family to the STM8L15x/STMP8L16x sub-family, you have to add the additional peripheral of the same type as first parameter in every function used from the firmware library. For the common features, a full compatibility, in terms of function parameter names, is guaranteed.

Additional peripheral instances are available in the high/medium+ density STM8L15x/STM8L16x devices (refer to *Section 4.4: USART on page 60*).

Refer to the STM8L10x microcontroller family reference manual (RM0013), STM8L15x microcontroller family reference manual (RM0031), STM8L101x datasheet and STM8L15x datasheet for more detailed information.

Table 16. USART special features

USART features	STM8L10x sub-family	STM8L15x/STM8L16x sub-family
Asynchronous mode	x	x
Hardware Flow Control		
Multibuffer communication (DMA)		x
Multiprocessor communication	x	x
Synchronous	x	x
Smartcard		x
Half-duplex (single-wire mode)		x
IrDA		x

3.9 Clock controller

The clock controller in the STM8L15x sub-family is a superset of the clock controller used in the STM8L10x sub-family:

- The common features are:
  - HSI/8 is the default system clock after startup
  - CCO feature, with more options for the STM8L15x sub-family
  - HSI and LSI features (low power, low cost but not accurate)
  - Peripheral clocks are disabled after reset. The user should enable a peripheral clock before using it.
- The additional features in the STM8L15x/STM8L16x sub-family are:

1. System clock switching: the clock switching feature provides an easy to use, fast and secure way for the application to switch from one system clock source to another: HSE, HSI, LSE and LSI (with configurable divider). The only system clock available in the STM8L10x sub-family is the HSI (with configurable divider).
2. The clock security system (CSS): if the HSE clock fails due to a broken or disconnected resonator or any other reason, the clock controller activates a stall-safe recovery mechanism by automatically switching to the HSI with the same division factor as that used before the HSE clock failure.
3. More HSE and LSE oscillators (higher cost but better accuracy)
4. More clock settings for new peripherals (LCD, RTC, DAC, DMA...)
5. The Clock Security System (CSS) to monitor LSE crystal clock source failures when the LSE is used as RTC clock. This feature is implemented on low, medium+ and high density devices.

The following table gives an overview of clocks and oscillators supported in the STM8L family.

Table 17. Overview of the clocks in the STM8L family

Clocks & Osc	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
LSE		32.768 kHz OSC	32.768 kHz OSC	32.768 kHz OSC
LSI	38 kHz RC	38 kHz RC	38 kHz RC	38KHz RC
HSE		1 - 16MHz OSC	1 - 16 MHz OSC	1 - 16 MHz OSC
HSI	16 MHz RC	16MHz RC	16 MHz RC	16 MHz RC
CCO CLK	f_{master} $f_{master/2}$ $f_{master/4}$ $f_{master/16}$	HSI/Prescaler LSI/Prescaler HSE/Prescaler LES/Prescaler	HSI/Prescaler LSI/Prescaler HSE/Prescaler LES/Prescaler	HSI/Prescaler LSI/Prescaler HSE/Prescaler LES/Prescaler
RTC CLK		32.768 kHz OSC 38 kHz RC 1 - 16 MHz OSC 16 MHz RC	32.768 kHz OSC 38 kHz RC 1 - 16 MHz OSC 16 MHz RC	32.768 kHz OSC 38 kHz RC 1 - 16 MHz OSC 16 MHz RC

3.9.1 LSI clock frequency

In the whole STM8L family, the low-speed internal clock (LSI) is an ultralow internal power source (a few µA), that can be permanently enabled to be used as the clock source for the application during the Active-halt mode. It is not accurate (error of a few 10%), but it can be periodically measured using the precise HSI clock to compensate for chip manufacturing variations or for the drift due to temperature changes for instance.

3.9.2 HSI clock frequency

In the whole STM8L family, the HSI internal oscillator is factory calibrated in intervals of +/-2% of the temperature range “5 to 25°C”. This value can be trimmed by the user within an interval of +3/-4% of the range in eight steps using three trimming register bits. This enables calibration in steps of about 1% of the range.

3.10 BEEP

In the STM8L15x/STM8L16x sub-family, the BEEP clock sources can be either the LSE or LSI clocks. However this feature is not available in the STM8L10x sub-family and the BEEP operates by default using the LSI clock source.

3.11 RTC

The RTC is available only in the STM8L15x/STM8L16x sub-family, with some additional features in the low, medium+ and high density STM8L15x/STM8L16x devices. Please refer to the AN3133 application note (“Using the STM8L15x/STM8L16x real time clock”).

3.12 DMA

The STM8L15x/STM8L16x sub-family is equipped with one DMA with 4 channels. The following table presents all peripheral DMA requests present in the sub-family.

Table 18. Overview of STM8L family DMA requests

Channels		STM8L15x/STM8L16x (1)		
		Low density STM8L15x	**Medium density STM8L15x**	**Medium+/High density STM8L15x/ High density STM8L16x**
DMA1	Channel 0	ADC I2C_Rx TIM2_CC1 TIM3_U TIM4_U	ADC I2C_Rx TIM1_CC3 TIM2_CC1 TIM3_U TIM4_U	ADC I2C_Rx TIM1_CC3 TIM2_CC1 TIM3_U TIM4_U AES_IN USART2_Tx SPI2_Rx TIM5_U
	Channel 1	ADC DAC_CH2TRIG SPI1_Rx USART_Tx TIM2_U TIM3_CC1 TIM4_U	ADC DAC_CH2TRIG SPI1_Rx USART_Tx TIM1_CC4 TIM2_U TIM3_CC1 TIM4_U	ADC SPI1_Rx DAC_CH2TRIG USART_Tx TIM1_CC4 TIM2_U TIM TIM2_CC1 TIM4_U USART3_Tx

Table 18. Overview of STM8L family DMA requests

Channels		STM8L15x/STM8L16x [1] (continued)		
		Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
DMA1	Channel 2	ADC SPI1_Tx USART_Rx TIM3_CC2 TIM4_U	ADC SPI1_Tx USART_Rx TIM1_U TIM1_CC1 TIM1_COM TIM3_CC2 TIM4_U	ADC SPI1_Tx USART_Rx TIM1_U TIM1_CC1 TIM1_COM TIM3_CC2 TIM4_U TIM5_CC1 USART3_Rx
	Channel 3	ADC I2C_Tx DAC_CH1TRIG TIM2_CC2 TIM4_U	ADC I2C_Tx DAC_CH1TRIG TIM1_CC2 TIM2_CC2 TIM4_U	ADC AES_OUT I2C_Tx DAC_CH1TRIG TIM1_CC2 TIM2_CC2 TIM4_U USART2_Rx SPI2_Tx TIM5_CC2

1. No DMA channel available in STM8L10x devices.

3.13 Memory

3.13.1 Flash program memory

The Flash program memory organization differs slightly in each sub-family.

The memory is organized in pages:

- STM8L15x/STM8L16x sub-family:
  - In low density STM8L15x devices, the Flash memory is organized in up to 128 pages of 64 bytes each. Each page is equal to a block of 64 bytes.
  - In medium density STM8L15x devices, the Flash memory is organized in up to 256 pages of 128 bytes each. Each page is equal to a block of 128 bytes.
  - In medium+ density STM8L15x devices, the Flash memory is organized in up to 128 pages of 256 bytes each. Each page is equal to two blocks of 128 bytes.
  - In high density STM8L15x and high density STM8L16x devices, the Flash memory is organized in up to 256 pages of 256 bytes each. Each page is equal to two blocks of 128 bytes.

A block is the maximum amount of memory that can be programmed in a single programming cycle.

- STM8L10x sub-family
  - In low density STM8L10x devices, the Flash memory is organized in up to 128 pages of 64 bytes. A page consists of a single block of 64 bytes.

Table 19. Overview of the STM8L family Flash interface

Flash features	STM8L10x	STM8L15x/STM8L16x			
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+ density STM8L15x	High density STM8L15x/ STM8L16x
Interface	Common read/write/protection interface				
Size range	Up to 8 Kbytes	Up to 8 Kbytes	Up to 32 Kbytes	Up to 32 Kbytes	From 32 Kbytes to 64 Kbytes
Address range	0x8000 - 0x9FFF	0x1000 - 0x10FF 0x8000 - 0x9FFF	0x1000 - 0x13FF 0x8000 - 0xFFFF	0x1000 - 0x13FF 0x8000 - 0xFFFF	0x1000 - 0x17FF 0x8000 - 0x17FFF
Block size	64 bytes	64 bytes	128 bytes	128 bytes	128 bytes
Page size	64 bytes	64 bytes	128 bytes	256 bytes	256 bytes
Option bytes	Up to 64 option bytes	Up to 64 option bytes	Up to 128 option bytes	Up to 128 option bytes	Up to 128 option bytes
User Boot Code (UBC)	From 3 pages up to 127pages	From 3 pages up to 127pages	From 2 pages up to 255pages	From 2 pages up to 255pages	From 2 pages up to 510 pages
Read-while-write (RWW)	Not supported	Not supported	Supported	Supported	Supported

Table 19. Overview of the STM8L family Flash interface (continued)

Flash features	STM8L10x	STM8L15x/STM8L16x			
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+ density STM8L15x	High density STM8L15x/ STM8L16x
Low power wait mode	Not supported	Supported	Supported	Supported	Supported
Low power run mode	Not supported	Supported	Supported	Supported	Supported

3.13.2 Data EEPROM memory

The data EEPROM memory organization differs slightly in each sub-family. The data EEPROM is organized in pages:

- STM8L15x/STM8L16x sub-family:
  - In low density STM8L15x devices, the data EEPROM is organized in up to 4 pages of 64 bytes each.
  - In medium density STM8L15x devices, the data EEPROM is organized in up to 8 pages of 128 bytes each.
  - In medium+ density STM8L15x devices, the data EEPROM is organized in up to 4 pages of 256 bytes each.
  - In high density STM8L15x and high density STM8L16x devices, the data EEPROM is organized to 8 pages of 256 bytes each.
- STM8L10x sub-family
  - In low density STM8L10x devices, the data EEPROM is organized in up to 32 pages of 64 bytes.

The start address of the data EEPROM is configured through the DATASIZE option byte in the STM8L10x sub-family.

The start address of the data EEPROM is always 0x1000 in all the STM8L10x and STM8L15x/STM8L16x sub-families.

Refer to the STM8L datasheets for more details.

3.13.3 Boot ROM memory

The Boot ROM memory containing the bootloader code is present in the devices for the STM8L15x/STM8L16x sub-family. It is not present in the STM8L10x sub-family. The Boot ROM size is 2 Kbytes and its start address is always 0x6000.

3.13.4 RAM memory

The RAM memory always starts from address 0. The first 256 bytes make up the zero page.

3.13.5 Stack

The space for the stack is always located at the end of the RAM memory. So its position in the address space varies depending on the RAM memory size. The stack pointer value is initialized to the upper address at reset and it is decremented each time a byte is pushed onto the stack. The stack size is 513 bytes in all STM8L devices.

3.14 Interrupt mapping

The interrupt vector mapping is compatible for STM8L10x and STM8L15x/STM8L16x sub-families except:

- The new added vectors to support the new peripherals in the STM8L15x/STM8L16x devices
- The TIM1, TIM5, SPI1, SPI2, DAC, SPI2, USART2, USART3 and AES interrupts which are not supported in the STM8L10x sub-family.
- The timer 4 trigger interrupt which is not supported in the STM8L10x sub-family.
- The auto-wakeup interrupt in the STM8L10x sub-family that is replaced by the RTC interrupt in the STM8L15x/STM8L16x sub-family.

The following table lists these differences between all sub-families.

Table 20. STM8L interrupt vector differences

N	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
2		DMA1_CHANNEL0_1	DMA1_CHANNEL0_1	DMA1_CHANNEL0_1
3		DMA1_CHANNEL2_3	DMA1_CHANNEL2_3	DMA1_CHANNEL2_3
4	AWU interrupt	RTC	RTC	RTC
5		External interrupt port E? PVD interrupt	EXTI port E/F PVD	EXTI port E/F PVD
6			External interrupt port G	External interrupt port G
7			External interrupt port H	External interrupt port H
. . .	. . .	. . .	. . .	. . .
16			LCD	LCD
17		System clock switch/? CSS interrupt	System clock switch/CSS interrupt/TIM1 break/DAC	System clock switch/CSS interrupt/TIM1 break/DAC
18		ADC1	ADC1	ADC1
19				USART2 Tx interrupt
20				USART2 Rx interrupt
21				USART3 Tx interrupt

Table 20. STM8L interrupt vector differences (continued)

N	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
22				USART3 Tx interrupt
23			TIM1 Update /overflow/trigger/COM	TIM1 Update /overflow/trigger/COM
24			TIM1 Capture/Compare	TIM1 Capture/Compare
25	TIM4 update/trigger interrupt	TIM4 update/overflow/ trigger interrupt	TIM4 update/overflow/	TIM4 update/overflow/
26				
27				TIM5 update/overflow/ trigger/break
28			TIM5 capture/compare	TIM5 capture/compare
29				SPI2 interrupt

Except for the differences listed above, all other interrupt vectors are identical for all products as shown in the following table.

Table 21. Overview of the STM8L family interrupt vectors

N	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
	RESET	**RESET**	**RESET**	**RESET**
	TRAP	**TRAP**	**TRAP**	**TRAP**
0		**External Top level Interrupt**	**External Top level Interrupt**	**External Top level Interrupt**
1	**Flash**	**Flash**	**Flash**	**F**lash
2		**DMA1 channels 0/1**	**DMA1 channels 0/1**	**DMA1 channels 0/1**
3		**DMA1 channels 2/3**	**DMA1 channels 2/3**	**DMA1 channels 2/3**
4	**AWU**	**RTC alarm interrupt**	**RTC alarm interrupt/LSE CSS interrupt**	**RTC alarm interrupt/LSE CSS interrupt**
5		External interrupt port E PVD interrupt	External interrupt port E/F PVD	External interrupt port E/F PVD
6	External interrupt port B	External interrupt port B	External interrupt port B/G	External interrupt port B/G
7	External interrupt port D	External interrupt port D	External interrupt port D/H	External interrupt port D/H
8	External interrupt pin 0	External interrupt pin 0	External interrupt pin 0	External interrupt pin 0

Table 21. Overview of the STM8L family interrupt vectors (continued)

N	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
9	External interrupt pin 1	External interrupt pin 1	External interrupt pin 1	External interrupt pin 1
10	External interrupt pin 2	External interrupt pin 2	External interrupt pin 2	External interrupt pin 2
11	External interrupt pin 3	External interrupt pin 3	External interrupt pin 3	External interrupt pin 3
12	External interrupt pin 4	External interrupt pin 4	External interrupt pin 4	External interrupt pin 4
13	External interrupt pin 5	External interrupt pin 5	External interrupt pin 5	External interrupt pin 5
14	External interrupt pin 6	External interrupt pin 6	External interrupt pin 6	External interrupt pin 6
15	External interrupt pin 7	External interrupt pin 7	External interrupt pin 7	External interrupt pin 7
16			LCD interrupt	LCD interrupt/AES interrupt
17		System clock switch/? CSS interrupt	System clock switch/CSS interrupt/TIM1 break/DAC	System clock switch/CSS interrupt/TIM1 break/DAC
18	Comparator 1 and 2 interrupt	Comparator 1 and 2 interrupt ADC1	Comparator 1 and 2 interrupt ADC1	Comparator 1 and 2 interrupt ADC1
19	TIM2 update/overflow/ trigger/break interrupt	TIM2 update/overflow/ trigger/break interrupt	TIM2 update/overflow/trigger/break interrupt	TIM2 update /overflow/trigger/break/ USART2 Tx interrupt
20	TIM2 capture/?compare interrupt	TIM2 capture/?compare interrupt	TIM2 Capture/Compare USART2 interrupt	TIM2 Capture/Compare USART2 Rx interrupt
21	TIM3 update/overflow/trigger/ break interrupt	TIM3 update/overflow/trigger/break interrupt	TIM3 Update/Overflow/Trigger/ Break interrupt	TIM3 Update/Overflow/Trigger/Break/ USART3 Tx interrupt
22	TIM3 capture/? compare interrupt	TIM3 capture/? compare interrupt	TIM3 Capture/Compare interrupt	TIM3 Capture/Compare interrupt USART3 Rx interrupt
23			TIM1 Update /overflow/trigger/COM	TIM1 Update /overflow/trigger/COM
24			TIM1 Capture/Compare	TIM1 Capture/Compare
25	TIM4 update/ trigger interrupt	TIM4 update/overflow/ trigger interrupt	TIM4 Update/overflow/trigger	TIM4 Update/overflow/trigger
26	SPI interrupt	SPI1 interrupt	SPI1 interrupt	SPI1 interrupt
27	USART1 Tx interrupt	USART1 Tx interrupt	USART1 Tx interrupt	USART1 Tx interrupt TIM5 update/overflow/ trigger/break

Table 21. Overview of the STM8L family interrupt vectors (continued)

N	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/High density STM8L15x/ High density STM8L16x
28	USART1 Rx interrupt	USART1 Rx interrupt	USART1 Rx interrupt TIM5 capture/compare	USART1 Rx interrupt TIM5 capture/compare
29	I2C1 interrupt	I2C1 interrupt	I2C1 interrupt	I2C1 interrupt/ SPI2 interrupt

3.15 Option bytes

The basic structure of the option byte area is compatible across the family. There are some differences detailed in the following table:

1. OPT4 and OPT5 (number of stabilization clock cycles for HSE and LSE oscillators and brownout reset respectively) are available only in the STM8L15x/STM8L16x sub-family and can be modified on the fly by the application in IAP mode.
2. The OPTBL option byte is available only for the STM8L15x/STM8L16x sub-family.
3. The independent watchdog option is the OPT4 in the STM8L10x and OPT3 in the STM8L15x/STM8L16x sub-family.
4. The user boot code size is the OPT2 in the STM8L10x and OPT1 in the STM8L15x/STM8L16x sub-family.
5. The DATASIZE option byte is available only for the STM8L10x sub-family.

Table 22. Option byte addresses

Address	Option Byte name	STM8L10x	STM8L15x/STM8L16x		
		Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/ High density STM8L15x/ High density STM8L16x
0x4800	ROP (Read-out protection)	OPT1	OPT0	OPT0	OPT0
0x4801					
0x4802	UBC (User boot code size	OPT2	OPT1	OPT1	OPT1
0x4803	DATASIZE	OPT3			
0x4804					
0x4805					
0x4806					
0x4807					

Table 22. Option byte addresses

Address	Option Byte name	STM8L10x	STM8L15x/STM8L16x		
		Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/ High density STM8L15x/ High density STM8L16x
0x4808	Independent Watchdog option byte	OPT4	OPT3	OPT3	OPT3
0x4809	Number of stabilization clock cycles for HSE and LES oscillators		OPT4	OPT4	OPT4
0x480A	BOR (Brownout Reset		OPT5	OPT5	OPT5
0x480B - 0x480C	Bootloader		OPTBL	OPTBL	OPTBL

4 Peripheral pinout through all STM8L sub-families

4.1 Timer pinout

The following table describes the timer pinout for both STM8L sub-families.

Table 23. Timer pinout

TIM pinout				Channels							
				CH1	CH1N	CH2	CH2N	CH3	CH3N	ETR	BKIN
TIM1 pinout	STM8L10x	Low density STM8L10x	Reset								
			Remap								
	STM8L15x/ STM8L16x	Low density STM8L15x	Reset								
			Remap								
		Medium density STM8L15x	Reset	PD2	PD7	PD4	PE1	PD5	PE2	PD3	PD6
			Remap								
		Medium+/high density STM8L15x/ high density STM8L16x	Reset	PD2	PD7	PD4	PE1	PD5	PE2	PD3	PD6
			Remap								
TIM2 pinout	STM8L10x	Low density STM8L10x	Reset	PB0		PB2				PB3	PA4
			Remap								
	STM8L15x/ STM8L16x	Low density STM8L15x	Reset	PB0		PB2				PB3	PA4
			Remap							PA4	
		Medium density STM8L15x	Reset	PB0		PB2				PB3	PA4
			Remap							PA4	
		Medium+/high density STM8L15x/ high density STM8L16x	Reset	PB0		PB2				PB3	PA4
			Remap							PA4	PG0
TIM3 pinout	STM8L10x	Low density STM8L10x	Reset	PB1		PD0				PD1	PA5
			Remap								
	STM8L15x/ STM8L16x	Low density STM8L15x	Reset	PB1		PD0				PD1	PA5
			Remap							PA5	
		Medium density STM8L15x	Reset	PB1		PD0				PD1	PA5
			Remap							PA5	
		Medium+/high density STM8L15x/ high density STM8L16x	Reset	PB1		PD0				PD1	PA5
			Remap	PI0		PI3				PA5 PG3	PG1

Table 23. Timer pinout

TIM pinout				Channels							
				CH1	CH1N	CH2	CH2N	CH3	CH3N	ETR	BKIN
TIM5 pinout	STM8L10x	Low density STM8L10x	Reset								
			Remap								
	STM8L15x/ STM8L16x	Low density STM8L15x	Reset								
			Remap								
		Medium density STM8L15x	Reset								
			Remap								
		Medium+/high density STM8L15x/ high density STM8L16x	Reset	PH6		PH7				PE7	PE6
			Remap								

4.2 SPI

The following table describes the SPI pinout for both STM8L families.

Table 24. SPI pinout

		STM8L10x		STM8L15x/STM8L16x					
	Channels	Low density STM8L10x		Low density STM8L15x		Medium density STM8L15x		Medium+/ High density STM8L15x/ High density STM8L16x	
		Reset	Remap	Reset	Remap	Reset	Remap	Reset	Remap
SPI1 pinout	NSS	PB4		PB4	PC5	PB4	PC5	PB4	PC5 PF0
	SCK	PB5		PB5	PC6	PB5	PC6	PB5	PC6 PF1
	MOSI	PB6		PB6	PA3	PB6	PA3	PB6	PA3 PF2
	MISO	PB7		PB7	PA2	PB7	PA2	PB7	PA2 PF3
SPI2 pinout	NSS							PG4	PI0
	SCK							PG5	PI1
	MOSI							PG6	PI2
	MISO							PG7	PI3

4.3 I2C

The following table describes the I2C pinout for both STM8L sub-families.

Table 25. I2C pinout

Channels	I2C1							
	STM8L10x		STM8L15x/STM8L16x					
	Low density STM8L10x		Low density STM8L15x		Medium density STM8L15x		Medium+/high density STM8L15x/ high density STM8L16x	
	Reset	Remap	Reset	Remap	Reset	Remap	Reset	Remap
SCL	PC1		PC1		PC1		PC1	
SDA	PC0		PC0		PC0		PC0	
SMBAL			PC4		PC4		PC4	

4.4 USART

The following table describes the USART pinout for both STM8L sub-families.

Table 26. USART pinout

USART pinout	Channels	STM8L10x		STM8L15x/STM8L16x					
		Low density STM8L10x		Low density STM8L15x		Medium density STM8L15x		Medium+/high density STM8L15x/ high density STM8L16x	
		Default	Remap	Default	Remap	Default	Remap	Default	Remap
USART1 pinout	TX	PC3				PC3	PA2 PC5	PC3	PA2 PC5
	RX	PC2				PC2	PA3 PC6	PC2	PA3 PC6
	CK	PC4				PC4	PA0	PC4	PA0
USART2 pinout	TX							PH5	
	RX							PH4	
	CK							PH6	

Table 26. USART pinout

USART pinout	Channels	STM8L10x		STM8L15x/STM8L16x					
		Low density STM8L10x		Low density STM8L15x		Medium density STM8L15x		Medium+/high density STM8L15x/ high density STM8L16x	
		Default	Remap	Default	Remap	Default	Remap	Default	Remap
USART3 pinout	TX							PG1	PF0
	RX							PG0	PF1
	CK							PG3	PF2

4.5 DAC

The following table describes the DAC pinout for the STM8L15x/STM8L16x sub-family.

Table 27. DAC pinout

Channels	STM8L10x	STM8L15x/STM8L16x		
	Low density STM8L10x	Low density STM8L15x	Medium density STM8L15x	Medium+/ High density STM8L15x/ High density STM8L16x
DAC_OUT1		PF0	PF0	PF0
DAC_OUT2				PF1

5 Revision history

Table 28. Document revision history

Date	Revision	Changes
07-Jun-2010	1	Initial release
05-Aug-2011	2	Document modified to add new STM8L15x devices.
08-Sep-2011	3	Updated document classification.

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