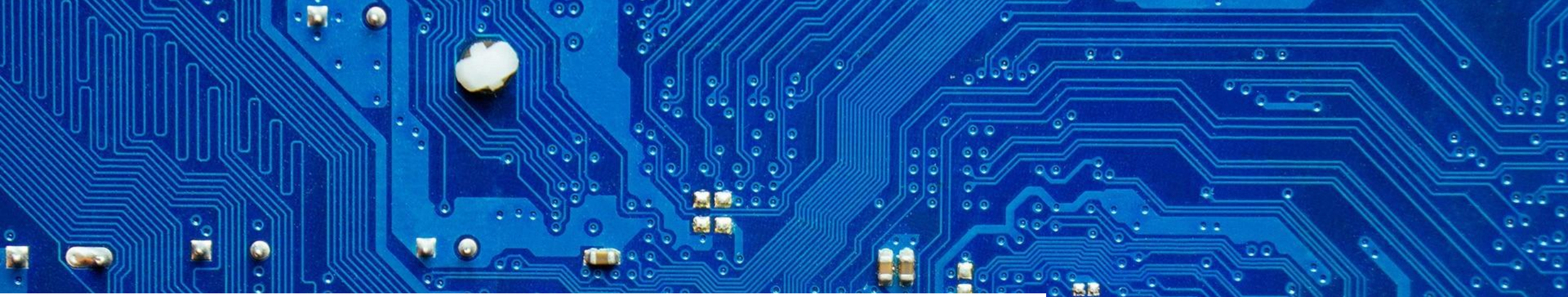


Gate Driver Design – 15kW Three-phase, Three-level AFE Bi-directional Power Converter

Arrow Asia Pac Ltd

18 Oct 2024, Version 1.1

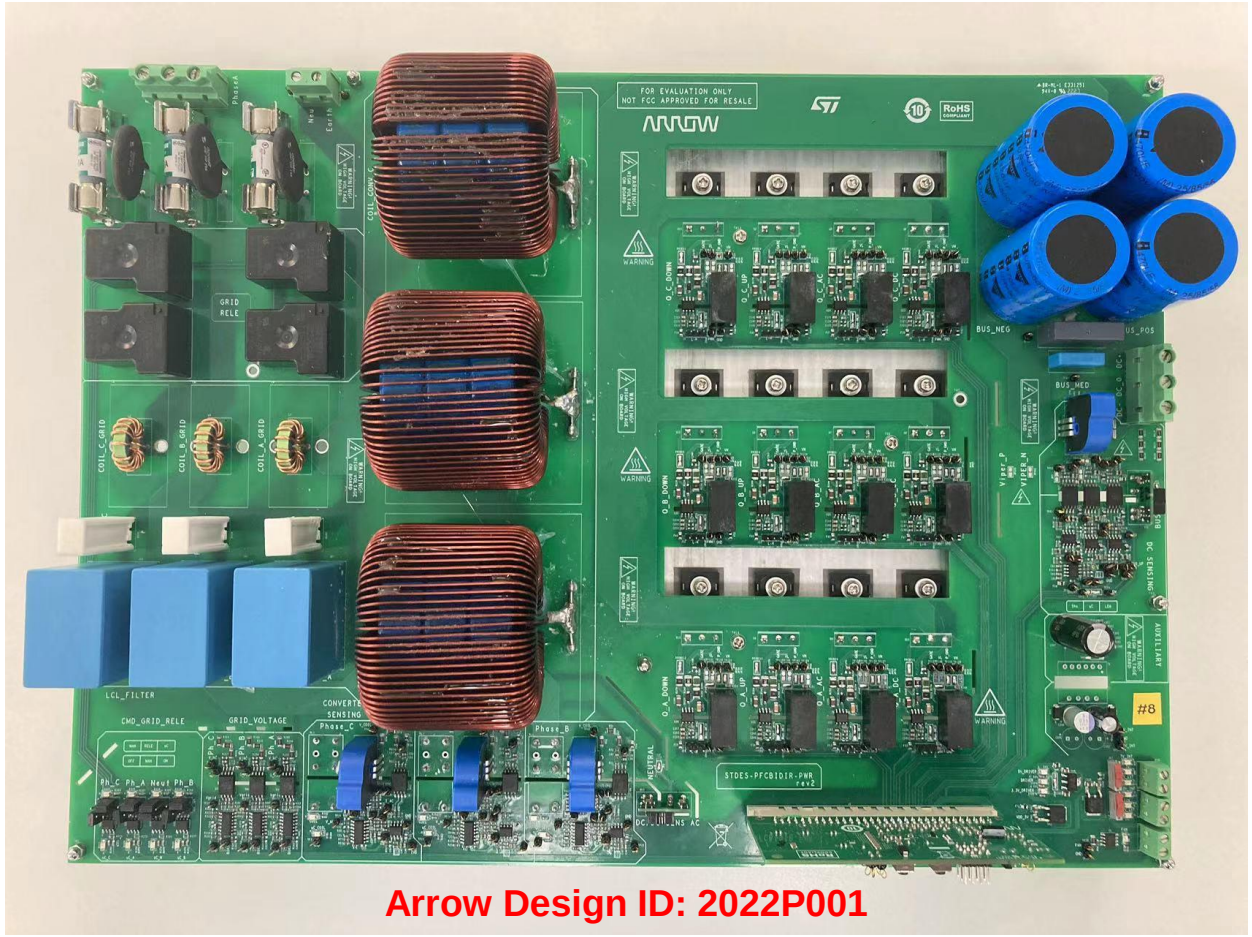
Sam Wong

ARROW

Contents

Introduction

15kW, 3 Phase, 3 Level Bidirectional Power Converter



Arrow Design ID: 2022P001

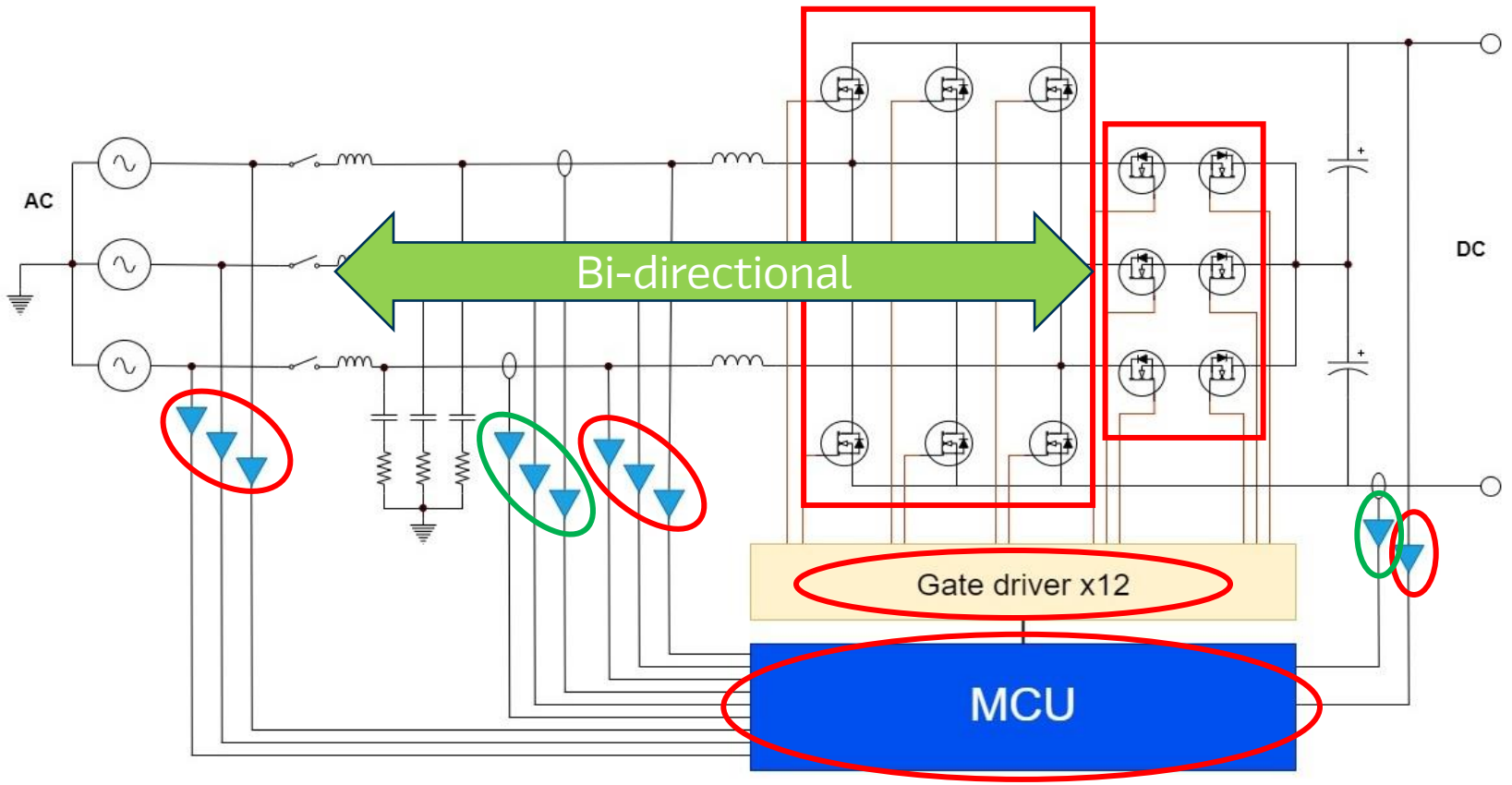
COMPLETED

Features

- AC/DC Bidirectional conversion
- Switching frequency: 70kHz
- Rated nominal AC voltage: $400VAC_{L-L}$
- Line Frequency: 50Hz
- Rated nominal DC voltage: 800VDC
- Nominal Power(Rectifier mode): 15kW max.
- Nominal Power(Inverter mode): 11kW max.
- Power Factor: >0.99
- Efficiency: >98%
- THD: <5%

Introduction

Block Diagram – Three-Level T-Type, Three-Phase Bidirectional Conversion



Core Chip

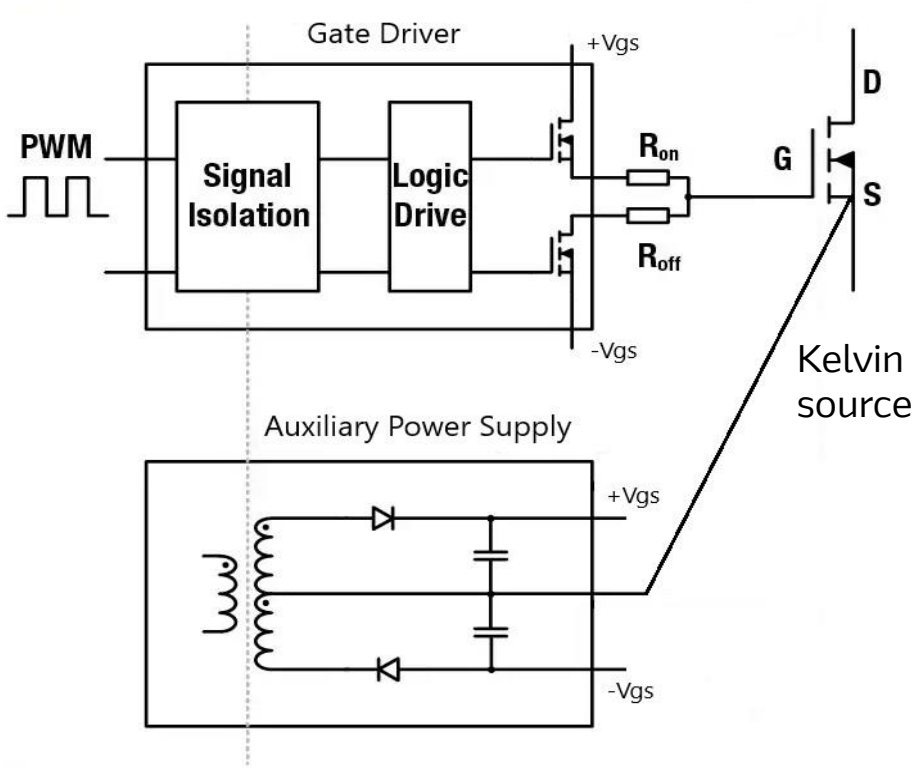
- MCU controller: STM32G474RET3
- Gate driver: STGAP2SiCSNCTR
- SiC MOS: SCTW40N120G2V / SCT070W120G3-4AG
- SiC MOS: SCTW35N65G2V/ SCT055W65G3-4AG
- Voltage sense
- Current sense

Gate Driver for SiC MOSFET

Criteria

The use of Silicon Carbide (SiC) MOSFETs benefit in higher switching frequency, higher operation voltage, better thermal conductivity and higher operation temperature, etc. But the driving methods are different from IGBT or Si MOSFET. Following are some criteria will be considered during the design process.

- Isolated or non-isolated circuit
- Negative gate voltage for turn-off
- Active Miller clamp
- Common-mode transient immunity (CMTI)
- Driving capability, Propagation delay time, etc.

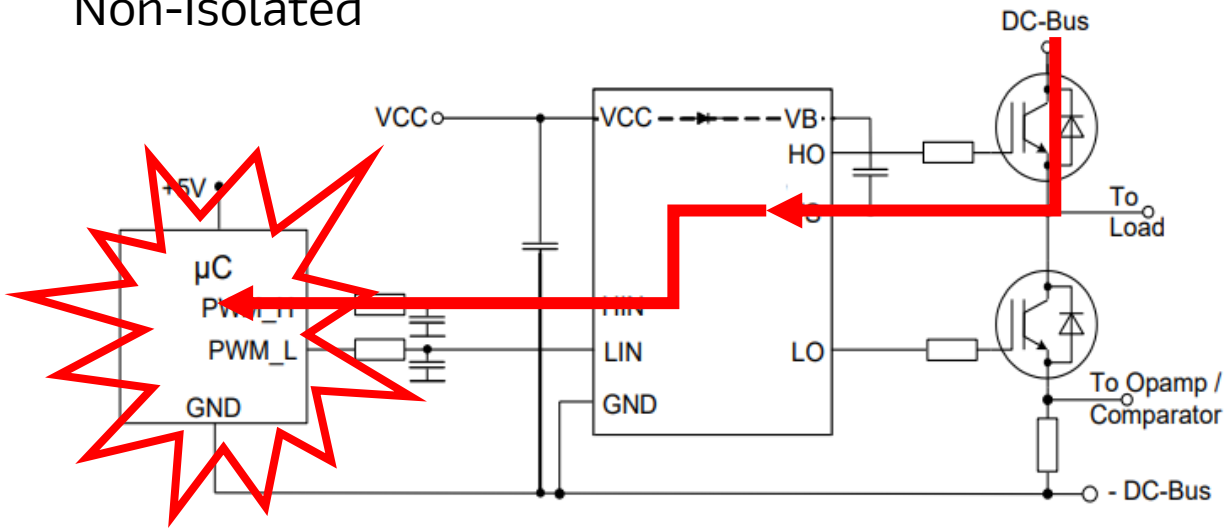


Gate Driver for SiC MOSFET

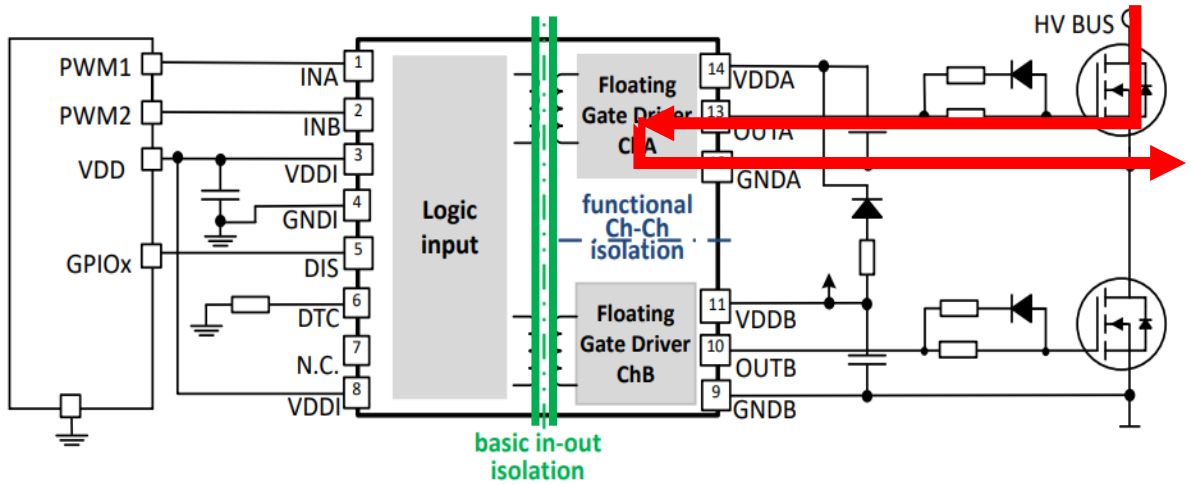
Isolated or non-isolated

- Safety reasons
- Protect human operator and MCU controller

Non-Isolated



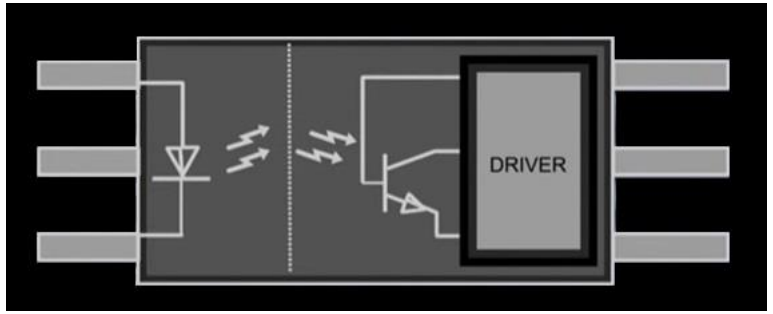
Isolated

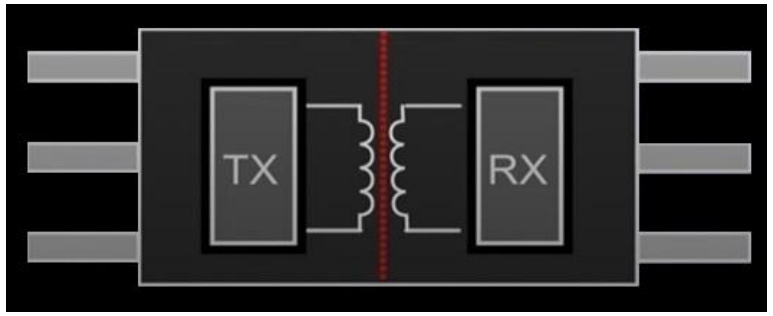


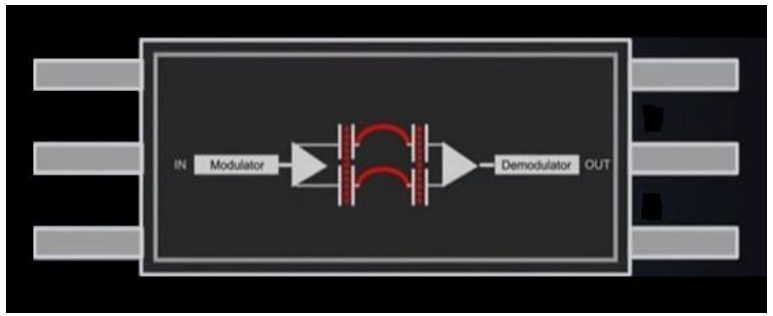
Gate Driver for SiC MOSFET

Type of Isolated gate driver

- Optical isolation
  - ➢ Mature, cost effective, larger size for high isolated voltage, performance decay over time
- Inductive isolation
  - ➢ Higher isolation voltage, less propagation delay, high switching frequency, higher cost
- Capacitive isolation
  - ➢ Latest technology, high reliability, minimal delays, small package



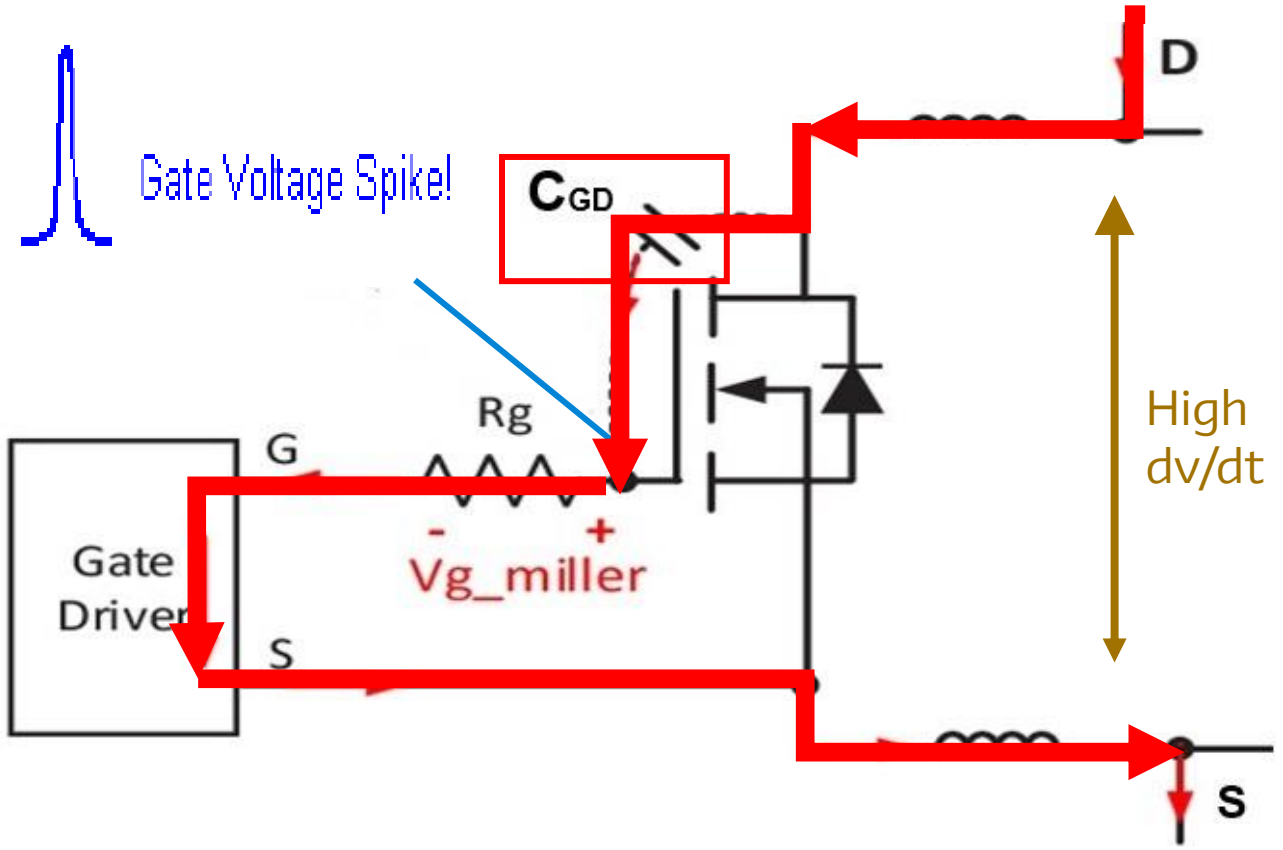




Gate Driver for SiC MOSFET

Negative gate voltage for turn-off

- Miller capacitance C_{GD}
- High dv/dt
- $i = C\frac{dv}{dt}$
- Gate voltage spike occur

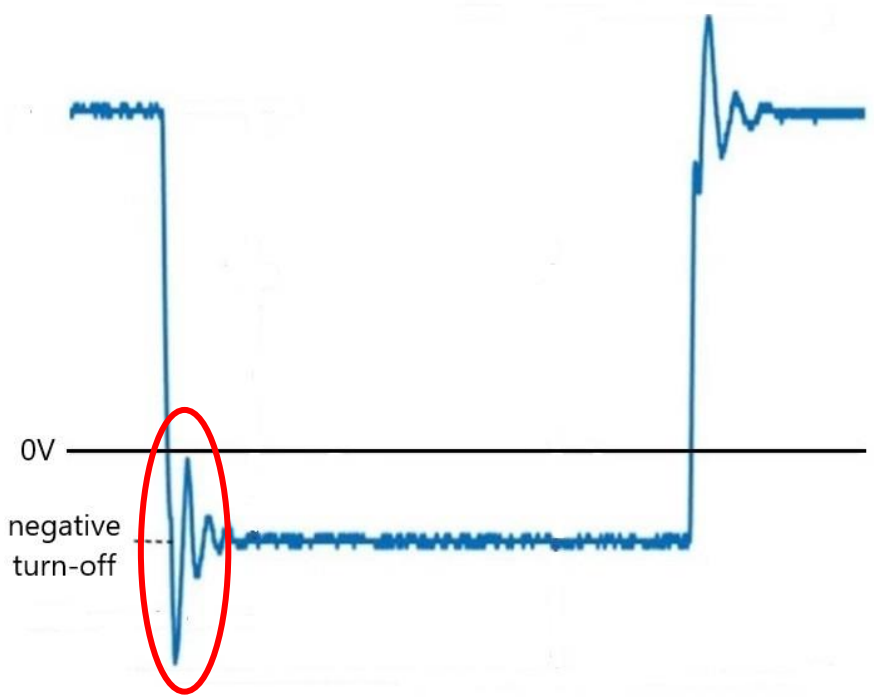


Gate Driver for SiC MOSFET

Negative gate voltage for turn-off (CONT.)

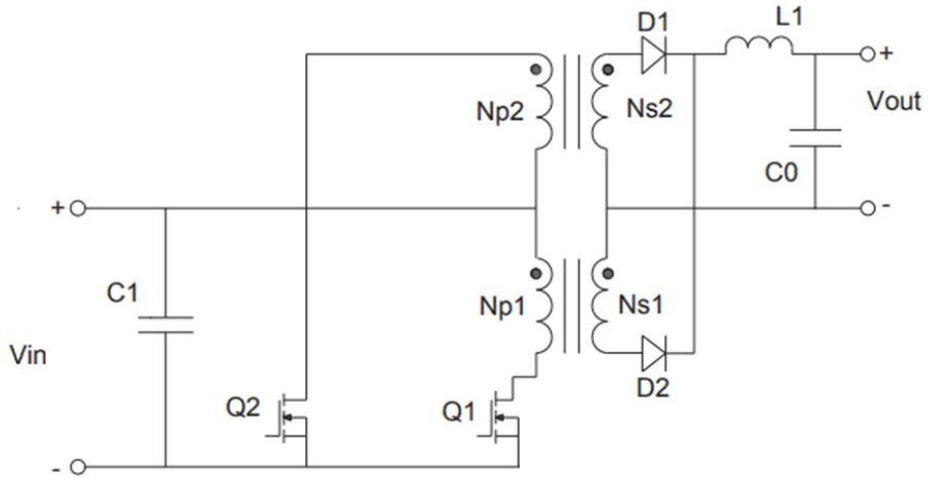
- Miller capacitance C_{GD}
- High dv/dt
- $i = C\frac{dv}{dt}$
- Gate voltage spike occur
- $V_{g\_miller} > V_{g\_th}$ → MOSFET turn-on
- Negative turn-off voltage provide a negative offset

V_{GS}	Gate-source voltage			-10 to 22		V
	Gate-source voltage (recommended operational values)			-5 to 18		
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, I_D = 1 mA	1.9	3.0	5.0	V

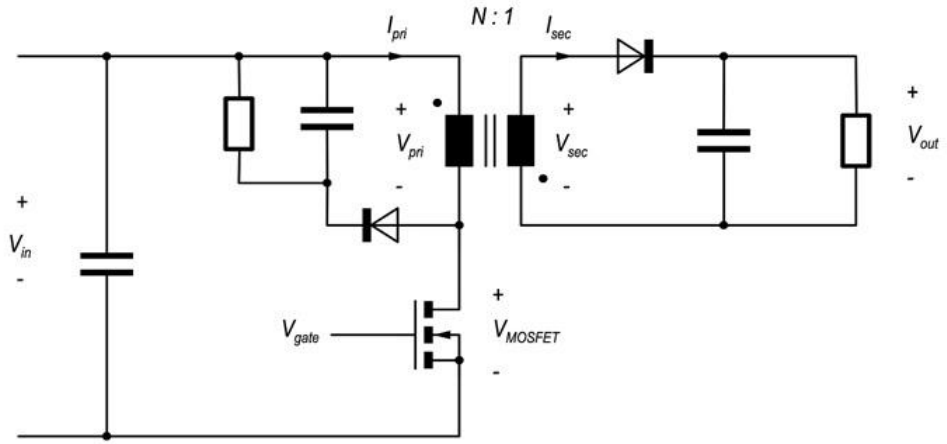


Gate Driver for SiC MOSFET

Isolated Power Source for Gate Driver



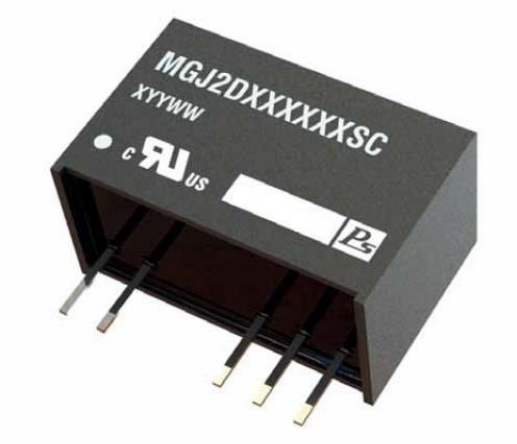
- Push-pull converter
- Non-regulated output
- Cost effective
- Small size
- Less efficiency

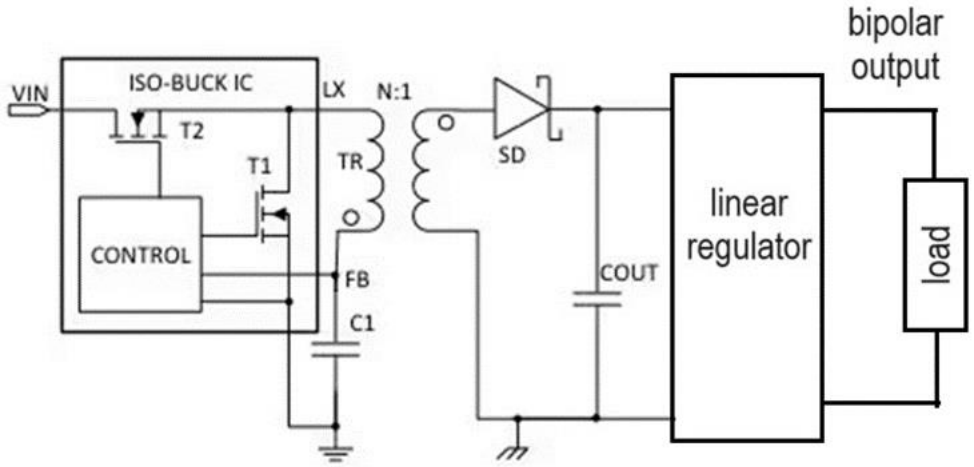


- Flyback converter
- Regulated output
- Medium cost
- A little bit complex
- Good efficiency

Gate Driver for SiC MOSFET

Isolated Power Source for Gate Driver





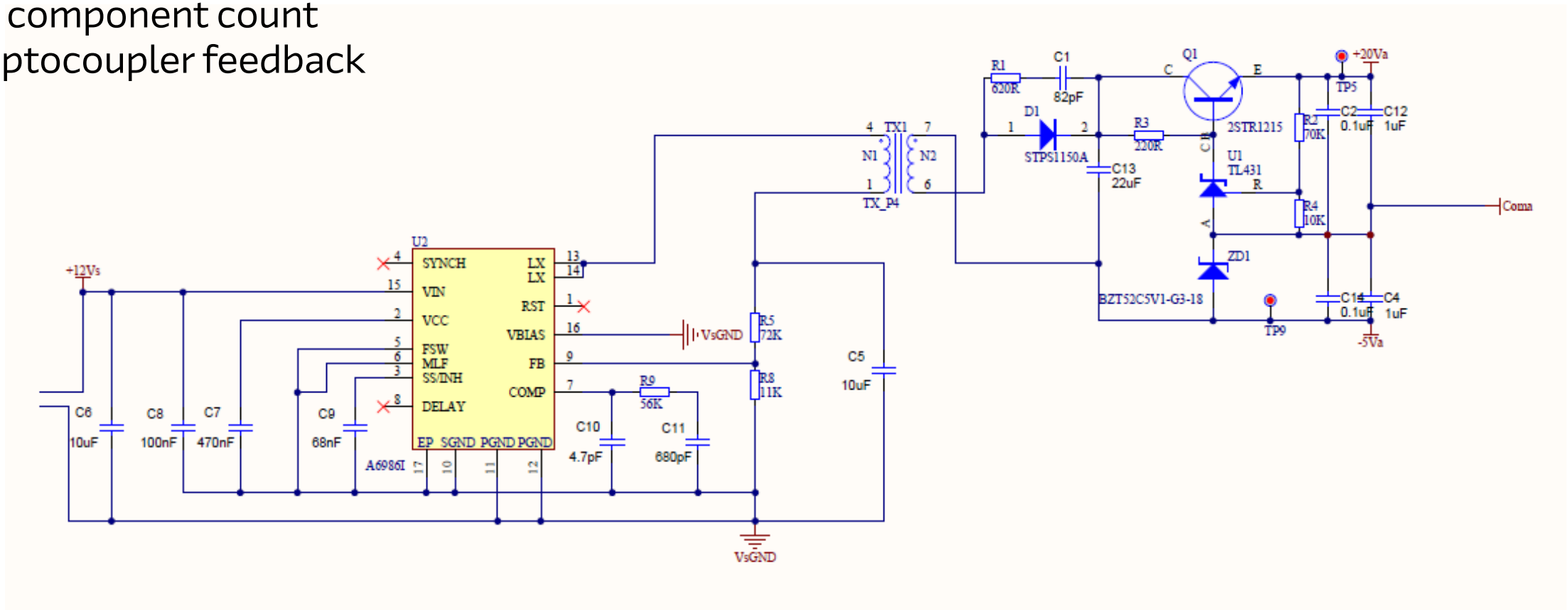
- DCDC module
- Non-regulated or regulated output
- High cost
- Fix footprint, easy to use
- Medium efficiency

- Iso-buck converter
- Regulated output
- Medium cost
- Flexibility design
- Good efficiency

Gate Driver for SiC MOSFET

Iso-buck converter

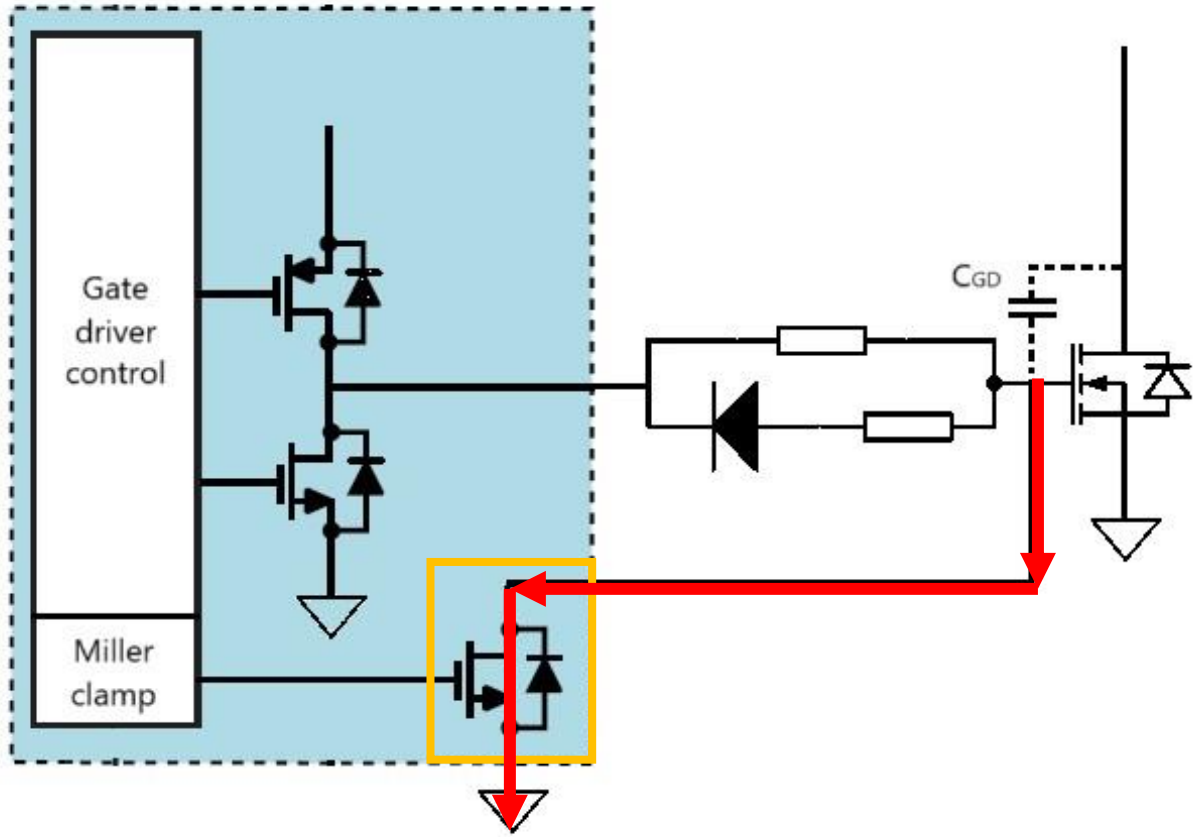
- **ST L6986I**
- Adjustable bipolar driving voltage
- Less component count
- No optocoupler feedback



Gate Driver for SiC MOSFET

Active Miller Clamp

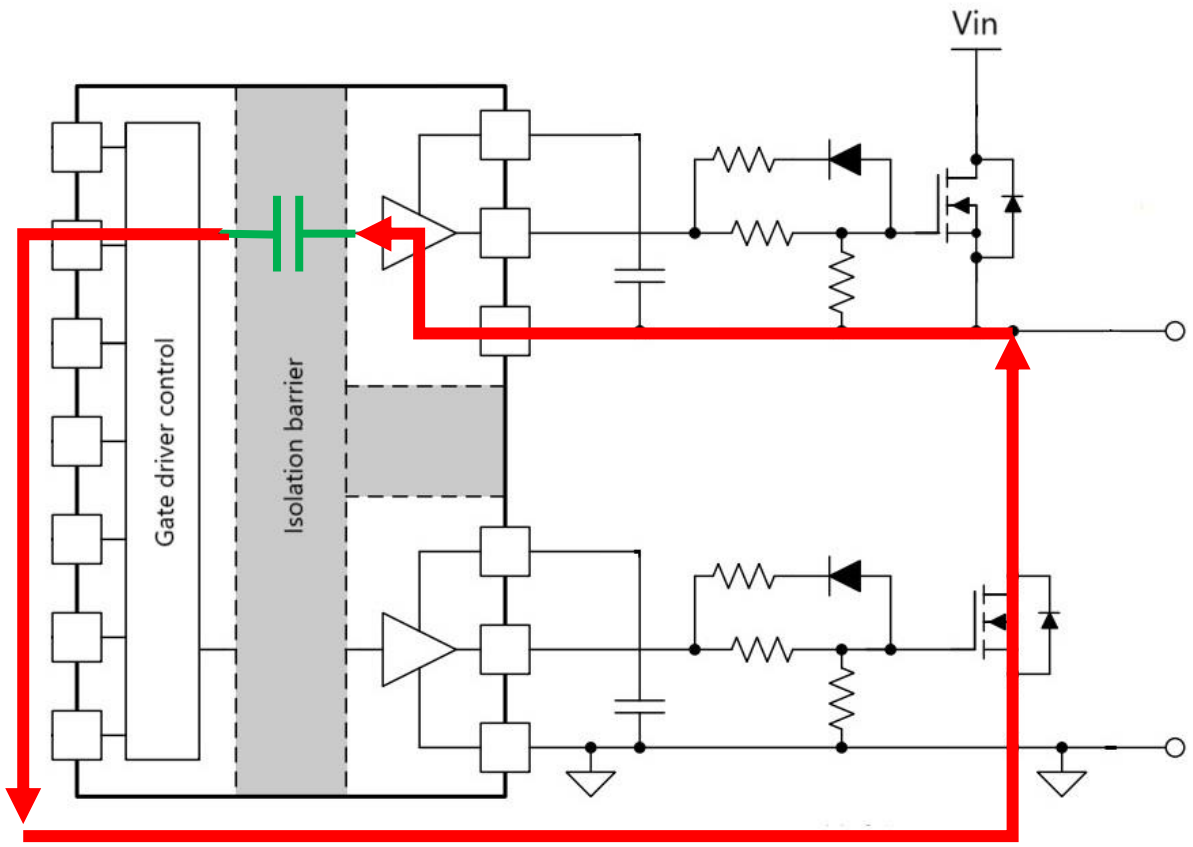
- The Clamp transistor of gate driver IC connect directly to SiC gate
- Activate the Clamp transistor when gate voltage below threshold
- Provide a low impendence path for Miller current
- Reducing gate ringing and undershoot



Gate Driver for SiC MOSFET

Common Mode Transient Immunity (CMTI)

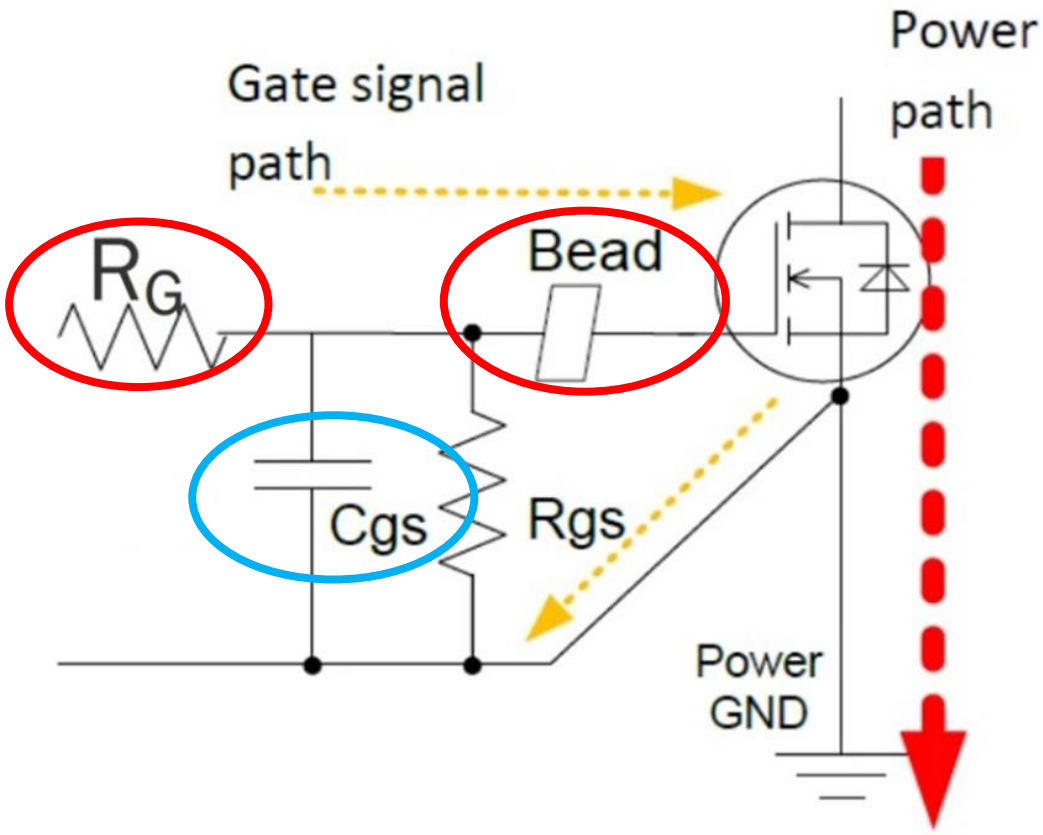
- High dv/dt induce high common mode noise → Couple to primary side by parasitic capacitor across the isolation barrier
- CMTI – The maximum tolerable rate of common mode voltage applied between isolated circuits (rise or fall). Unit is kV/us or V/ns
- High CMTI – No error occur when striking the insulation barrier with very high slew rate



Gate Driver Optimization

Use of Components

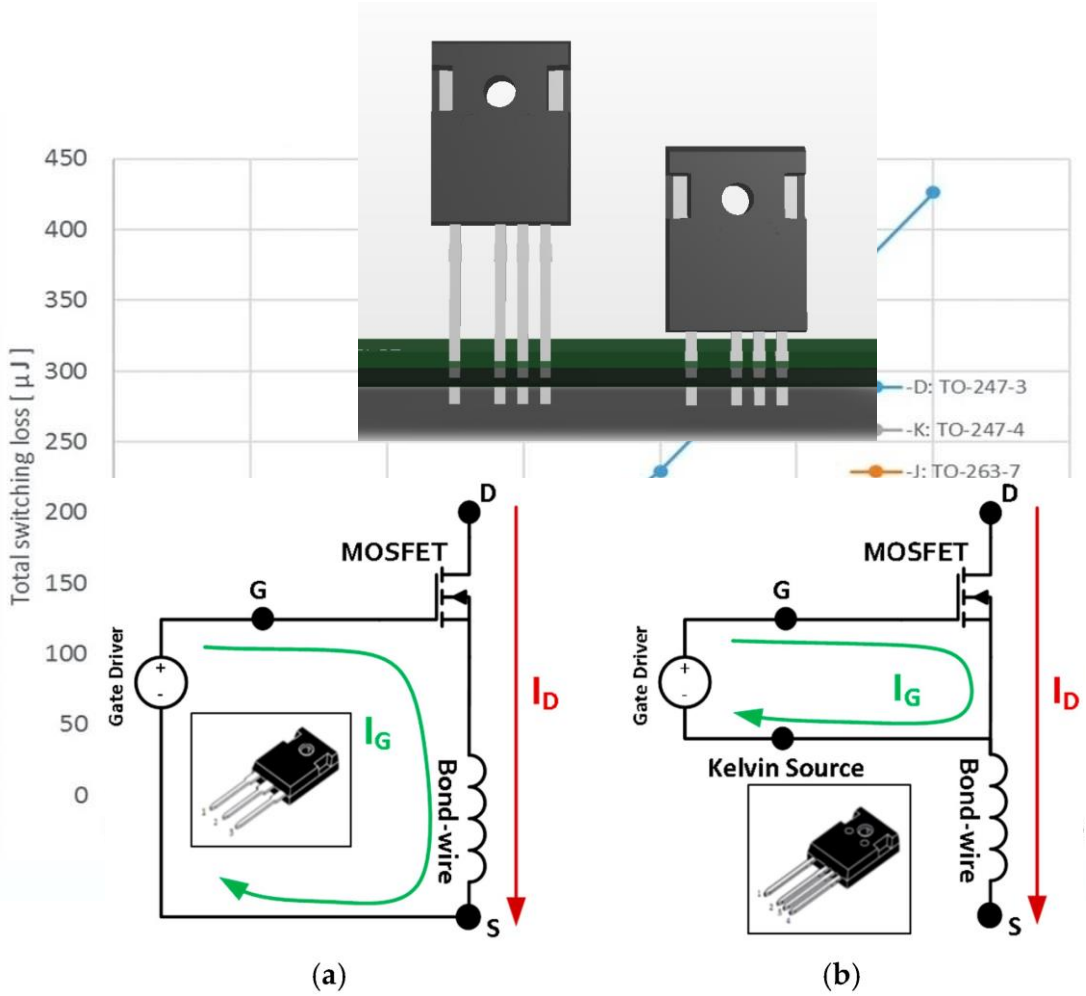
- Adding damping effects, such as gate resistor and ferrite bead
- Placed a decoupling capacitor between the gate and source of the MOSFET



Gate Driver Optimization

Use of Components (CONT.)

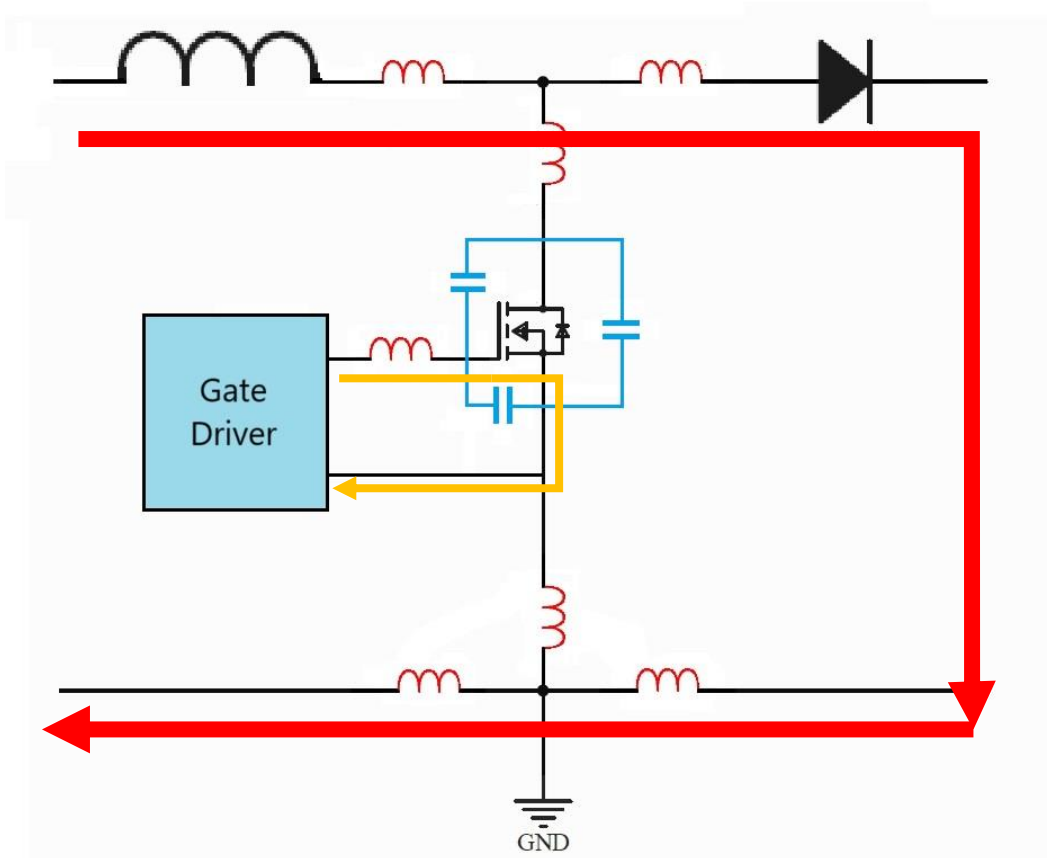
- Adding damping effects, such as gate resistor and ferrite bead
- Placed a decoupling capacitor between the gate and source of the MOSFET
- Keep the shortest leads when using through-hole components → Minimize parasitic inductance
- Use a SiC MOSFET with Kelvin source → Minimize parasitic inductance



Gate Driver Optimization

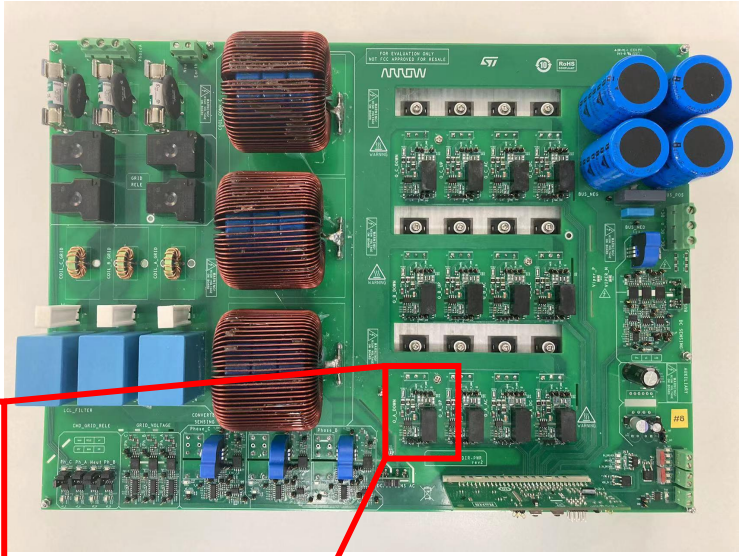
PCB layout

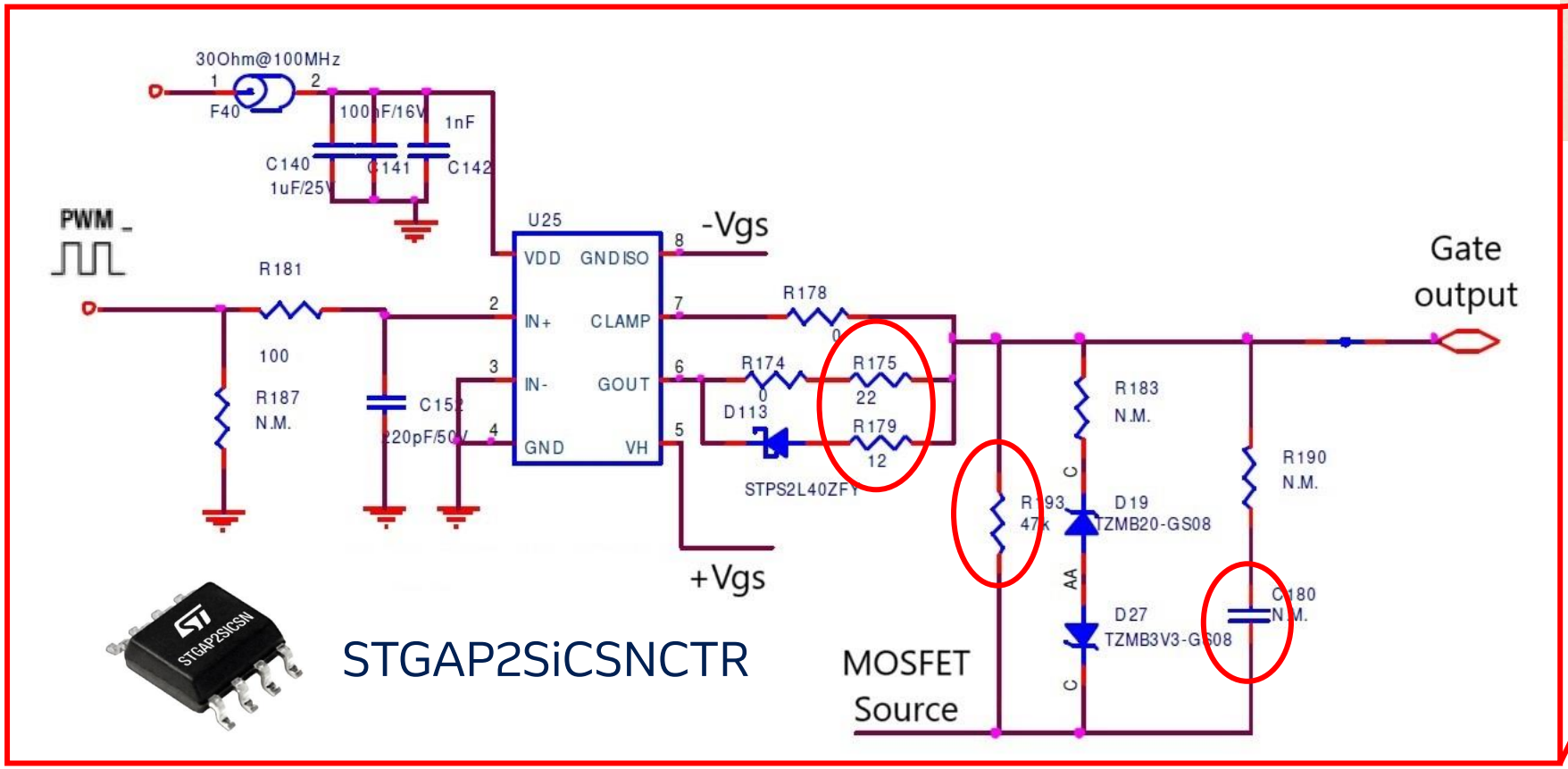
- Minimize distance from gate driver to MOSFET
- Minimize the gate loop area
- Use short wide traces
- Use large overlapping pours for the DC bus
- Minimize overlap of switching nodes to the bus and other signals
- Keep sensitive signals away from high-frequency magnetics
- Keep power loop and gate driver signals separated
- Use symmetrical gate connection for parallel MOSFET



Design Example

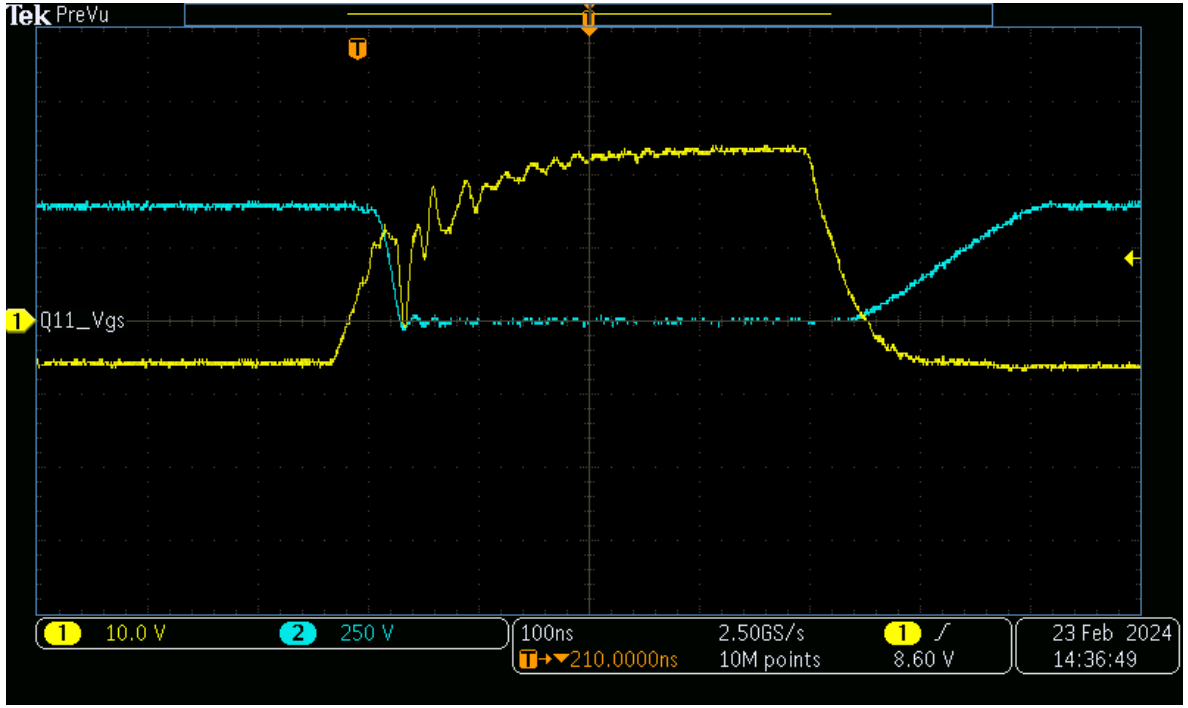
15kW, 3 Phase, 3 Level Bidirectional Power Converter



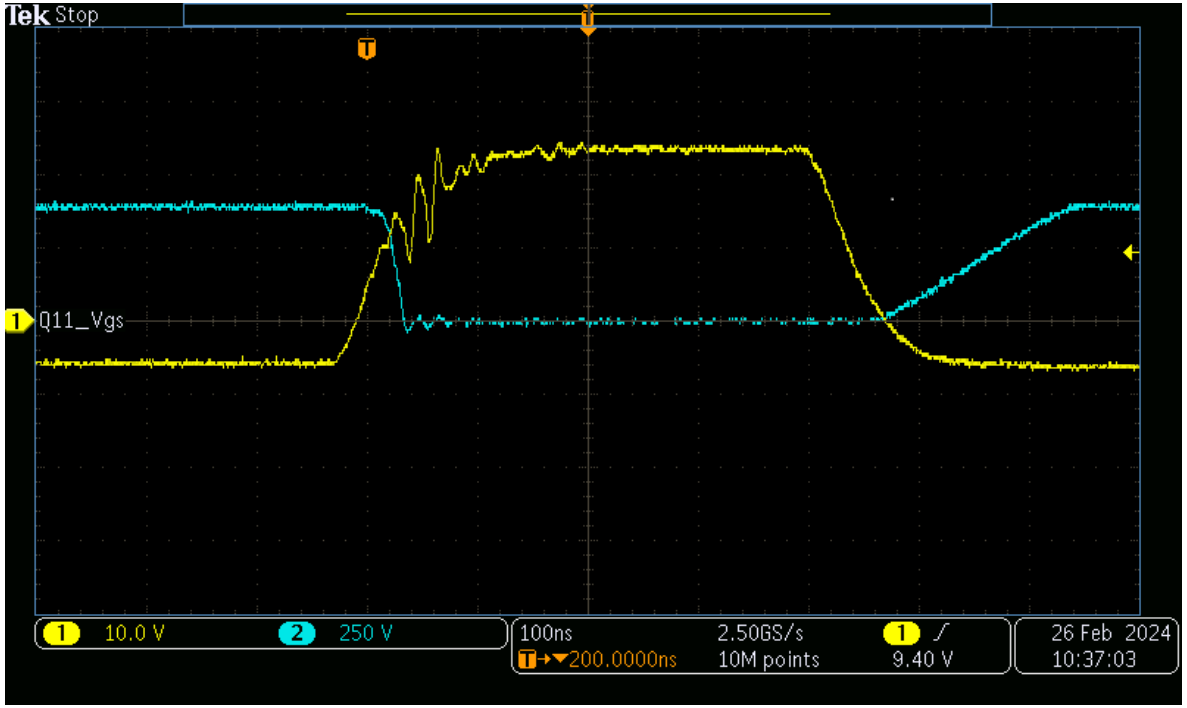


Design Example

15kW, 3 Phase, 3 Level Bidirectional Power Converter



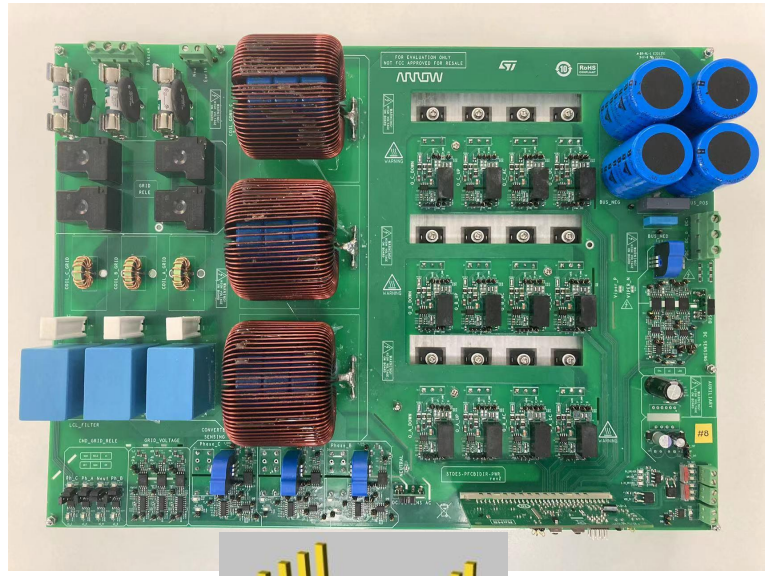
Before modification



After modification

Design Example

15kW, 3 Phase, 3 Level Bidirectional Power Converter

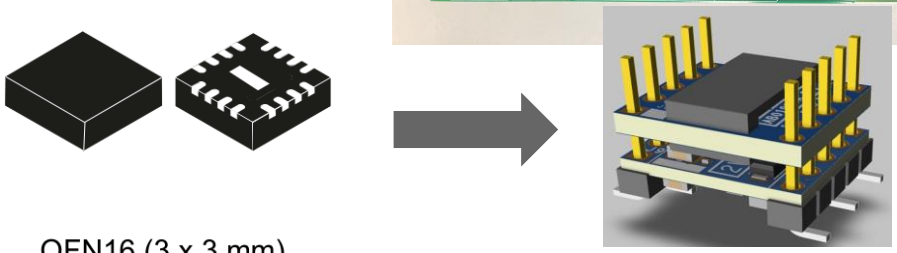


L6983i: 2W Iso_buck Converter for SiC Gate Drive Power Supply

L6983i

Features

- 3.5 V to 38 V operating input voltage
- 200kHz to 1MHz programmable switching frequency
- Primary output voltage regulation / no optocoupler required
- 4.5 A source/sink peak primary current capability
- Internal Loop Compensation
- 2 µA shut down current
- Internal soft-start
- Overvoltage protection, output voltage sequencing, Thermal protection
- Enable, Power good, Synchronization to external clock
- QFN16 (3x3 mm) package



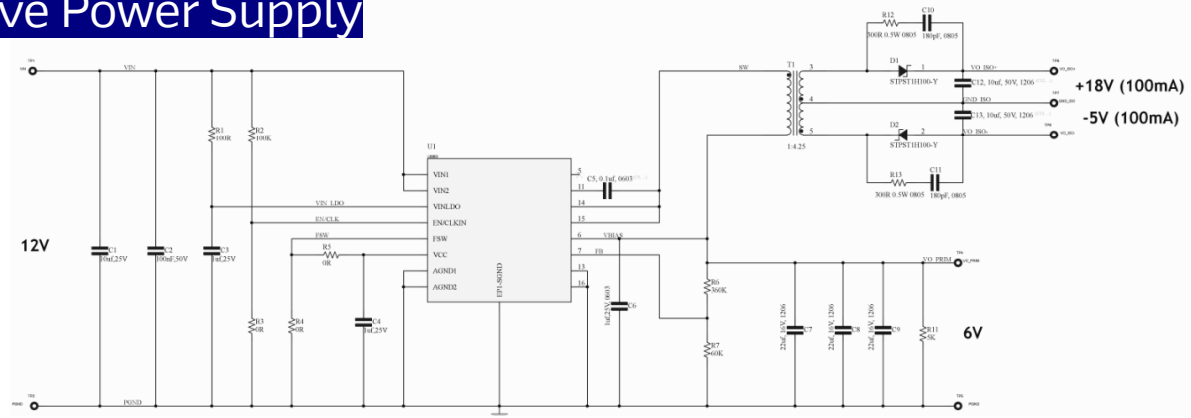
QFN16 (3 x 3 mm)

Applications

- Isolated IGBT/SiC MOSFET gate drive supply
- OBC (On-board charge) for HEV/EV
- Electric traction systems

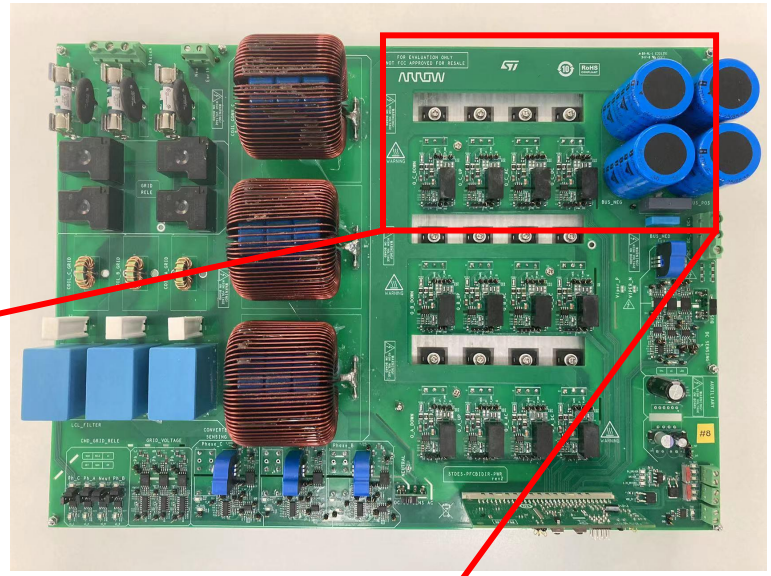
2W Iso_buck Converter for SiC Gate Drive Power Supply

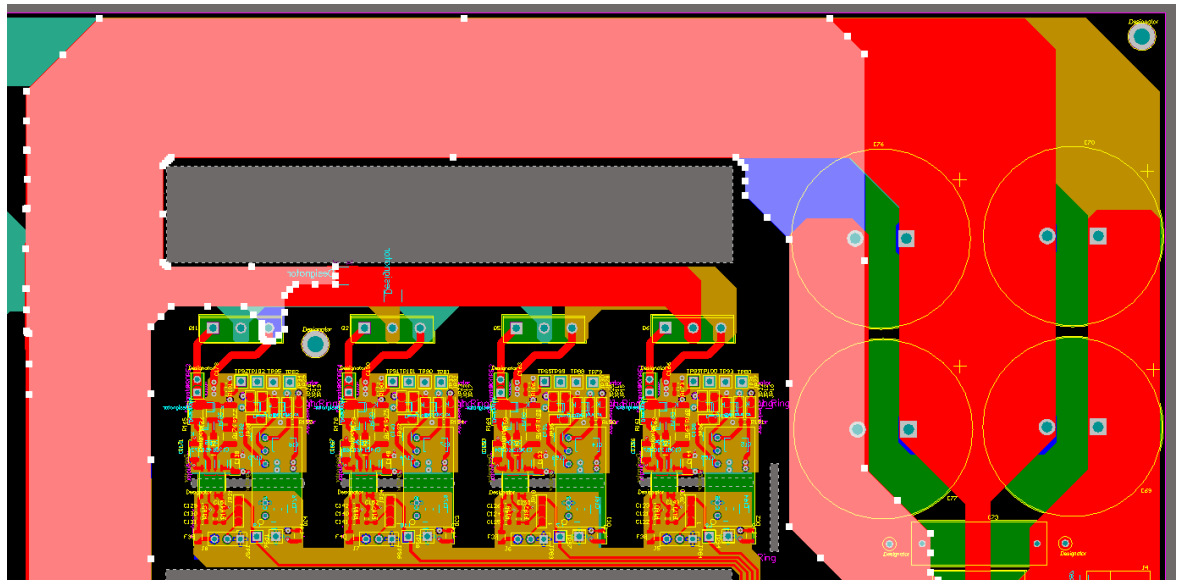
Drive Power Supply

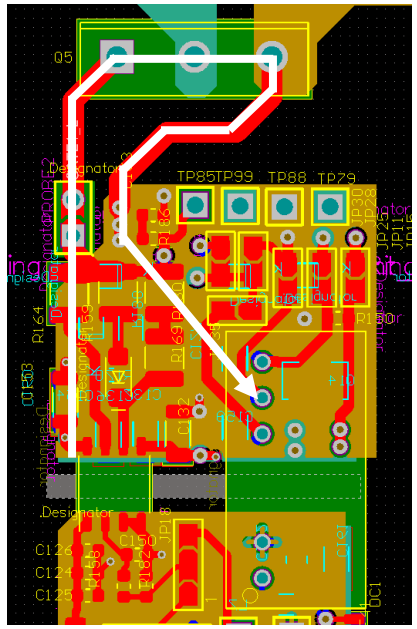


Design Example

15kW, 3 Phase, 3 Level Bidirectional Power Converter







Summary

Design tips to achieve 3H performance

– High efficiency, High power density, High thermal conductivity

- Select suitable SiC MOSFET for target application – voltage rating, current rating, package, etc.
- Optimized gate driver design to maximized performance
- Gate driver with sufficient driving capability, high CMTI, low propagation delay should be use
- Miller Clamp function is strongly recommended
- Negative gate-source voltage for robust MOSFET turn-off
- Minimize circuit parasitic
- Gate resistors, gate-source capacitors can be added

Your best SiC design partner

Arrow Open Lab

Design & Projects

https://www.arrowopenlab.com/HkOpenLab/ESC_Solution.html

Thank You