Full-Bridge Micro-inverter based on silicon carbide (SiC) power transistor

Prepared by: AEC – High Power LAB (HPL)

Outline

1. Specification
2. System Block Diagram
3. Schematic/PCBA/Assembly
4. PLL Structure
5. Control Algorithm
6. Firmware Package
7. Key Parts
8. Test Results
9. Release Package

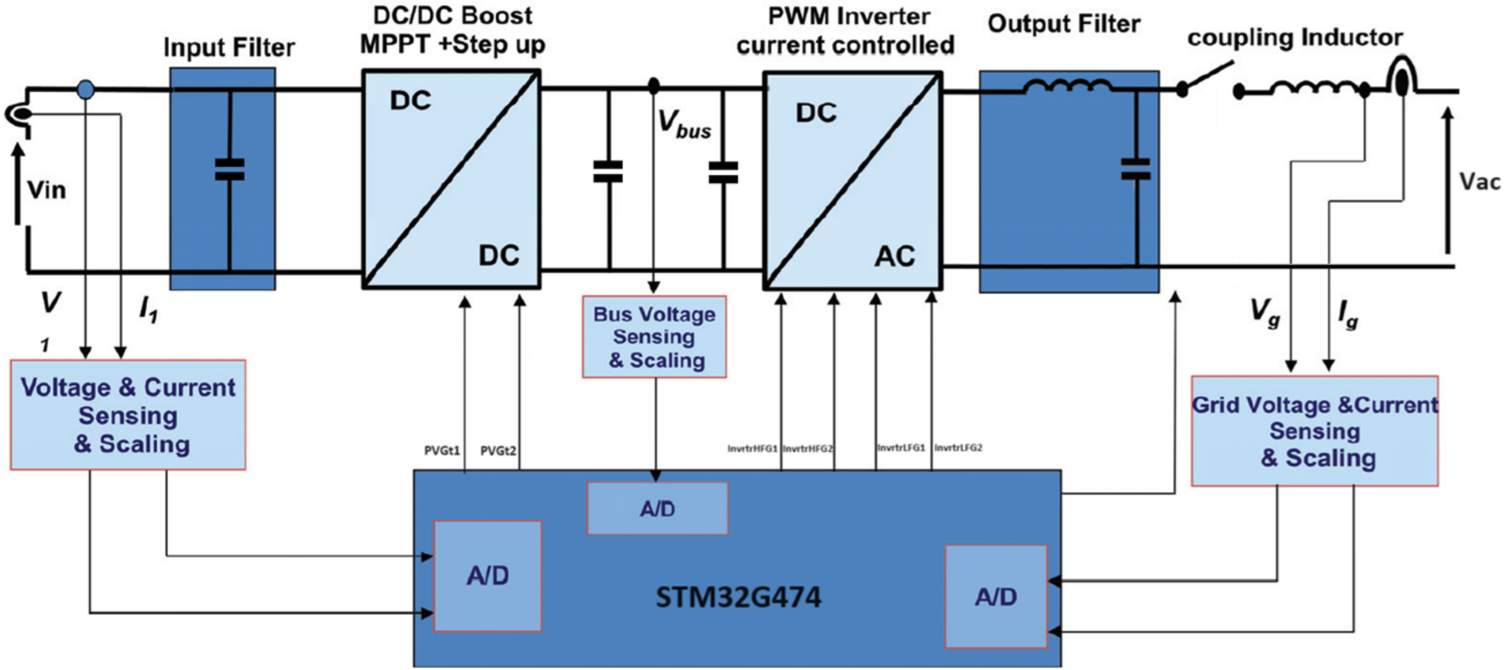
1. Specifications(MPPT)

Parameter	Value
Vin_normal (normal input voltage)	36V
Vin_max (maximum input voltage)	55V
Vin_min (minimum input voltage)	18V
MPPT_DC input range	20V to 40V
Iin (nominal input current)	12A
Imax (maximum input current)	18A

1. Specifications (Inverter)

Parameter	Value
Vbus (DC-DC nominal output voltage)	380V
Vbus_max (DC-DC maximum output voltage)	400V
Vac (AC nominal output voltage)	110VAC/60Hz, 220VAC/50Hz
Iac (AC maximum output current)	1.8A/220VAC, 3.6A/110VAC
Pac (maximum output power)	400W

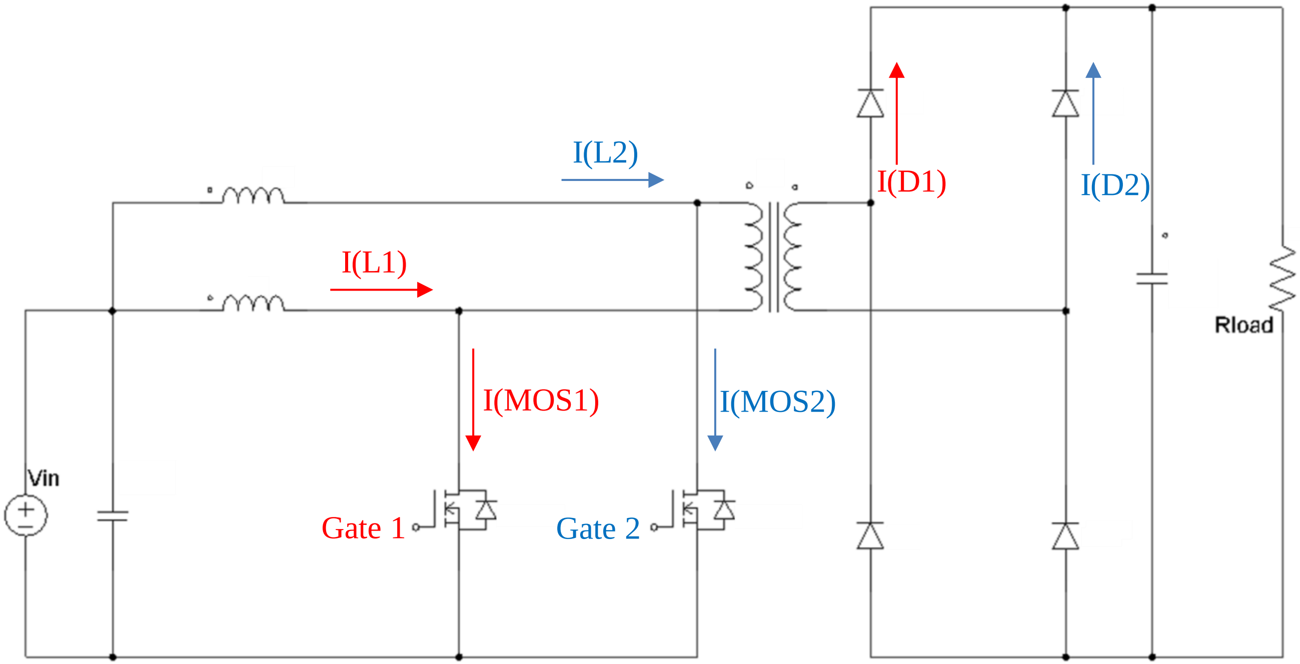
2. System Block Diagram



Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

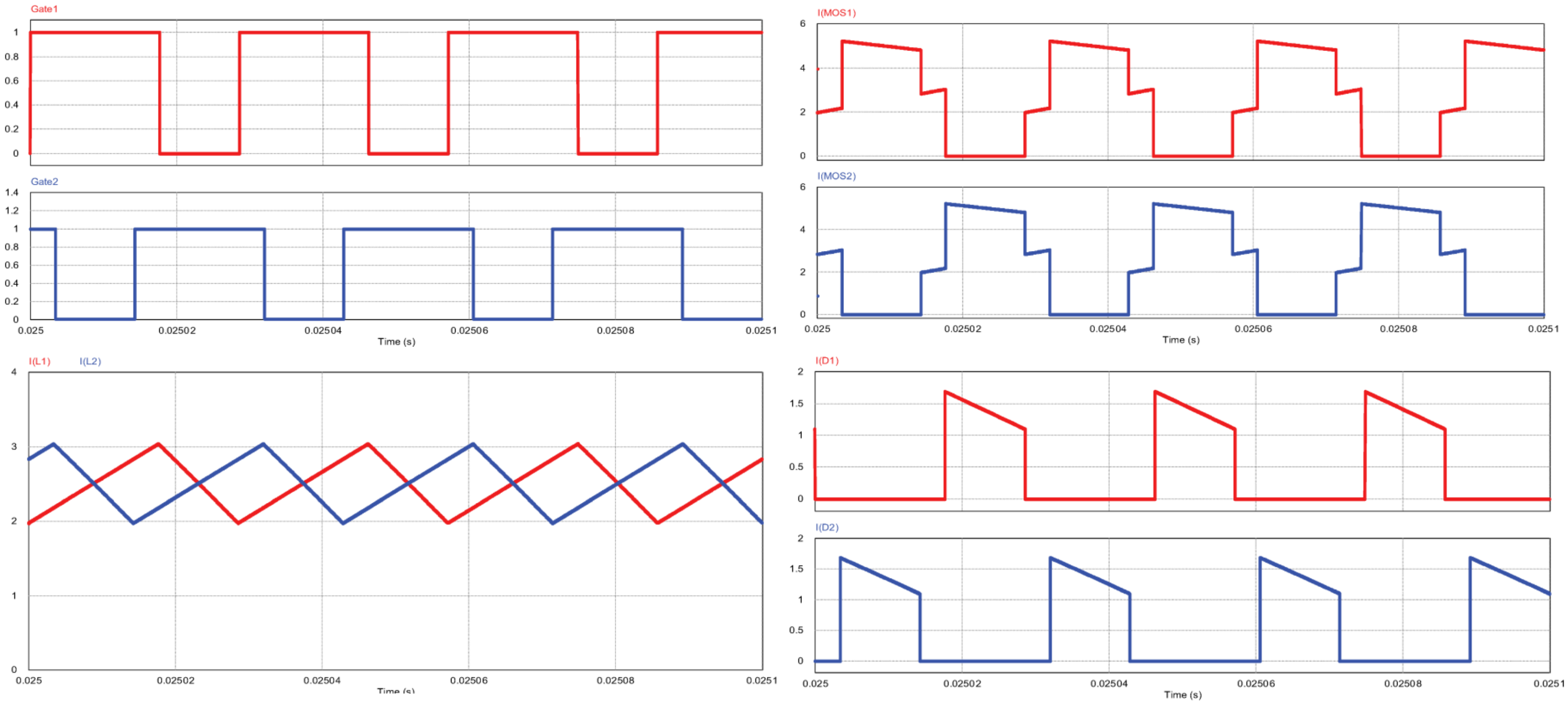
DC-DC Converter



Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-DC Converter (waveform)



Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-DC Converter (Parameter Design)

Calculation of the maximum duty cycle: In this topology the switch duty cycle is always >0.5. Let's call D the time beyond $T_s/2$ for which the MOSFET is still closed:

$$D_{max} = \frac{t_{on,max}}{T_s} - 0.5 = 0.2 \qquad (1)$$

$$t_{on,max} = 0.7 \times T_s \qquad (2)$$

Calculation of maximum input power:

$$P_{in} = \frac{P_{out}}{\eta} = \frac{400}{0.94} = 425.5W \qquad (3)$$

Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-DC Converter (Parameter Design)

Calculation of maximum average input current:

$$I_{in,max} = \frac{P_{in}}{V_{in,min}} = \frac{425.5}{18} = 23.6A \quad (4)$$

Calculation of the maximum switch RMS current:

$$I_{rms,max} = \frac{\sqrt{2-D}}{2} \times I_{in,max} = \frac{\sqrt{2-0.2}}{2} \times 12.8 = 8.6A \quad (5)$$

Calculation of the maximum average output current:

$$I_{out,max} = \frac{P_{out}}{V_{out,min}} = \frac{400}{370} = 1.08A \quad (6)$$

Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-DC Converter (Parameter Design)

Calculation of transformer turn ratio:

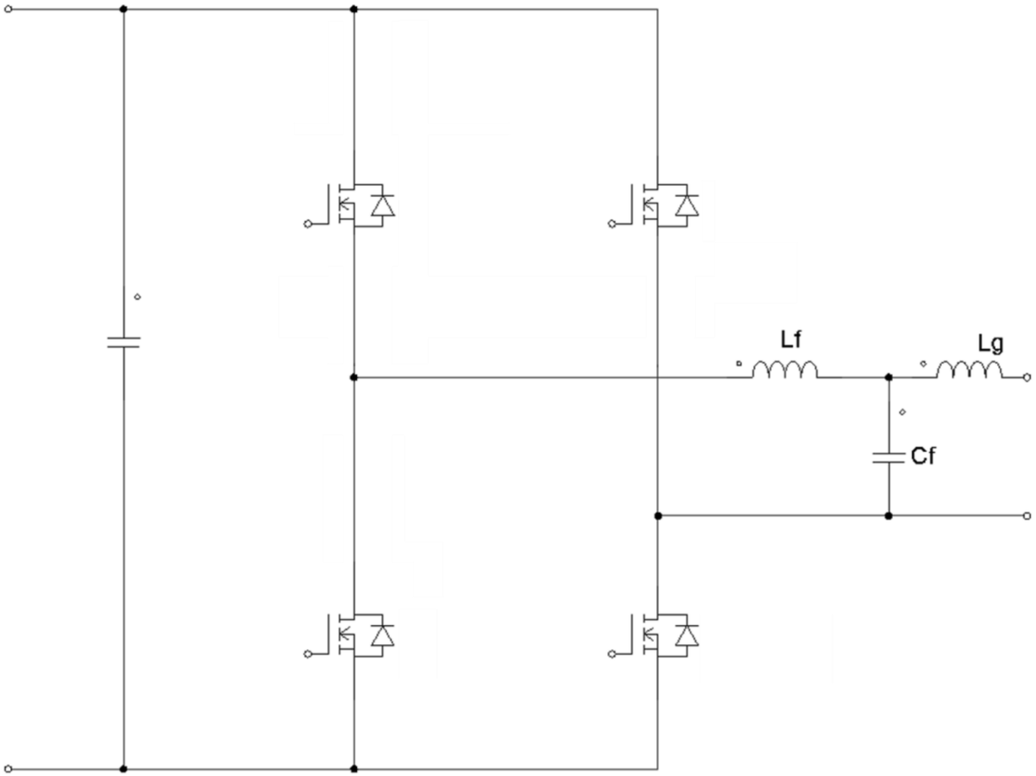
$$\frac{N_2}{N_1} = \frac{\frac{V_{out}}{2} \times (1 - D)}{2 \times V_{in}} = \frac{\frac{380}{2} \times (1 - 0.2)}{2 \times 30} = 2.53 \qquad (7)$$

where V_{in} is chosen as the average between the maximum and minimum input voltage value. The final transformer turn ratio has been chosen equal to 2.6.

Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-AC Converter



Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-AC Converter (Parameter Design)

The minimum value of capacitance required on the DC bus is calculated according to the following equation:

$$C_{bus} = \frac{4P_{out}}{V_{bus,min}^2} t_1 = \frac{4 \times 400 \times 4.17 \times 10^{-3}}{370^2} = 48.74\mu F \quad (8)$$

where t_1 is given by

$$t_1 = 4.17ms = \frac{1}{4 \times f_{grid}} = \frac{1}{4 \times 60} \quad (9)$$

A total capacitance of about twice the calculated value, rated at 450 V and having an operating temperature of 105 °C, is selected for the inverter implementation. The capacitor bank is realized with the parallel connection of four $22\mu F$, 450 V capacitors.

Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-AC Converter (Parameter Design)

The value of L_f is designed to limit the current ripple within 20% of the nominal current value. The following equations have been used to calculate the filtering inductance value:

$$L_f = \frac{1}{n}\frac{\left(V_{bus} - V_{grid,pk}\right) \times D}{\Delta i \times f_{sw}} = \frac{1}{3}\frac{(380 - 155) \times 0.75}{0.73 \times 25 \times 10^3} = 3.1mH \qquad (10)$$

where n is the number of inverter levels ($+V_{bus}$, 0 and $-V_{bus}$) and D is the inverter duty cycle.

Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-AC Converter (Parameter Design)

The filter capacitor value is selected to limit the exchange of reactive power below 2.5% of nominal active power:

$$P_{reactive} < 0.05 \times P_{active} \quad (11)$$

$$X_{C_f} \geq \frac{V_{grid}^2}{0.025 \times P_{active}} = \frac{230^2}{10} = -j5290\Omega \quad (12)$$

$$C_f \leq \frac{1}{j\omega X_{C_f}} = \frac{1}{2\pi \times 60 \times 5290} = 501.43nF \quad (13)$$

Source: AN4070 Application note (www.st.com)

2. System Block Diagram (cont.)

DC-AC Converter (Parameter Design)

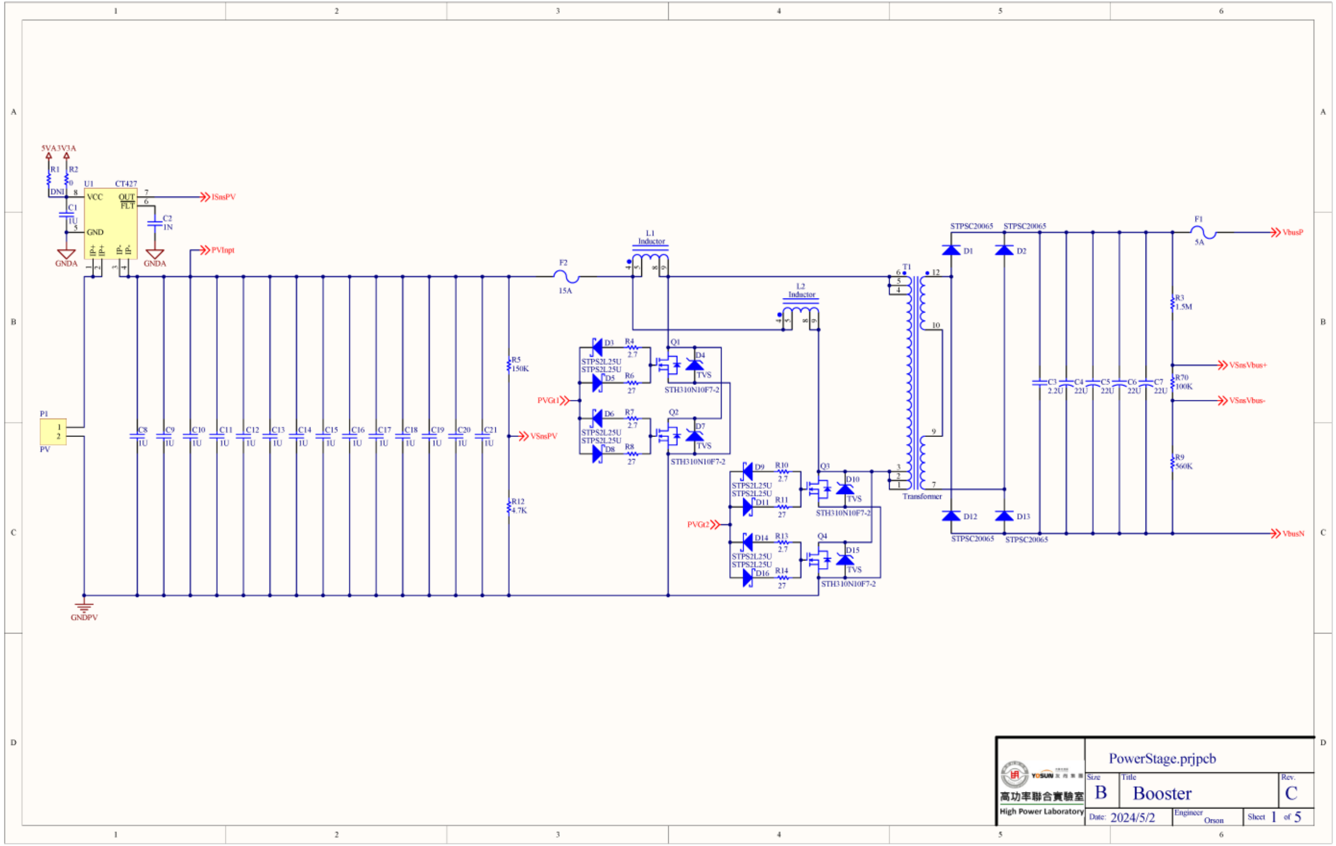
To avoid resonance problems for the filter due to low and high order harmonics, the resonant frequency should be chosen in a range between ten times the line frequency and one half of the switching frequency. The resonant frequency of an LCL filter is given by:

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_f+L_g}{L_f \times L_g \times C_f}} \qquad (14)$$

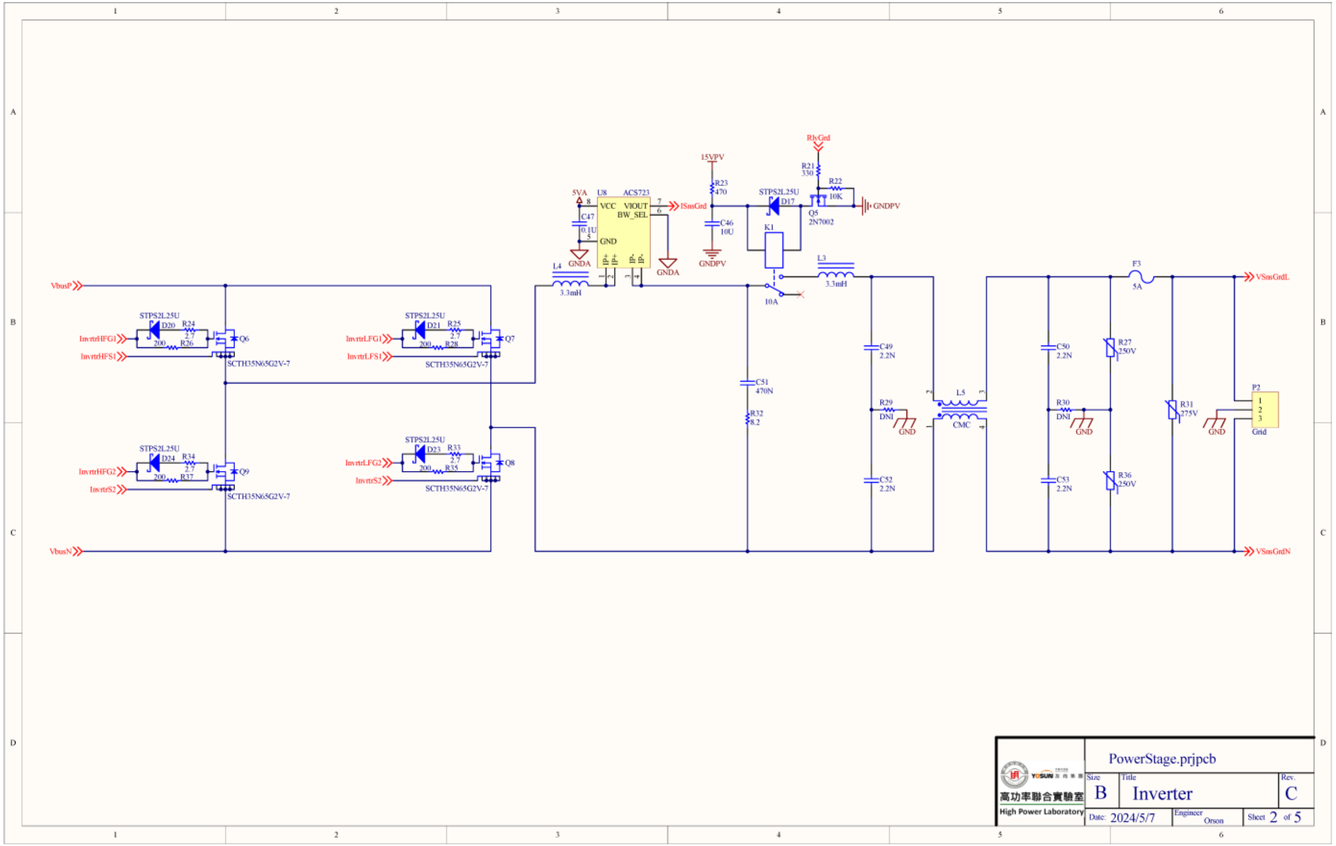
Choosing a filter capacitor value of 470nF and a grid coupling inductor value equal to the filtering inductor value of 3.3mH, the resulting filter resonant frequency is equal to 5.7 kHz which falls in the frequency range mentioned above.

Source: AN4070 Application note (www.st.com)

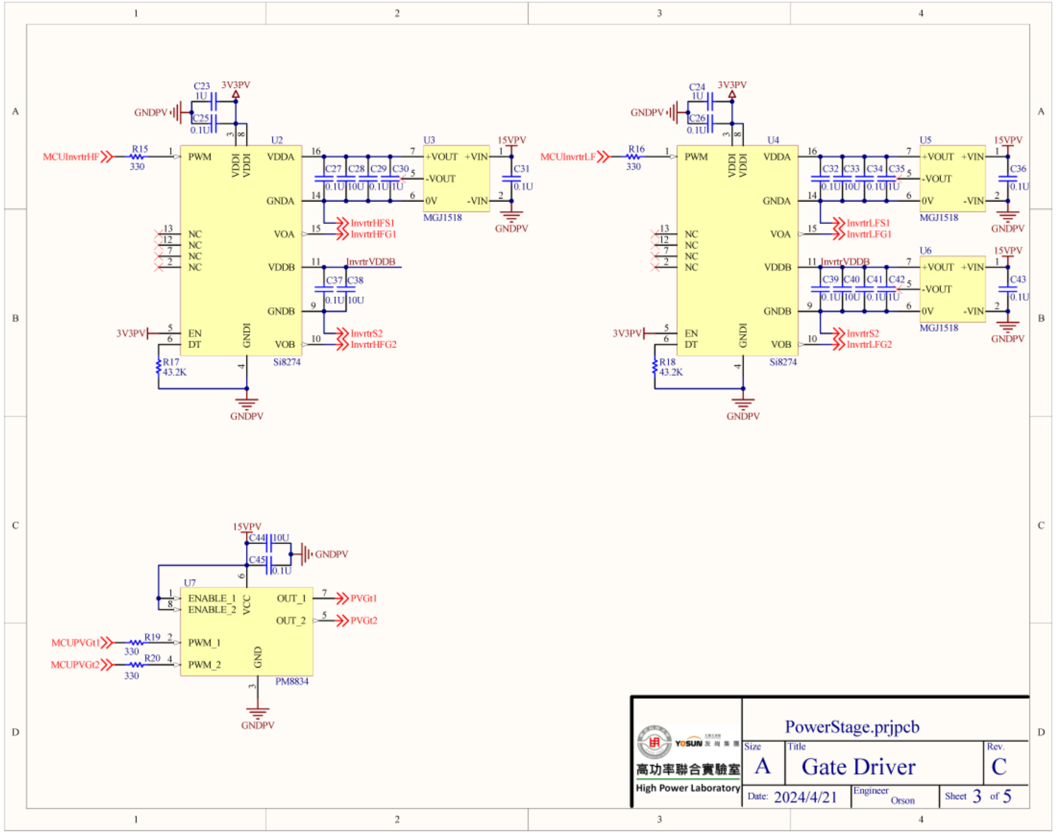
3. Schematic/PCBA/Assembly



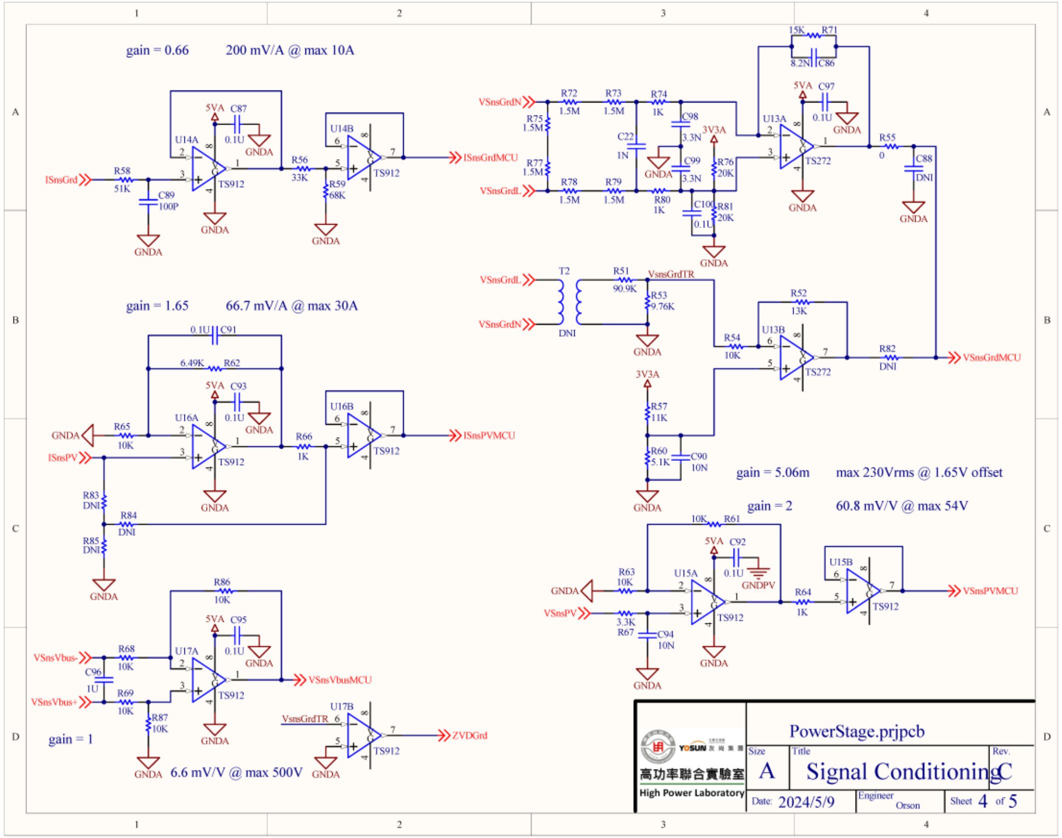
3. **Schematic**/PCBA/Assembly (cont.)



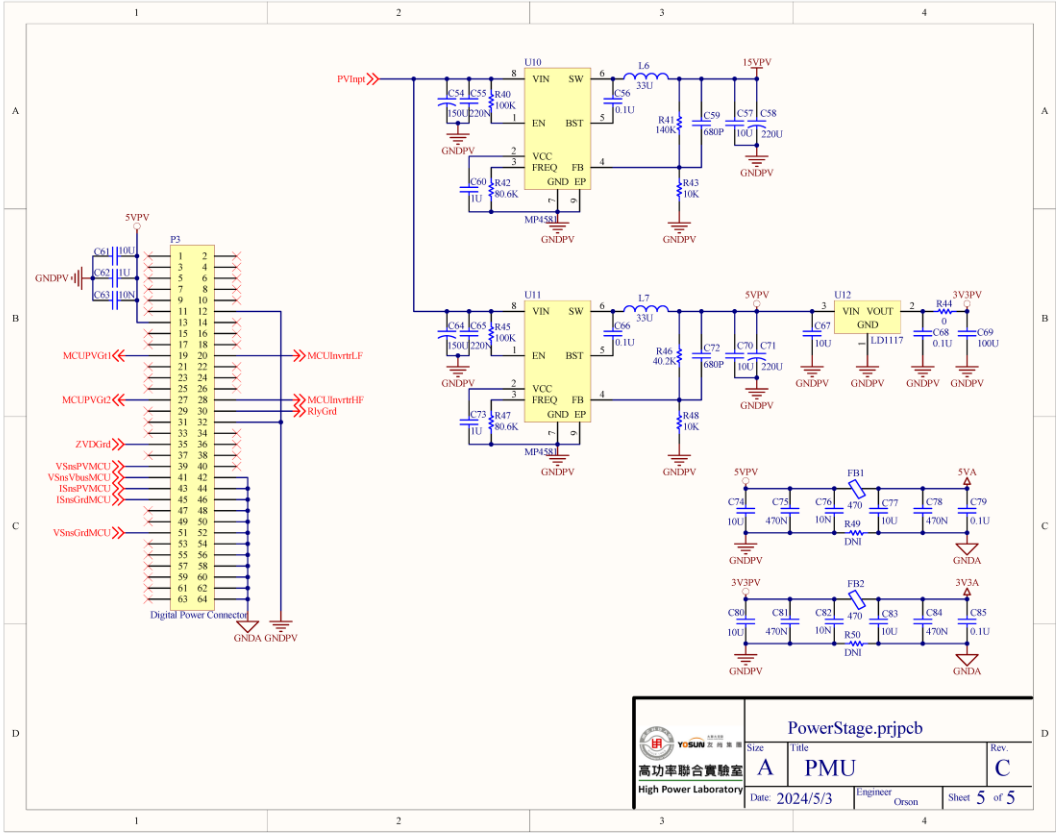
3. **Schematic**/PCBA/Assembly (cont.)



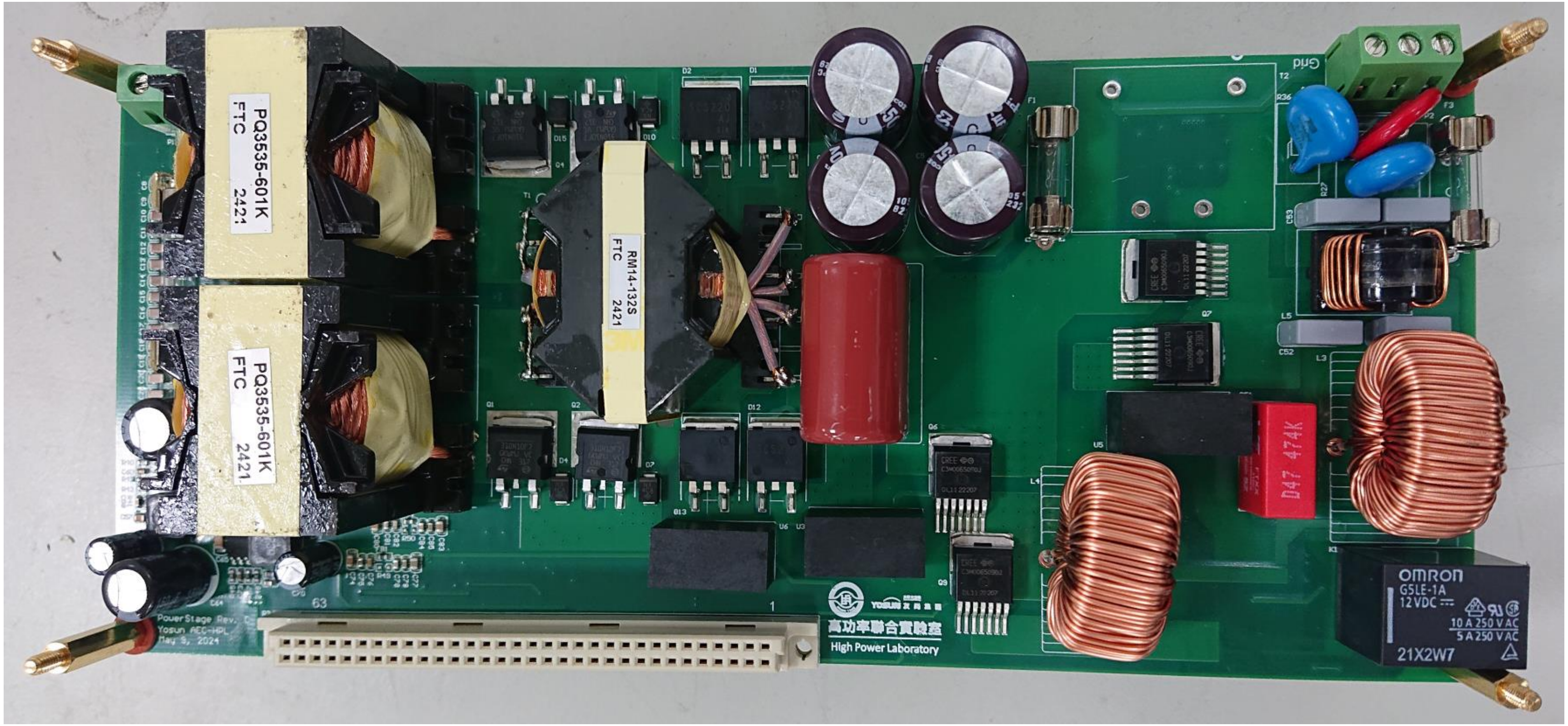
3. **Schematic**/PCBA/Assembly (cont.)



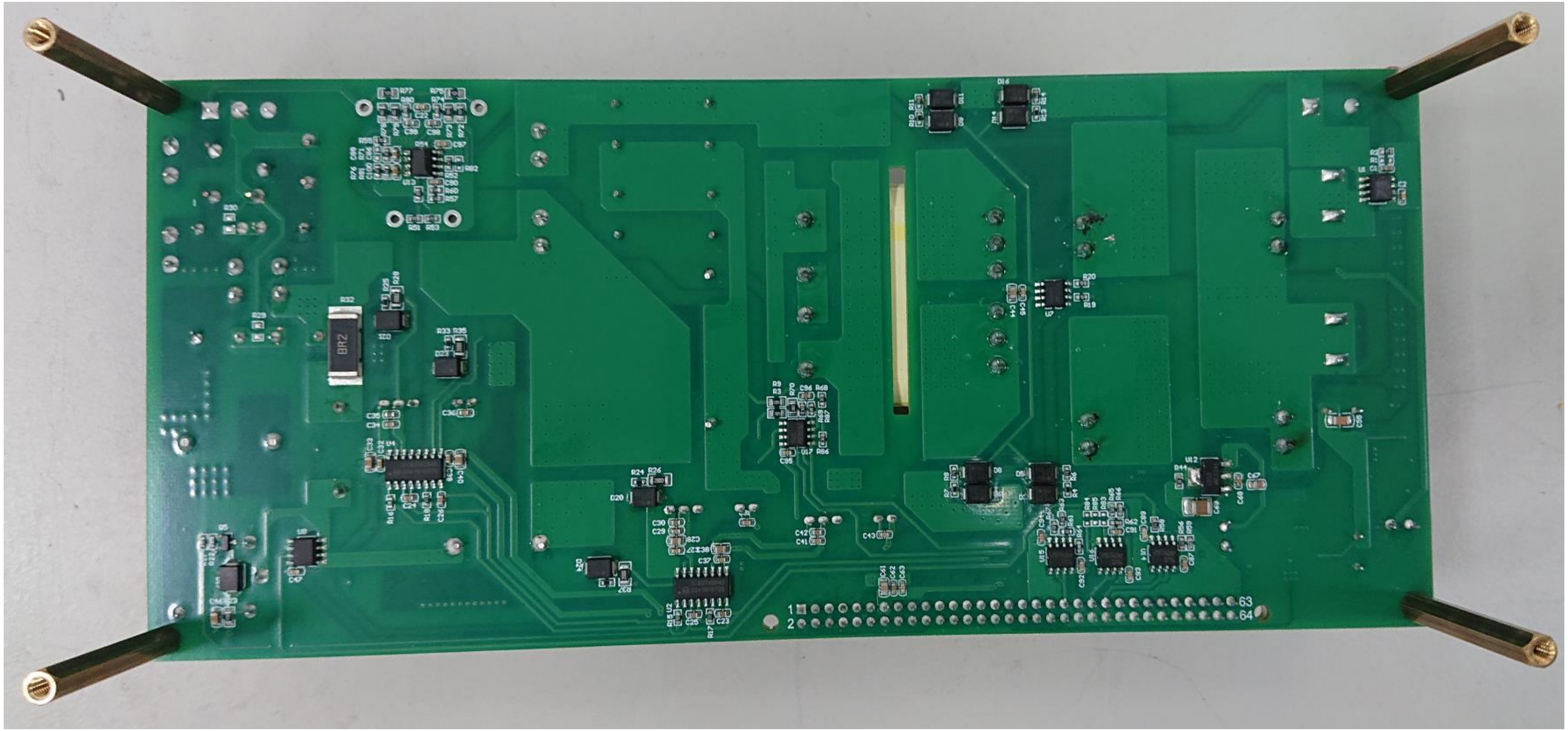
3. **Schematic**/PCBA/Assembly (cont.)



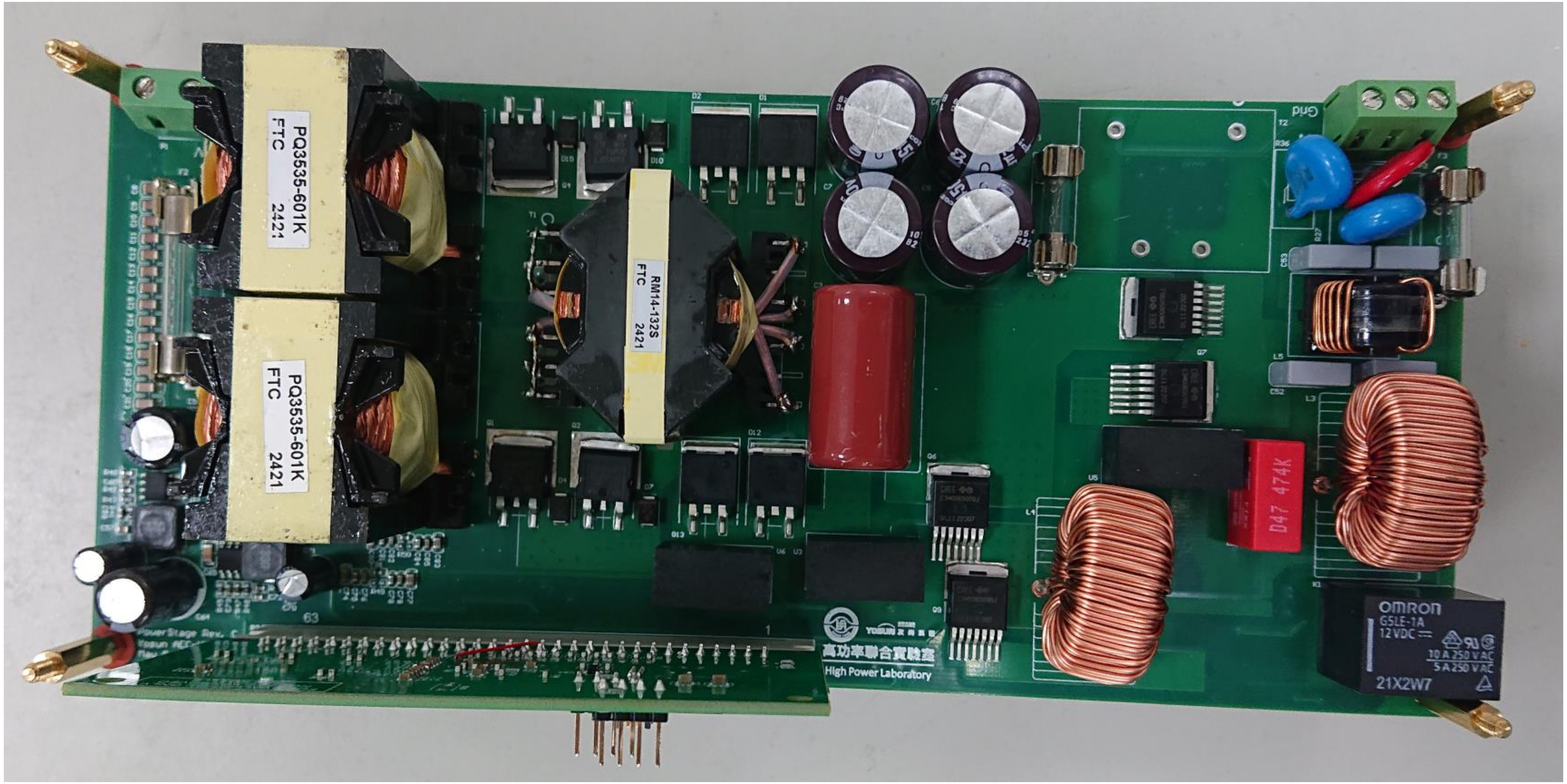
3. Schematic/**PCBA**/Assembly



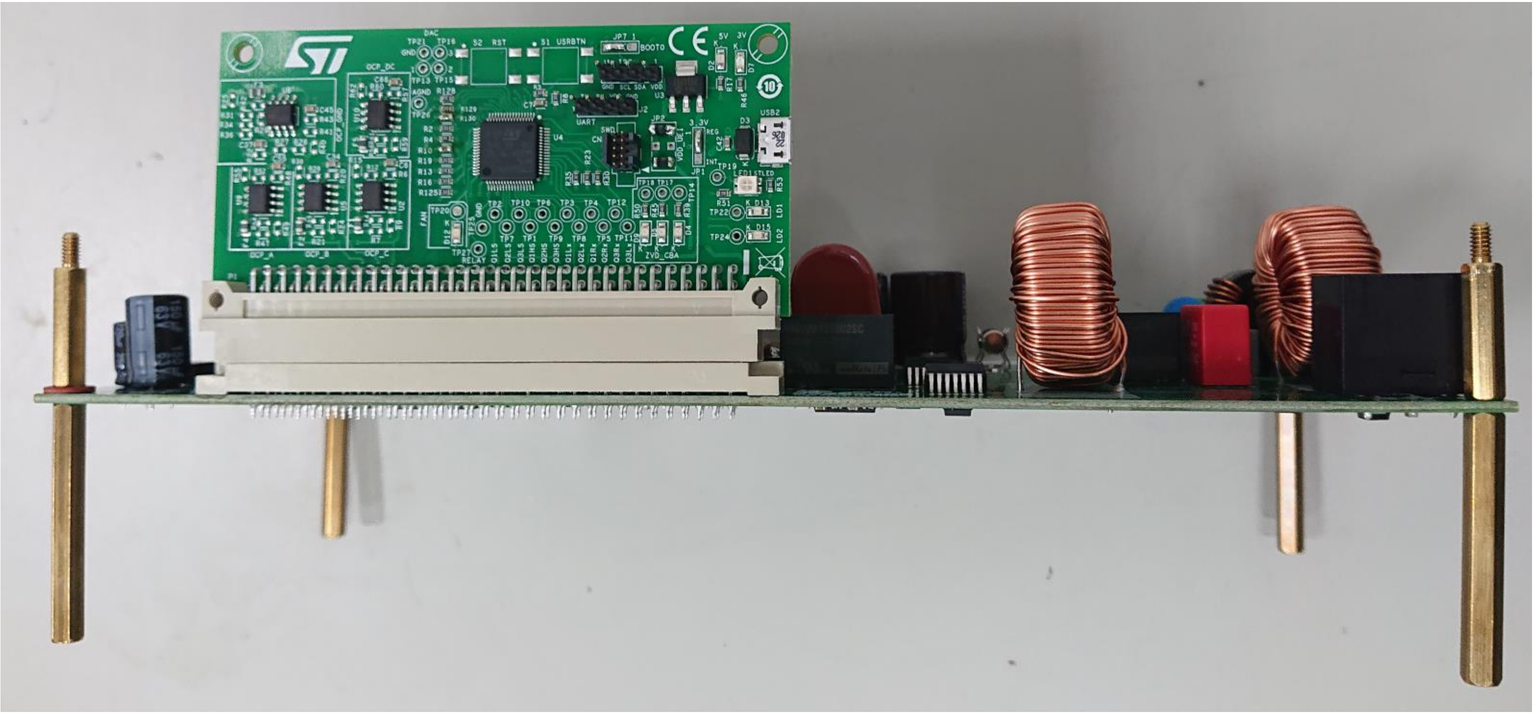
3. Schematic/**PCBA**/Assembly (cont.)



3. Schematic/PCBA/**Assembly**



3. Schematic/PCBA/**Assembly** (cont.)



4. PLL Structure

Knowing the two voltage components V_β and V_α, the transformation from the stationary reference frame to the d-q rotating frame is given as follows.

$$\begin{bmatrix} V_d \\ V_q \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} \quad (8)$$

where θ is the angle between the d-q reference frame and the stationary reference frame. The reverse transformation is given by:

$$\begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} = \begin{bmatrix} \cos\theta & -\sin\theta \\ \sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} V_d \\ V_q \end{bmatrix} \quad (9)$$

where

$$\begin{bmatrix} V_\beta \\ V_\alpha \end{bmatrix} = \begin{bmatrix} V_m \cos\theta_e \\ V_m \sin\theta_e \end{bmatrix} \quad (10)$$

Source: AN4070 Application note (www.st.com)

4. PLL Structure (cont.)

Then the two components on the d-q reference frame are:

$$V_d = V_m \cos\theta_e \cos\theta + V_m \sin\theta_e \sin\theta = V_m \cos(\theta - \theta_e) \quad (11)$$

$$V_q = -V_m \cos\theta_e \sin\theta + V_m \sin\theta_e \cos\theta = V_m \sin(\theta - \theta_e) \quad (12)$$

Therefore, if $\theta = \theta_e$, the two components are reduced

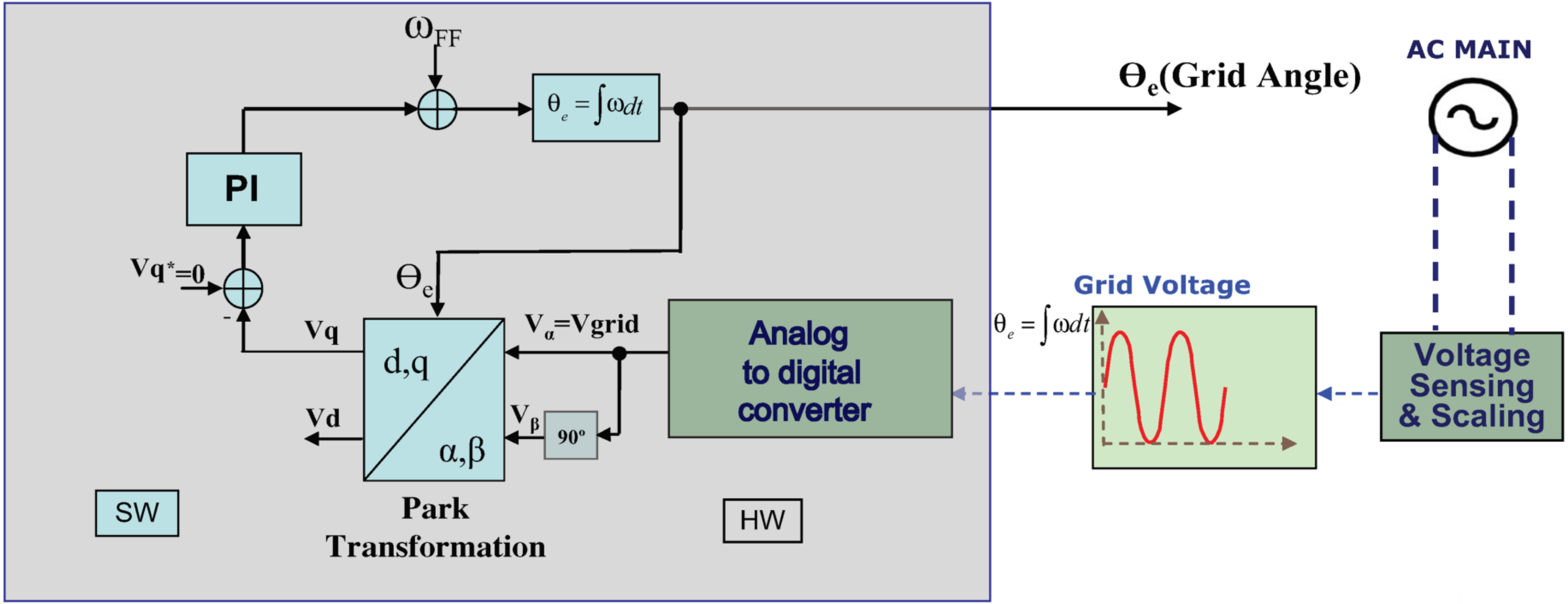
$$V_d = V_m \quad (13)$$

$$V_q = 0 \quad (14)$$

The grid voltage angle is detected using PLL structure.

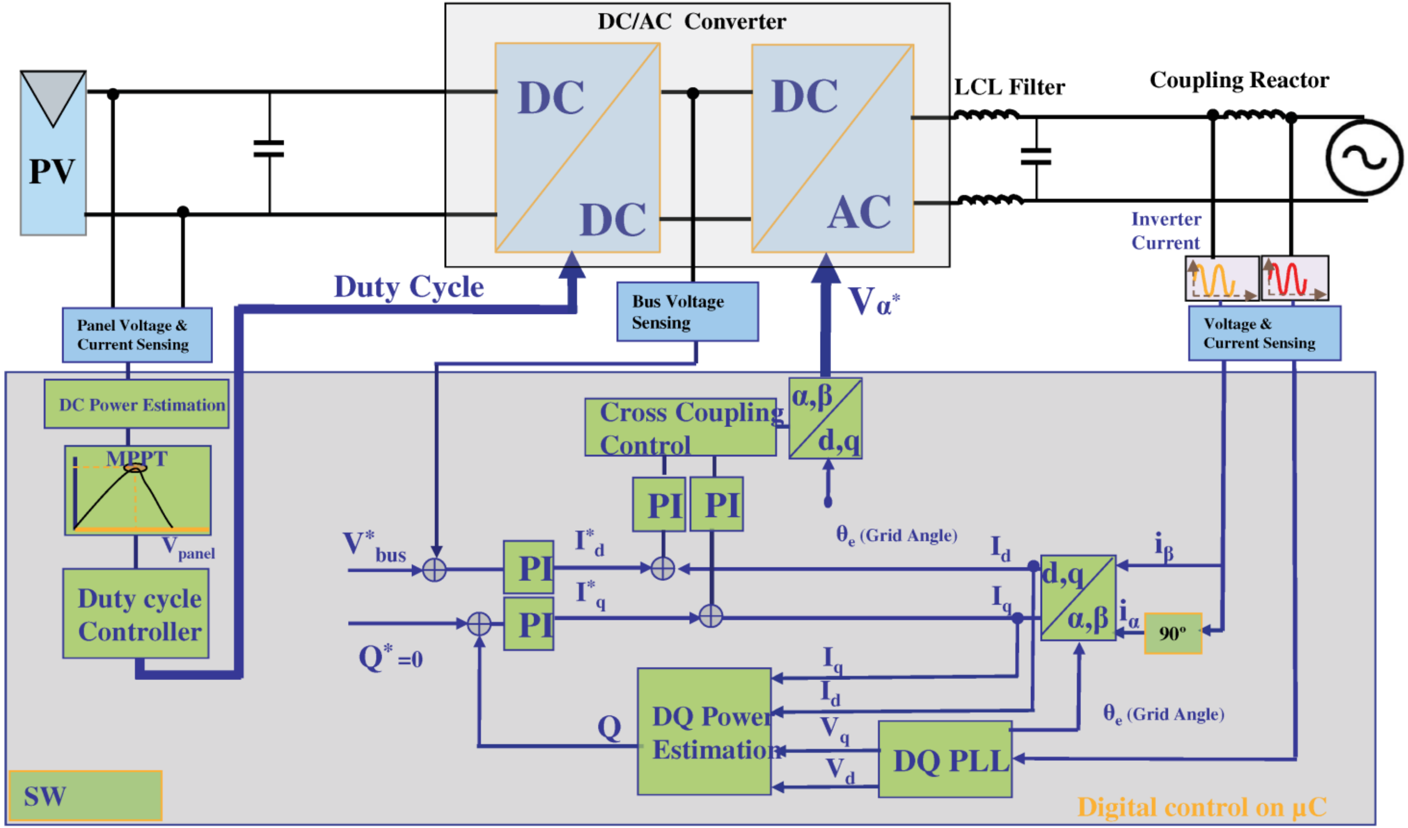
Source: AN4070 Application note (www.st.com)

4. PLL Structure (cont.)



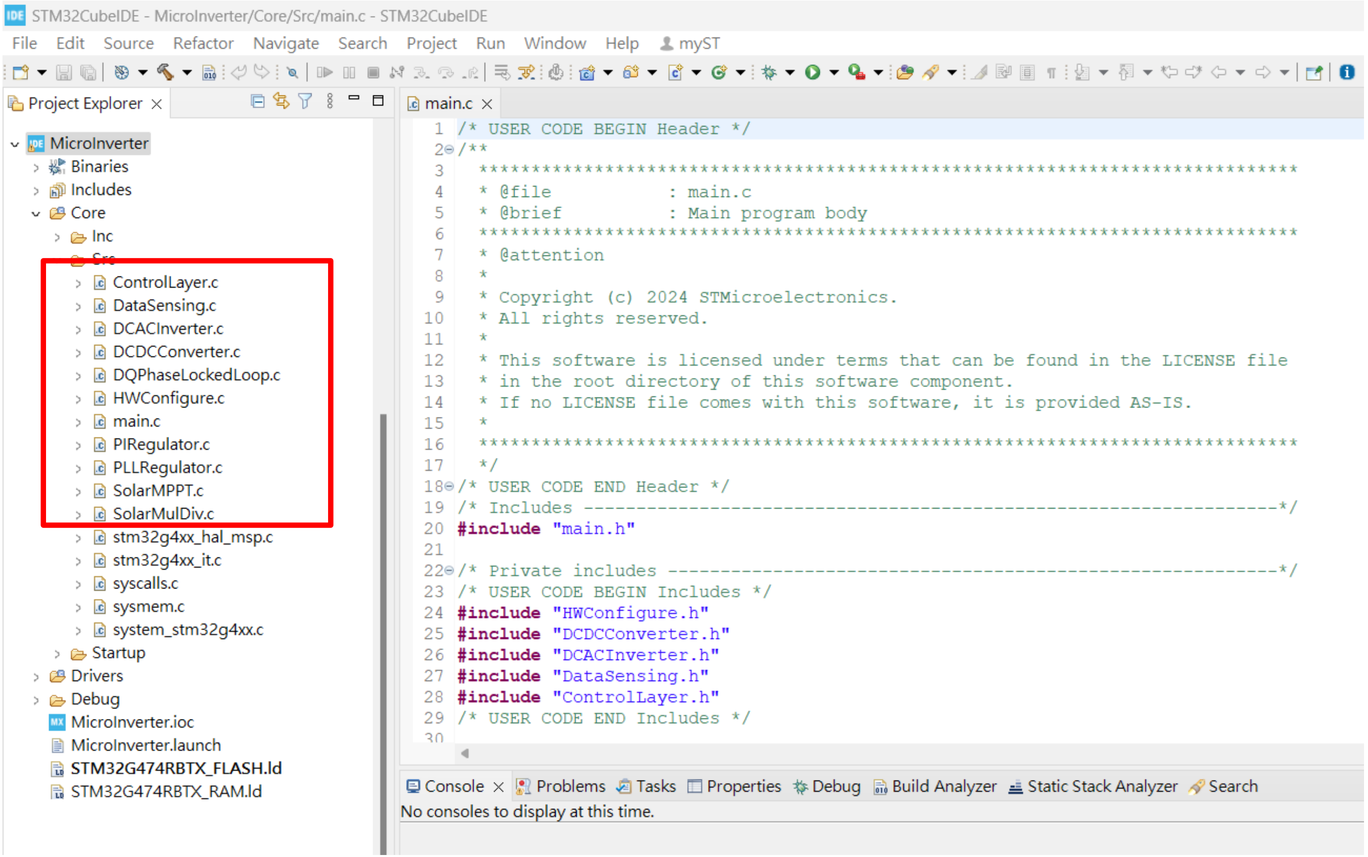
Source: AN4070 Application note (www.st.com)

5. Control Algorithm



Source: AN4070 Application note (www.st.com)

6. Firmware Package



6. Firmware Package (cont.)

The Src folder contains all .c files that contribute to the power management.

1. **ControlLayer.c**: the core of the firmware. It contains a lot of functions for the closed and open loop control;
2. **DataSensing.c**: configures the data sensing section for closed loop control;
3. **DCACInverter.c**: contains all functions with regard to the DC-AC section;
4. **DCDCConverter.c**: contains all functions with regard to the DC-DC section;
5. **DQ_PhaseLockedLoop.c**: contains the DQ-PLL implementation for a single-phase and the anti-islanding protection routine;

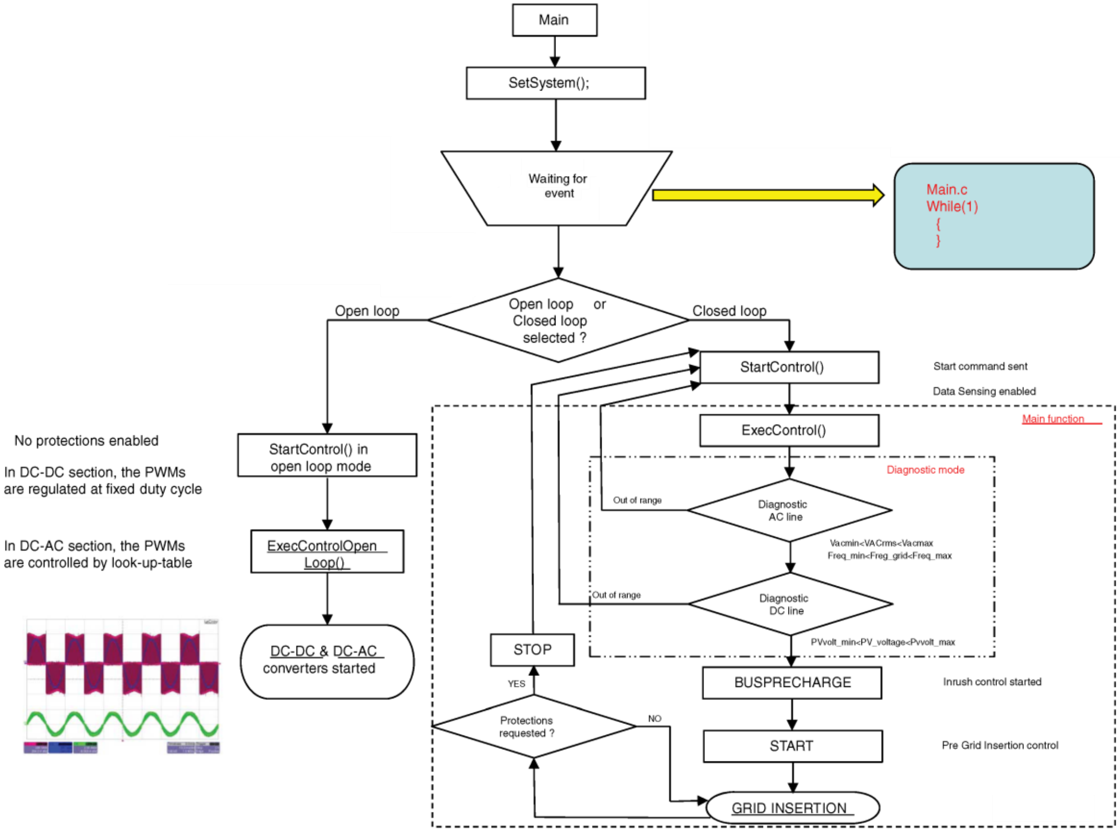
Source: AN4070 Application note (www.st.com)

6. Firmware Package (cont.)

6. **HWconfigre.c**: configures the ADC and timer peripherals;
7. **main.c**: includes the main loop function and the system parameters management;
8. **PIRegulator.c**: includes several PI regulators for the closed loop control;
9. **PLLRegulator.c**: includes two PI regulators for the closed loop control, the PID_Bus_Voltage and PLL_PID regulator;
10. **SolarMPPT.c**: includes the maximum power point tracking algorithm for the DC-DC control;
11. **SolarMulDiv.c**: includes the calculations used for the closed loop control.

Source: AN4070 Application note (www.st.com)

6. Firmware Package (cont.)



Source: AN4070 Application note (www.st.com)

7. Key Parts

Item	Description	P/N	Q'ty	Vendor
1	MCU, LQFP64	STM32G474RE	1	STMicroelectronics
2	Low Dropout Voltage, Voltage Regulator 1.3A, 3.3 V 3+Tab-Pin	LD1117S33CTR	1	STMicroelectronics
3	4 A dual low-side MOSFET driver	PM8834	1	STMicroelectronics
4	Op Amp, 3.5MHz, 5 → 15 V, 8-Pin	TS272IDT	1	STMicroelectronics
5	Low Power, Op Amp, RRIO, 1MHz, 3 → 15 V, 8-Pin	TS912ID	4	STMicroelectronics
6	N-Channel MOSFET, 180 A, 100 V, 3-Pin	STH310N10F7-2	4	STMicroelectronics
7	SiC N-Channel MOSFET, 45 A, 650 V, 7-Pin	SCT055H65G3-7	4	STMicroelectronics
8	650V 20A, Automotive 650 V power Schottky silicon carbide diode	STPSC20065GY-TR	4	STMicroelectronics

7. Key Parts (cont.)

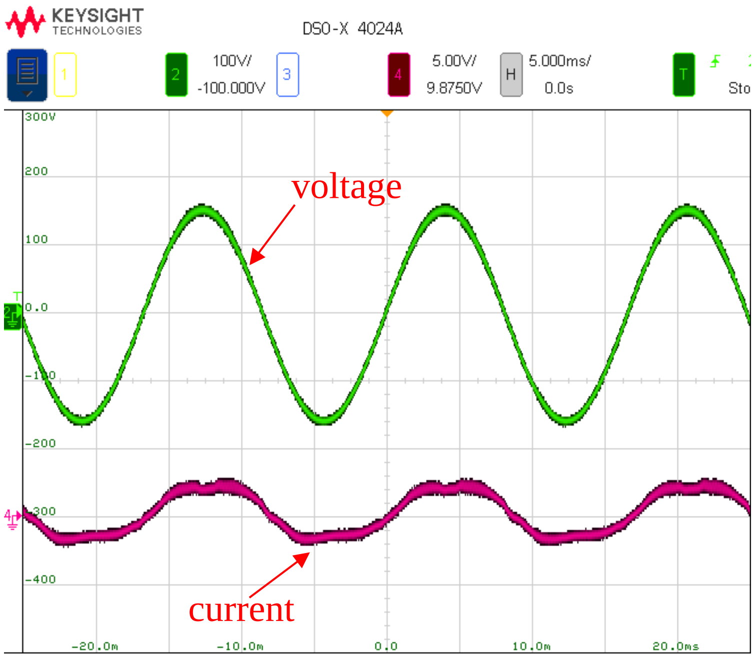
Item	Description	P/N	Q'ty	Vendor
9	25V 2A, Schottky Diode, 2-Pin	STPS2L25U	13	STMicroelectronics
10	DIODE, SMA, ESD Suppressors / TVS Diodes 600W 5.0V Unidirect	SMAJ5.0A-TR	2	STMicroelectronics
11	ESD PROTECTION	ESDA6V1L	1	STMicroelectronics
12	N-Channel MOSFET, 115 mA, 60 V, 3-Pin	2N7002LT1G	1	onsemi
13	100V, 0.8A, High-Efficiency, Synchronous, Step-Down Buck Converter with Integrated Power MOSFETS	MP4581GN	2	MPS
14	Uni-Directional TVS Diode, 600W, 2-Pin	SMBJ100A-13-F	4	DiodesZetex
15	XtremeSense TMR Current Sensor with Ultra-Low Noise and <0.7% Total Error	CT427-HSN830DR	1	CROCUS
16	1µF Multilayer Ceramic Capacitor MLCC 50V dc ±10% , SMD	UMK107BJ105KA-T	10	Taiyo Yuden

7. Key Parts (cont.)

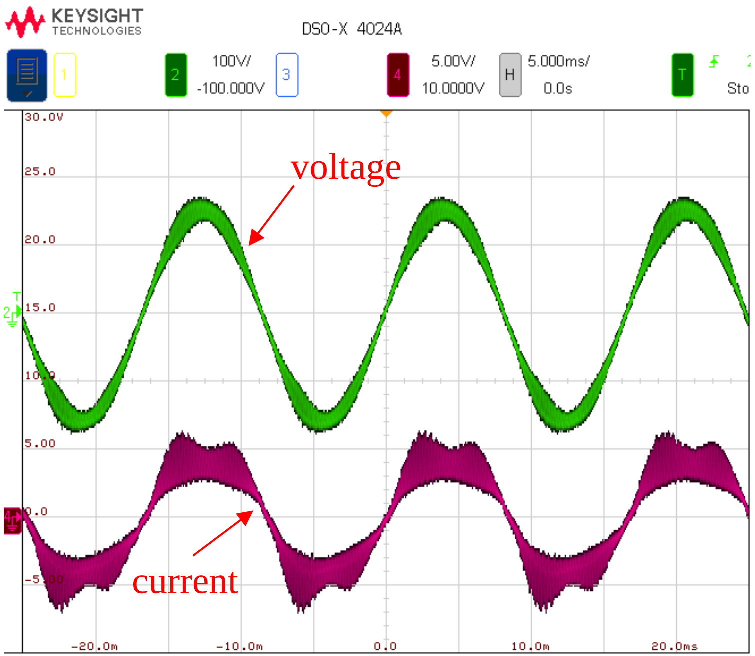
Item	Description	P/N	Q'ty	Vendor
17	1nF MLCC 50V dc ±10% , SMD	UMK107B7102KAHT	2	Taiyo Yuden
18	Multilayer Ceramic Capacitors MLCC - SMD/SMT 1206 100VDC 1uF 10% X7R MIDHIGH VOL	HMK316B7105KL-T	14	Taiyo Yuden
19	100nF MLCC 50V dc ±10% , SMD	UMJ107BB7104KAHT	26	Taiyo Yuden
20	10µF MLCC 25V dc ±10% SMD	TMK212BBJ106KGHT	14	Taiyo Yuden
21	MLCC - SMD/SMT 1206 100VDC 0.22uF 10% X7R MID HIGH VOL	HMK316B7224KL-T	2	Taiyo Yuden
22	680pF Multilayer Ceramic Capacitor MLCC 100V dc ±10% , SMD	HMK107SD681KA-T	2	Taiyo Yuden
23	10nF MLCC 50V dc ±10% , SMD	UMK107B7103KAHT	5	Taiyo Yuden
24	100µF MLCC 16V dc ±20% SMD	EMK325ABJ107MM-P	1	Taiyo Yuden
25	470nF MLCC 25V dc ±10% SMD	TMK107B7474KAHT	4	Taiyo Yuden
26	100pF MLCC 100V dc ±10% SMD	HMK107SD101KA-T	1	Taiyo Yuden

8. Test Results

Input Voltage and Current



200W output

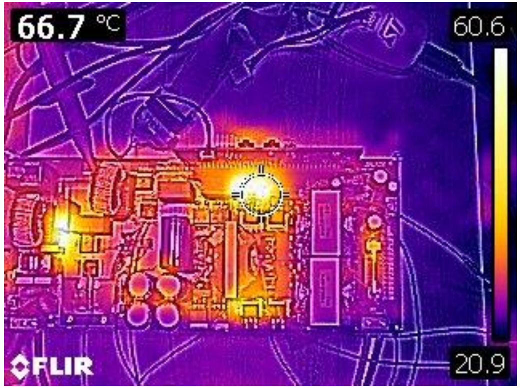


403W output

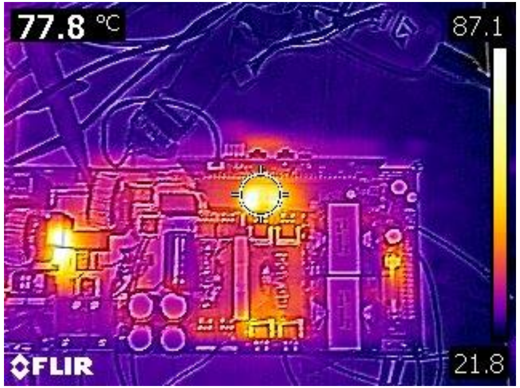
8. Test Results (cont.)

Thermal Image

200W output



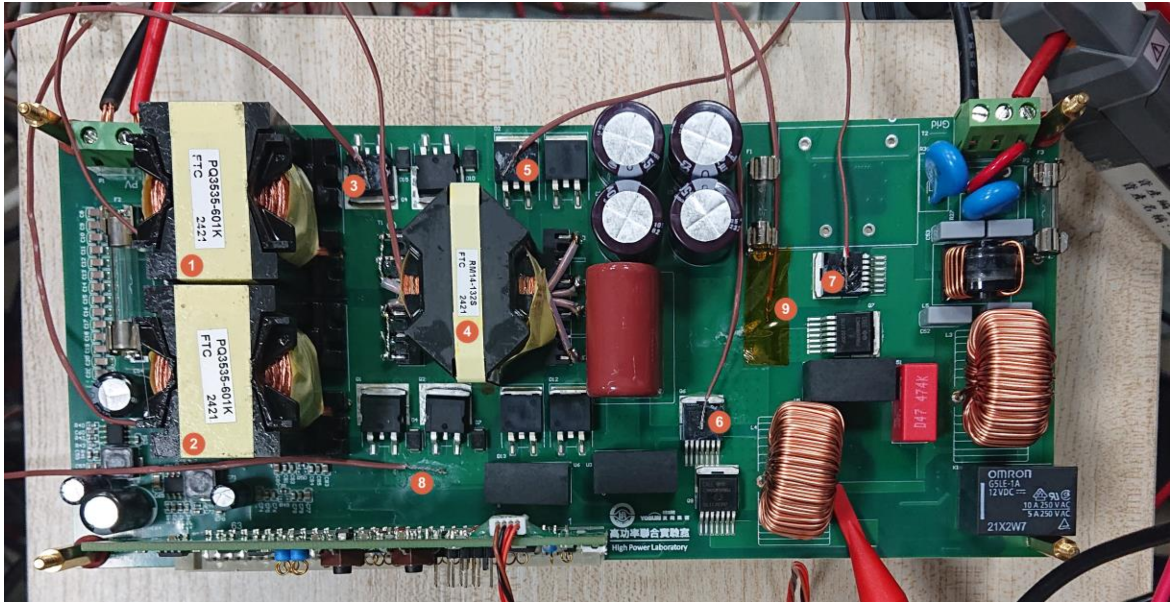
300W output



403W output

8. Test Results (cont.)

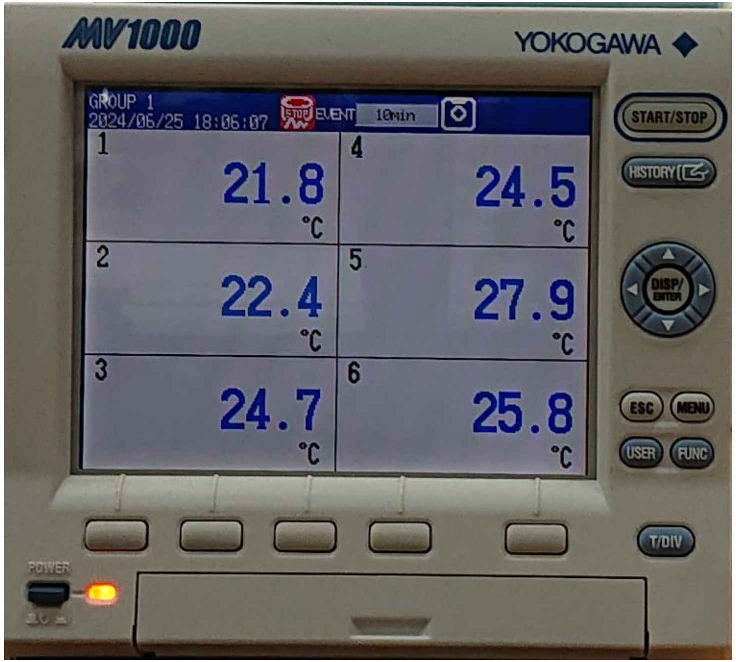
Temperature Probing

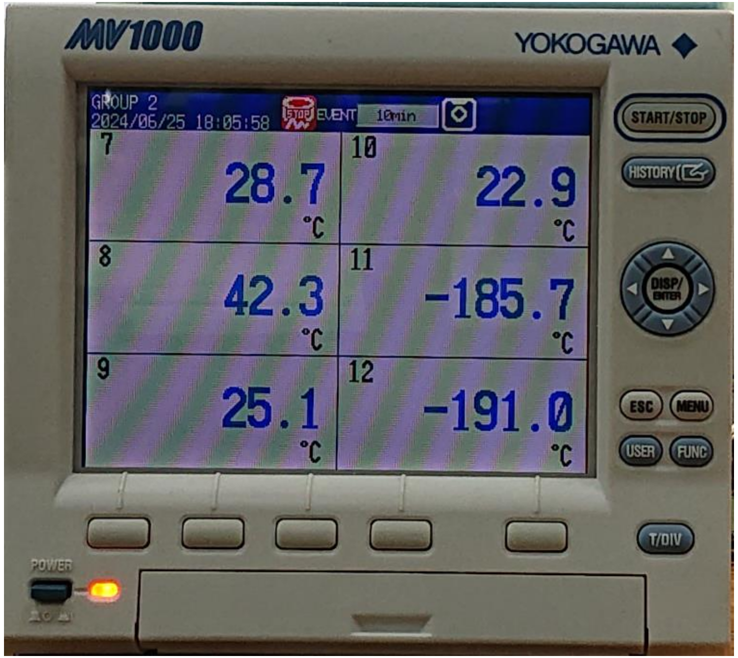


Channel No.	Component
1	L1
2	L2
3	Q4
4	T1
5	D2
6	Q6
7	Q7
8	Low Side Copper
9	High Side Copper

8. Test Results (cont.)

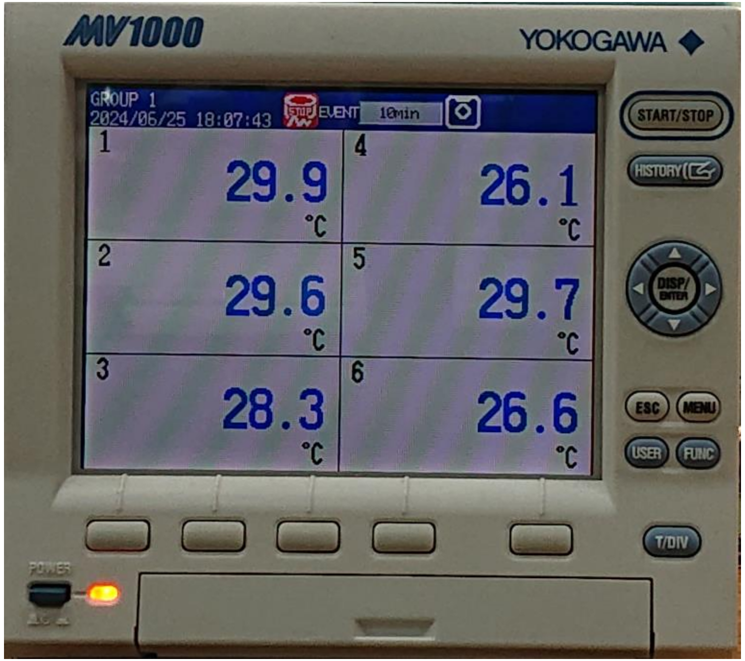
Temperature Probing (200W)

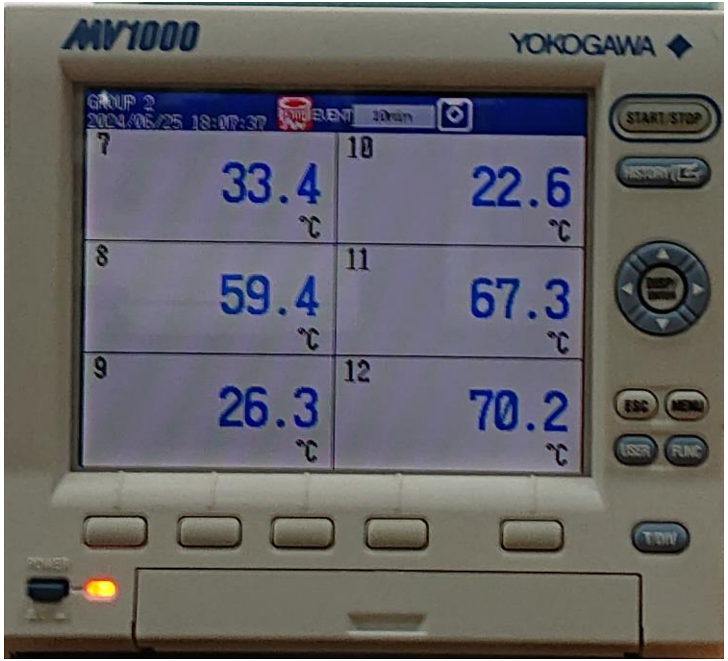




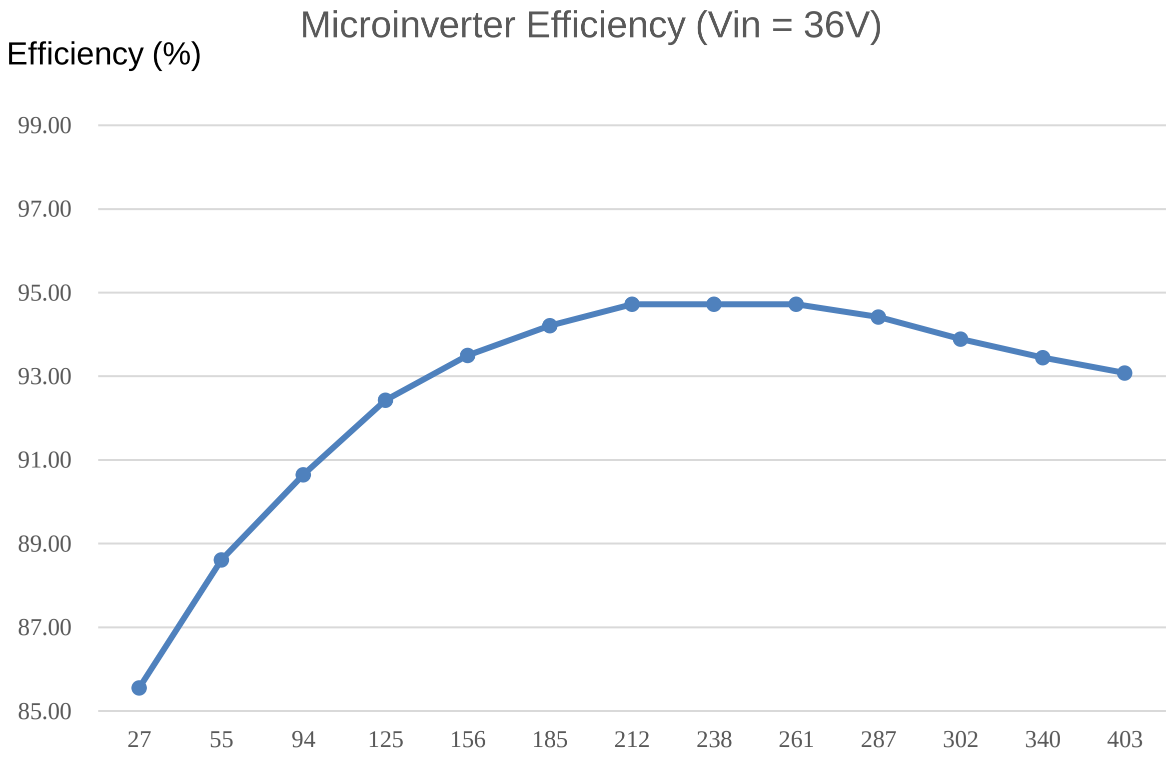
8. Test Results (cont.)

Temperature Probing (403W)



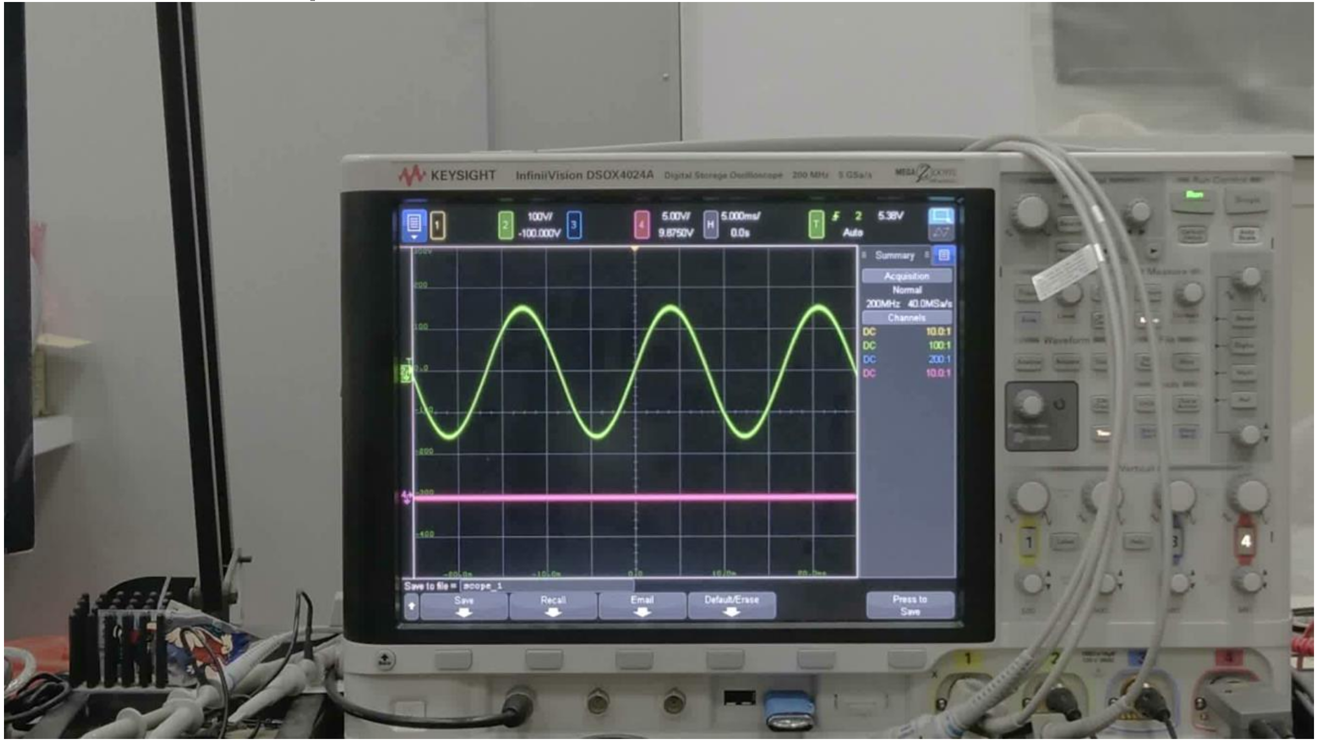


8. Test Results (cont.)



8. Test Results (cont.)

1. Grid-connected (DC source)
   0A~12A@36V input



9. Release Package

1. Schematic
2. BOM
3. Gerber File
4. SMD Pick-place Table
5. Firmware (Source Code)

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Thank you

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