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50 kW Digital DC-AC Inverter Based on SiC ACEPACK and STM32H743

Rain XU

Power & Energy
Competence
Center



Agenda

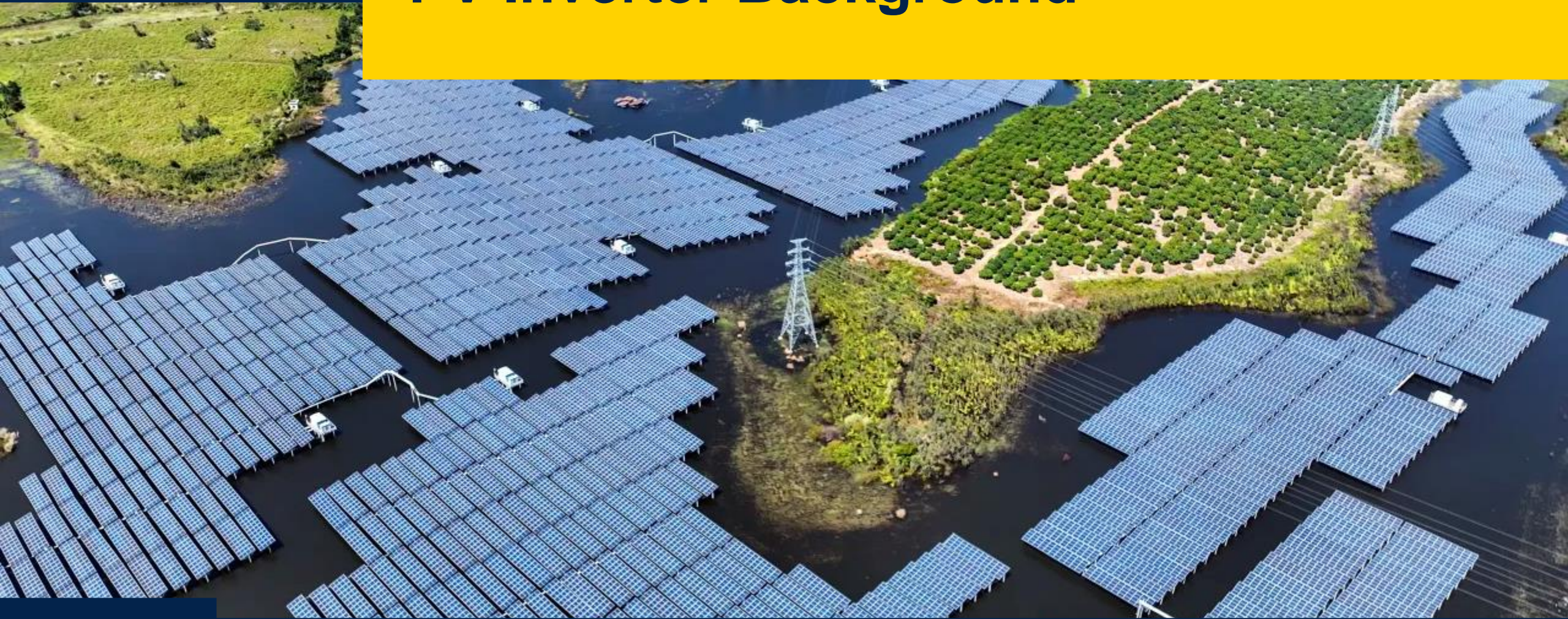
1 PV Inverter Background

2 ST PV Digital Solution

3 ST PV Board Performance

4 Summary

PV Inverter Background





PV inverters

Residential installations

Typically <5 kW



Commercial and industrial buildings

5 kW-1 MW



Ground-mounted power plants

1-100 MW

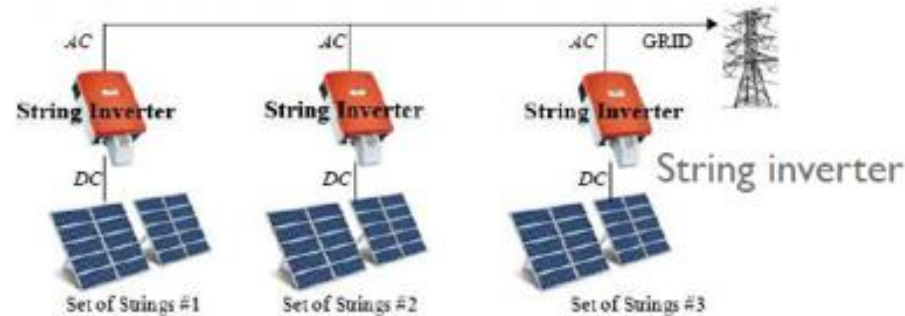


PV inverters

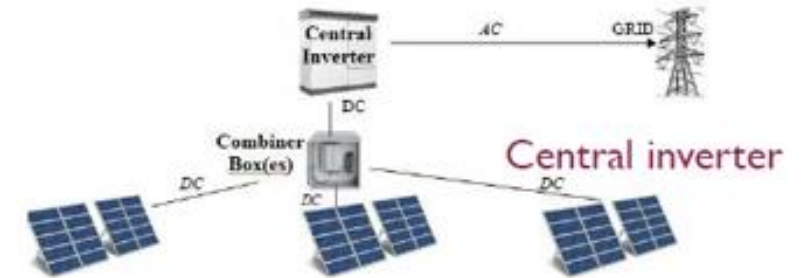


Micro-inverter

Micro-inverters are used for low-power installations up to 300W. The input voltage is generally 48V or 62V.



Single-phase or three-phase string inverters are used for residential and commercial PV installations up to 120kW.



Central PV inverters are used in installations supplying beyond 200kW.



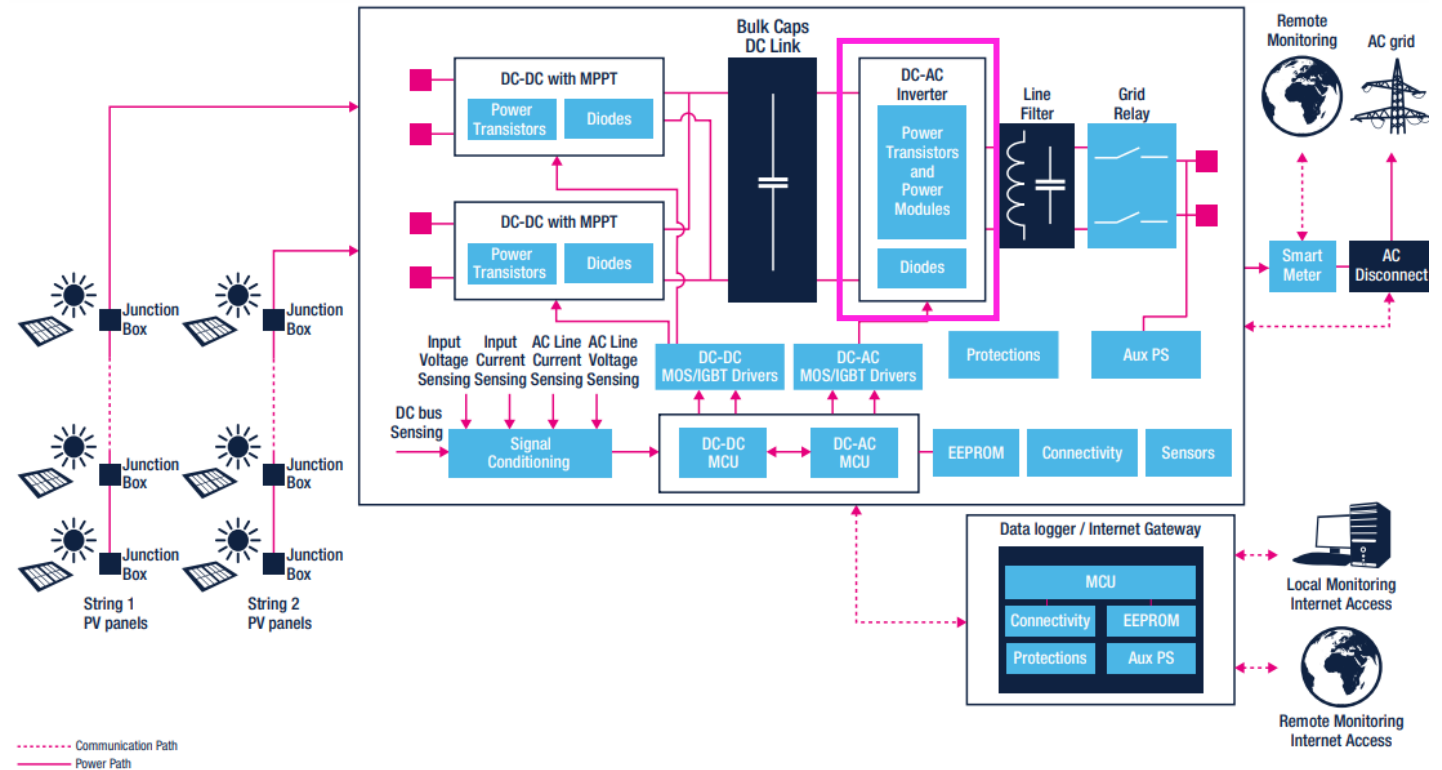
String inverters

Input specs and requirements

Input voltage	200-1100 Vdc
Normal voltage	600 Vdc
Input current	120 A max@450 V
MPPT voltage	200-1000 Vdc
MPPT number	4

Output specs and requirements

Output voltage	312~480 V L-L
Frequency	50 Hz / 45~55 Hz
Output power	50 kW normal (55 kW max)
Thd	< 3 %
Power factor	0.8 ~ -0.8
Eff	98.5%



Benefits of SiC

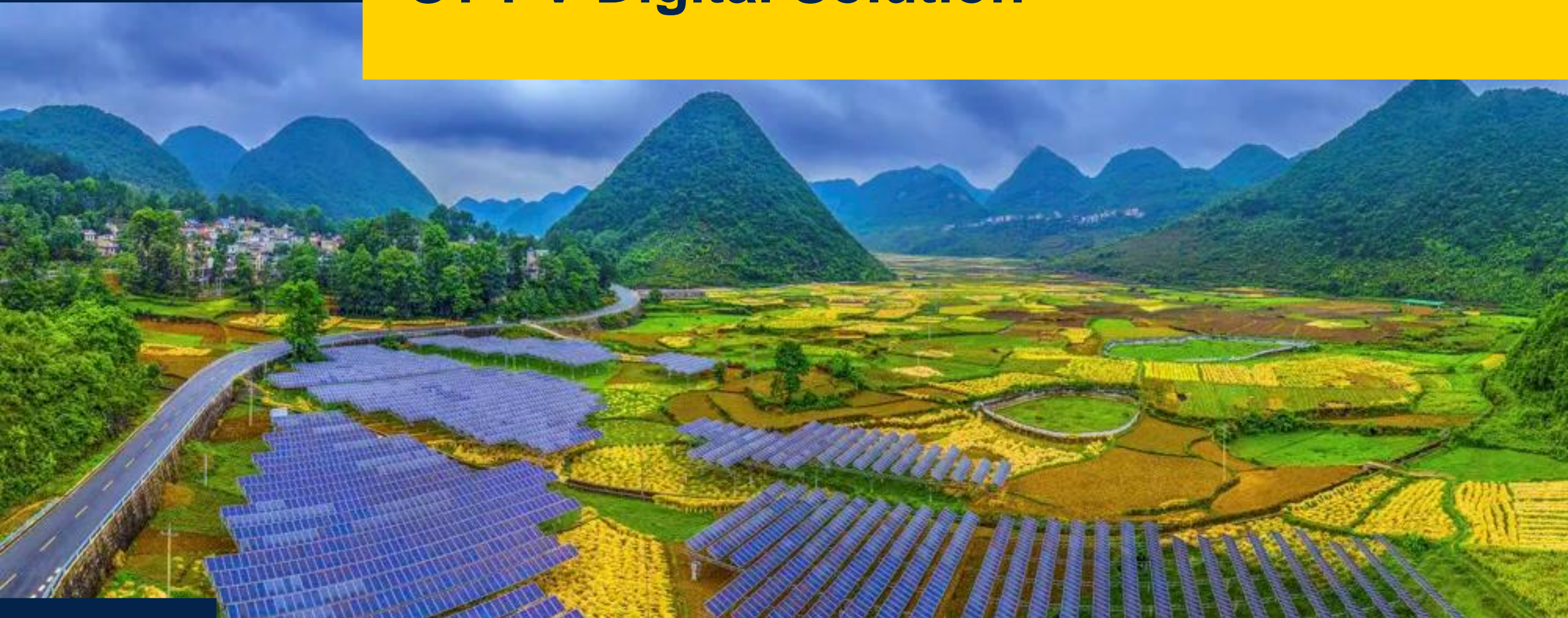
Extremely low switching losses and ultralow $R_{DS(on)}$

Good thermal performance

Easy to drive

Very fast and robust intrinsic body diode

ST PV Digital Solution



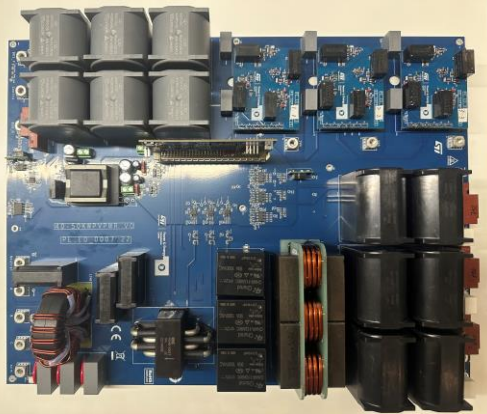
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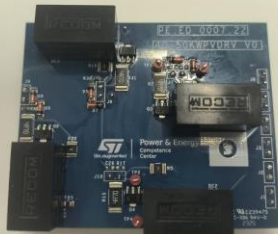
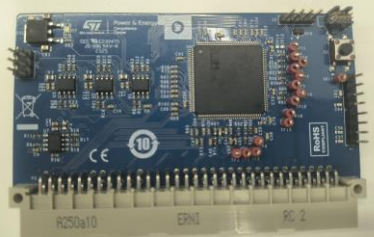
50 kW T-type DC-AC PV Inverter



Solution board
available



T type three-level DC-AC with ACEPACK module



Application key features:

- DC input voltage 800 VDC, rated output power 50 kW · switching frequency 40 kHz
- Output AC voltage: Three-phase 380 VAC with 45 Hz up to 55 Hz
- Maximum output current: 84 ARMS
- Peak efficiency 98.89% (800Vdc)
- 0.99 power factor with lower than 3% THD @ full load operation
- STM32H743ZGT6

Key products

STM32H743ZGT6
A2U8M12W3-FC *3 (9.5mΩ 1200 V & 6mΩ 750 V SiC module)
STGAP2SICSC (galvanic insulated gate driver)
IPC product: L6565, ISOSD61, (L6983i)
Schottky diodes: STPS1150A, STPS2H100A, STPS2L60A
GPA : TSV914IDT, LD29080S33R, STLM20W87F, LD29080DT50R

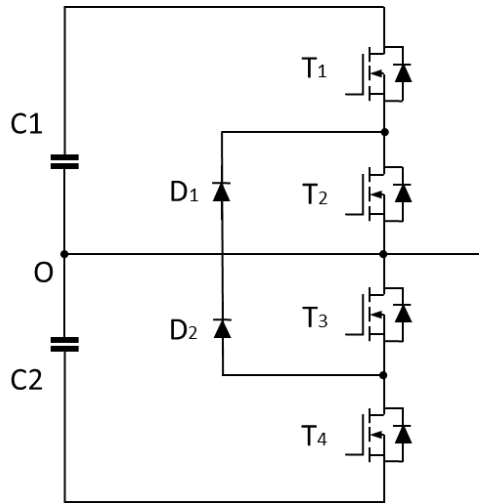
Key benefits

- Higher efficiency achieved based SiC module
- Low output LCL filter cost with 40 kHz frequency
- Higher reliability, low design complexity



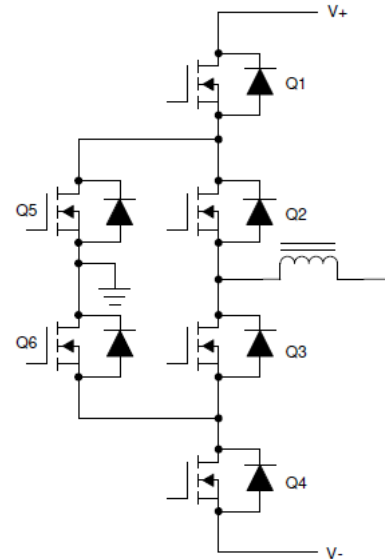
Topology Comparison

INPC



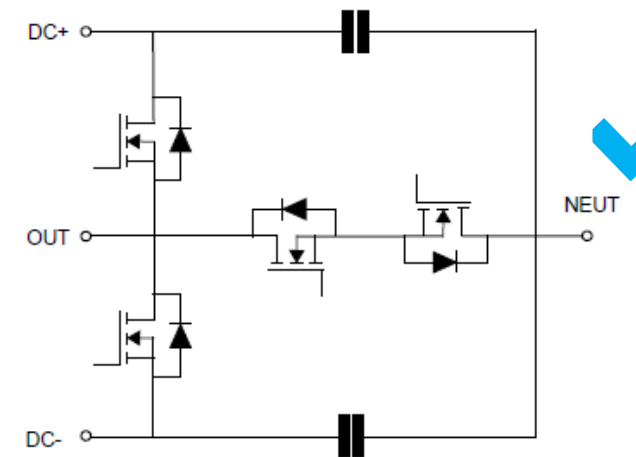
- + Suitable for high bus voltage
- + 3-level topology
- Shoot-through issue
- Control complexity: medium-high
- Component count: high
- 2 devices in the main current path

ANPC



- + Suitable for high bus voltage
- + Better for thermal
- + 3-level topology
- Shoot-through issue
- Control complexity: high
- Component count: high
- 2 devices in the main current path

TNPC

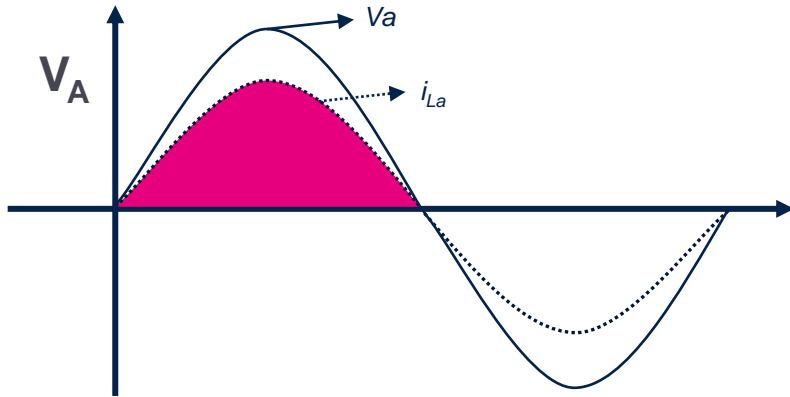


- + Component count: low
- + 2 device in the main current path
- + 3-level topology
- Shoot-through issue
- Control complexity: medium-high
- Suitable for bus voltage ≤ 850 V

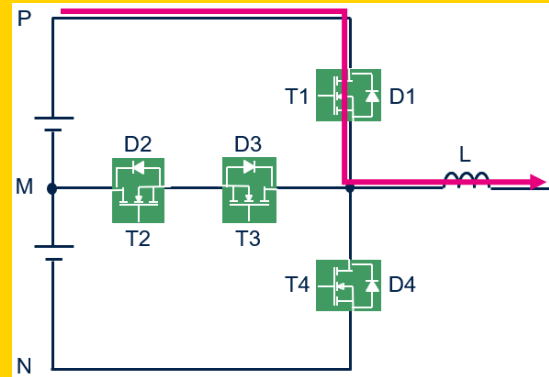


T-type Three Phase Operation SiC MOS

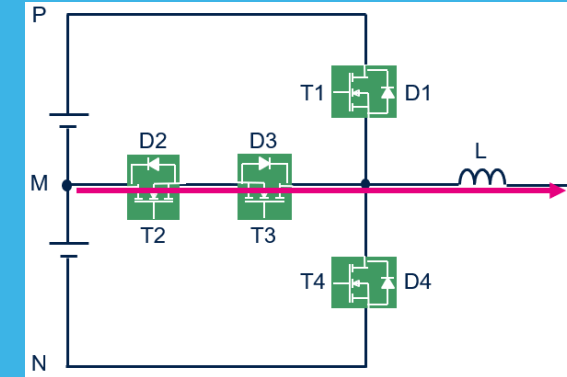
$V_a > 0, i_{La} > 0$



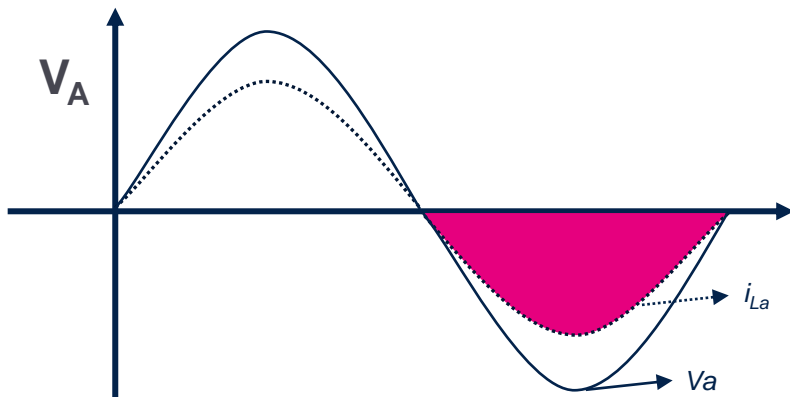
T1 on (=1), energy releasing



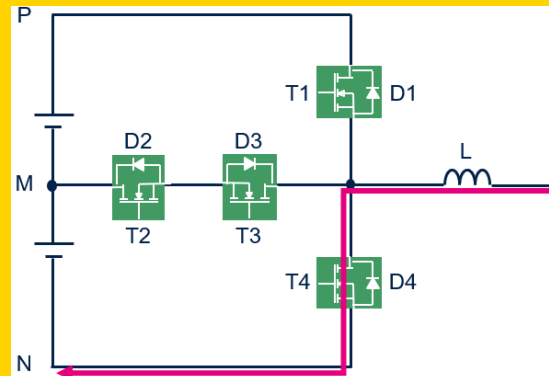
T3 on (=1), energy releasing



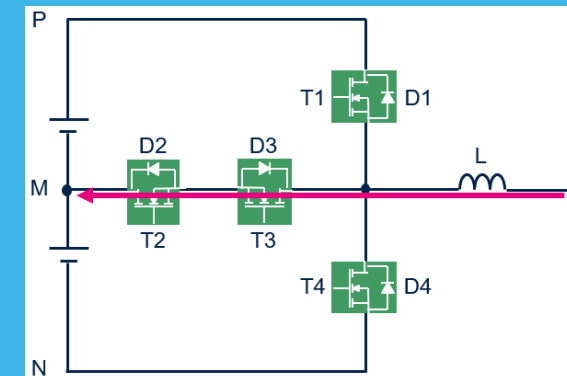
$V_a < 0, i_{La} < 0$



T4 on (=1), energy releasing



T2 on (=1), energy releasing



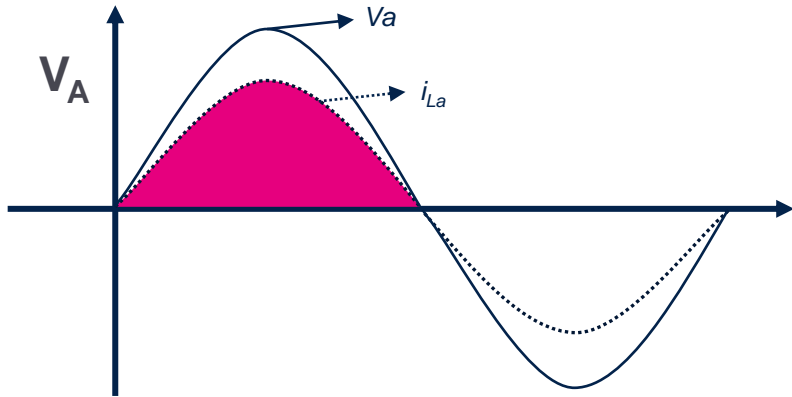
- Current from BUS CAP to inductor through MOS T1 or T4
- Energy from BUS CAP to inductor and output

- Current from output to M-point and inductor through MOS T2 and T3
- Energy from output to M-point and inductor

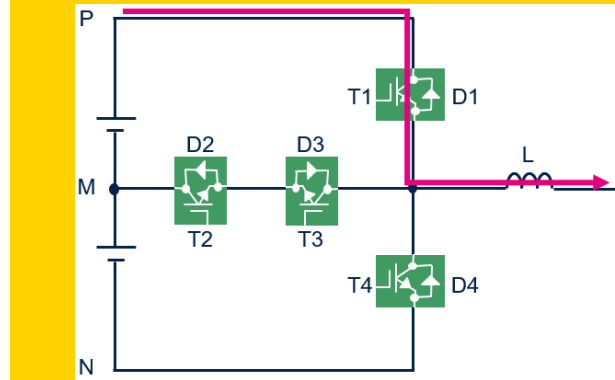


T-type Three Phase Operation Si IGBT

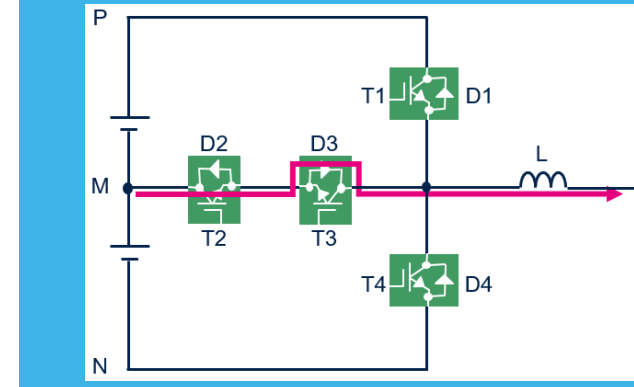
$V_a > 0, i_{La} > 0$



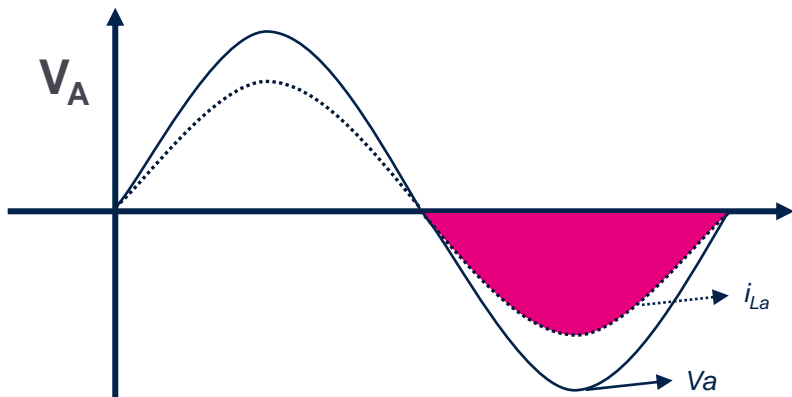
T1 on (=1), energy releasing



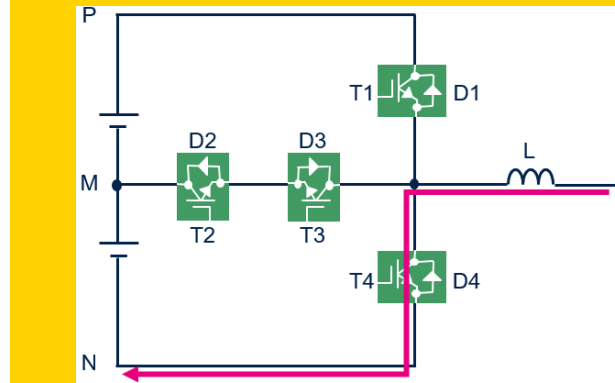
T3 on (=1), energy releasing



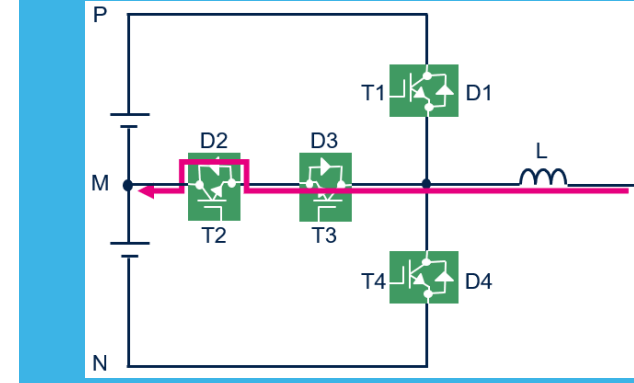
$V_a < 0, i_{La} < 0$



T4 on (=1), energy releasing



T2 on (=1), energy releasing



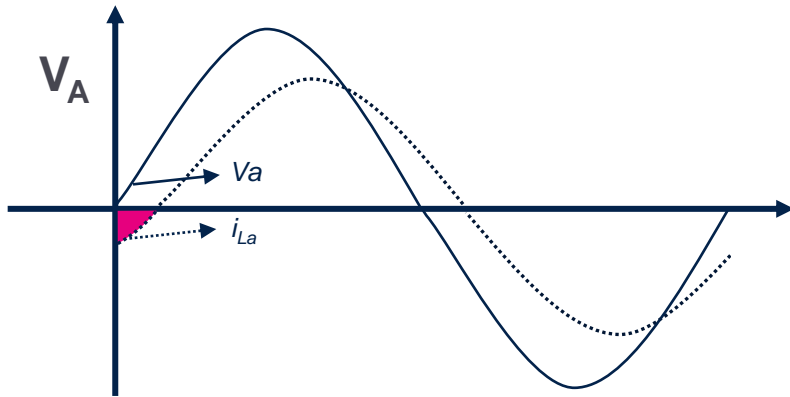
- Current from BUS CAP to inductor through MOS T1 or T4
- Energy from BUS CAP to inductor and output

- Current from output to M-point and inductor through MOS T2&Diode D3 or MOS T3&Diode D2
- Energy from output to M-point and inductor

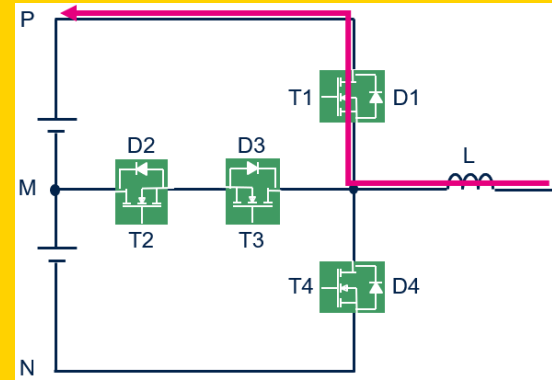


T-type Three Phase Operation SiC MOS

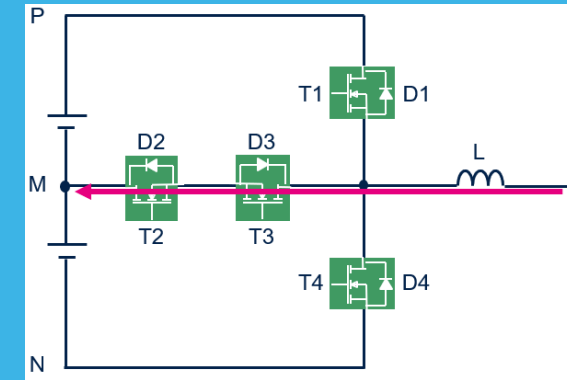
$V_a > 0, i_{La} < 0$



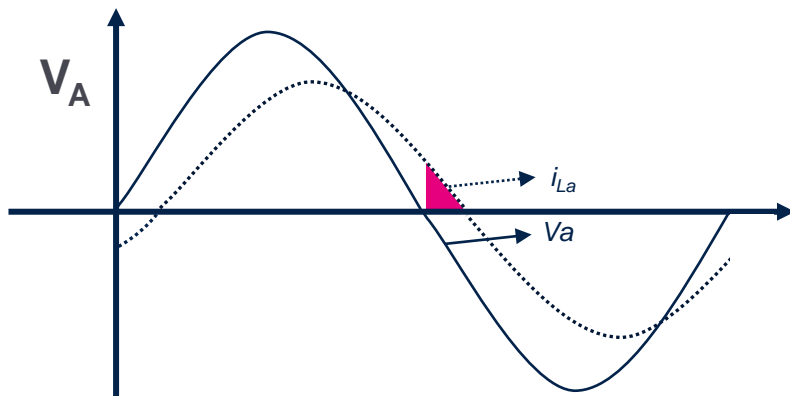
T1 on (=1), energy releasing



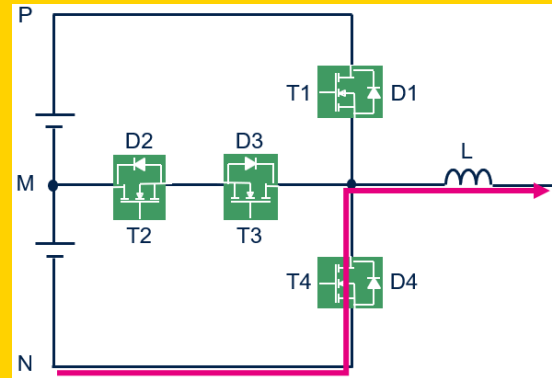
T3 on (=1), energy releasing



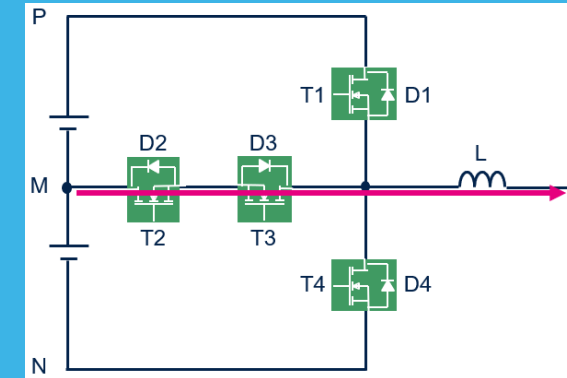
$V_a < 0, i_{La} > 0$



T4 on (=1), energy releasing



T2 on (=1), energy releasing



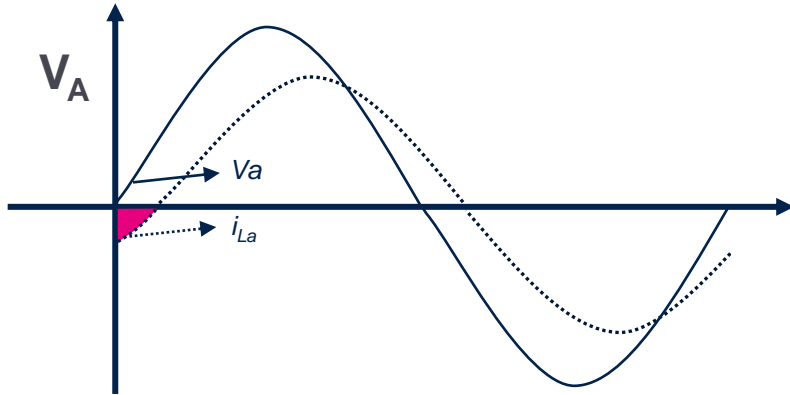
- Current from inductor to BUS CAP through MOS T1 or T4
- Energy from output and inductor to BUS CAP

- Current from output to M-point and inductor through MOS T2 and T3
- Energy from output to M-point and inductor

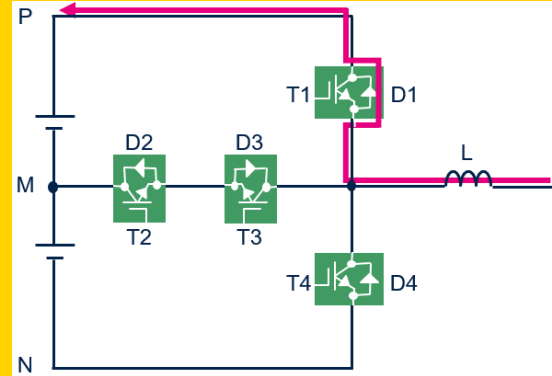


T-type Three Phase Operation Si IGBT

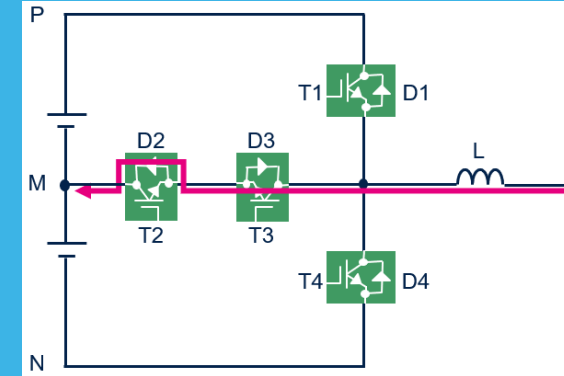
$V_a > 0, i_{La} < 0$



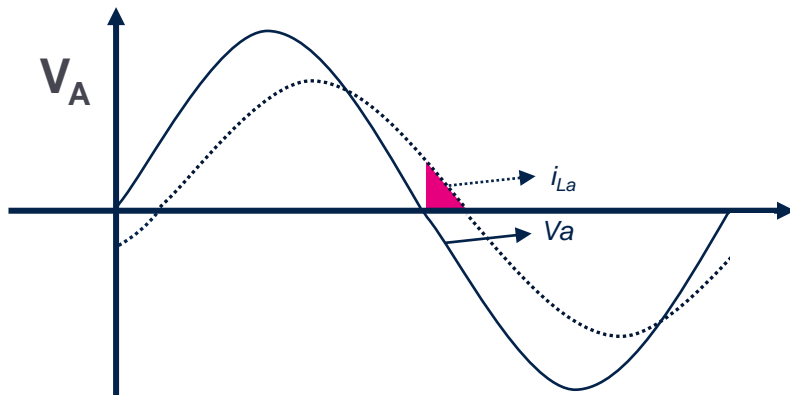
T1 on (=1), energy releasing



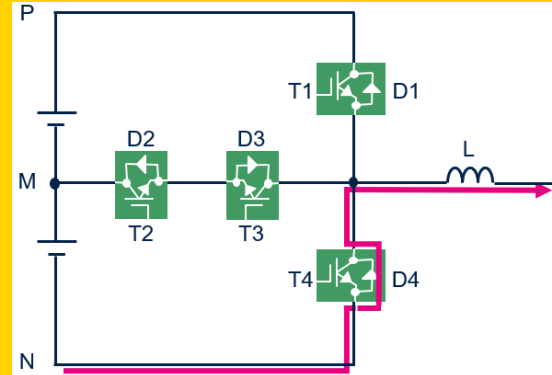
T3 on (=1), energy releasing



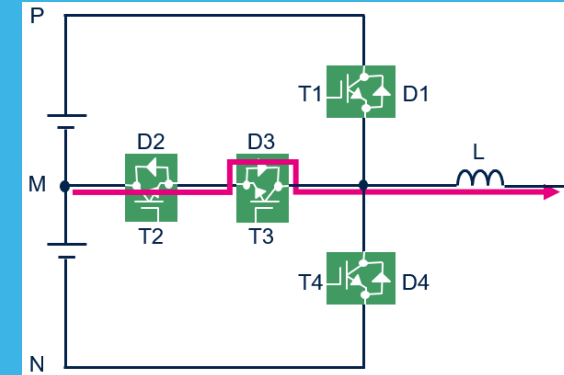
$V_a < 0, i_{La} > 0$



T4 on (=1), energy releasing



T2 on (=1), energy releasing



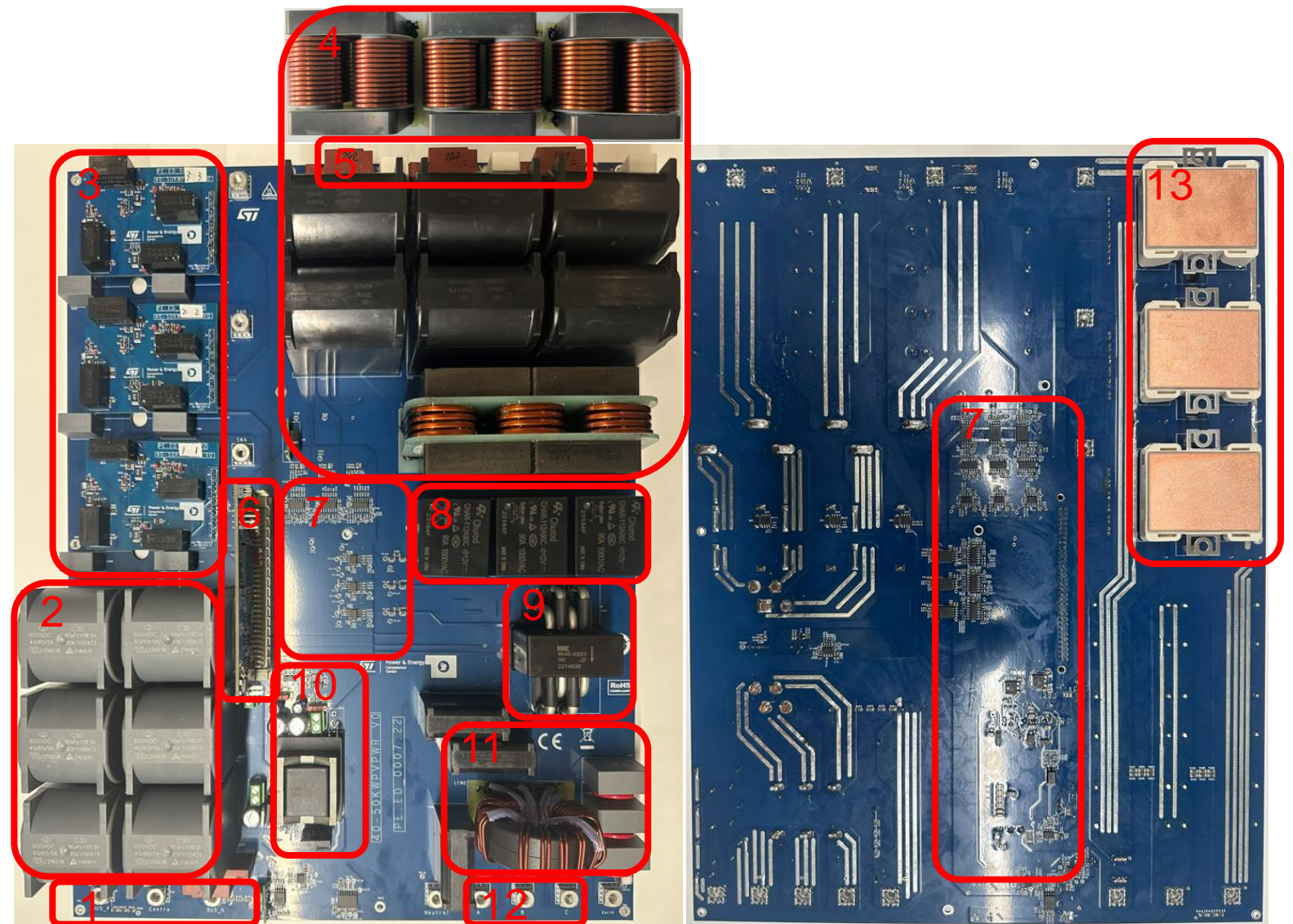
- Current from inductor to BUS CAP through diode D1 or D4
- Energy from output and inductor to BUS CAP

- Current from output to M-point and inductor through MOS T3&Diode D2 or MOS T2&Diode D3
- Energy from output to M-point and inductor



Board Assembly Overview

1. DC input connector
2. BUS CAP
3. Driver board
4. LCL filter
5. Inductor current sensor
6. Control board
7. Sensing circuit
8. Relay
9. Residual current sensor
10. Aux power circuit
11. EMI filter
12. AC output connector
13. SiC module

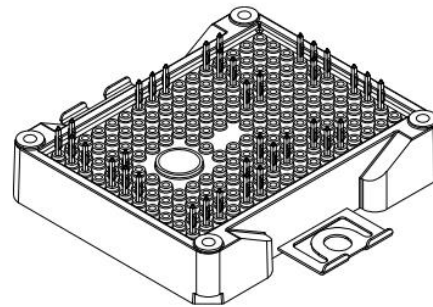


WxLxH: 300 x 400 x 70 mm

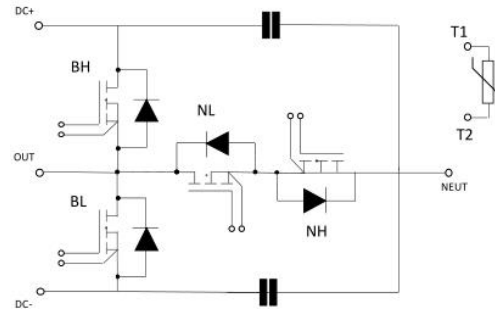


SiC Module-A2U8M12W3

ACEPACK 2 power module, 3-level topology based on silicon carbide power MOSFETs: 750 V & 1200 V, 100 A



ACEPACK 2



Features

- ACEPACK 2 power module:
 - NH and NL: 750 V 6 mΩ of typical $R_{DS(on)}$ each switch
 - BH and BL: 1200 V 9.5 mΩ of typical $R_{DS(on)}$ each switch
 - 2.5 kVrms insulation
 - Integrated NTC temperature sensor
 - DC link capacitors between DC BUS and neutral
 - AIN DBC improved thermal performance
 - Press-fit contact pins

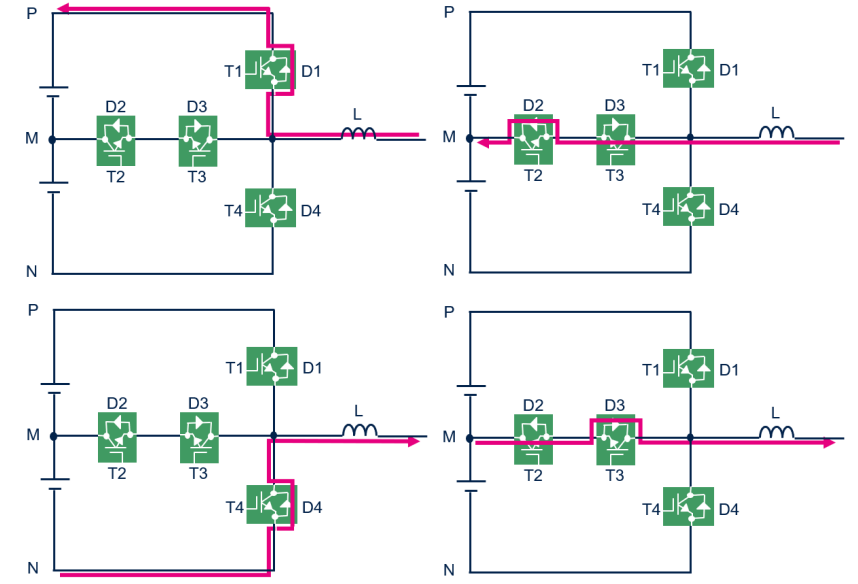
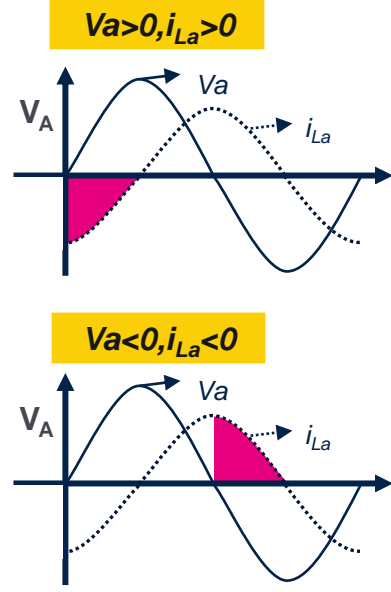
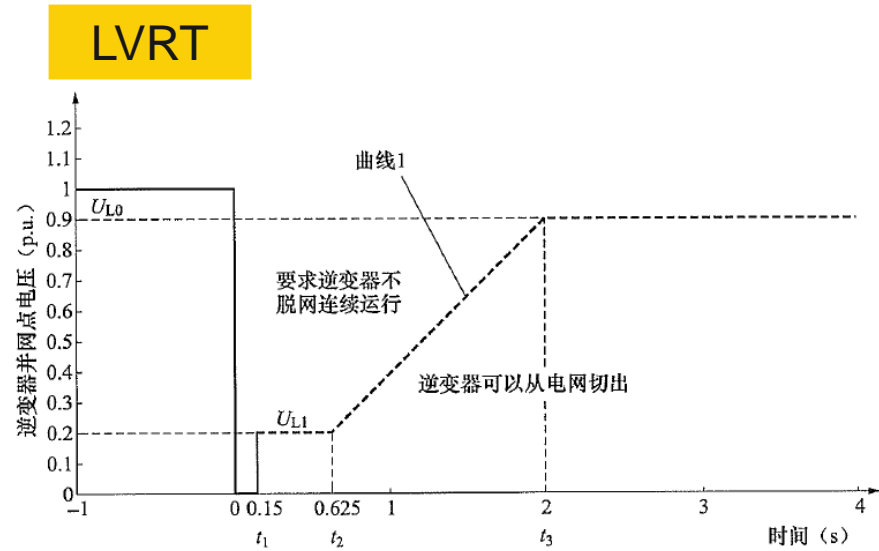
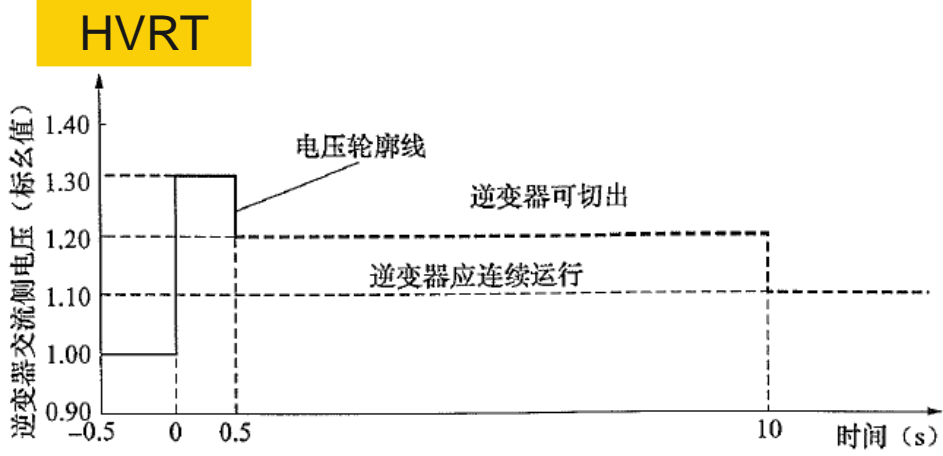
Application

- DC-DC converters



SiC Module-A2U8M12W3

Operation

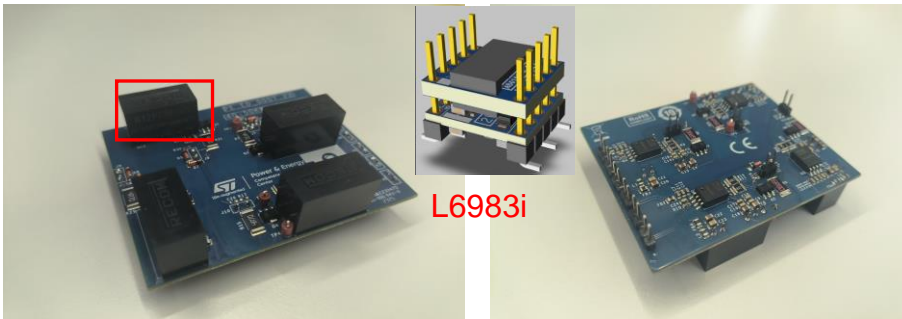


Three-phase symmetrical LVRT or HVRT fault:

$$I_{qmax} \leq 1.05 * I_{rated} = 79.8A$$

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	$V_{GS} = -5 V, I_{SD} = 100 A$	-	5.2	-	V
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	$V_{GS} = -5 V, I_{SD} = 100 A$	-	4.15	-	V

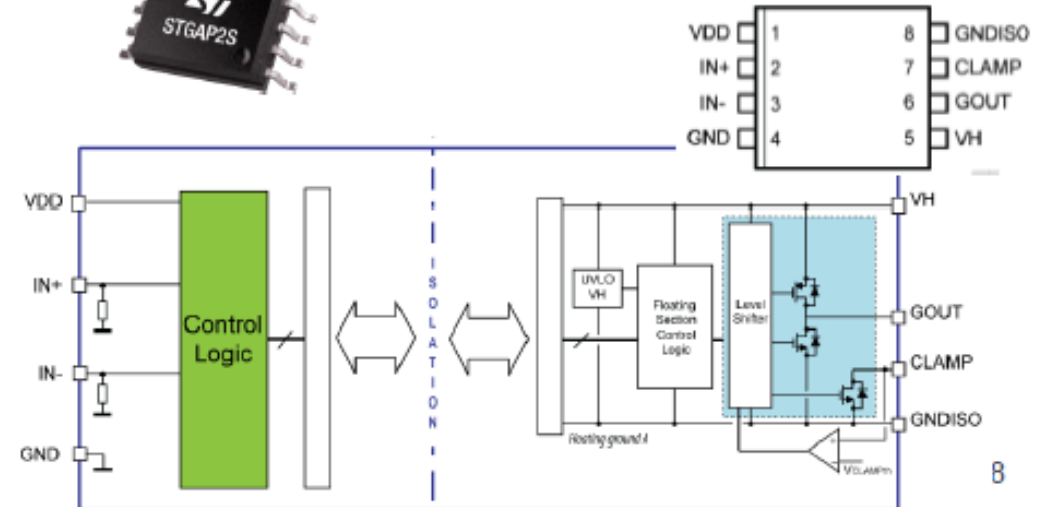
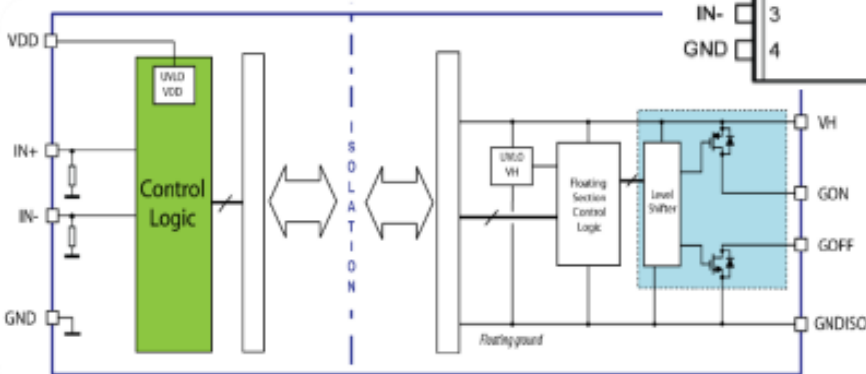
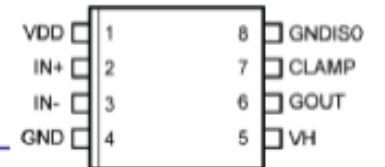
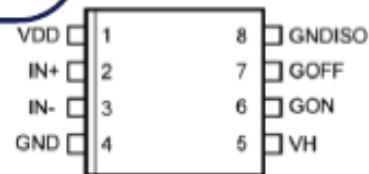
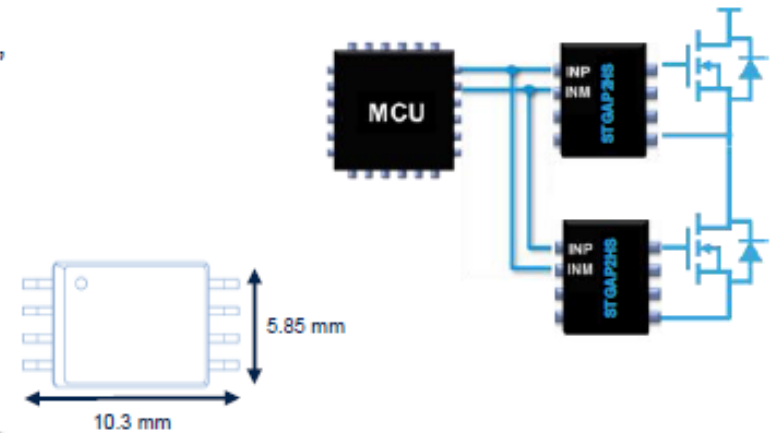
STGAP2 Wide Galvanic Isolation



6 kV_{pk} galvanic isolation – 4A single gate drivers

- 3V3 / 5 V logic inputs (logic thresholds 1/3, 2/3 of VDD)
- Up to 26 V supply voltage
- 4 A Sink/Source current capability
- Short propagation delay: 75 ns
- UVLO Function (Si MOS-IGBT & SiC options)
- Stand-by function
- 100 V/ns CMTI
- High voltage rail up to 1200 V
- Thermal shut-down protection

- Active High & Active Low input pins, for HW interlocking
- **STGAP2HSM, STGAP2SICS:** Separated Outputs option for easy gate driving tuning
- **STGAP2SHSCM, STGAP2SICSC:** Miller CLAMP pin option to avoid induced turn-on
- SO-8W Package (Wide Body)

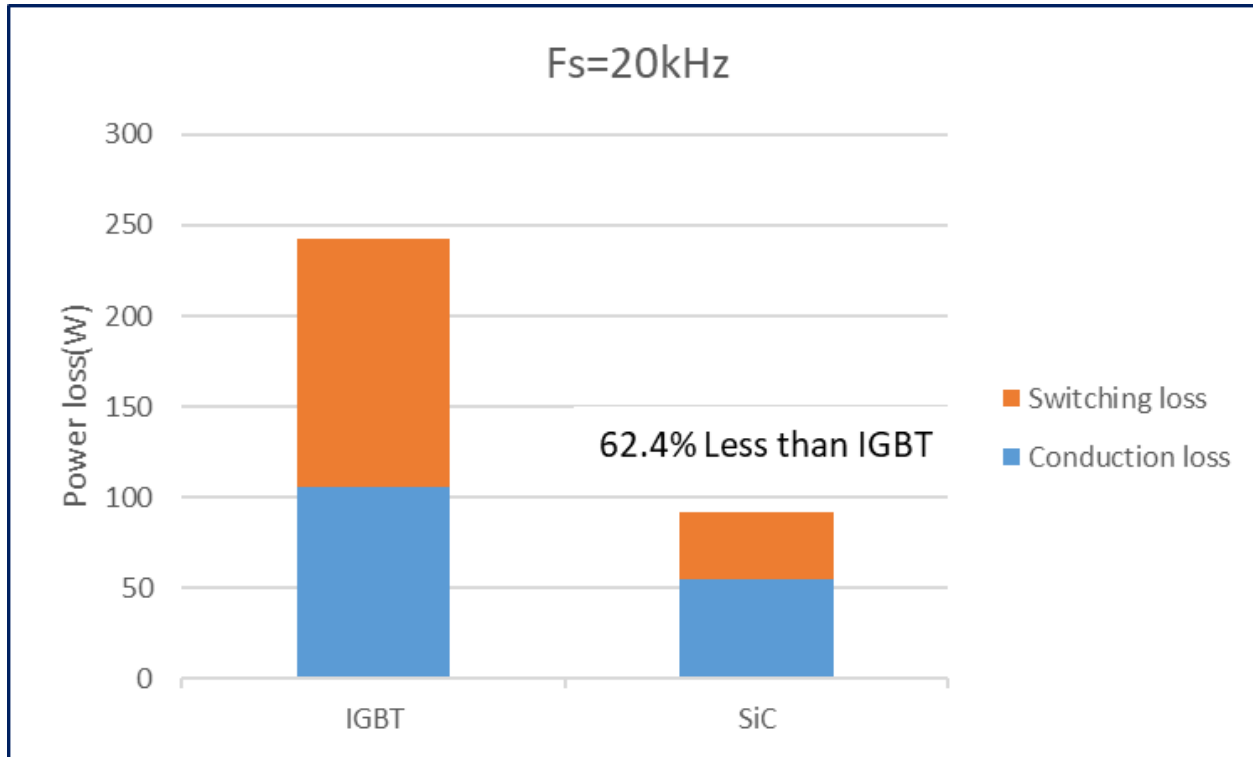




Power Loss Contrast At Full Load

F_{sw}=40 kHz, P_o=50 kW

SW type	fs(kHz)	P _{conduction} (W)				P _{sw} (W)						Eff(%)
		P _{cond} (T1+T4)	P _{cond} (T2+T3)	P _{cond} (D1+D4)	P _{cond} (D2+D3)	P _{on} (T1+T4)	P _{off} (T1+T4)	P _{on} (T2+T3)	P _{off} (T2+T3)	P _{rec} (D1+D4)	P _{rec} (D2+D3)	
ST SiC	40	31.015	24.136	0	0	37.226	13.314	0	10.577	0	11.28	98.72%
ST SiC	20	31.015	24.136	0	0	18.613	6.657	0	5.288	0	5.64	98.94%
IGBT	40	47.613	26.693	0	30.854	115.39	119.16	0	0	0	40.9	97.26%
IGBT	20	47.613	26.693	0	30.854	57.7	59.588	0	0	0	20.451	98.05%



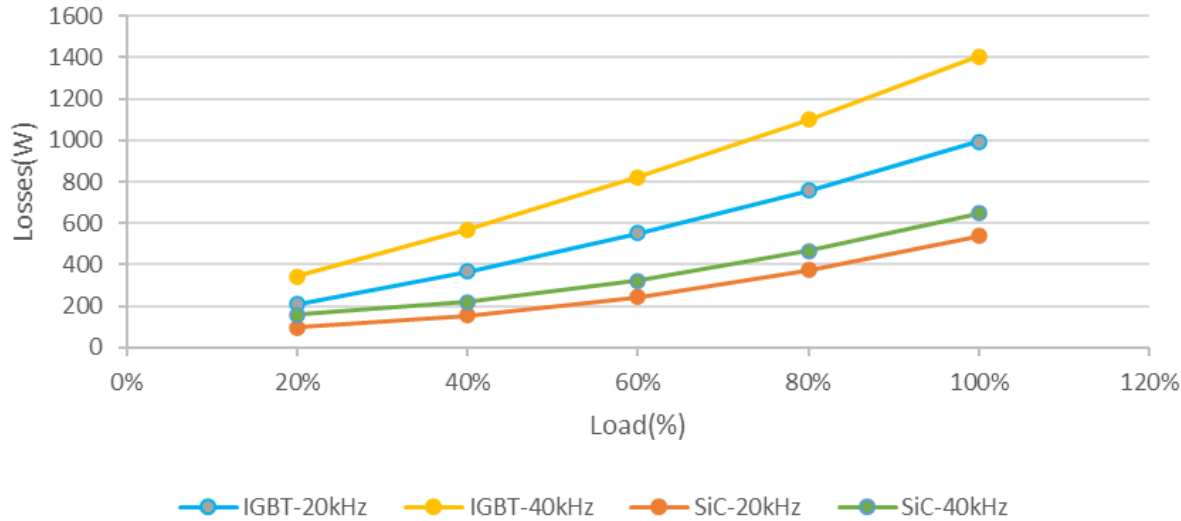
Type	IGBT	SiC	%
Conduction loss	105.1653	55.151	52.44%
Switching loss	137.739	36.198	26.28%

Lower conduction loss → 47.56% less
 Lower switching loss → 73.72% less

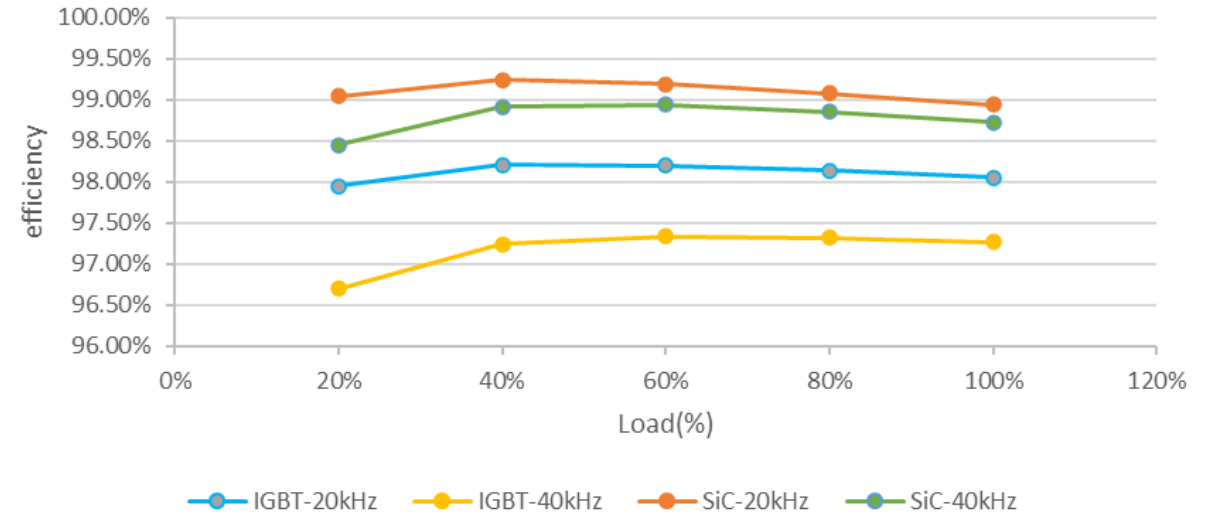


SiC: Lower Losses, Higher Efficiency

Inverter losses vs %load



Inverter efficiency vs %load



SiC MOSFET module shows lower loss over the whole load range

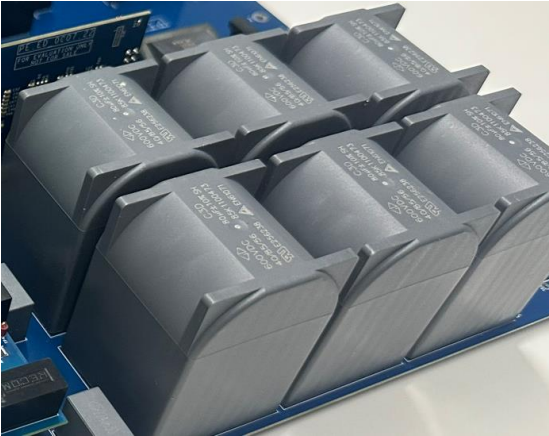
SiC MOSFET module shows higher efficiency over the whole load range

Lower losses mean smaller cooling system and high efficiency mean better performance



BUS CAP & LCL Filter Optimization

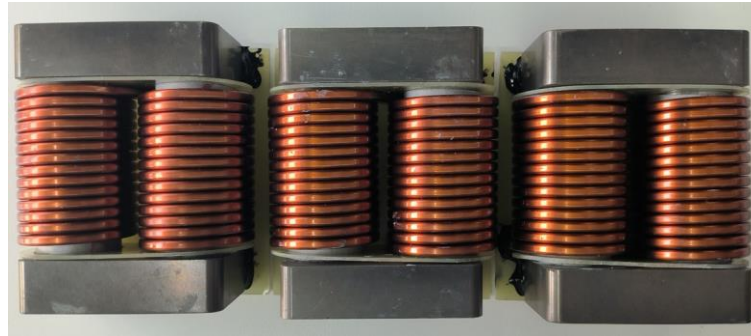
BUS CAP



- + Higher frequency
- + Lower capacitance

120 μF

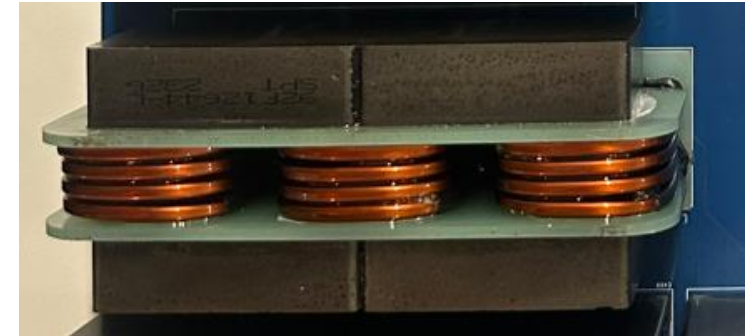
Inverter inductor L_f



- + Higher frequency
- + Lower inductance

80 μH

Grid inductor L_g



- + Higher frequency
- + Lower inductance

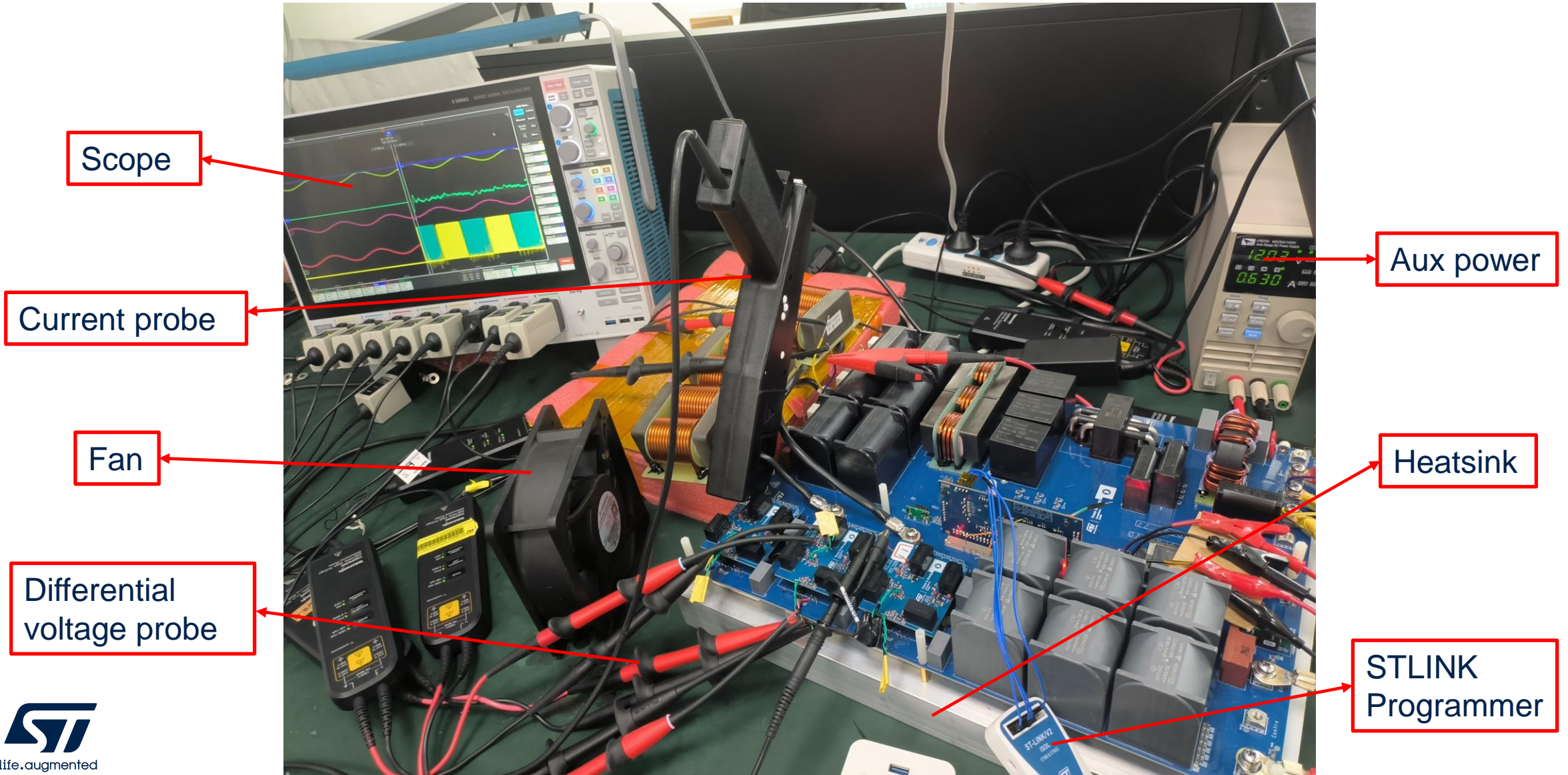
6 μH

ST PV Board Performance





50 kW PV Test Platform



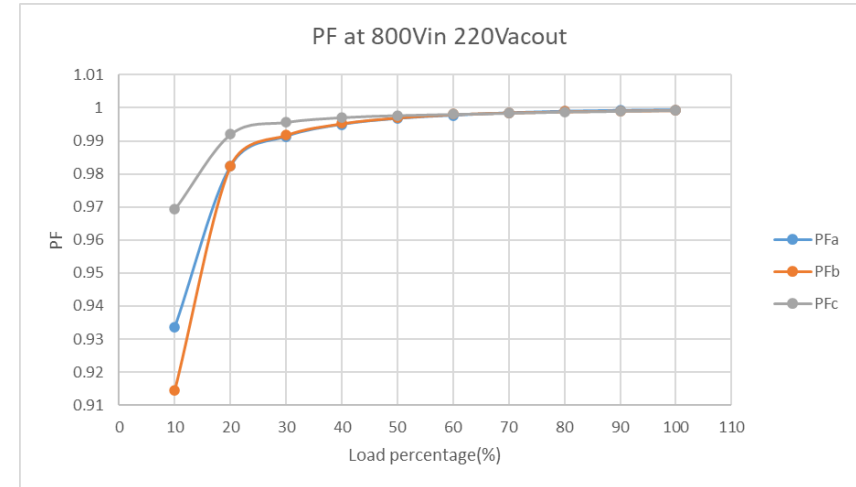


Efficiency, Power Factor & Harmonics

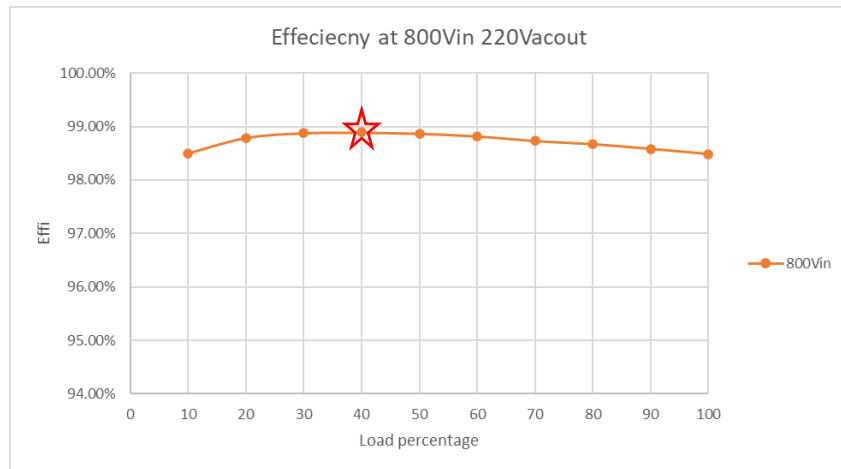
800Vin 220Vacout

Load %	Effe	PF			thd		
		A	B	C	A	B	C
10	98.49%	0.93373	0.91461	0.9693	10.53%	15.63%	10.00%
20	98.79%	0.98242	0.98248	0.99199	5.60%	7.52%	4.61%
30	98.88%	0.99134	0.99176	0.99568	3.96%	5.38%	3.42%
40	98.89%	0.99499	0.9953	0.99711	3.12%	4.22%	3.09%
50	98.87%	0.99678	0.99708	0.99772	2.36%	3.35%	3.06%
60	98.82%	0.99772	0.99806	0.99808	2.27%	2.75%	3.07%
70	98.73%	0.99846	0.99858	0.99844	2.16%	2.56%	2.89%
80	98.67%	0.99893	0.99892	0.9988	2.12%	2.45%	2.77%
90	98.58%	0.9992	0.99915	0.99901	1.95%	2.30%	2.72%
100	98.48%	0.99936	0.99929	0.99922	2.03%	2.10%	2.77%

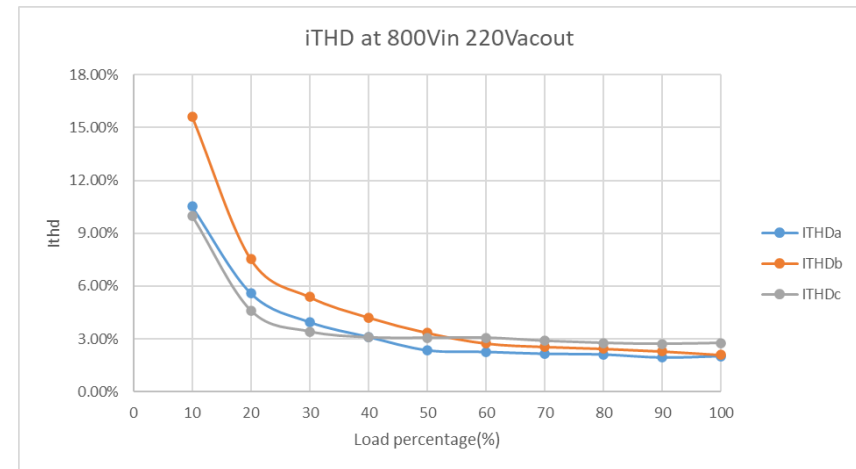
PF at 800Vin 220Vacout



Peak efficiency 98.89% at 800Vin 220Vacout



iTHD < 3% at full load



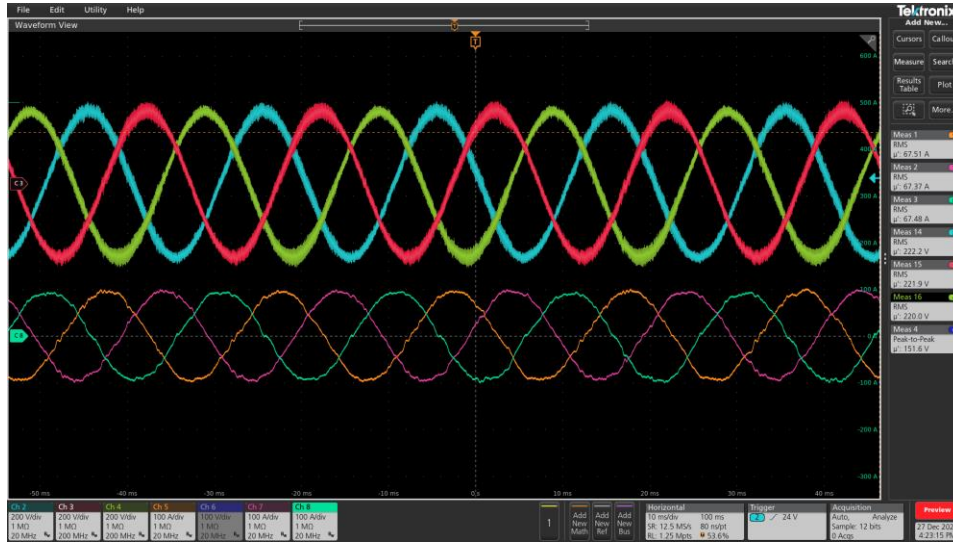


50kW T-type DC/AC PV Inverter PF Range

800Vin 220Vacout 50kw

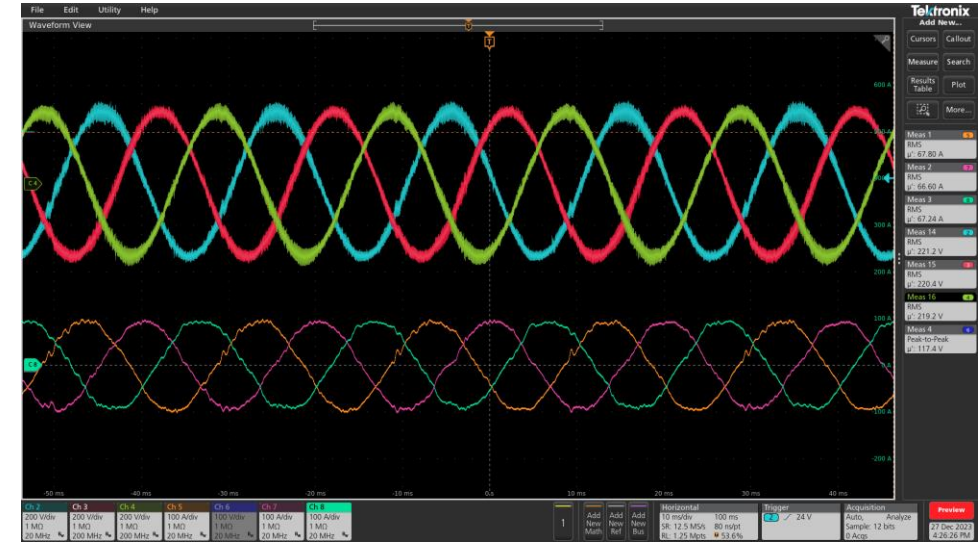
PF=0.8 voltage lead current

VoutA →
VoutB →
VoutC →
IoutA →
IoutB →
IoutC →

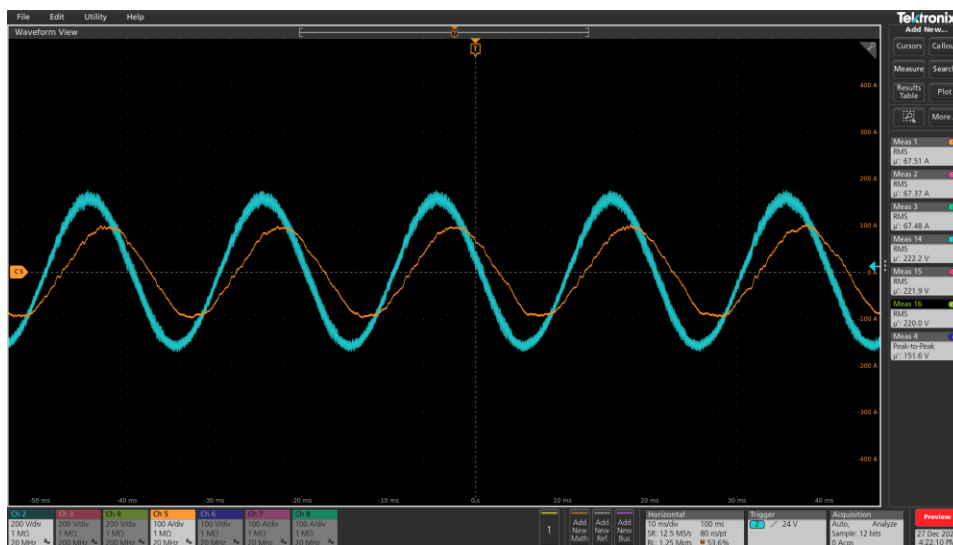


PF=0.8 voltage lag current

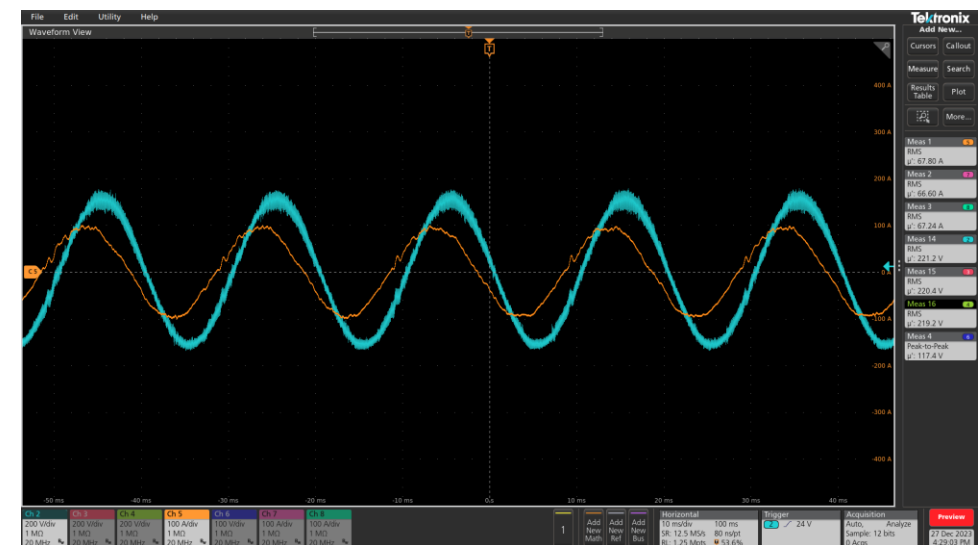
VoutA →
VoutB →
VoutC →
IoutA →
IoutB →
IoutC →



VoutA →
IoutA →



VoutA →
IoutA →



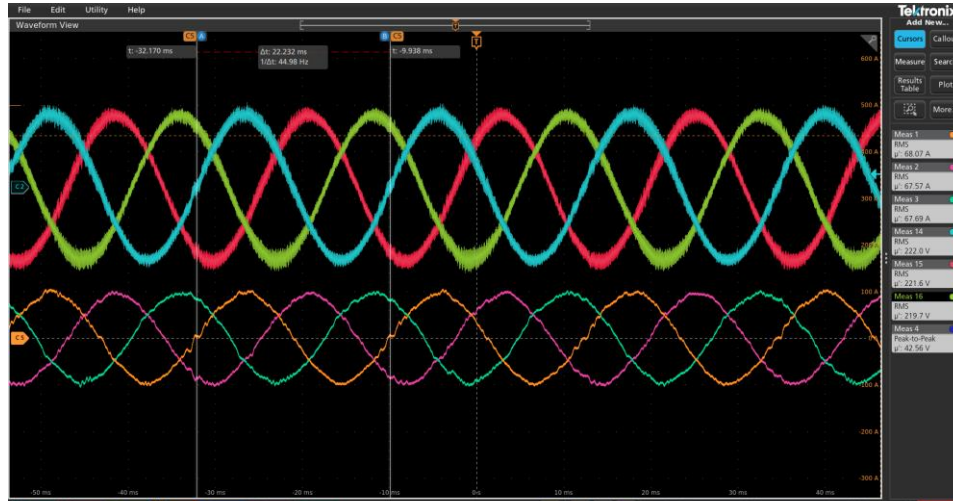


50kW T-type DC/AC PV Inverter Frequency Range

800Vin 220Vacout 50kw

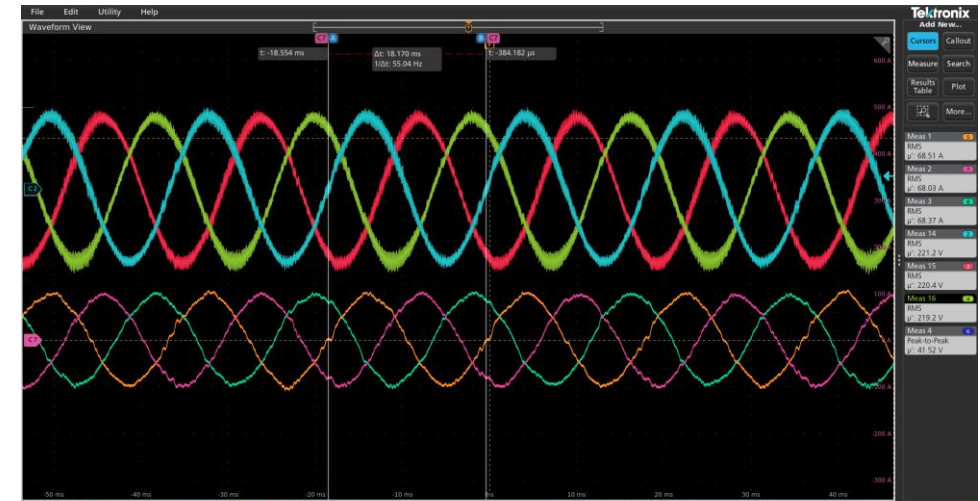
Frequency=45 Hz

VoutA →
VoutB →
VoutC →
IoutA →
IoutB →
IoutC →

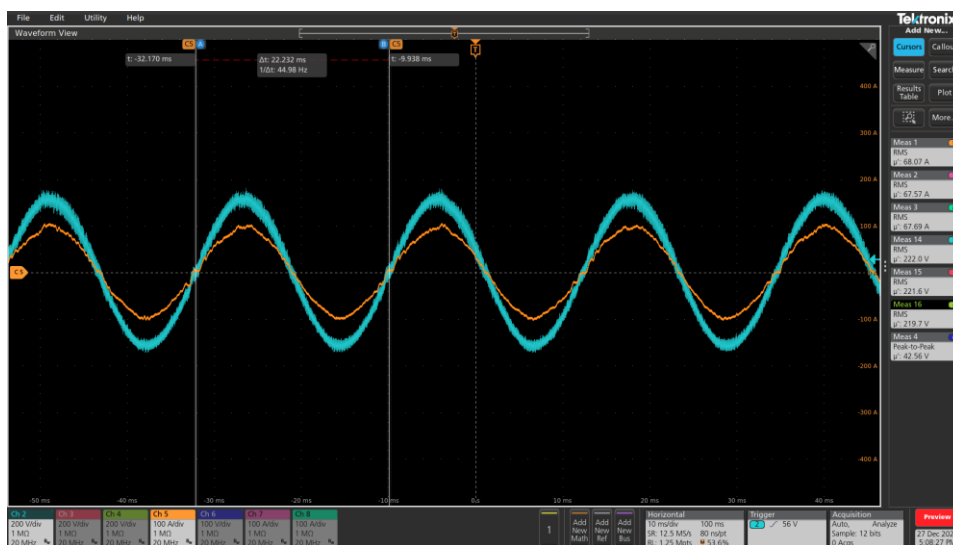


Frequency=55 Hz

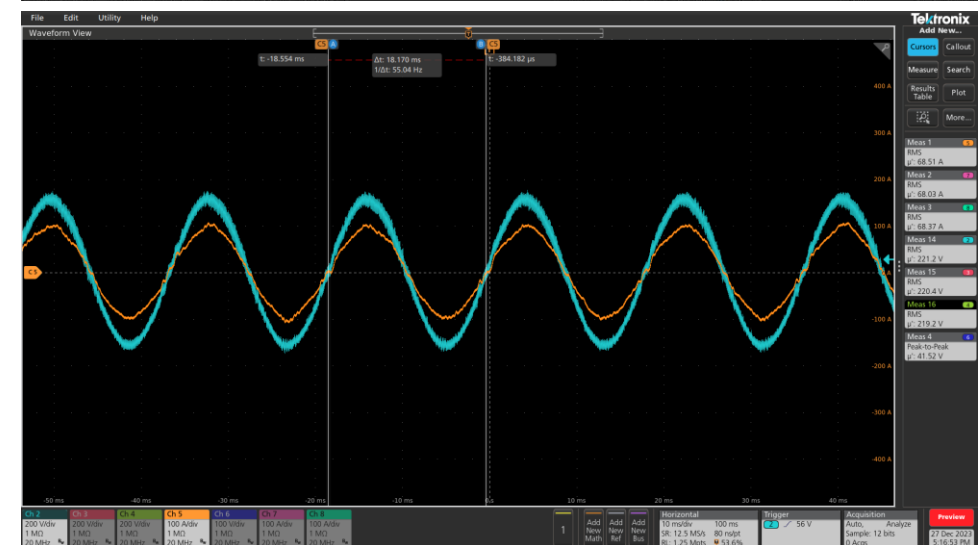
VoutA →
VoutB →
VoutC →
IoutA →
IoutB →
IoutC →



VoutA →
IoutA →



VoutA →
IoutA →



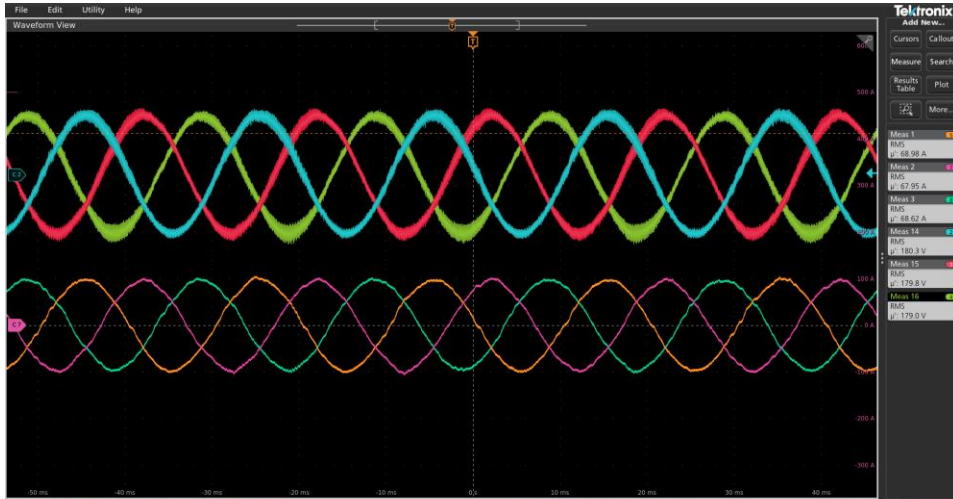


50kW T-type DC/AC PV Inverter Vout Range

800Vin

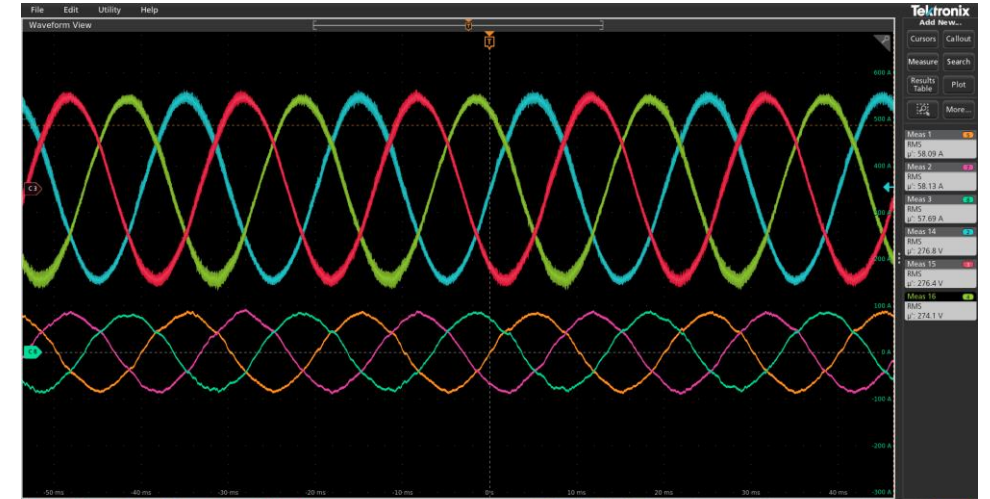
Vout=310 V(L-L)

- VoutA →
- VoutB →
- VoutC →
- IoutA →
- IoutB →
- IoutC →

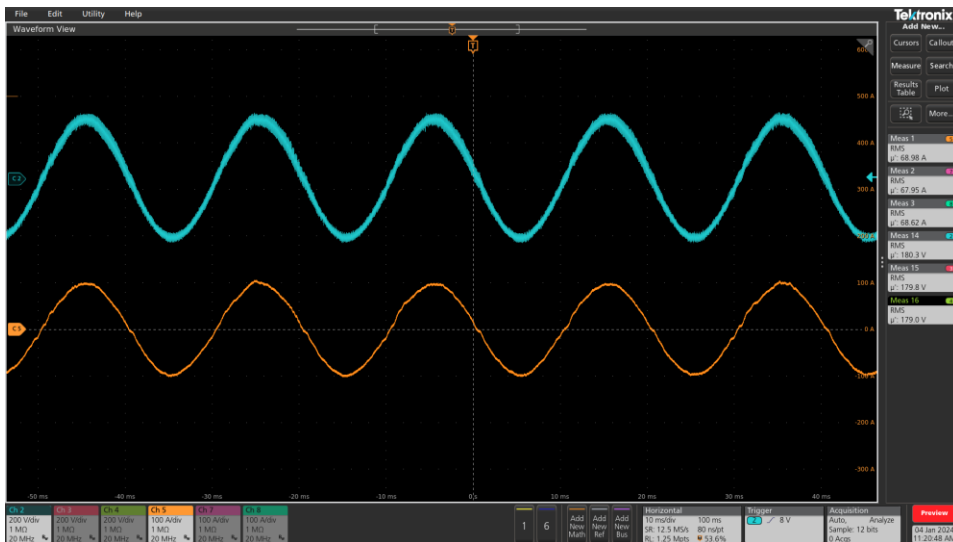


Vout=476 V(L-L)

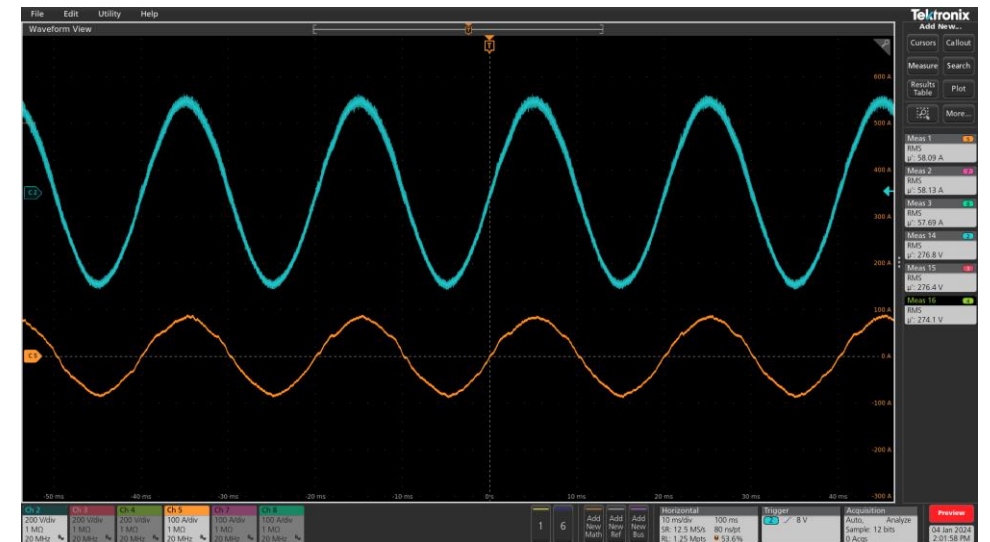
- VoutA →
- VoutB →
- VoutC →
- IoutA →
- IoutB →
- IoutC →



- VoutA →
- IoutA →



- VoutA →
- IoutA →

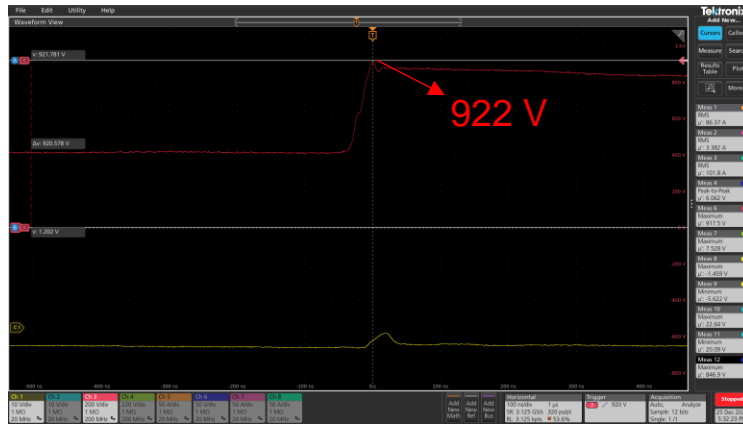




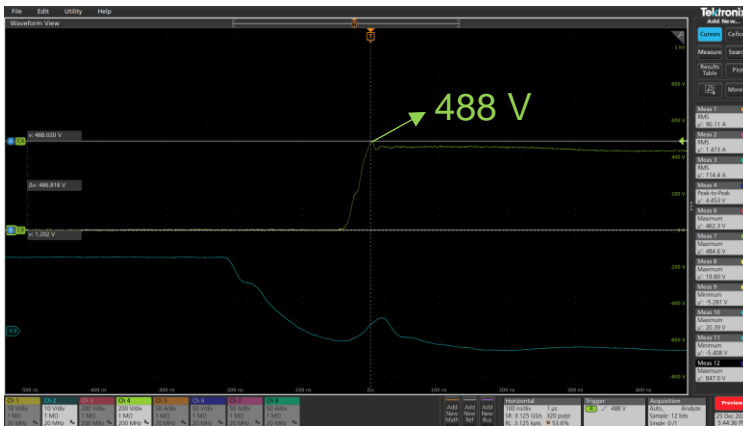
50kW T-type DC/AC PV inverter

Vds Spike

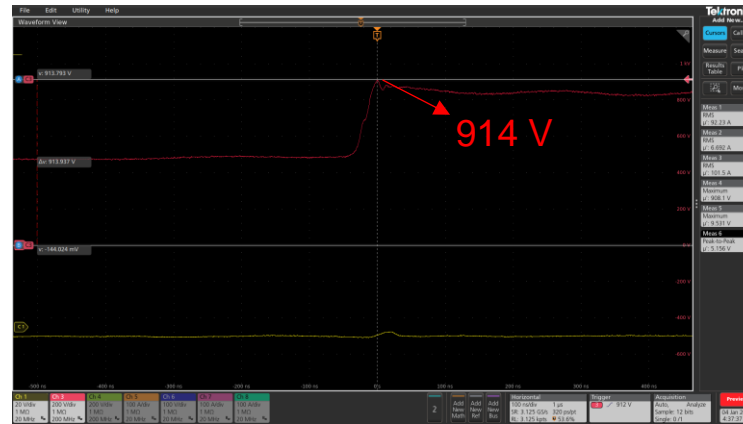
850Vin 220Vacout 50kw
Vertical bridge(PF=1)



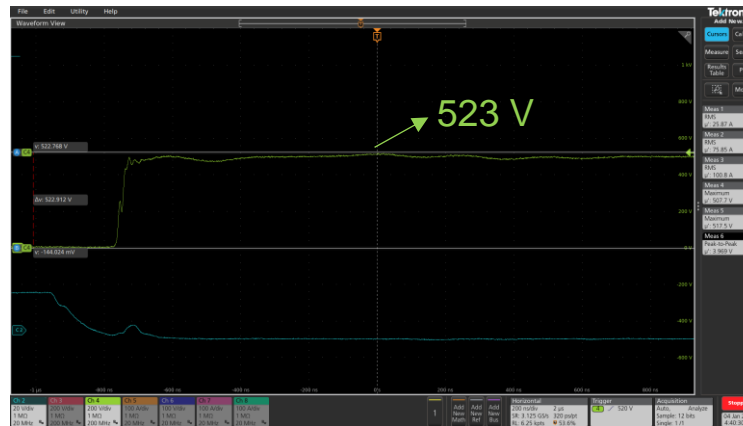
Horizontal bridge(PF=1)



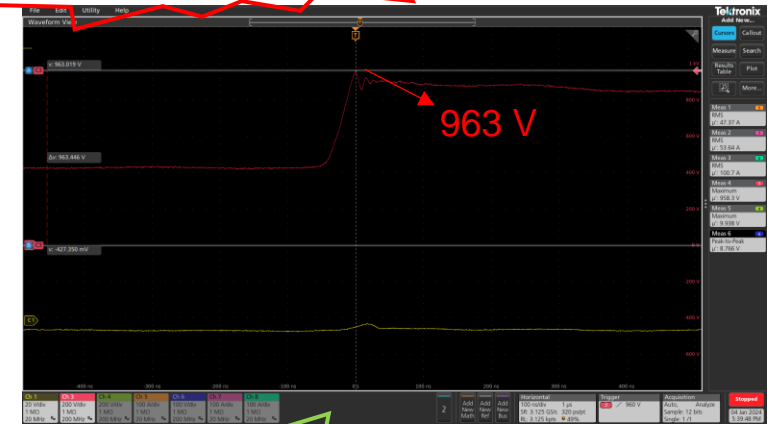
Vertical bridge(PF=0.8 lead)



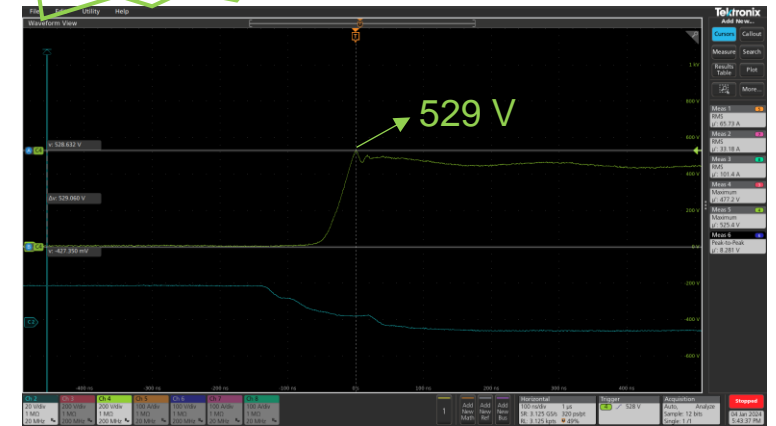
Horizontal bridge(PF=0.8 lead)



Vertical bridge(PF=0.8 lag)



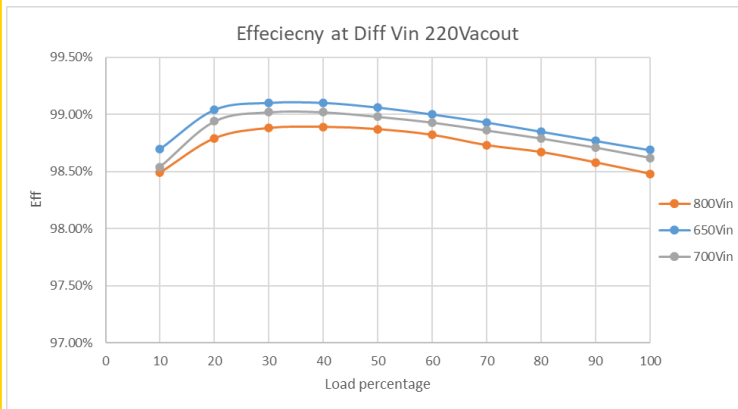
Horizontal bridge(PF=0.8 lag)



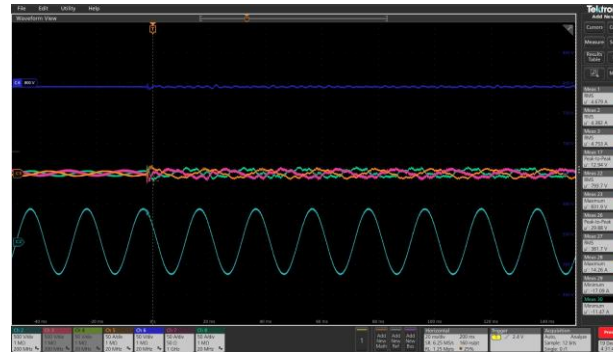


Final EVAL Results

Efficiency

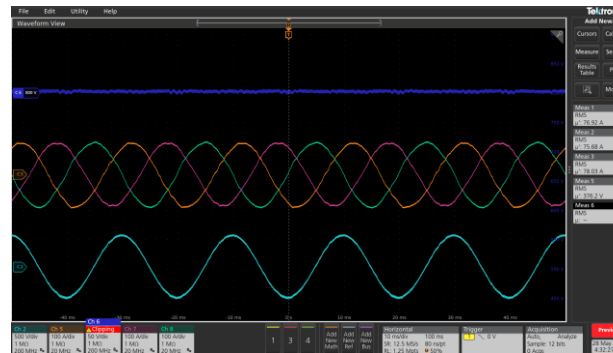


Waveforms



CH5,7,8-ABC output Current ; CH6-Input voltage ;
CH2-Output voltage

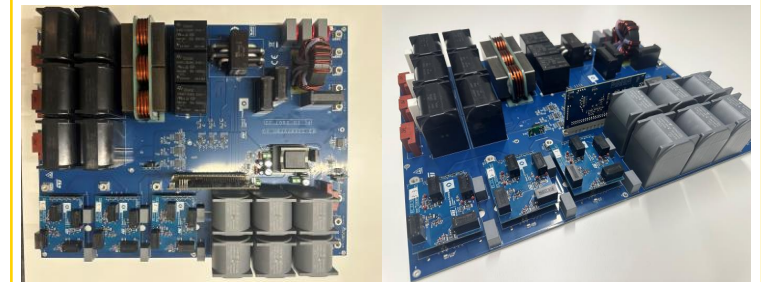
Startup



CH5,7,8-ABC output Current ; CH6-Input voltage ;
CH2-Output voltage
800 V 50 kW output

Key performance result

1. 650-850 Vdc input voltage; 310-476 V output voltage;
45-55 Hz output frequency; 50 kW output max power
2. Peak efficiency 99.10% @ 650 Vdc input;
98.89% @ 800 V input
3. PQ/PF control method in SW control



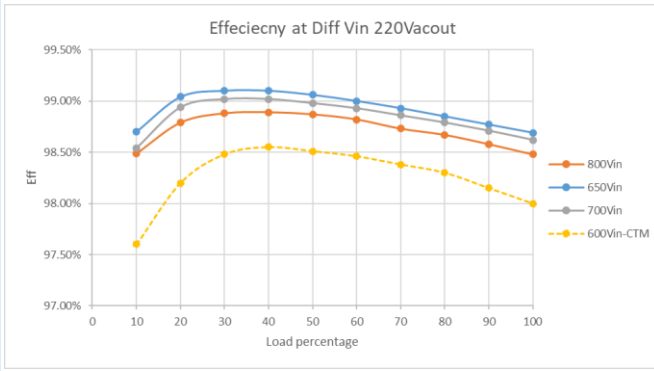
WxLxH:300 x 400 x 70 mm



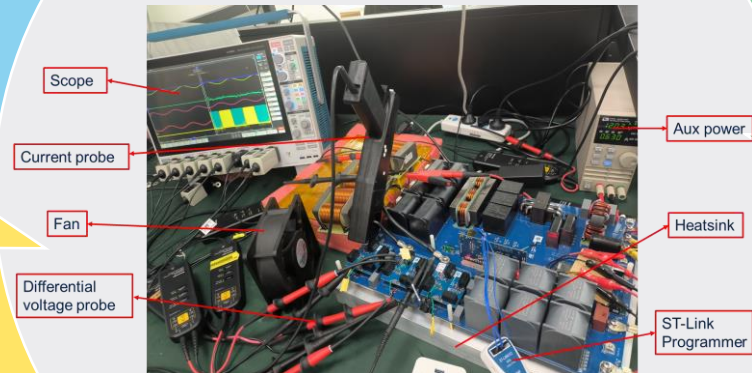
Summary

High efficiency

- 98.89% @ 800 Vdc
- 99.10% @ 650 Vdc



A2U8M12W3



High power density

- 75 W/in³

BUS CAP	Inverter Inductor Lf	Grid Inductor Lg
+ Lower Capacitance 120uF	+ Lower Inductance 80uH	+ Lower Inductance 6uH

High frequency

- 40 kHz

High reliability

- Gen 3 SiC technology
- ACEPACK2 package
- Integrated NTC
- AIN DBC



life.augmented

50 kW Digital DC-AC Inverter Based on SiC ACEPACK and STM32H743

Leah XIAO

Power & Energy
Competence
Center



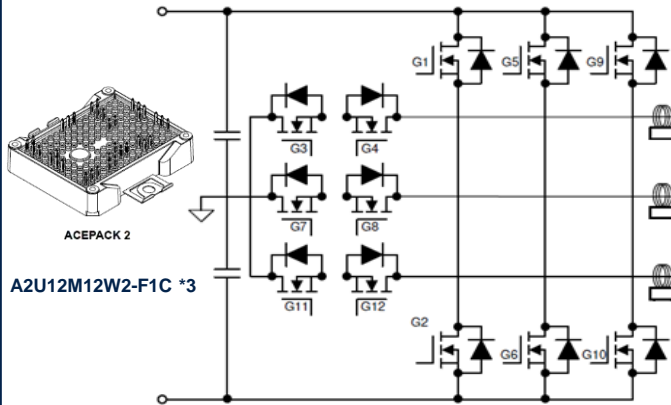


50kW DC/AC for PV Inverter

PE.ED_ED_0007.22



3-level t-type topology



PCBA outlook



Application key features:

- Input DC voltage: 650Vdc-850VDC
- Output AC voltage: 380 VAC L-L
- Switching frequency: 40 kHz
- Peak efficiency: 98.89% (800 Vdc)
- ≥ 0.99 PF and $\leq 3\%$ THD @ full load operation
- Active and reactive power control
- 0.8 leading to 0.8 lagging adjustable
- Fully digital power Stage with STM32H7 MCU

Key products

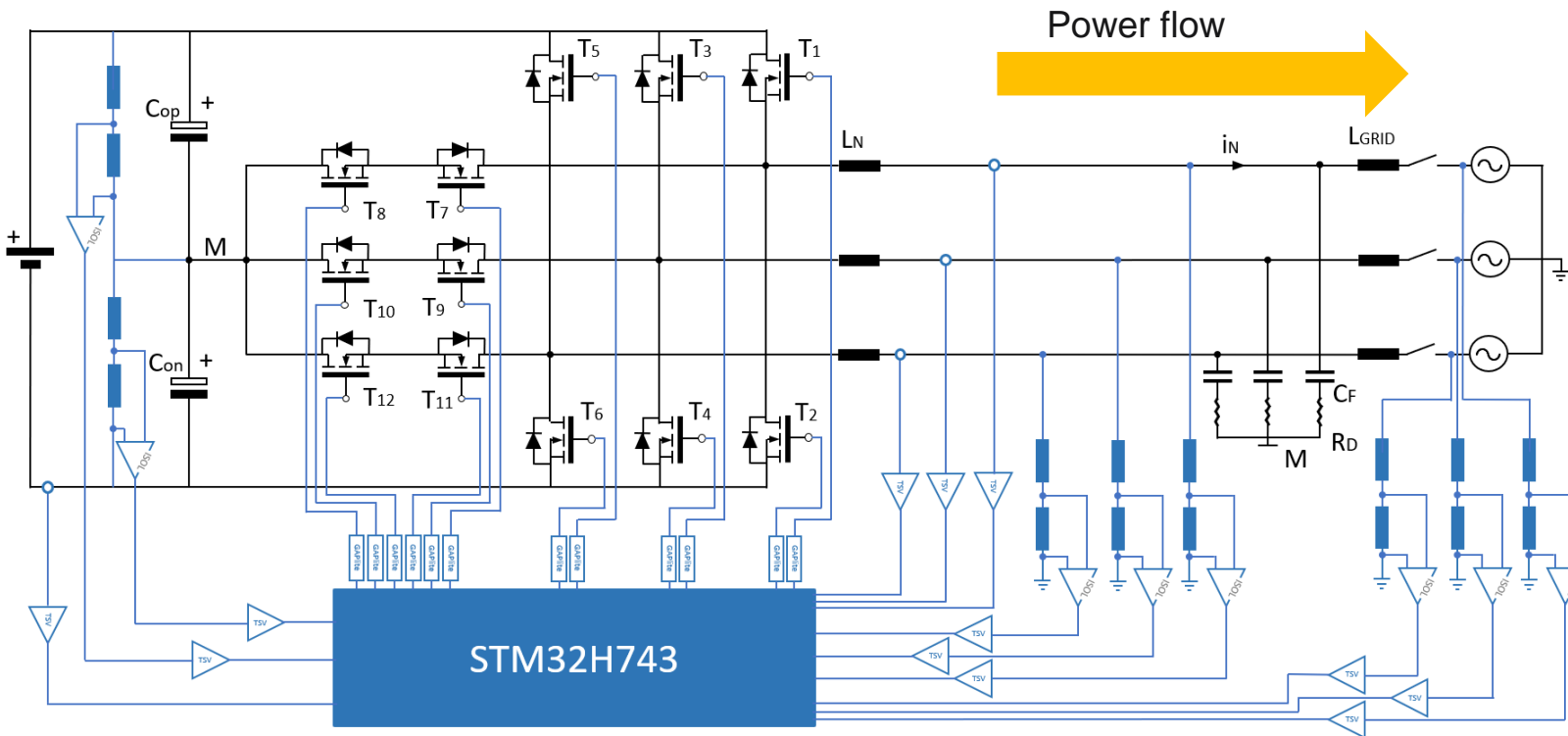
MCU: STM32H743ZGT6 (32-bit MCU with 480 MHz CPU frequency)
 SiC MOSFET: A2U8M12W3-FC*3 (9.5mΩ 1200 V & 6mΩ 750 V SiC module)
 Gate driver: STGAP2SICSC (galvanic insulated)
 IPC & GPA: ISOSD61, LM393DT, TSV912IDT, TSV914IDT

Key benefits

- ✓ SiC modular approach with full digital power control for high flexibility in system design
- ✓ Compact output LCL filter with switching frequency up to 40 kHz on power stage
- ✓ Support major functions (anti-islanding, RCMU) for PVI product design reference



Functional Block & Main Firmware Features



DC-AC

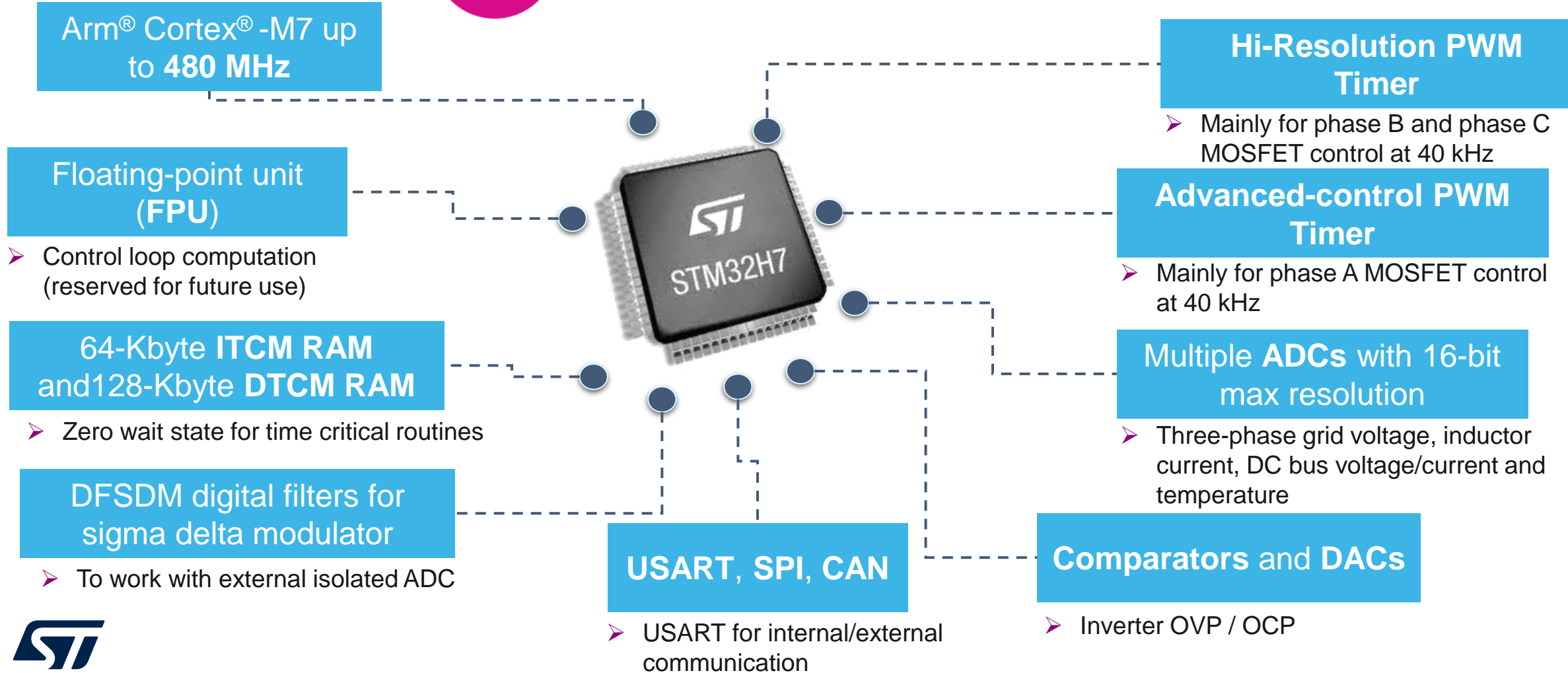
- 3-phase grid-connection controlled by DQ
- Active and reactive power control
- Overvoltage protection
- Overcurrent protection
- Thermal protection
- Anti-islanding, residual current detection
- Higher operating frequency
- Flexible digital design customization to meet specific customer needs
- Communication interfaces
(UART asynchronous protocol for external/internal communications)



Inverter Digital Platform - STM32H743



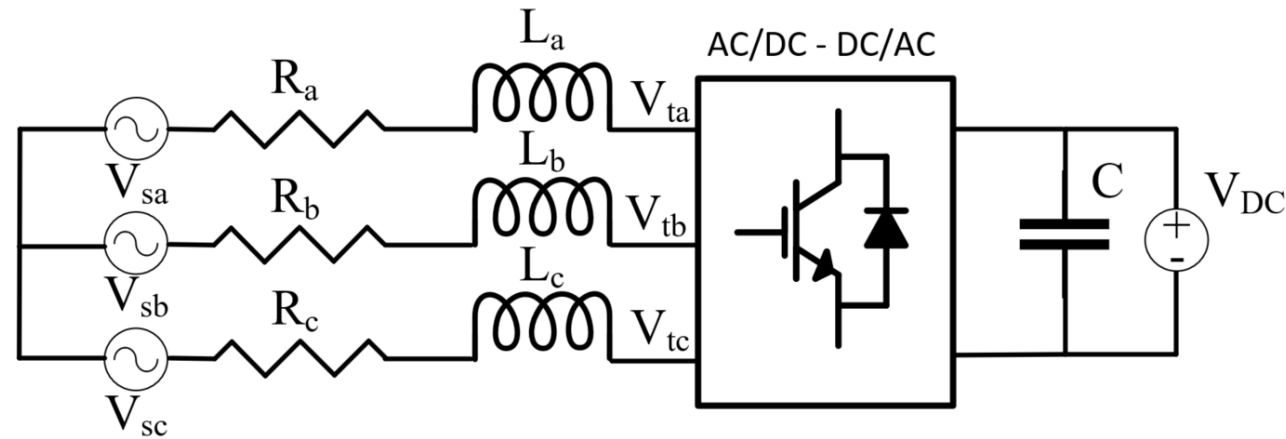
Configurations of MCU key functions on digital inverter





VSC Model (Plant)

Model of voltage source converter "VSC"



$$\begin{cases} L \frac{di_a}{dt} + Ri_a = V_{ta} - V_{sa} \\ L \frac{di_b}{dt} + Ri_b = V_{tb} - V_{sb} \\ L \frac{di_c}{dt} + Ri_c = V_{tc} - V_{sc} \end{cases}$$

Clarke
 $abc \Rightarrow \alpha\beta$

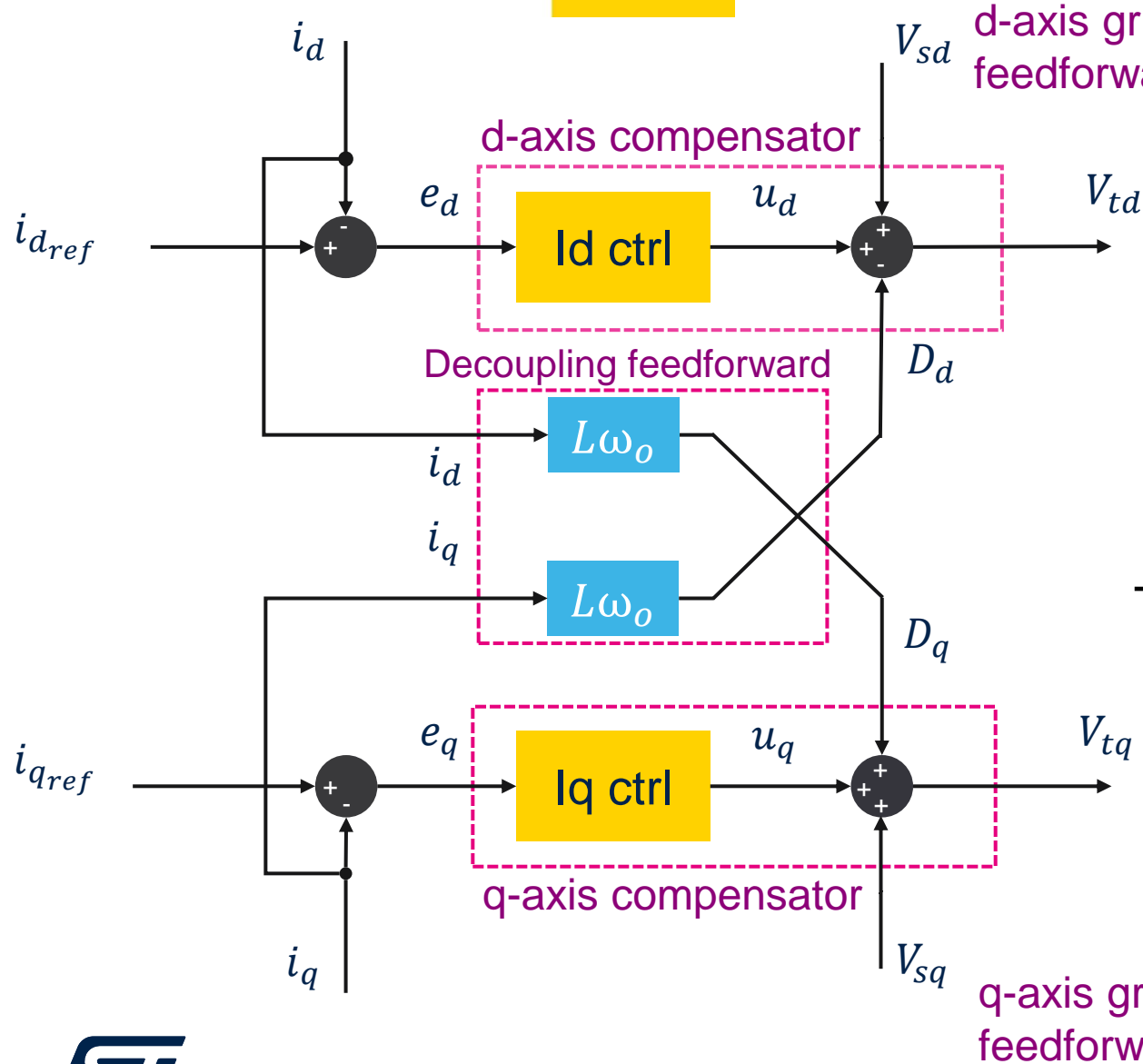
$$\begin{cases} L \frac{di_\alpha}{dt} + Ri_\alpha = V_{t\alpha} - V_{s\alpha} \\ L \frac{di_\beta}{dt} + Ri_\beta = V_{t\beta} - V_{s\beta} \end{cases}$$

Park
 $\alpha\beta \Rightarrow qd$

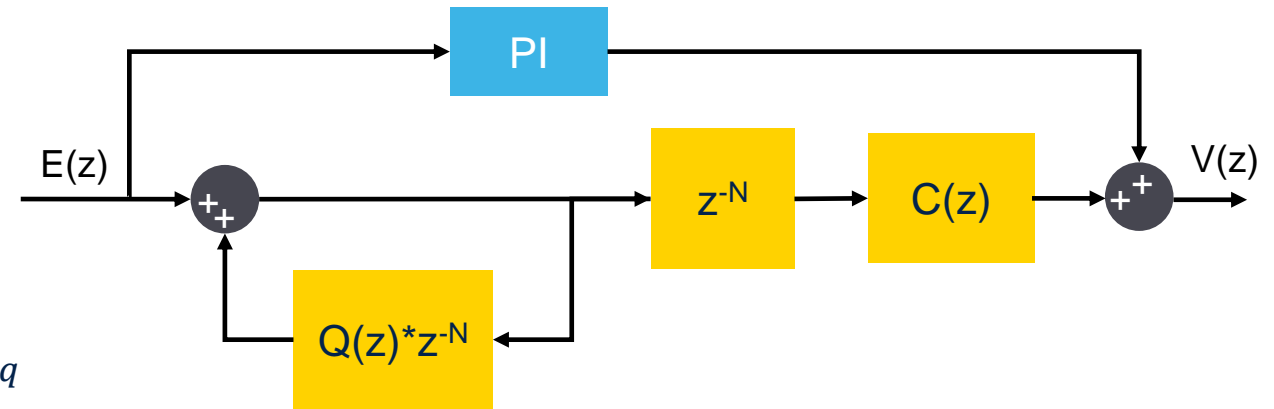
$$\begin{cases} L \frac{di_d}{dt} + Ri_d - \omega(t)Li_q = V_{td} - V_{sd} \\ L \frac{di_q}{dt} + Ri_q + \omega(t)Li_d = V_{tq} - V_{sq} \\ \frac{d\rho}{dt} = \omega(t) \end{cases}$$



Current Loop With Decoupling Control



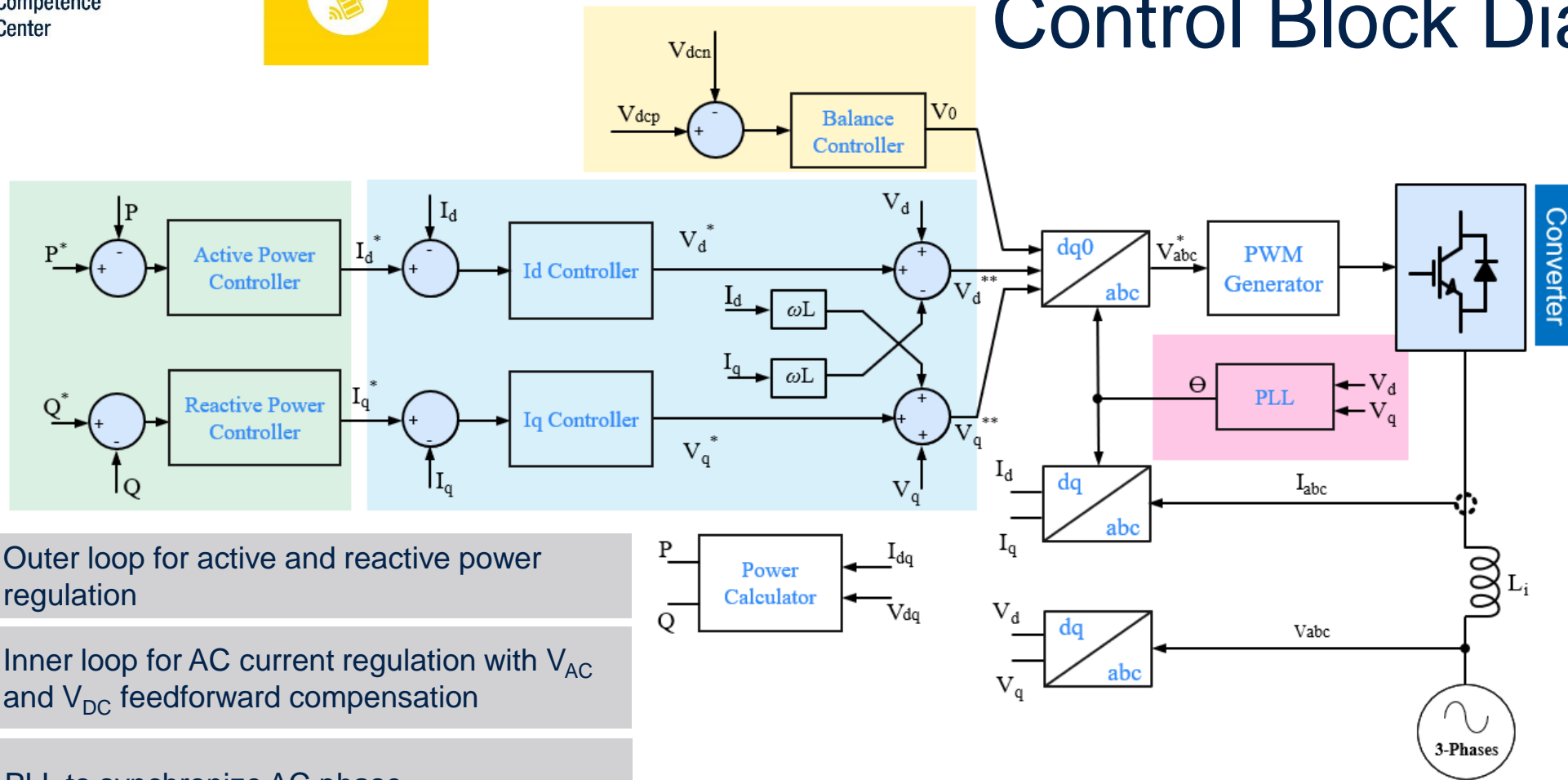
$$\begin{cases} V_{td} = \left(k_p + \frac{k_i}{s} + RC(z) \right) (i_{dref} - i_{dfeed}) - \omega_0 L i_q + V_{sd} \\ V_{tq} = \left(k_p + \frac{k_i}{s} + RC(z) \right) (i_{qref} - i_{qfeed}) + \omega_0 L i_d + V_{sq} \end{cases}$$



PI + repetitive controller is applied to achieve better static and dynamic performance on current controlling



Control Block Diagram



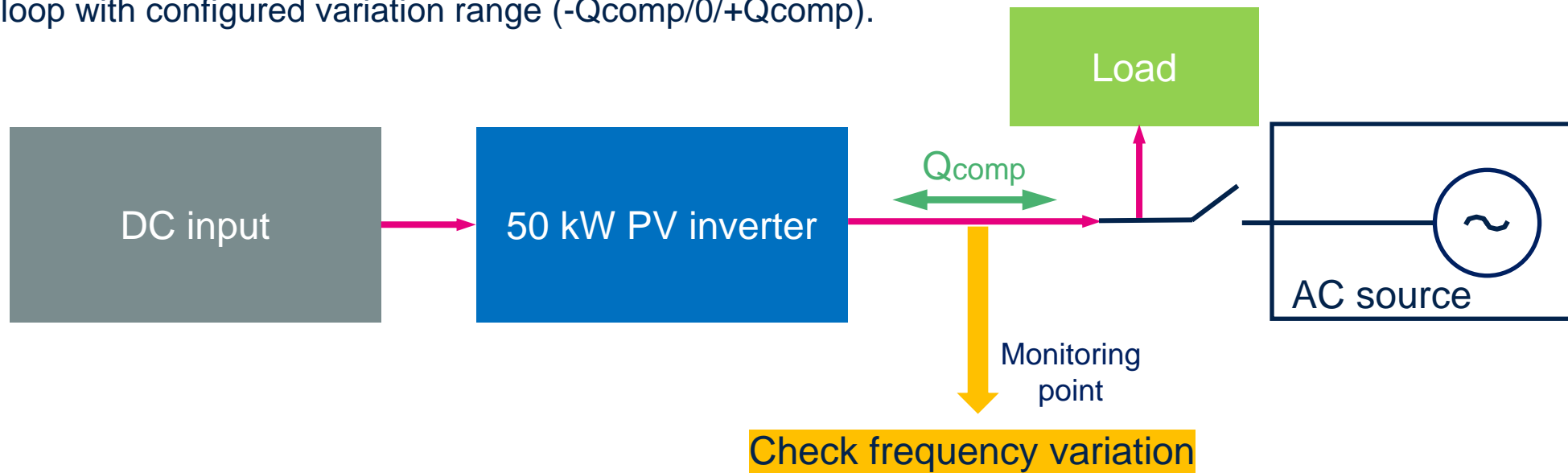
Power loop	Outer loop for active and reactive power regulation
Current loop	Inner loop for AC current regulation with V_{AC} and V_{DC} feedforward compensation
PLL loop	PLL to synchronize AC phase
Bus balance loop	Balance three-level bus neutral-point

- Power loop: 20 kHz
- Current loop: 20 kHz
- PLL loop: 20 kHz
- Bus balance control: 20 kHz



Active detection - reactive disturbance compensation method

- By variation of reactive power as disturbance signal, the existence of AC grid could be detected by checking frequency variation.
- The disturbance compensation of reactive power (Q_{comp}) will be injected to the output of control loop with configured variation range ($-Q_{comp}/0/+Q_{comp}$).

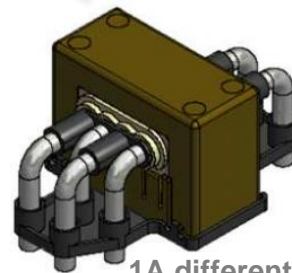
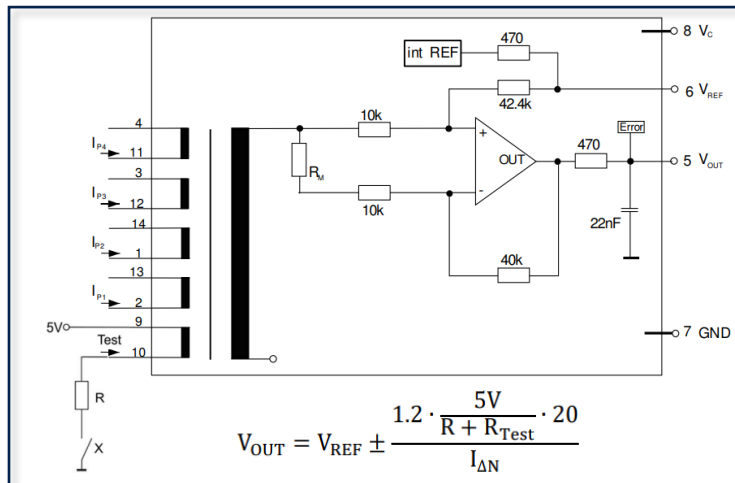
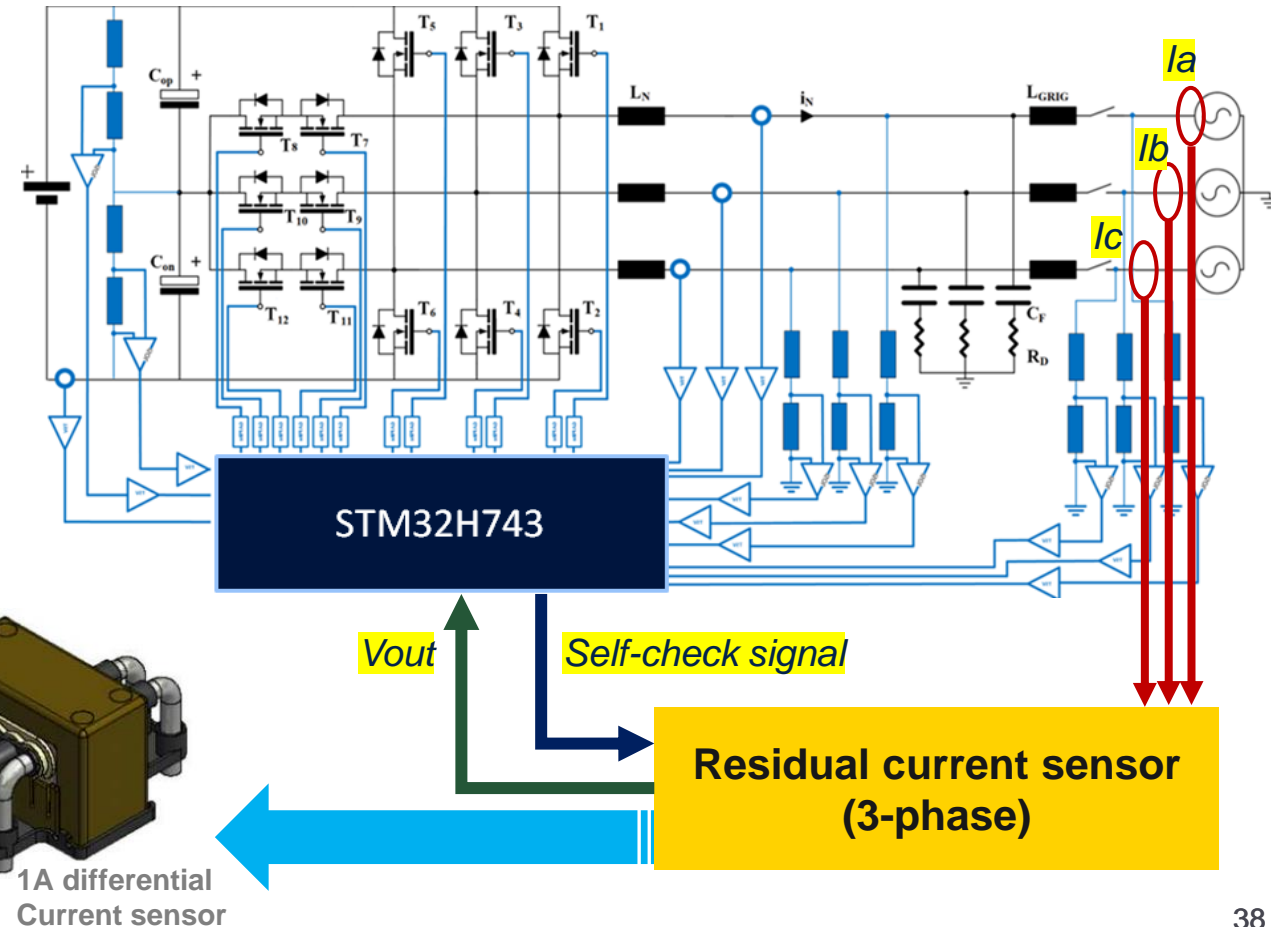




Residual Current Protection

Residual current monitoring with self-checking

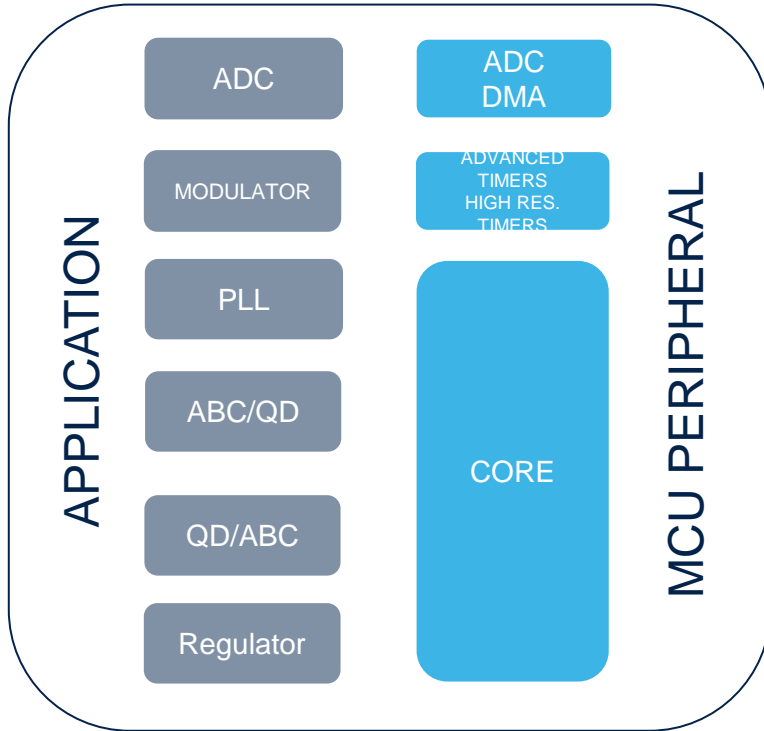
- Self-checking feature:
Before powering up (grid relay off), MCU sends a “self-check” signal to check the functionality of current sensor
- Residual current detection:
After powering up (grid relay on), the MCU will keep monitoring the residual current (within a configured value)



1A differential
Current sensor



MCU Configuration For Control Loop



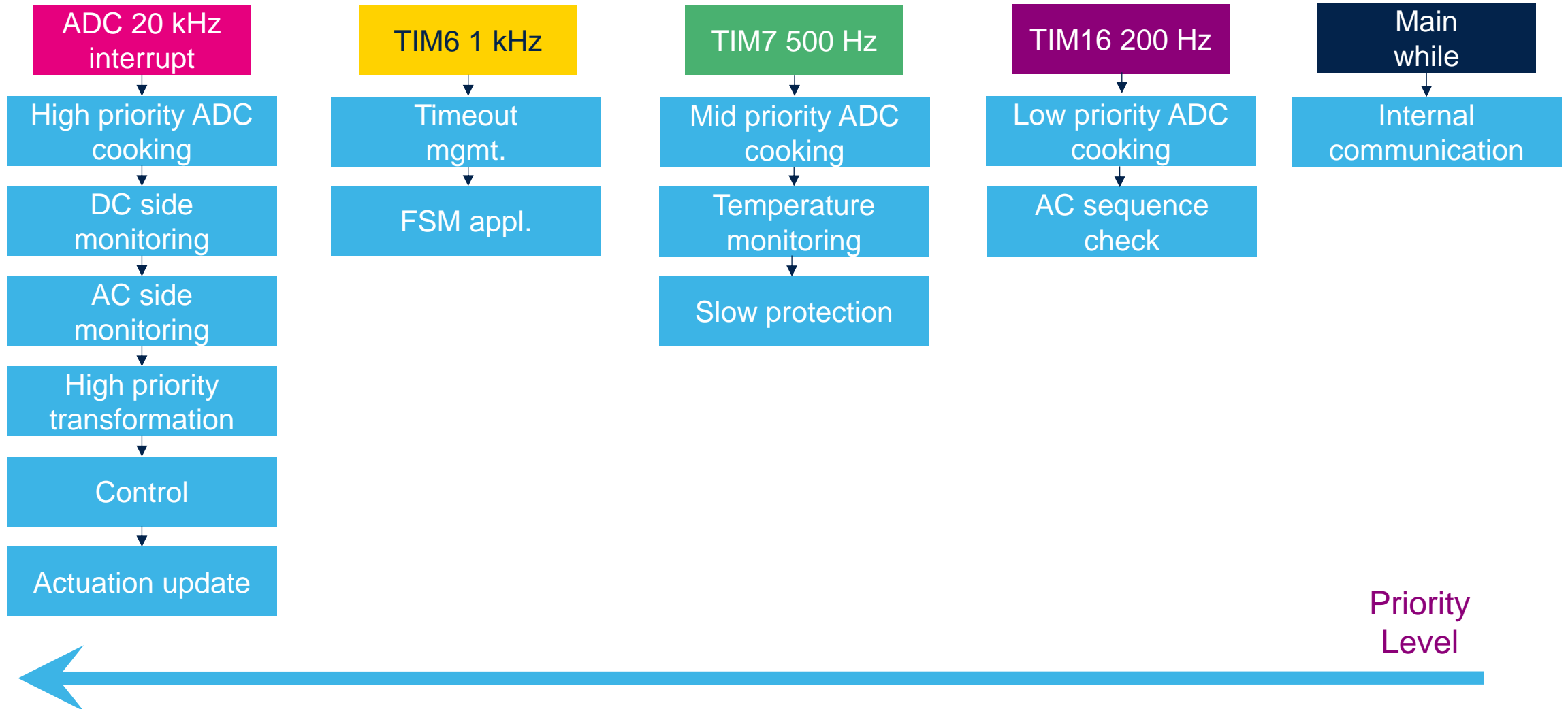
IMPLEMENTATION

Task	Used peripherals
Outer loop & inner loop	ADC based interrupt
Modulator	High resolution + advanced timers
Sensing	ADC & DMA

STM32H743	Timer	Channel w DT	Output
Advanced timers	TIM1	2	4
High-resolution timers	HRTIM	4	8

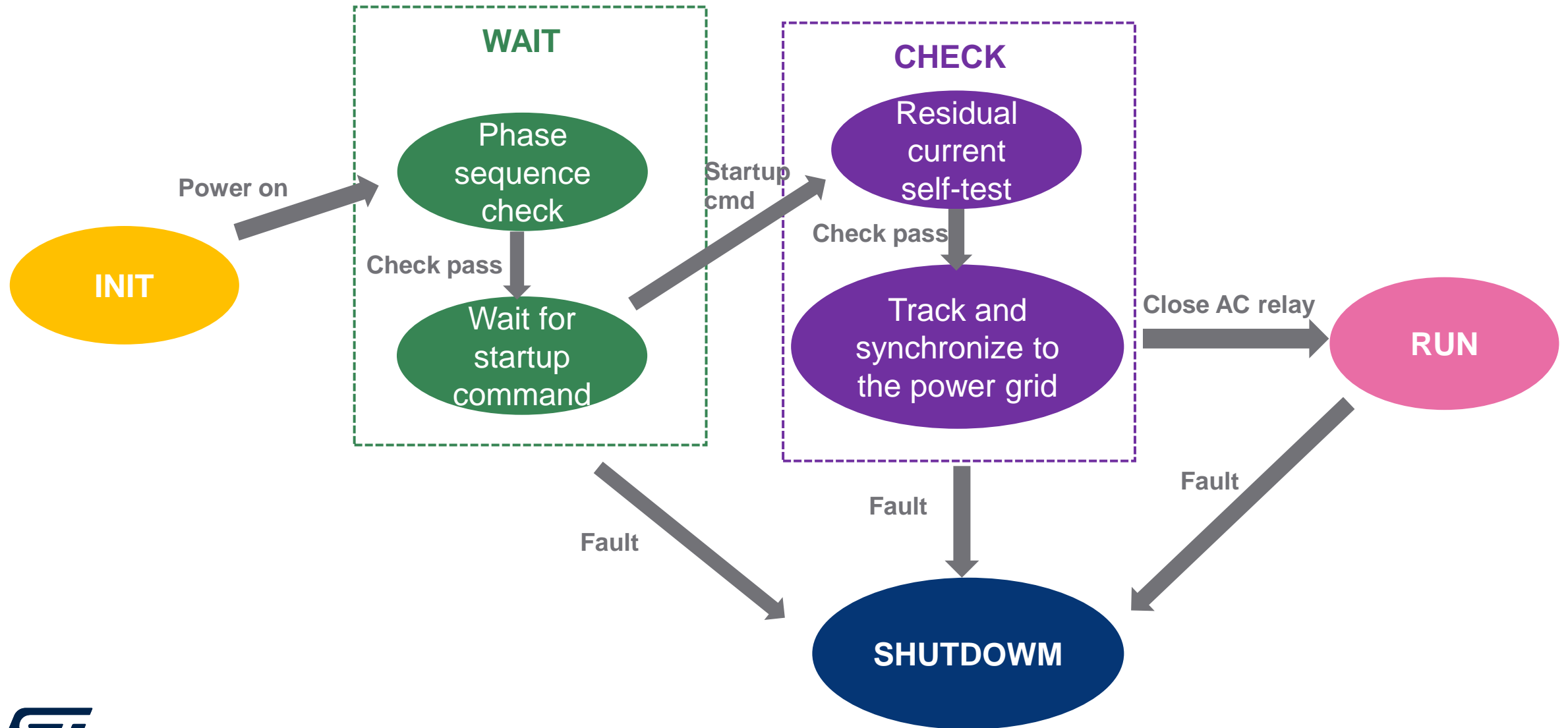


Firmware Configuration



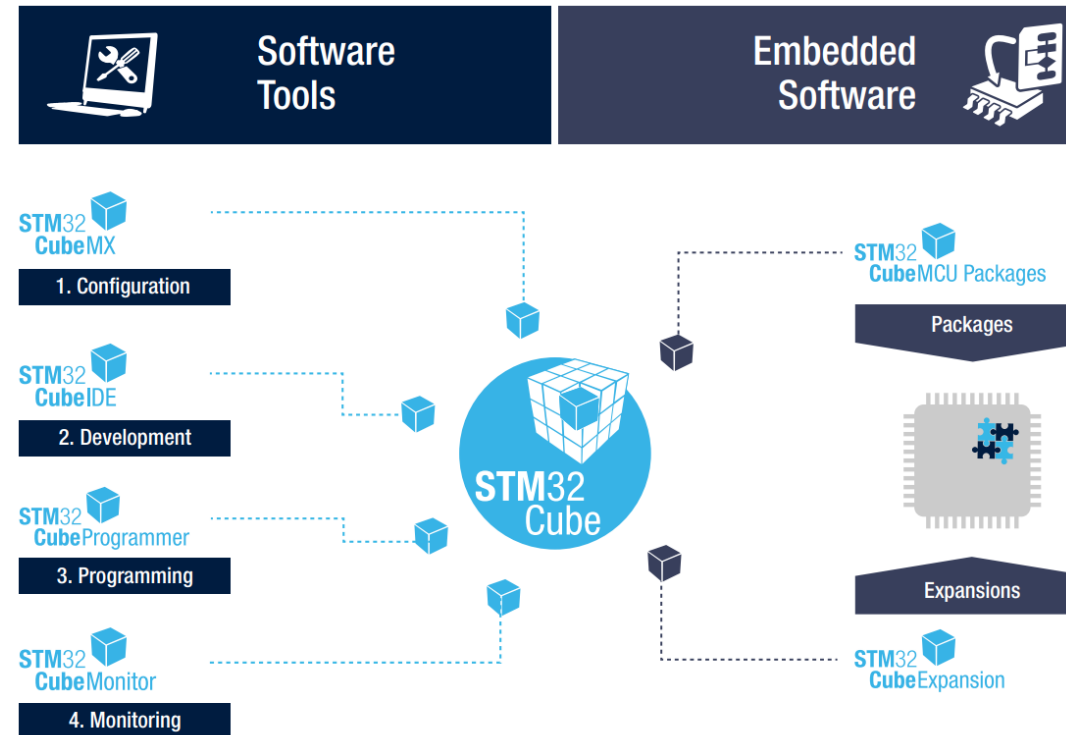


State Machine





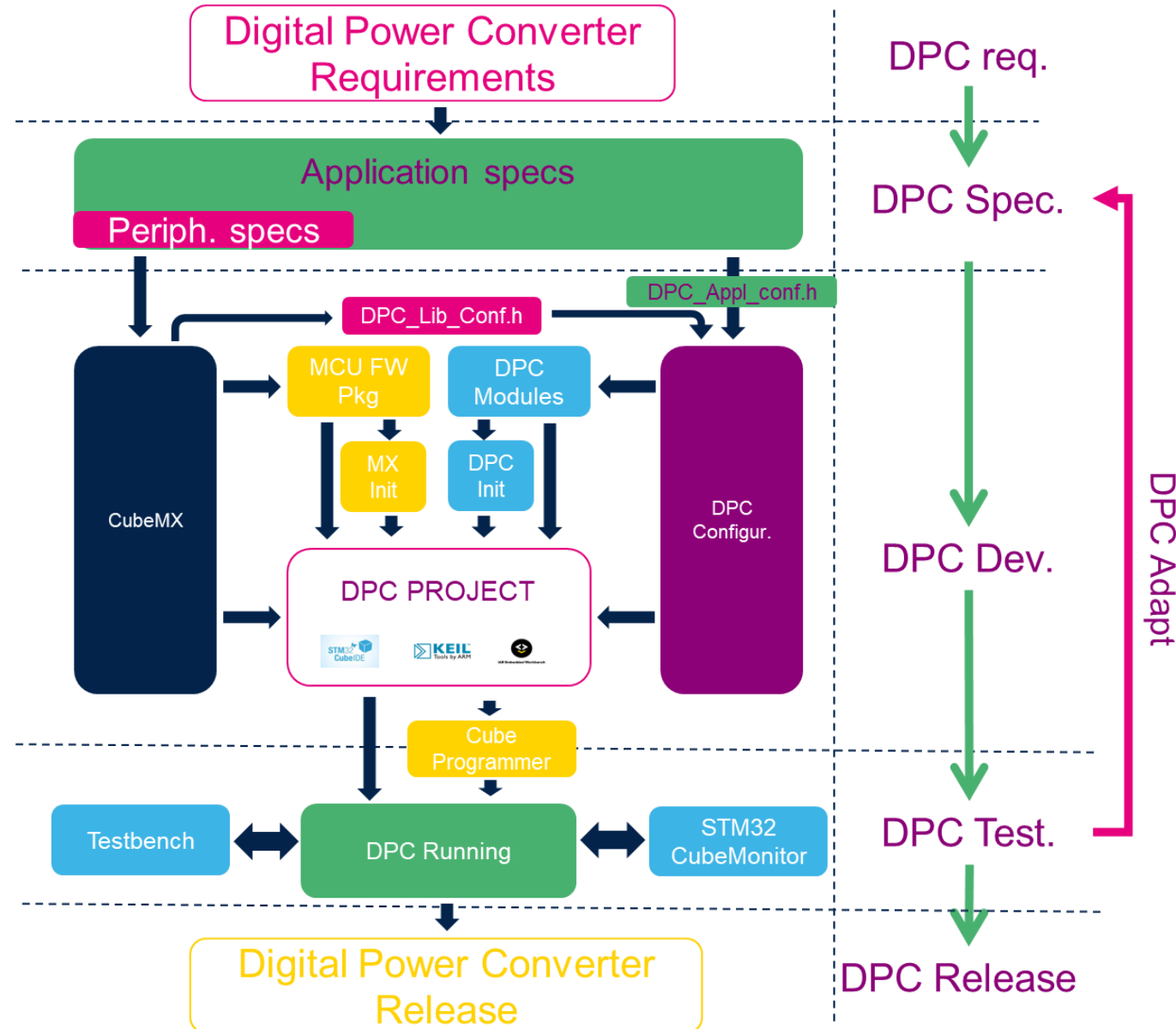
STM32Cube Ecosystem



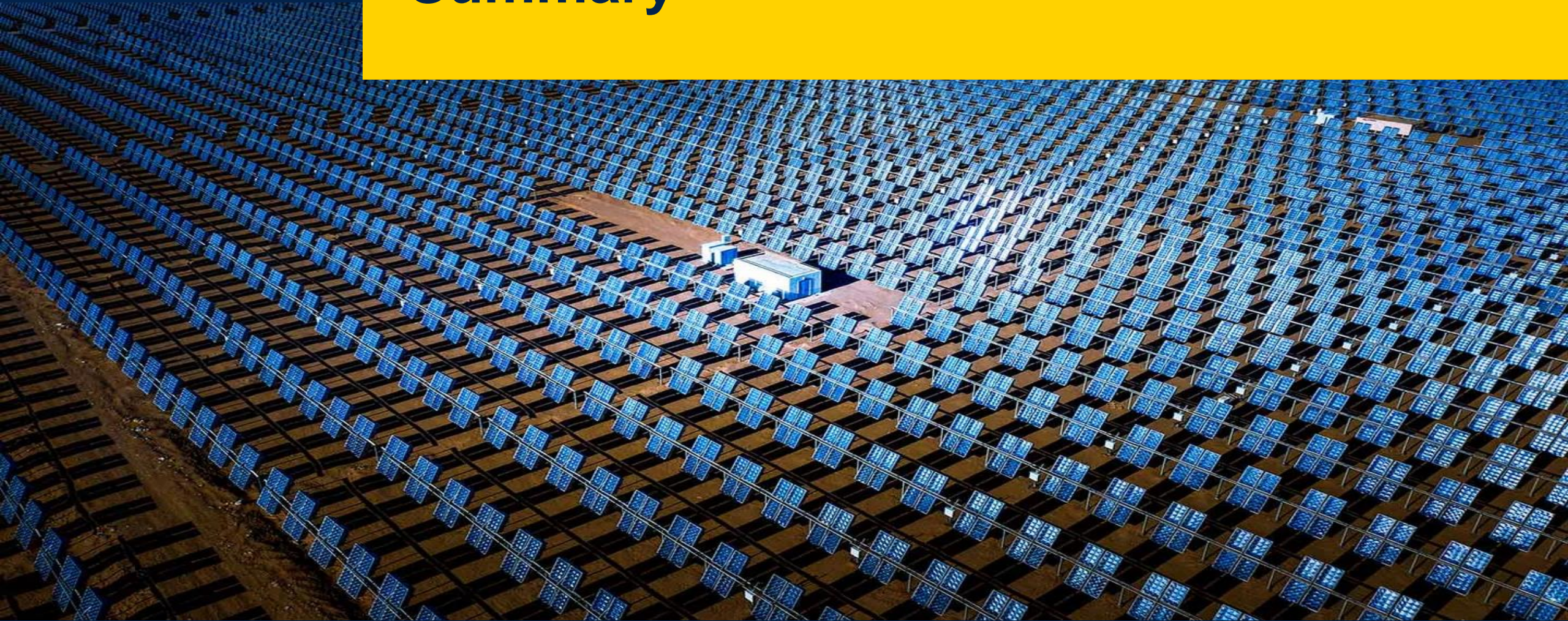
The STM32Cube ecosystem is a software solution for STM32 microcontrollers and microprocessors, created for both designers interested in a free comprehensive development environment for STM32 microcontrollers and microprocessors, and for users looking to integrate STM32 software in their existing IDE, such as Keil or IAR IDEs.



DPC Dev. Flow



Summary





ST SiC and STM32H7 based solution help achieve high performance PV inverters

With high efficiency & high power density trends, more requirements to PV inverter

ST provides advanced components & total solution to customers (SiC MOSFETs/SiC diode/STGAP/STM32)

ST 50 kW **T-type inverter** solution can achieve peak efficiency 98.89%(800 Vdc), 99.10%(650 Vdc)

User manual & BOM & SCH & PCB boards have all been ready now



**Industrial Summit
download center**



**ST Power & SPIN
microsite (CN Only)**



Our technology starts with You



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