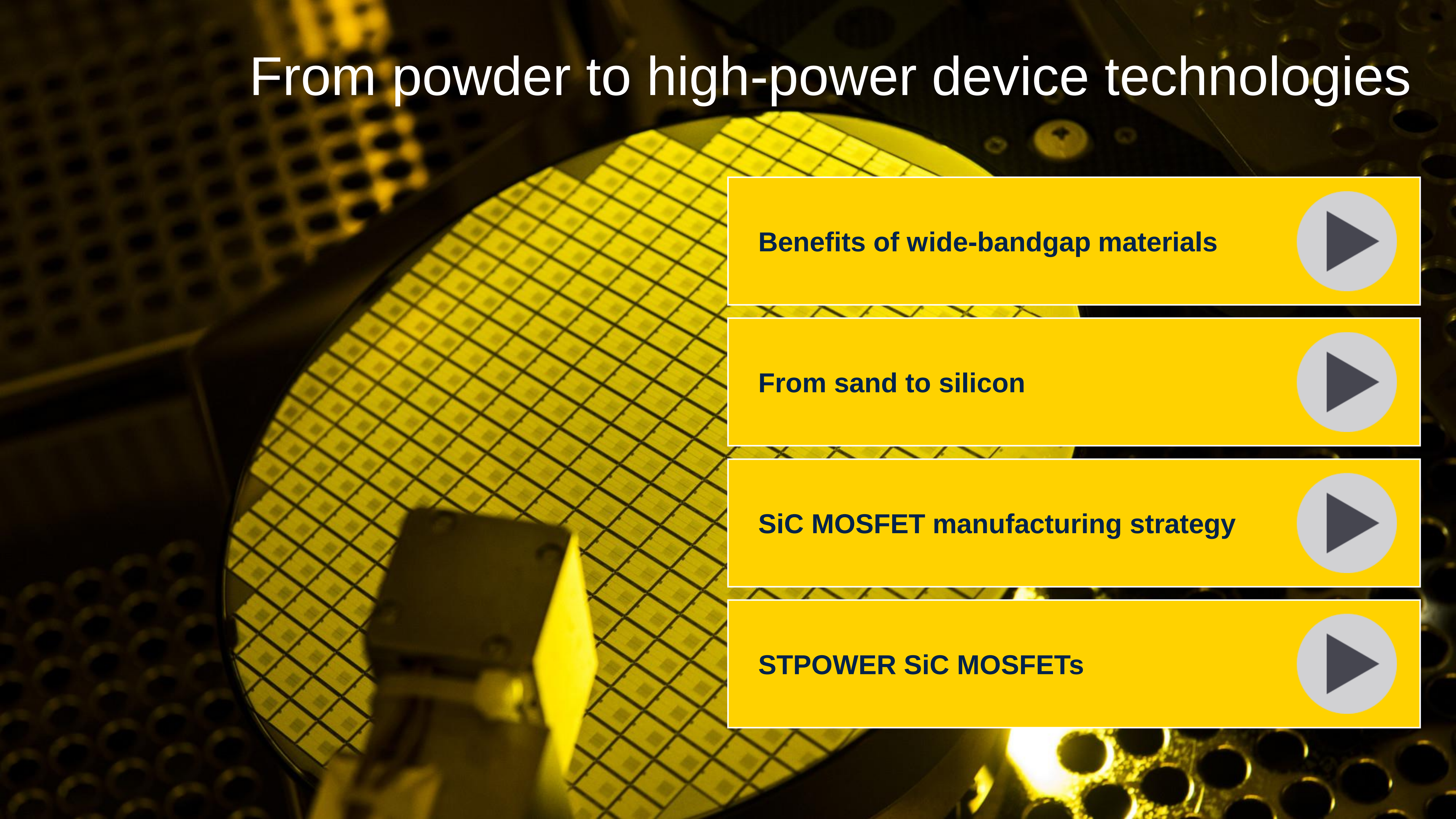
From powder to high-power device technologies



Benefits of wide-bandgap materials

From sand to silicon

SiC MOSFET manufacturing strategy

STPOWER SiC MOSFETs

Benefits of wide-bandgap materials in power conversion

SiC and GaN exhibit unique and complementary properties

	Si	SiC-4H	GaN
Bandgap (eV)	1.1 eV	3.2 eV	3.4 eV
Electron mobility μ_n (cm^2/V s)	1450	900	2000
Breakdown electric field E_{br} (MV/cm)	0.3	3	3.5
Saturation electron drift velocity v_s (10^7 cm/sec)	1	2.2	2.5
Thermal conductivity Θ (W/cm K)	1.5	3.8	1.3

Less heat	high conversion efficiency
High frequency	smaller passive components
High power density	miniaturization
High temperature tolerance	reliable operation in hostile environments

- Longer range
- Increased performance
- Reduced weight
- Lower cooling requirements
- Less stress on batteries

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From quartz to trichlorosilane (TCS)

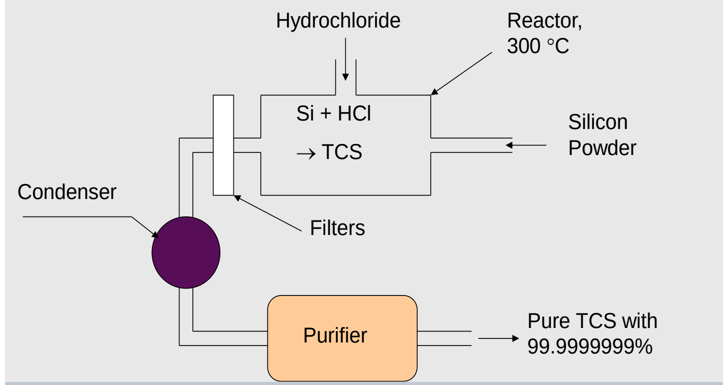
Quartz sand

Silicon dioxide SiO_2

Metallurgical-grade silicon

$SiO_2 + C \xrightarrow{2000^oC} Si + CO_2$

MGS reacts with HCl



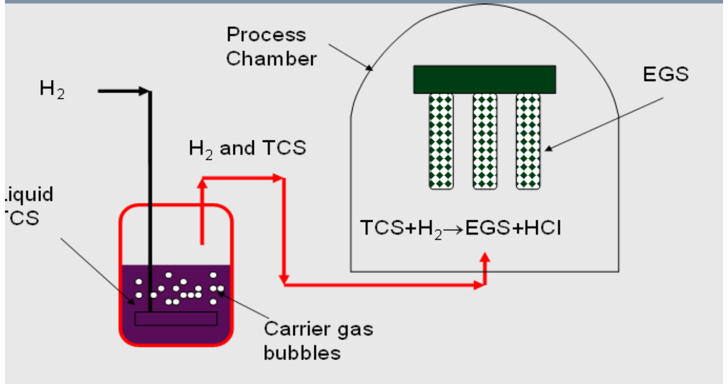
Trichlorosilane (TCS) $SiHCl_3$ forms

From trichlorosilane to silicon

Purified trichlorosilane

By vaporization and condensation

React TCS with H_2

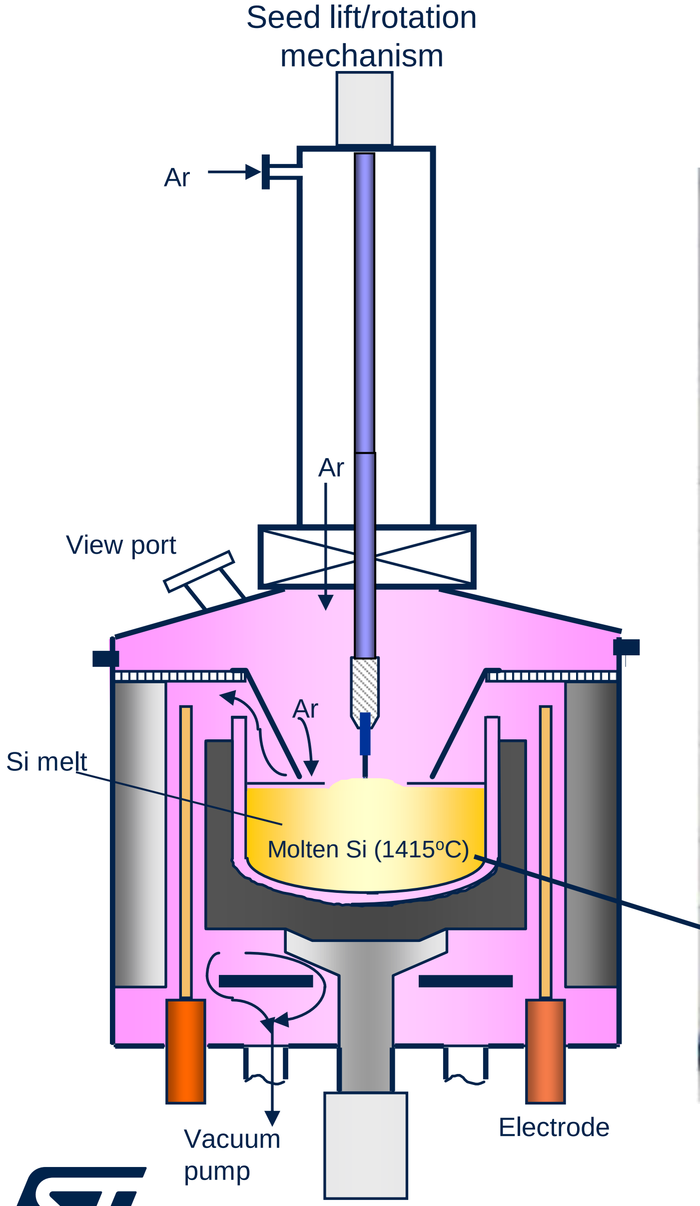


Polysilicon is formed
$2SiHCl_3$ (g) + $2H_2$ (g) → 2Si (s) + 6HCl (g)

Pull single crystal ingot

From melted electronic-grade silicon (EGS)

Starting wafer
Czochralski (CZ) crystal growth



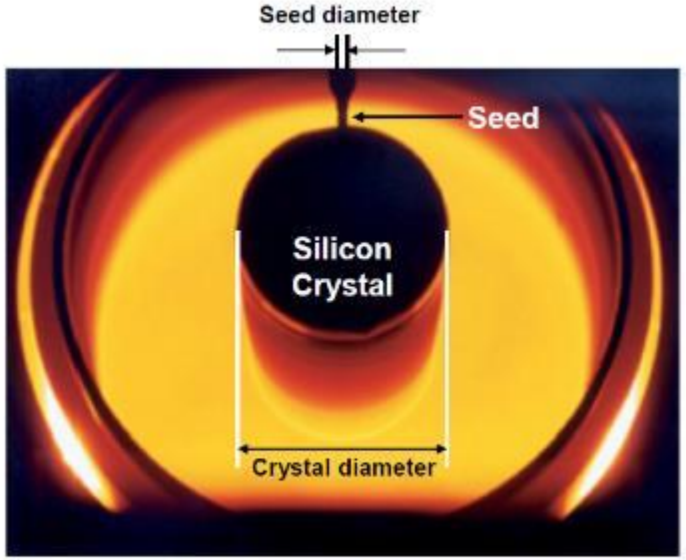
A typical ingot is about 1 or 2 meters in length

The ingot is sliced into hundreds of smaller circular wafers

Each wafer yields hundreds or thousands of integrated circuits

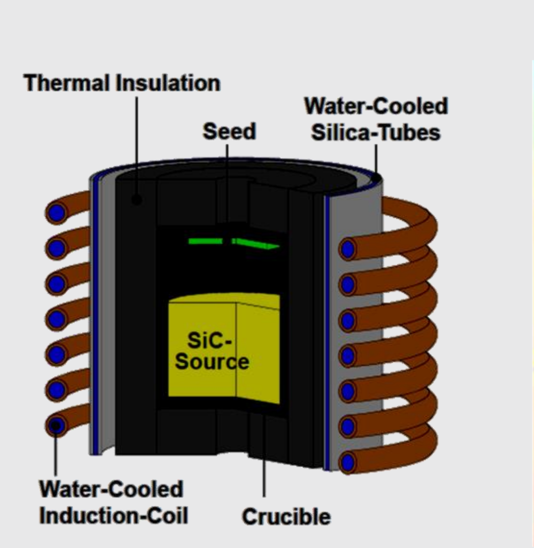
SiC vs Si crystal growth

Silicon liquid-phase growth (Czochralski of floating-zone) T 1414ºC

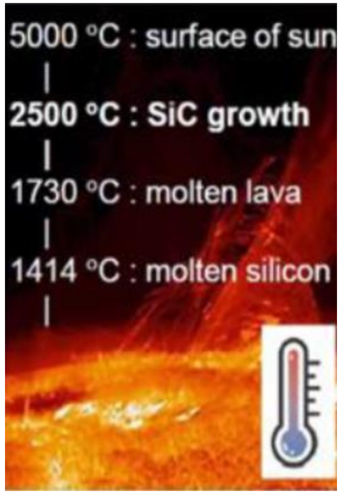


Silicon-monocrystal during growth from the melt

SiC vapor-phase transportation (PVT) T 2500ºc



Schematic Illustration of Growth Reactor



How hot?

- SiC does not melt (sublimation process is needed)
- High-temperature process (2500ºC)
- Growth rate ≤ mm/h
- Wafering (sawing, polishing, etc.) very difficult due to material hardness

Wafer manufacturing

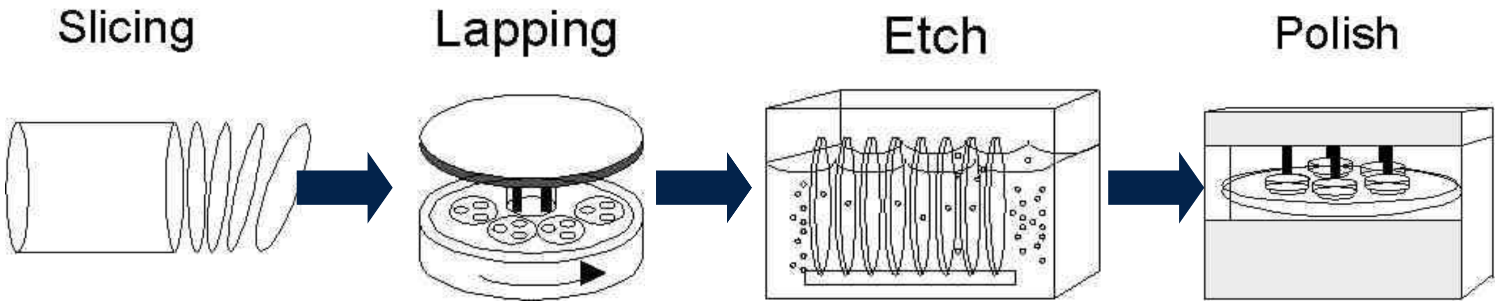
The silicon crystal is sliced by diamond-tipped saw into thin wafers

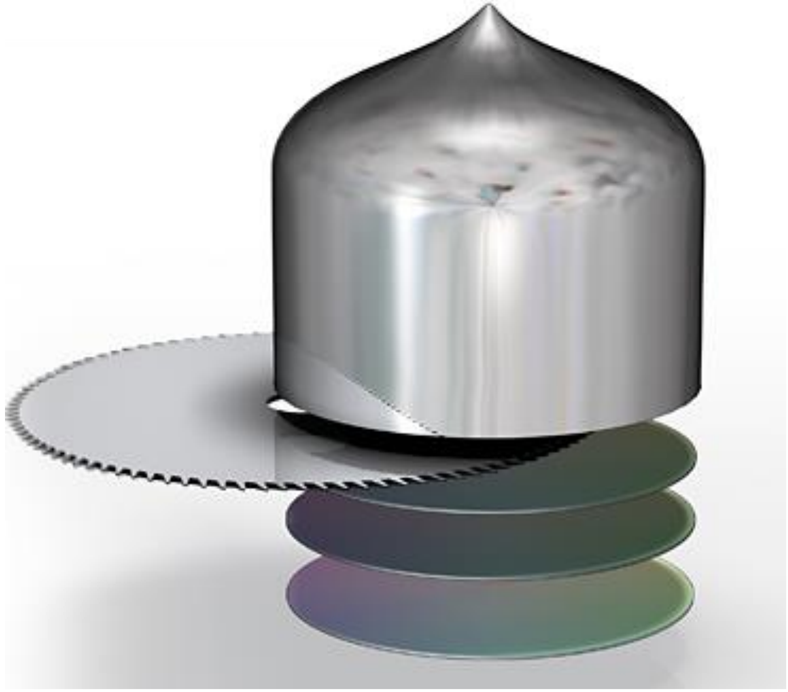
Sorted by thickness

Damaged wafers removed during lapping

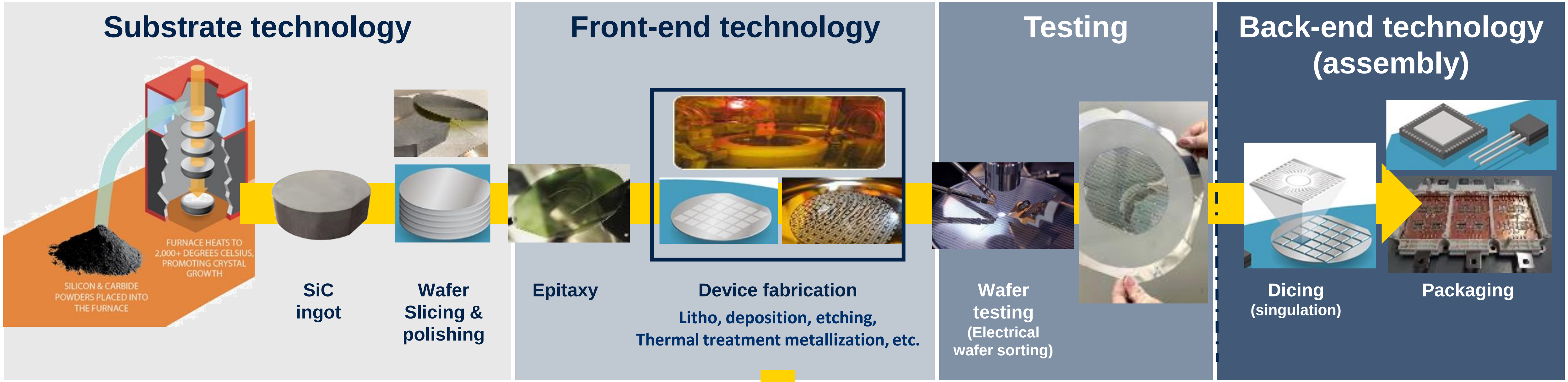
Wafers etched in chemical to remove remaining crystal damage

Polishing smooths uneven surface left by sawing process





MOSFET manufacturing from powder to final product



Substrate technology

SiC ingot

Wafer Slicing & polishing

Front-end technology

Epitaxy

Device fabrication

Litho, deposition, etching,
Thermal treatment metallization, etc.

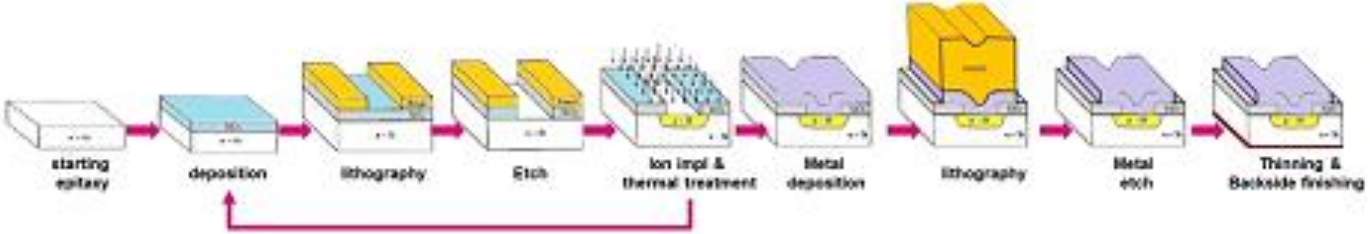
Testing

Wafer testing
(Electrical wafer sorting)

Back-end technology (assembly)

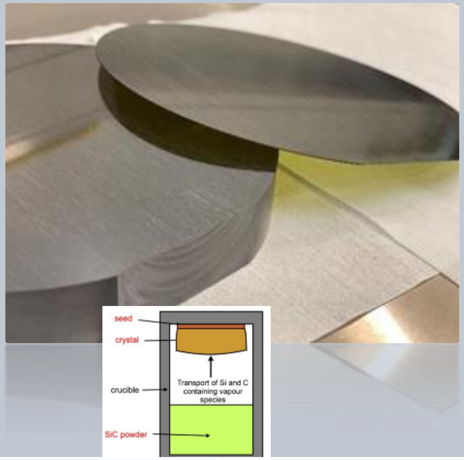
Dicing
(singulation)

Packaging

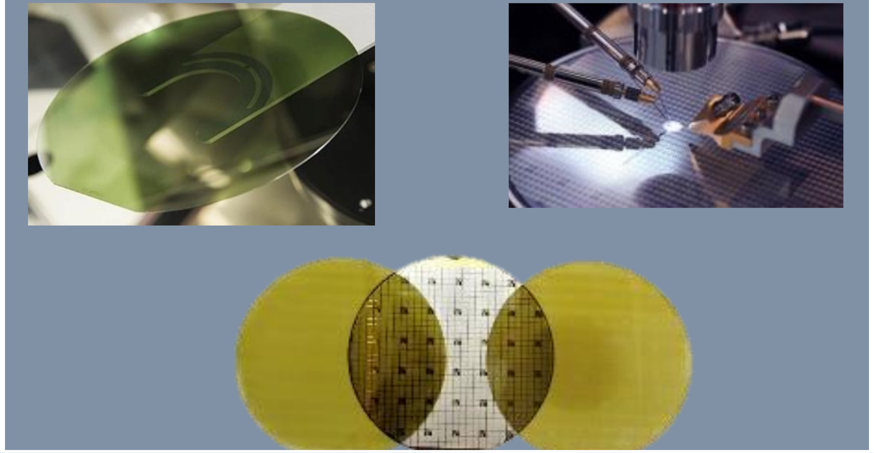


SiC MOSFET manufacturing

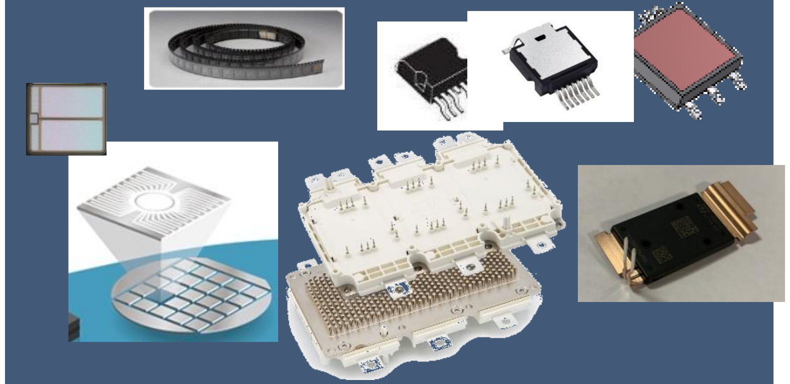
Substrate technology
From powder to ingot



Front-end technology
With epy and EWS testing



Back-end technology
Bare dice, discrete, modules



Norrköping (R&D)

Catania (Italy) Substrate fab (2024)

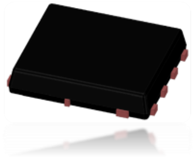
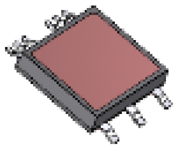
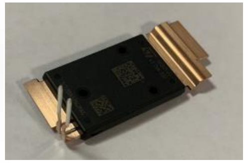
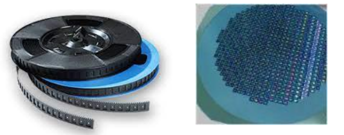
Catania (Italy)

Singapore

Shenzhen (China)

Bouskoura (Morocco)

SiC MOSFET packages

	PowerFLAT 8x8 STD & DSC	H2PAK-7L	HU3PAK	ACEPAK SMIT	HiP247 3L, 4L, & 4L HC	STPAK	Bare dice
Package							
	Surface mounting				**Through-hole**	**Special package solutions**	
Characteristics	❑ Very thin (< 1 mm) ❑ Well accepted in power conversion ❑ Dual-side cooling option ❑ Leadless ❑ **Industrial domain**	❑ **AG-qualified at 175°C** ❑ Kelvin source for optimized driving ❑ High runner for automotive customers	❑ **AG-qualified at 175°C** ❑ **Top-side cooling** ❑ Kelvin source for optimized driving ❑ Very good thermal dissipation	❑ **AG-qualified at 175°C** ❑ **Isolated top-side cooling** ❑ Suitable for different configurations (HB, dual die, etc.) ❑ High power ❑ Modular approach	❑ **AG-qualified at 200°C** ❑ **Very common industry standard** ❑ Kelvin source option for optimized driving ❑ High-creepage version (1200 and 1700 V) in development	❑ **Unique solution for traction inverter** ❑ **AG-qualified at 200°C** ❑ **Very high thermal dissipation efficiency** ❑ Sense pin for optimized driving ❑ Multisintered package	❑ **WLBI & KGD** ❑ **T&R or RWF options** ❑ **Compliant with the stringent automotive quality requirements**

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SiC MOSFET series positioning

Breakdown voltage	650 V		750/900 V	1200 V			1700 V
Series	Gen2	Gen3	Gen3	Gen1	Gen2	Gen3	Gen1
On-state resistance	18-55 mΩ	14-55 mΩ	11 mΩ	52-520 mΩ	21-75 mΩ	15-70 mΩ	65 mΩ & 0.7 Ω
Focus applications	**OBC & DC-DC** **Renewable energy** **Power supply** **Industrial drives**	**OBC & DC-DC** **Power supply** **Solar** **Telecom & server**	**DC-DC** **Renewable energy** **Telecom & server**	**Photovoltaic** **HVAC** **Power supply**	**OBC & DC-DC** **Inverter** **Street lighting** **Charging stations** **Industrial drives**	**Inverter** **DC-DC** **Power supply**	**DC-DC** **Power supply** **Renewable energy**

Gen 3 (G3): ES available, MAT 30 achieved
(Gen 3 product portfolio according to current product plan)