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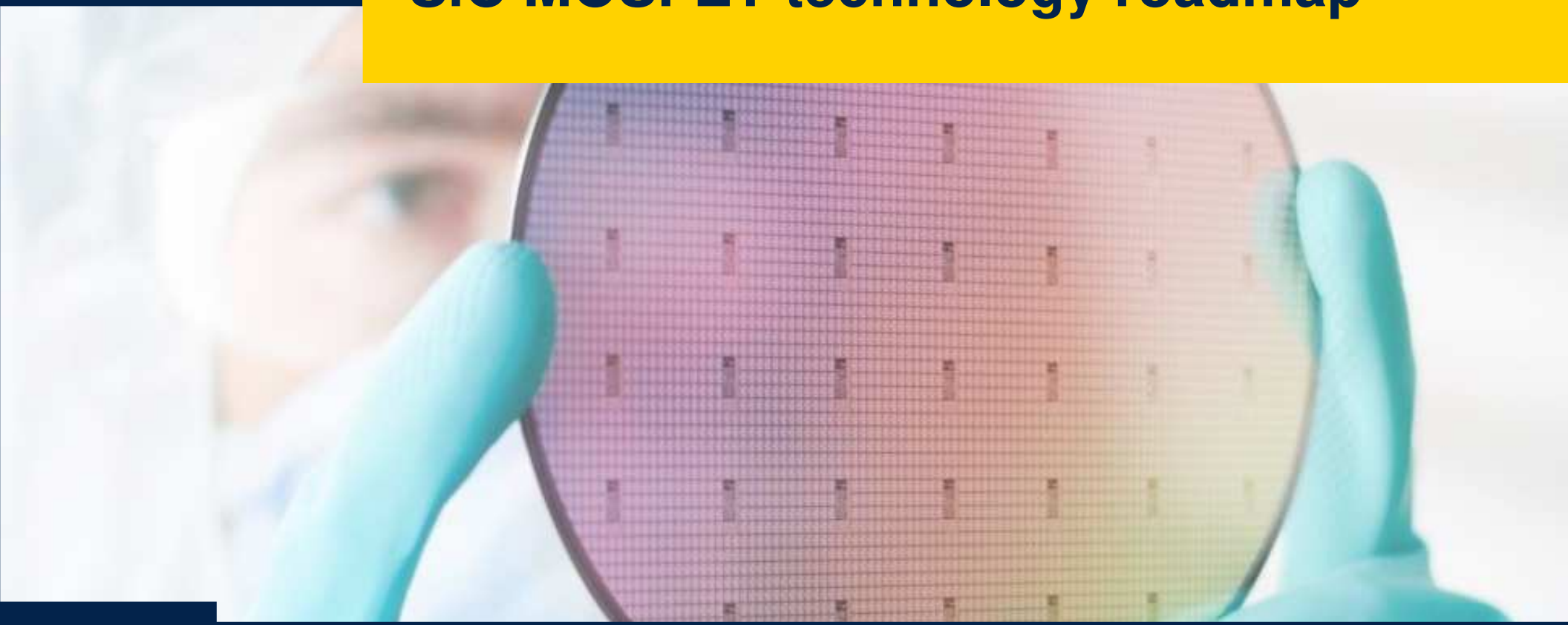
意法半导体碳化硅MOS技术发展路线和中国市场战略

孙君颖

STPOWER

SiC MOSFET technology roadmap



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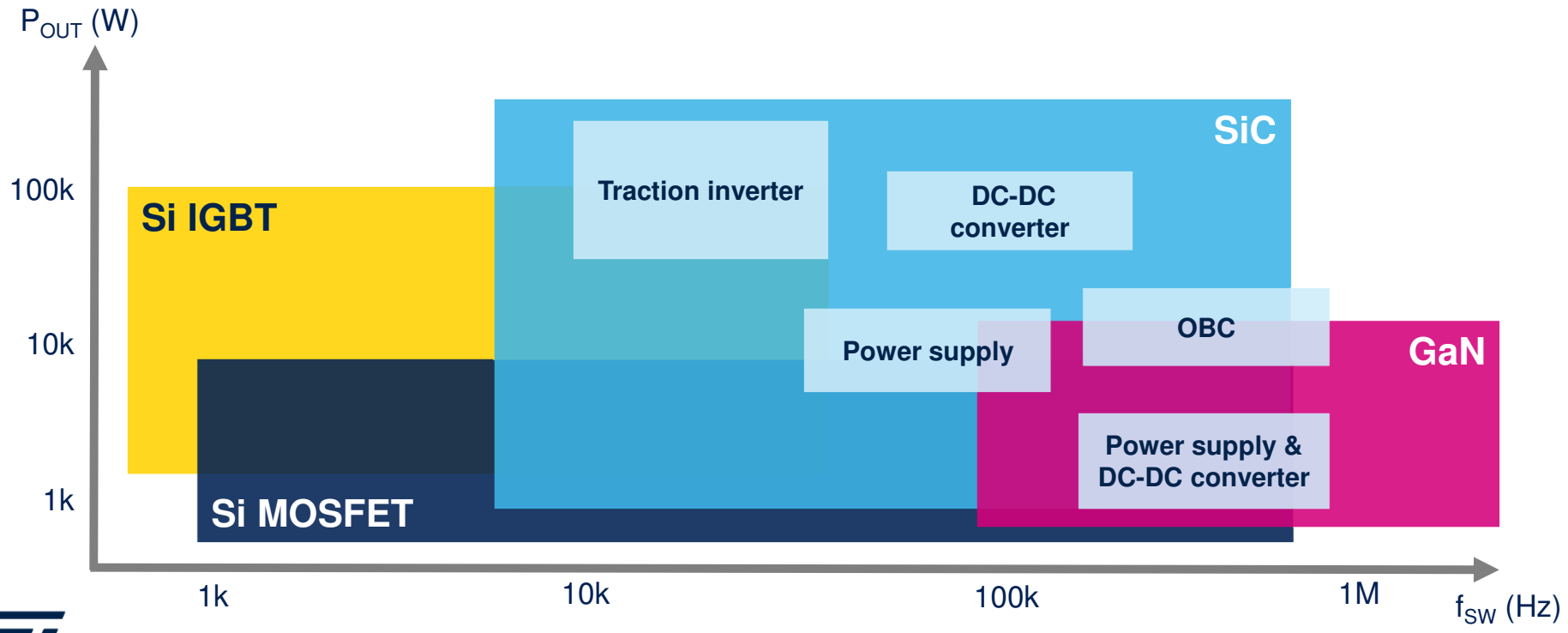
Power semiconductors for key applications

SiC MOSFET technology offers the best performance in high voltage, high frequency, and high-power system applications



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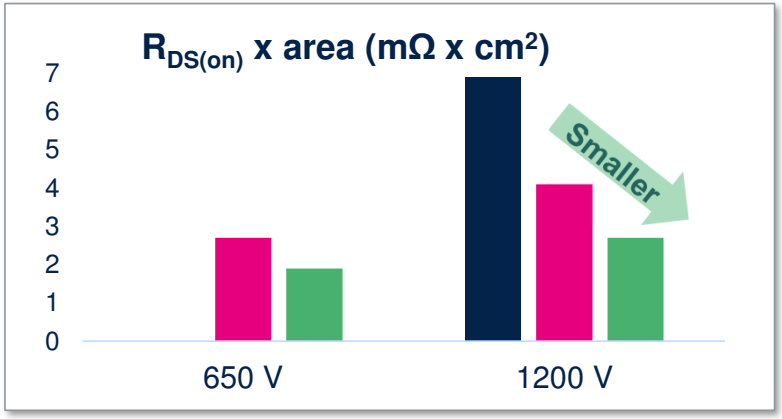
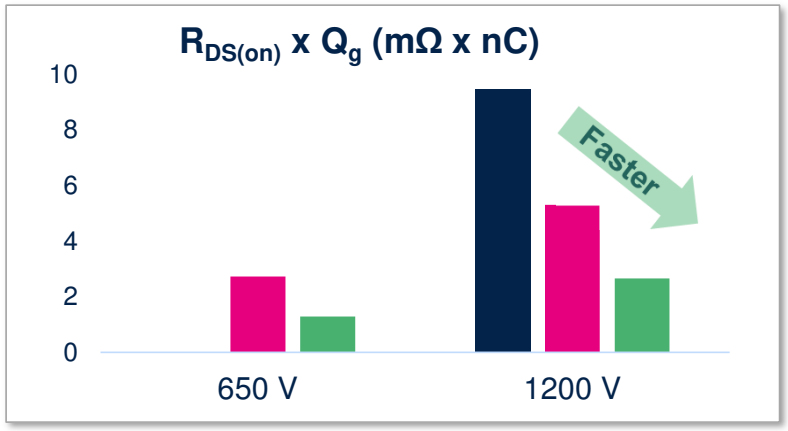
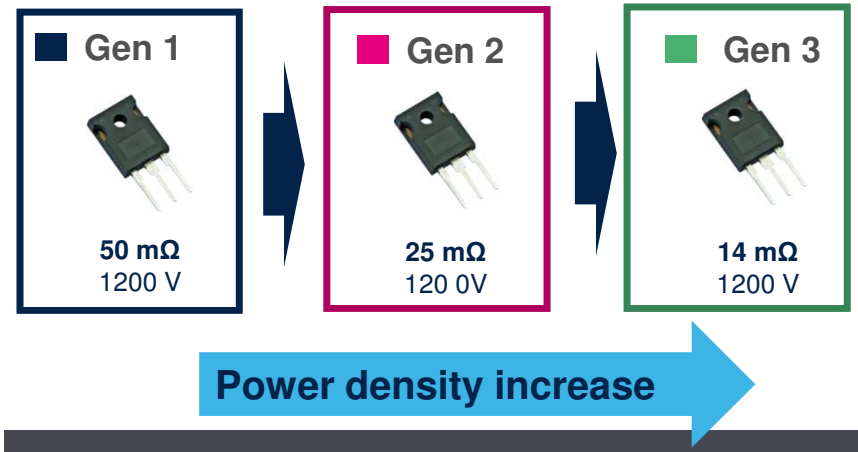
SiC MOSFET state-of-the-art technology evolution
Figure of Merits







Relentless advancement

- Lower Ron x area → lower Ron for a given chip size or smaller chip size for a given Ron, higher current capability, lower conduction losses
- Lower Ron x Qg → lower switching losses, higher frequency (small form factor board, TCO)

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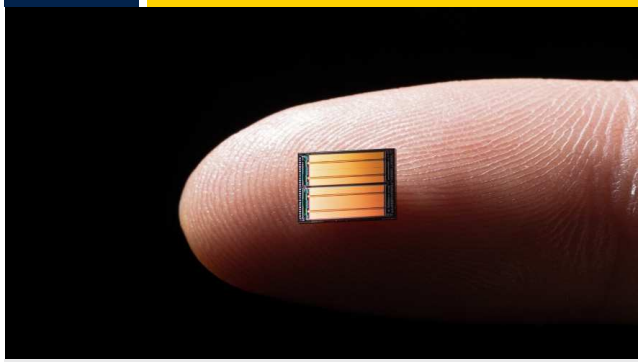
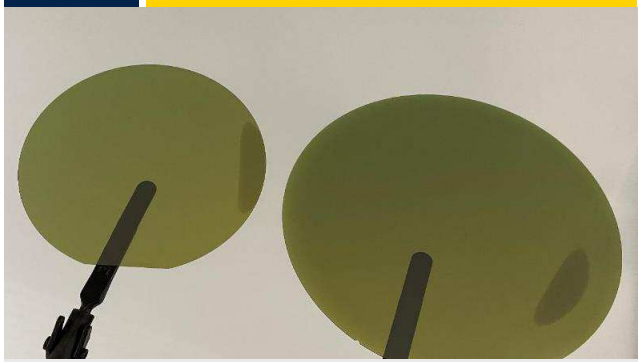
SiC MOSFET range in evolution

Gen3 — Planar technology



- Planar technology
- Ron*A FoM:
  - 750 V (1.8 mΩ*cm²)
  - 1200 V (2.8 mΩ*cm²)
- 650 V, 750 V, 900 V, 1200 V
- Technology qualified
- In full production

Gen4 — Planar technology with pitch reduction



- Ron: lower vs. Gen3
- Integrated Rg, lower driving voltage, possibility for large die, and current and temp. sensors
- Same processes as Gen3
- Commercial maturity by Q3 2024

Gen5 — Planar technology smallest achievable pitch

- Very high-density structure
- 15 V & 18 V driving options
- Further Ron reduction vs Gen4
- Thinner die
- Development to be started at 8”
- Technology qualification by Q2 2025

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More on planar technology

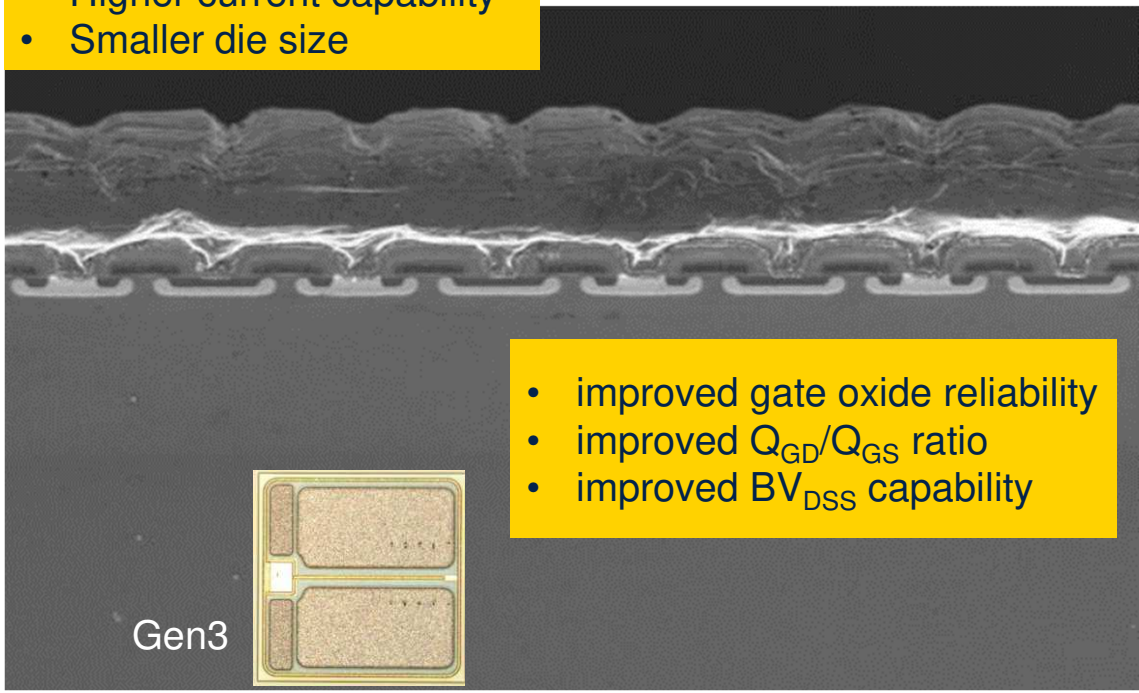
Simple process → High manufacturability

Scalability
High channel mobility → Lowest Ron*area

Low intrinsic capacitance → Best dynamic performance

Gate oxide protected to high electric field → High reliability in application

- Higher strip density,
- Lower Ron*A,
- Higher current capability
- Smaller die size



- improved gate oxide reliability
- improved Q_{GD}/Q_{GS} ratio
- improved BV_{DSS} capability

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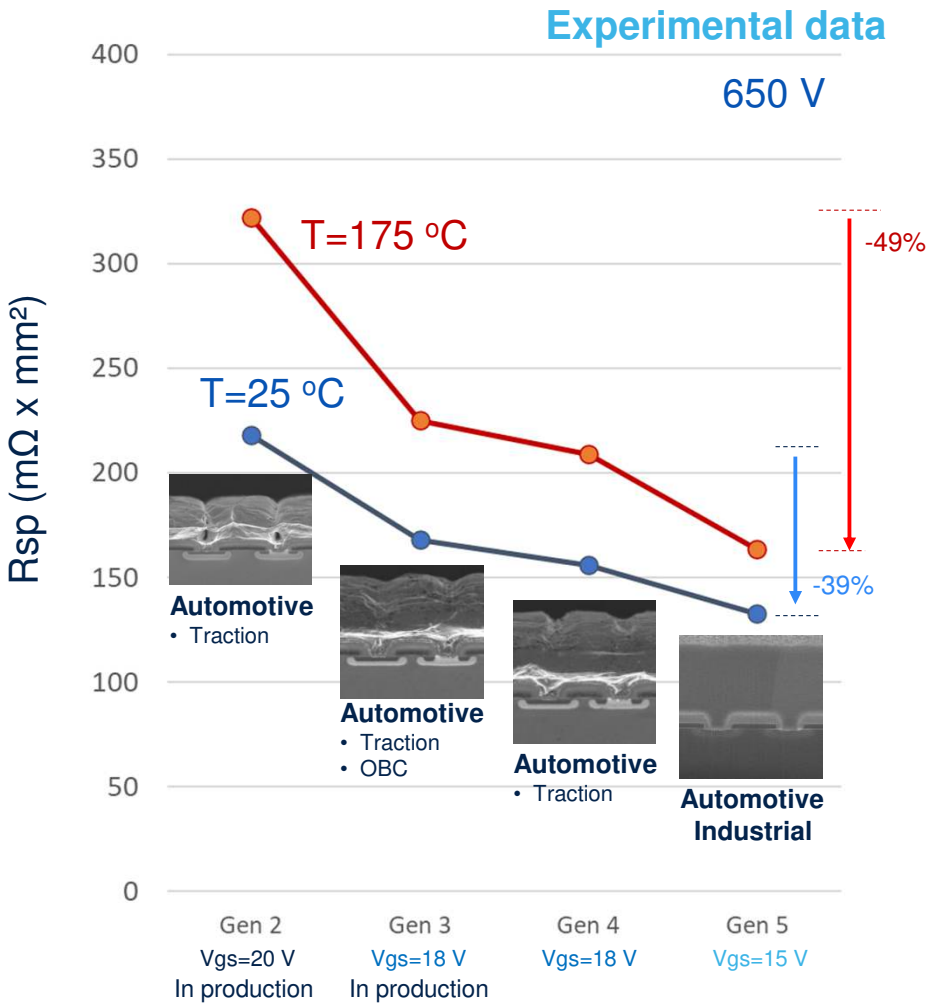
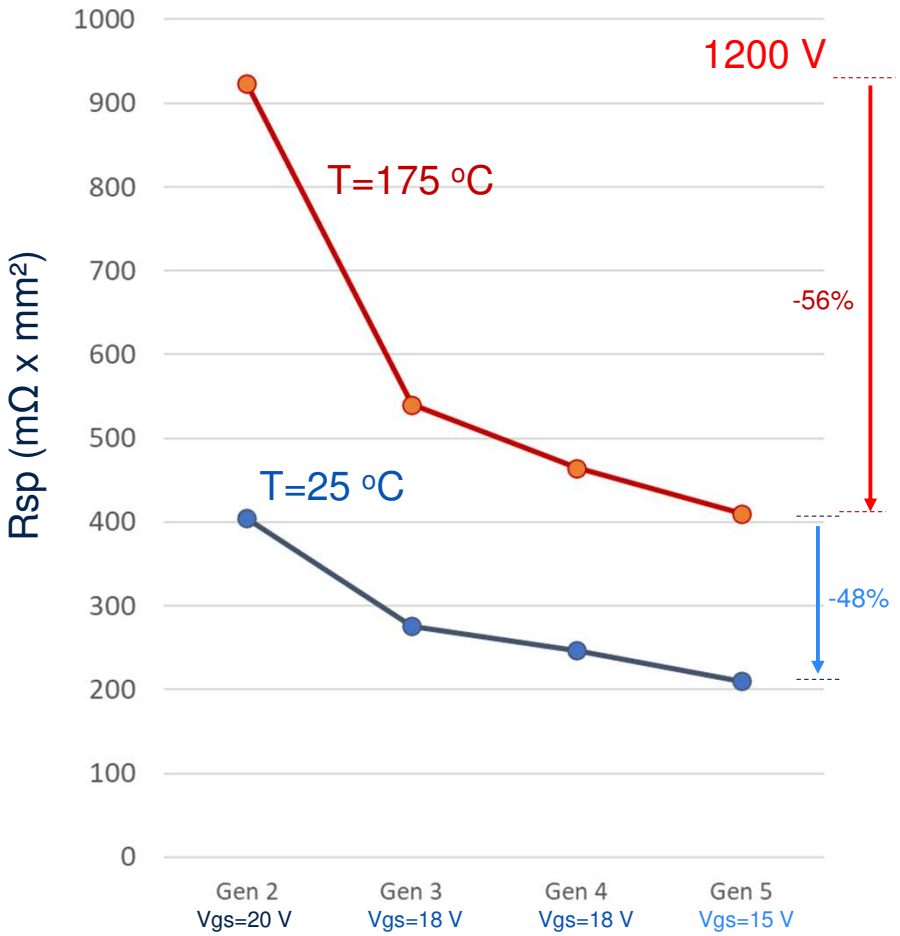
SiC planar MOSFET technology evolution

Experimental data





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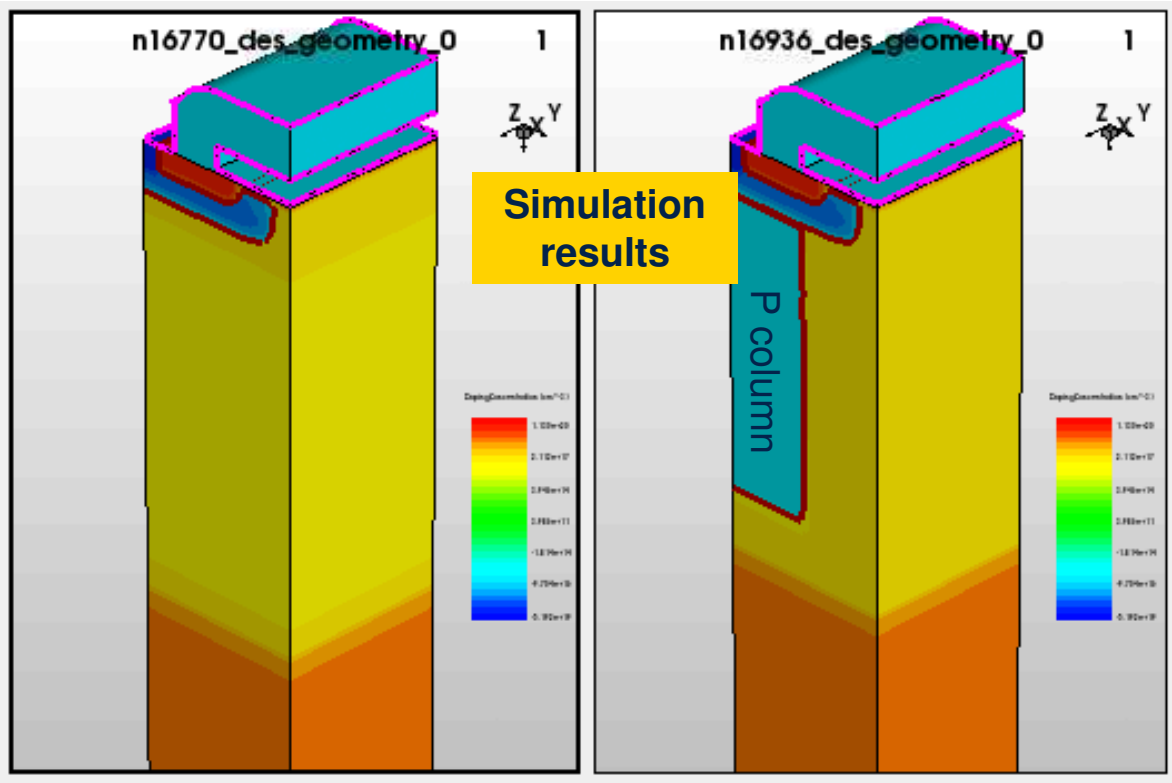
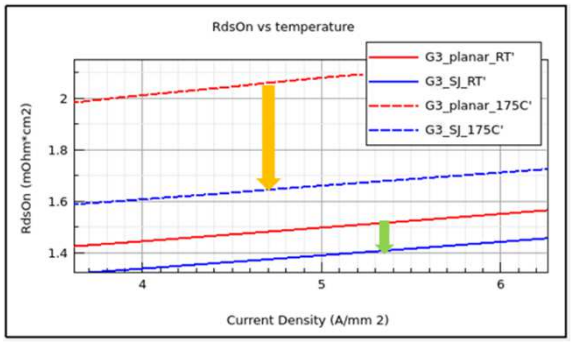
Coming technology: MDSiC in superjunction structure



Planar

Charge balanced drain



IV simulation

	RT	175°C
650 V	- 7%	- 20%
1200 V	- 34%	- 59%

Comparison with same planar structure

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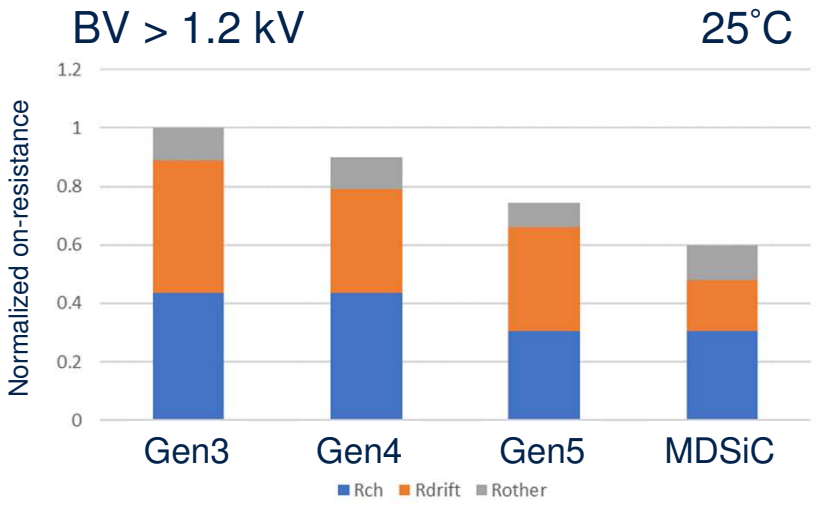
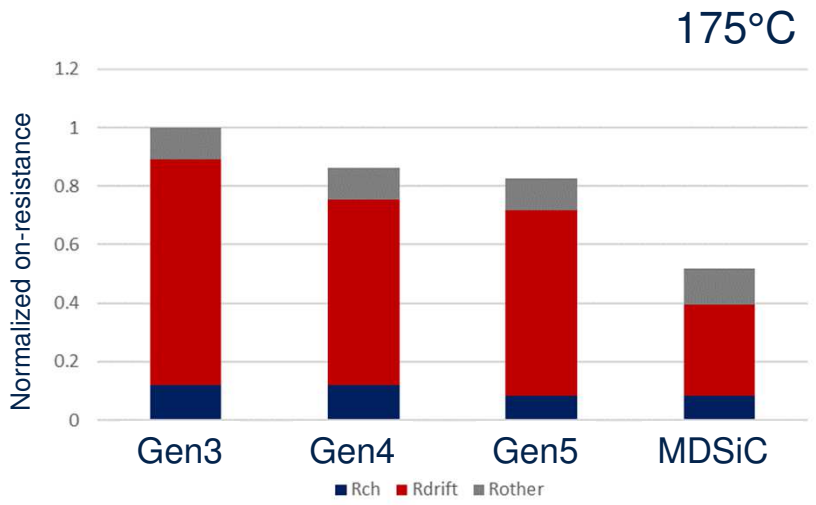
On-resistance devices
Impact on temperature performance





Planar technology evolution improves RT performance by acting on channel resistance component

Multidrain (MDSiC) improves HT performance by acting on drain resistance component

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SiC package technologies

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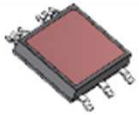
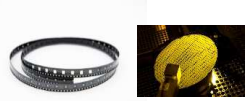
SiC MOSFET package technologies

PowerFLAT 8x8 STD & DSC	TO-LL	H2PAK-7L	HU3PAK	ACEPACK SMIT	HiP247 (3 ,4, long leads)	STPAK	Bare dice
							

Surface mounting					Through-hole	Special package solutions	
Very thin (< 1mm) Well accepted in power conversion Dual-side cooling option Leadless **Industrial domain**	**2.4 mm** (max) thickness Good Rthj-a performance Leadless **Industrial domain** **Kelvin source** for optimized driving Good thermal dissipation	**AG qualified at 175°C** Kelvin source for optimized driving High runner for automotive customers	**AG qualified at 175°C** **Top side cooling** Kelvin source for optimized driving Very good thermal dissipation	AG qualified at 175°C Isolated top side cooling Suitable for different configurations (HB, dual die, etc.) High power Modular approach	**AG qualified at 200°C** **Very common industry standard** Kelvin source option for optimized driving High creepage version (1700 V) in development	**Unique solution for traction inverter** **AG qualified at 200°C** **Very high thermal dissipation efficiency** Sense pin for optimized driving Multisintered package	**WLBI & KGD** **T&R or RWF options** **Compliant with the most stringent automotive quality requirements**

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Updated to correspond to latest figures

The evolution of ST's market position in SiC

Over 100 customers and over 170 programs awarded

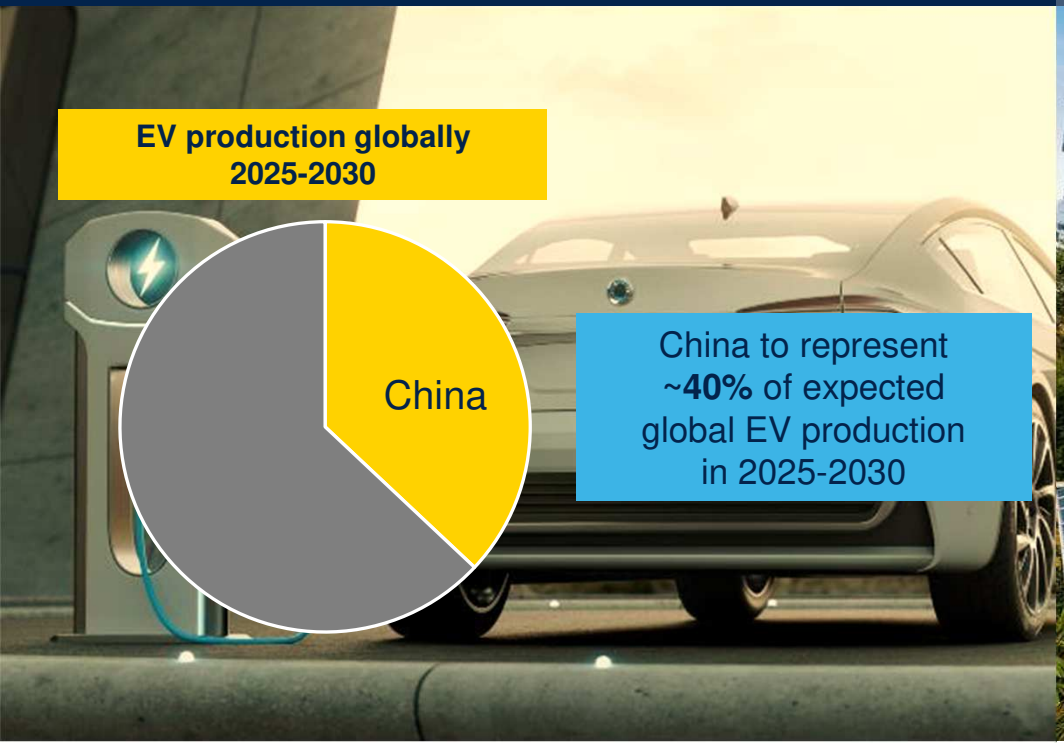
ST market position in SiC

- **$1.14B revenues in 2023 (+60% vs. 2022)**
- **$5B+ revenue opportunity by 2030**
- **>40% market share in SiC MOSFETs and modules**

Source: Omdia

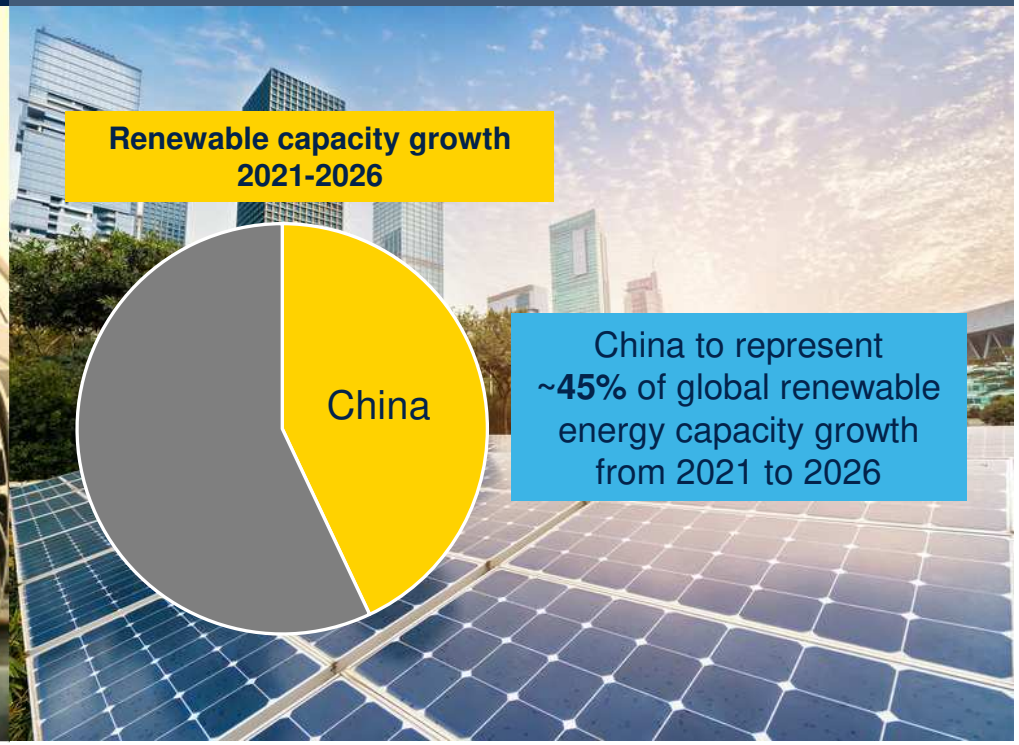
China is a major market for silicon carbide

Automotive electrification



Source LMC Automotive, 2023

Power & Energy



Source IEA, 2022

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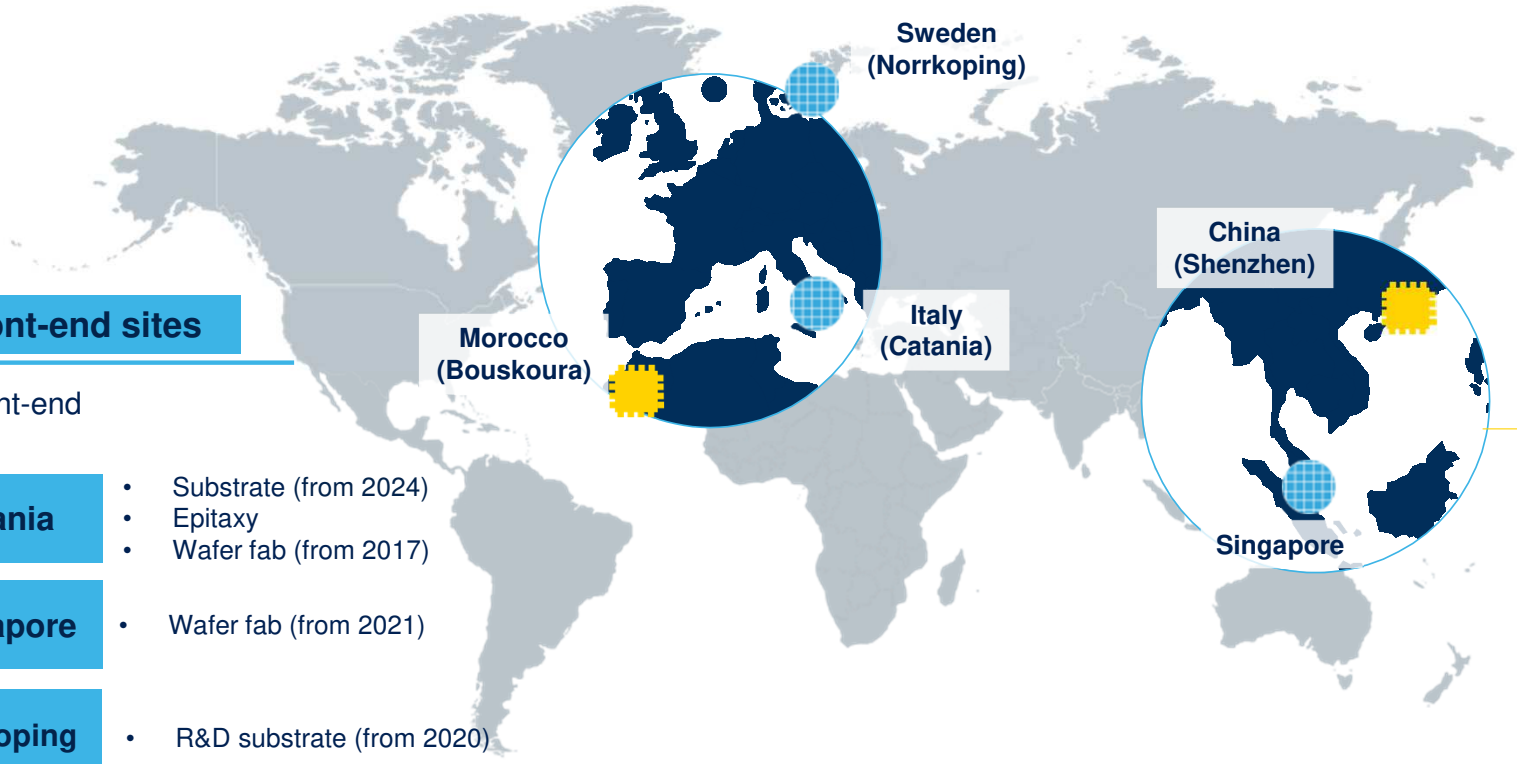
ST silicon carbide manufacturing operations



3 x front-end sites

Front-end

Catania	• Substrate (from 2024) • Epitaxy • Wafer fab (from 2017)
Singapore	• Wafer fab (from 2021)
Norrkoping	• R&D substrate (from 2020)

2 x back-end sites

Back-end

- **Shenzhen**
- **Bouskoura**

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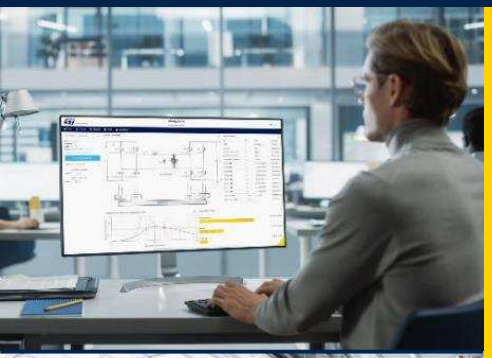
ST is in an integrated device manufacturer (IDM)

Full control and optimization of the value chain



Integrated Device Manufacturer (IDM)

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- Process development and qualification
- Chip design
- Wafer fabrication
- Assembly & test
- Sales & support

Fabless semiconductor company

Semiconductor foundry

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Vertically integrating for supply chain robustness

Raw material → SiC ingots & substrates → SiC dice manufacturing → discrete/module design & manufacture → Finished products

Norrköping SiC substrate R&D plant

- 150 mm production
- 200 mm with industrial quality and yields

Catania new integrated SiC plant

- Pilot production started in 2023*
- 150 mm substrates + epitaxy (converting to 200 mm)

* targeting > 40% substrate in-sourcing by 2024

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ST and Sanan Optoelectronics joint venture agreement

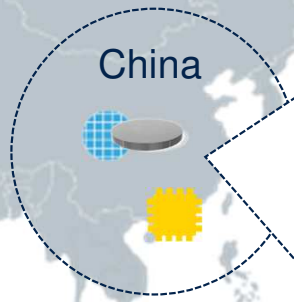
ST and Sanan Optoelectronics have signed an agreement to create a 200mm silicon carbide (SiC) device manufacturing Joint Venture (JV) in Chongqing, China

Supporting the rising demand for **car electrification and industrial power and energy** applications in China

Production to start in **Q4 2025** and **full buildout** is expected **in 2028**

JV to serve as a **dedicated foundry** to ST for its Chinese customers (China for China)

Sanan to build & operate separately a **200mm SiC substrate plant,** using its own SiC substrate process, to fulfill the JV needs



Substrate site (200 mm)

Substrate

Chongqing* (Sanan)

Front-end site (200 mm)

Epitaxy + front-end

Chongqing* (JV)

Back-end site

Back-end

Shenzhen (ST)

* FAB is under construction

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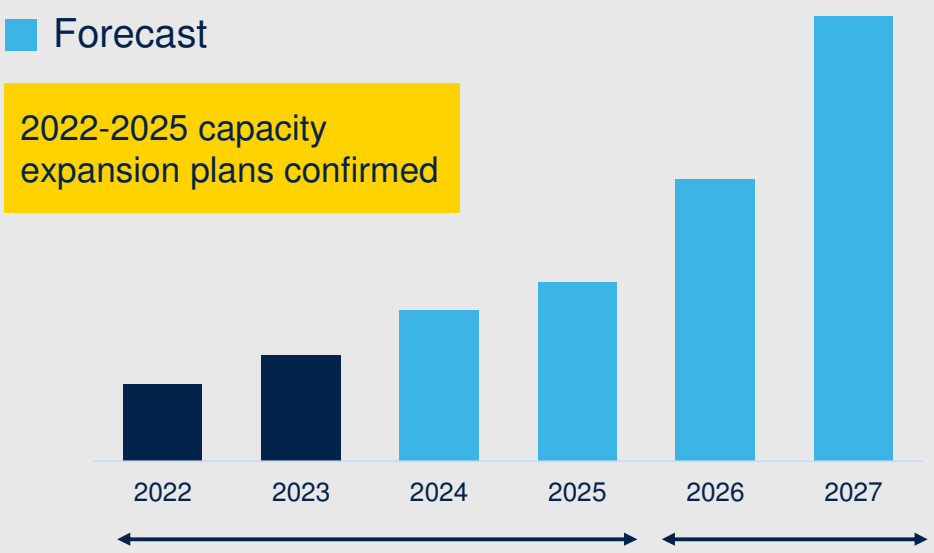
Expanding SiC device manufacturing capacity

Normalized front-end capacity evolution



Front-end fabs

Back-end fabs

Supported by investments in back-end capacity in Bouskoura and Shenzhen, and ramp of internal substrate manufacturing in Catania

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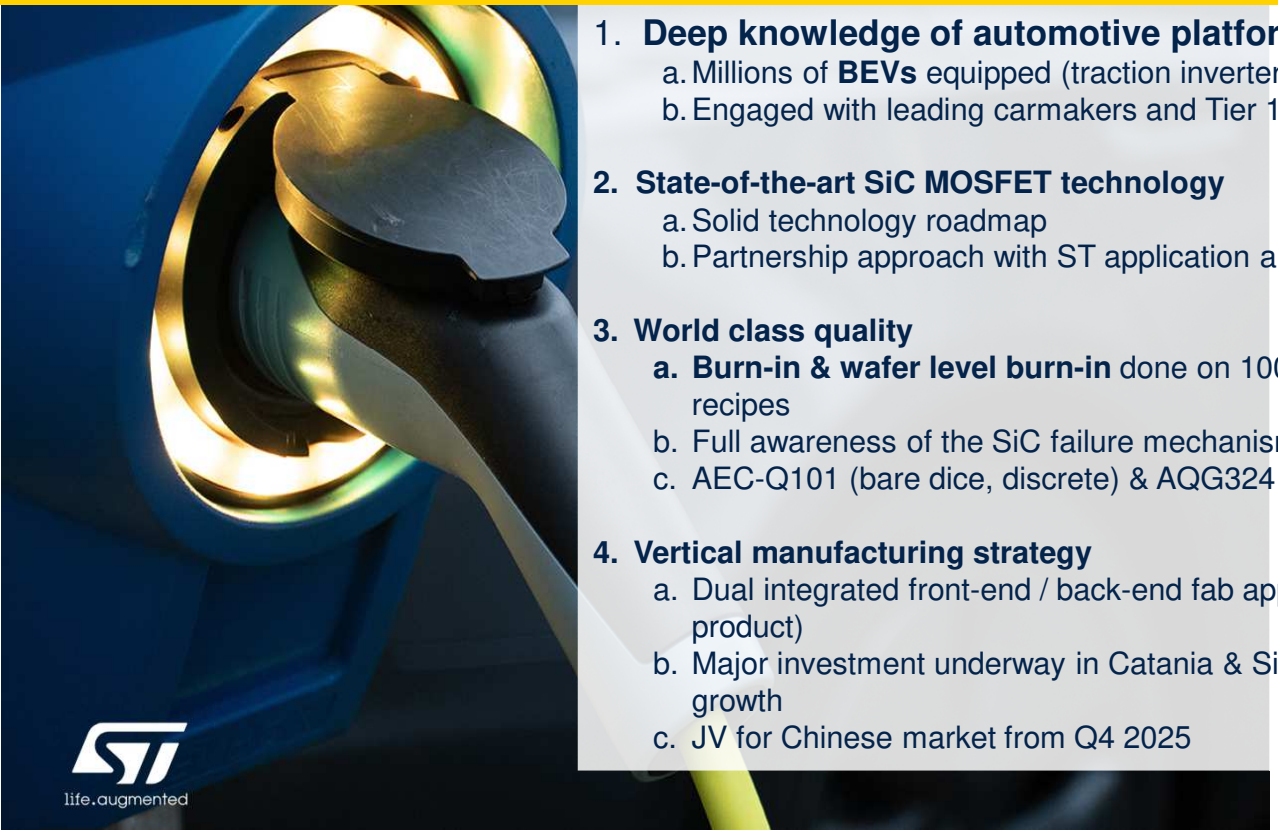
* JV with Sanan in China to address the local market

Removed the exact figures in point 1

Key Takeaways
Reasons to work with ST SiC MOSFET

ST is the best partner to grow in the electrification world



1. **Deep knowledge of automotive platforms**
   a. Millions of **BEVs** equipped (traction inverter & OBC/DC-DC) with ST SiC MOSFETs **since 2017**
   b. Engaged with leading carmakers and Tier 1 across the globe

2. **State-of-the-art SiC MOSFET technology**
   a. Solid technology roadmap
   b. Partnership approach with ST application and modeling technical support

3. **World class quality**
   a. **Burn-in & wafer level burn-in** done on 100% of shipped parts in series production with optimized recipes
   b. Full awareness of the SiC failure mechanisms
   c. AEC-Q101 (bare dice, discrete) & AQG324 (Modules) with additional robustness trials

4. **Vertical manufacturing strategy**
   a. Dual integrated front-end / back-end fab approach (from in-house substrate production to finished product)
   b. Major investment underway in Catania & Singapore front-end fabs to increase capacity and sustain growth
   c. JV for Chinese market from Q4 2025

Our technology starts with You

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