RF matching network design guide for STM32WL Series

Introduction

The STM32WL Series microcontrollers are sub-GHz transceivers designed for high-efficiency long-range wireless applications including the LoRa®, (G)FSK, (G)MSK and BPSK modulations.

This application note details the typical RF matching and filtering application circuit for STM32WL Series devices, especially the methodology applied in order to extract the maximum RF performance with a matching circuit, and how to become compliant with certification standards by applying filtering circuits.

This document contains the output impedance value for certain power/frequency combinations, that can result in a different output impedance value to match. The impedances are given for defined frequency and power specifications.

1 General information

This document applies to the STM32WL Series Arm®-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Table 1. **Acronyms**

Acronym	Definition
BALUN	Balanced to unbalanced circuit
BOM	Bill of materials
BPSK	Binary phase-shift keying
(G)FSK	Gaussian frequency-shift keying modulation
(G)MSK	Gaussian minimum-shift keying modulation
GND	Ground (circuit voltage reference)
LNA	Low-noise power amplifier
LoRa	Long-range proprietary modulation
PA	Power amplifier
PCB	Printed-circuit board
PWM	Pulse-width modulation
RFO	Radio-frequency output
RFO_HP	High-power radio-frequency output
RFO_LP	Low-power radio-frequency output
RFI_N	Negative radio-frequency input (referenced to GND)
RFI_P	Positive radio-frequency input (referenced to GND)
Rx	Receiver
SMD	Surface-mounted device
SRF	Self-resonant frequency
SPDT	Single-pole double-throw switch
SP3T	Single-pole triple-throw switch
Tx	Transmitter
RSSI	Received signal strength indication
NF	Noise figure
Z_{OPT}	Optimal impedance

References

[1] T. S. Bird, *"Definition and Misuse of Return Loss [Report of the Transactions Editor-in-Chief],"* in IEEE Antennas and Propagation Magazine, vol. 51, no. 2, pp. 166-167, April 2009.

[2] Banerjee, Amal. *Automated broad and narrow band impedance matching for RF and microwave circuits*. Cham, Switzerland: Springer, 2019.

[3] White, Joseph F. *High frequency techniques: an introduction to rf and microwave design and computer simulation*. Place of publication not identified: John Wiley, 2016.

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[5] Ludwig, Reinhold, and Pavel Bretchko. *RF circuit design: theory and applications*. Upper Saddle River, New Jersey: Prentice-Hall, 2000.

[6] Khan, Ahmad S. *Microwave engineering: concepts and fundamentals*. Boca Raton: CRC Press, Taylor and Francis Group, 2014. Print.

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[9] Steer, Michael B. *Microwave and RF design: networks*. NC State University: University of North Carolina Press, 2019. Print.

[10] Ghannouchi, Fadhel M., and Mohammad S. Hashmi. *Load-pull techniques with applications to power amplifier design*. Dordrecht New York: Springer, 2013. Print.

2 RF basics

2.1 RF terminology

2.1.1 Power

The power is the measure of the RF signal, often expressed in dBm, calculated from P (in mW) by the following formula:

$$dBm = 10 \times \log_{10}\left(\frac{P}{1\,mW}\right)$$

2.1.2 Gain

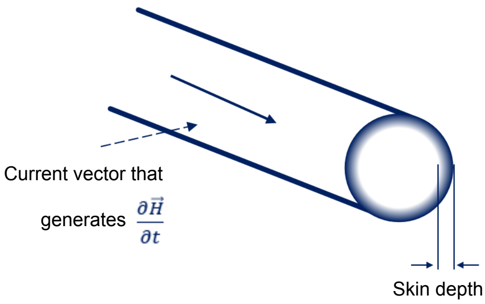
The gain is the ratio of the output power of an amplifier device, to the input power (expressed in dB).

2.1.3 Loss

In RF, the losses are divided in two types:

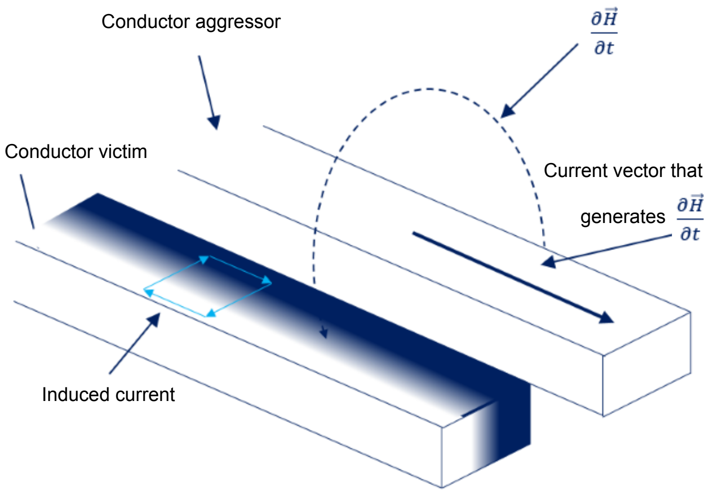
- Losses by mismatch due to impedance mismatch or incorrect transmission line design
- The ohmic losses due to:
  - dielectric loss that depends on the laminate and pre-impregnated materials used in the board manufacturing .
  - conduction loss:
    - skin effect, the most common source of ohmic loss in RF (resistance increasing with frequency)

Figure 1. Skin effect



    - proximity effect (resistance increasing due to magnetic field interaction between conductors)

Figure 2. Proximity effect



In both cases, not all power is transmitted from one stage to the next, and therefore less power is radiated by the antenna.

2.1.4 Reflection coefficient (Γ), voltage standing wave ratio (VSWR) and return loss (RL)

When a signal flows from a source to a load via a transmission line, if there is a mismatch between the characteristic impedance of the transmission line and the load, then a portion of the signal is reflected from the load to the source.

Remember: In most cases an RF load (here represented by Z_L or just the word "load") is usually an antenna.

The polarity and the magnitude of the reflected signal depends on whether the load impedance is higher or lower than the line impedance.

The reflection coefficient (Γ) is the measure of the amplitude of the reflected wave versus the amplitude of the incident wave. It can also be described in terms of load impedance (Z_L) and the characteristic impedance of the transmission line (Z_0) as shown below.

$$\Gamma = \frac{V^-}{V^+} = \frac{Z_L - Z_0}{Z_L + Z_0}$$

The voltage standing wave ratio (VSWR or just SWR, pronounced "viswar") is the measure of the accuracy of the impedance matching at a point of connection. VSWR is defined as the maximum voltage by the minimum voltage ratio of the standing wave on the line. It can also be expressed as a function of the reflection coefficient ratio, as follows.

$$VSWR = \frac{V_{Z\max}}{V_{Z\min}} = \frac{1+\Gamma}{1-\Gamma}, \qquad 1 \leq VSWR \leq \infty$$

If VSWR = 1.0, there is no reflected power.

The return loss (RL) is a function of the reflection coefficient but expressed in dB.

$$RL = 10 \times \log_{10}\left(\frac{P_{incident}}{P_{reflected}}\right) = P_{incident} - P_{reflected}$$

$$\Rightarrow P_{reflected}\ (in\ \ dB) = P_{incident}\,(in\ \ dB) - RL$$

$$\Rightarrow P_{reflected}\,(in\ \ dB) = P_{incident}\,(in\ \ dB) - RL$$

Numerically, RL has a value between 0 dB and ∞. When RL = 0 dB, the reflected power is equal to the incident power and no power reaches the load. The RL is always positive (see document [1]).

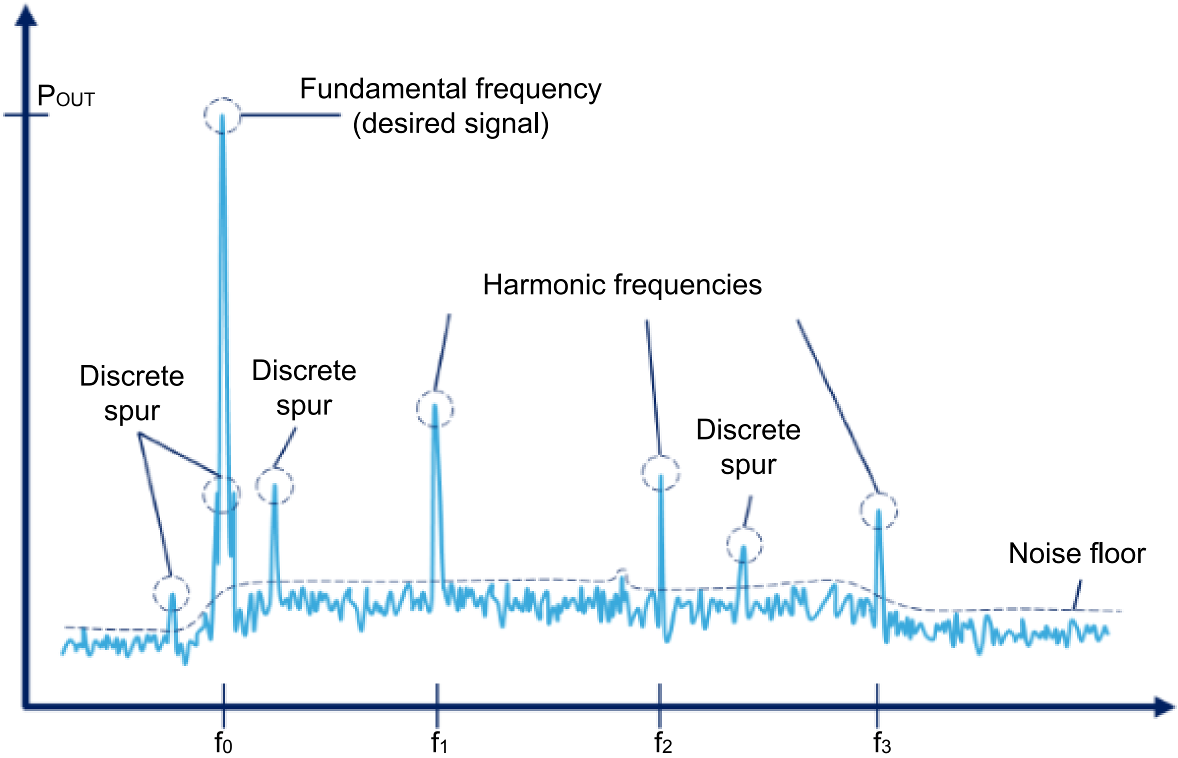
See Appendix B for numerical representation of these quantities.

2.1.5 Harmonics and spurious

The harmonics are the integer multiples of input or output frequency (fundamental frequency).

The spurious are the non-integer multiples of input frequency (unwanted frequencies).

Figure 3. Representation of fundamental signal, harmonics and spurious power over frequency



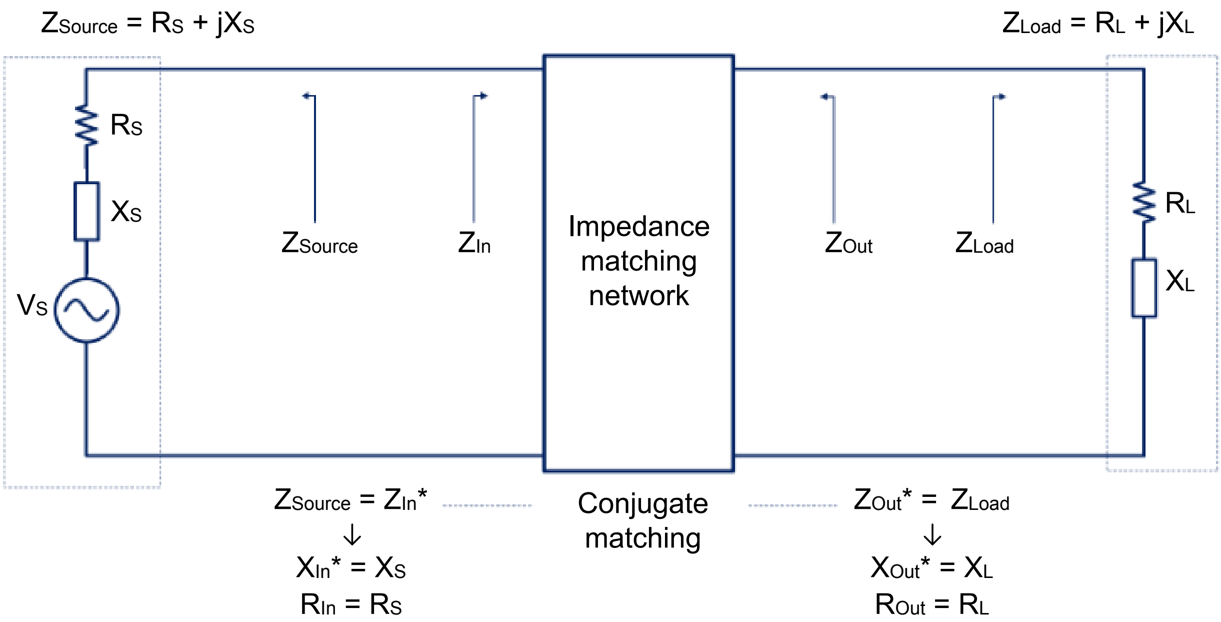
2.2 Impedance matching and Smith chart

In RF, the reference impedance has a real value of 50 Ω. In some cases, due to design or technology constraints, the optimum impedance of the PA (power amplifier) and/or the optimum impedance of the LNA (low-noise amplifier) are usually never at 50 Ω. This is the reason why an impedance matching network must be designed.

The impedance matching is a technique to guarantee that maximum/optimum signal power is transferred from the signal source to the receiving device, to ensure minimum signal power reflection back to the source. The matching is done by a reactive network.

The figure below does not represent the transmission line (assuming Z_0 = 50 Ω).

Figure 4. Conjugated impedances presented by an impedance matching network between the source impedance (such as RF PA) and the load impedance (such as an antenna)

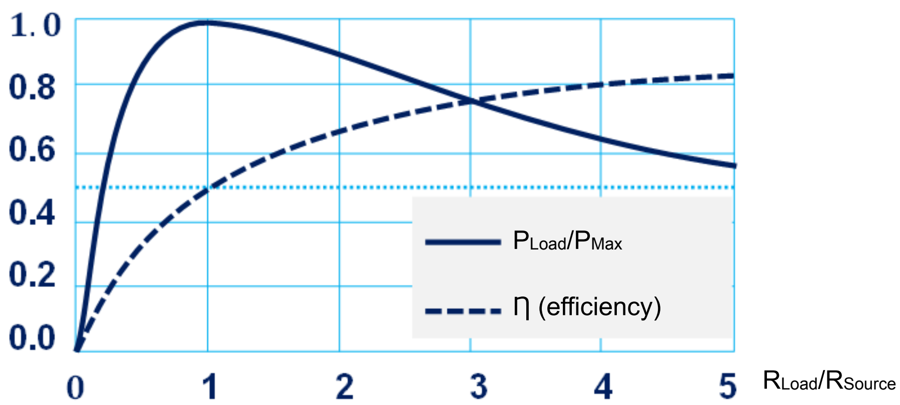


According to the document [2], no electronic signal processing circuit (especially those operating at hundreds of MHz and tens of GHz, such as telecommunication/wireless communication equipment or consumer electronic devices) can operate without impedance matching between its sub-circuits.

There are two types of impedance matching: broad/wide and narrow bands. Broad/wide impedance matching is more difficult to achieve.

In the figure below, when the ratio between R_{LOAD} and R_{SOURCE} is equal to 1, the maximum power is transferred by the source to the load with an efficiency of 50 %.

Figure 5. Relationship between power at load and maximum power delivered by the source



The optimum impedance matching for PA or LNA can be calculated or simulated, but very often a fine tuning is needed. To perform this impedance tuning, a spectrum analyzer is used to measure the output power after implementing the matching network.

2.2.1 Normalized impedance

The impedance values on the Smith chart are normalized by a known value that is the characteristic impedance of the transmission line (usually 50 Ω). To normalize an impedance value, both real and imaginary part are divided by the reference value, as in the following example.

$$Z = (R + jX)\ \Omega \quad \Rightarrow \quad \frac{Z}{Z_0} = \frac{R}{Z_0} + j\frac{X}{Z_0} \Rightarrow z = r + jx \quad (unitless)$$

where Z_0 is the characteristic impedance of the transmission line.

Note: Uppercase letters are used to represent the value without normalization, while lowercase letters are used to represent the normalized values.

When reading an impedance value on Smith chart, do not forget to de-normalize the value by multiplying by Z_0.

Example

If the read value is 0.5 + j0.2, the impedance value is 25 + j10. To convert the imaginary part X (reactance) of the impedance read on the Smith chart, use the following formulas:

- For a negative value (capacitive reactance):

  $$C = \frac{1}{2\pi f \times Z_0 \times X}$$

  if Z_0 = 50, f = 915 MHz, and the value read is -0.3, the capacitor value is C = 11.60 pF.

- For a positive value (inductive reactance):

  $$L = \frac{Z_0 \times X}{2 \times \pi \times f}$$

  if Z_0 = 50, f = 915 MHz, and the value read is 0.3, the inductor value is L = 2.6 nH.

2.2.2 Read a Smith chart

A Smith chart is represented with the normalized impedance graduations ($z = Z/z_0$).

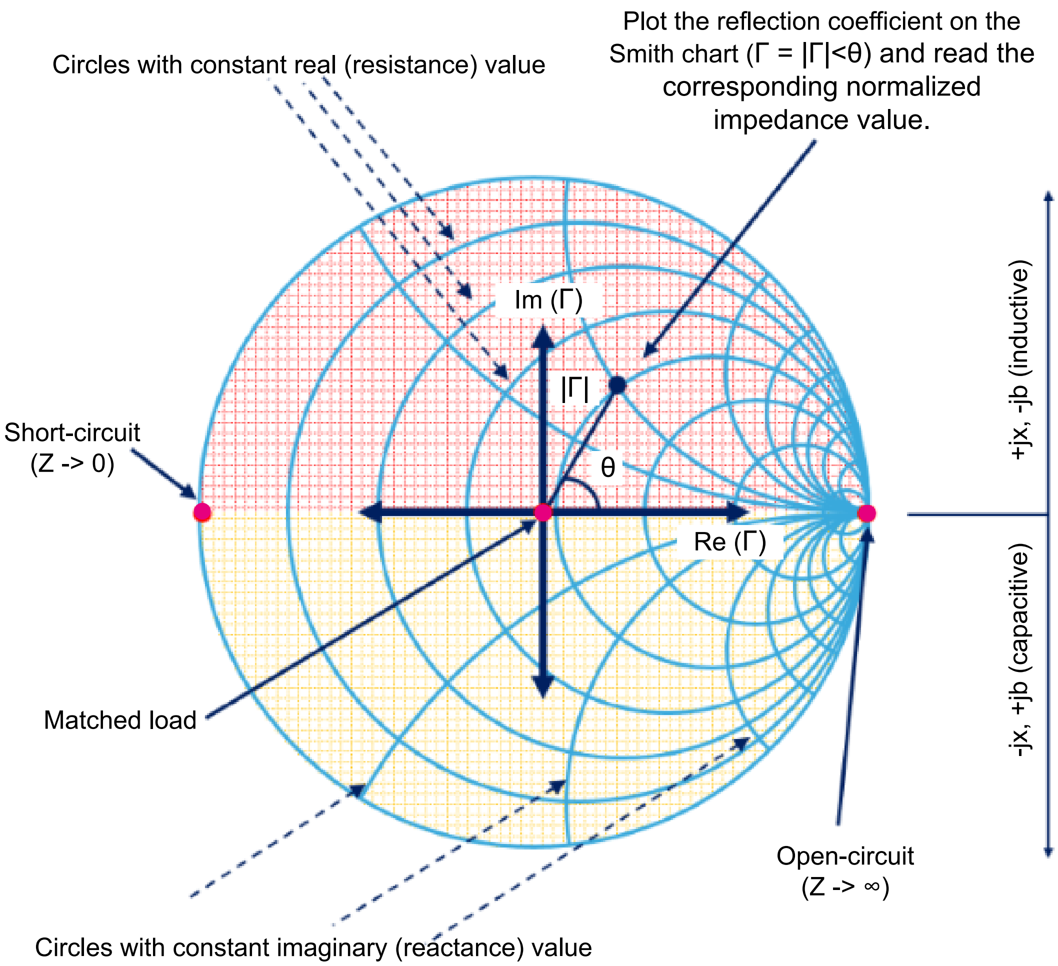
With Z_0 = 50 Ω, when there is matching, Z = z_0 , so the normalized impedance at 50 Ω is 1 and it is the center of the Smith chart.

The goal, when determining a matching network, is to converge towards the center of the Smith chart.

The figure below represents the Smith chart axis:

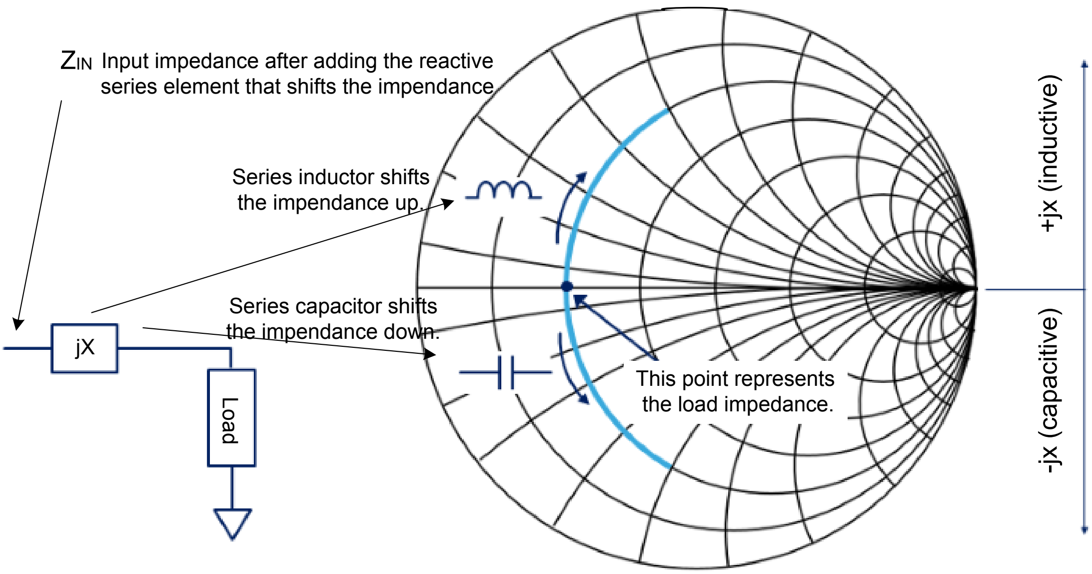
- The horizontal axis of the Smith chart represents a pure resistor: at the left side, z = 0 (short circuit) and at the right side z = ∞.
- The upper section (red part) of the horizontal axis represents impedances with positive imaginary part (series inductor +jx or parallel capacitor -jb).
- The lower section (yellow part) of the horizontal axis represents impedances with negative imaginary part (series capacitor +jx or parallel inductor -jb).

Figure 6. Simple representation of the Smith chart characteristics



The figure below shows the result when placing an inductor or capacitor in series with the load (or source impedance).

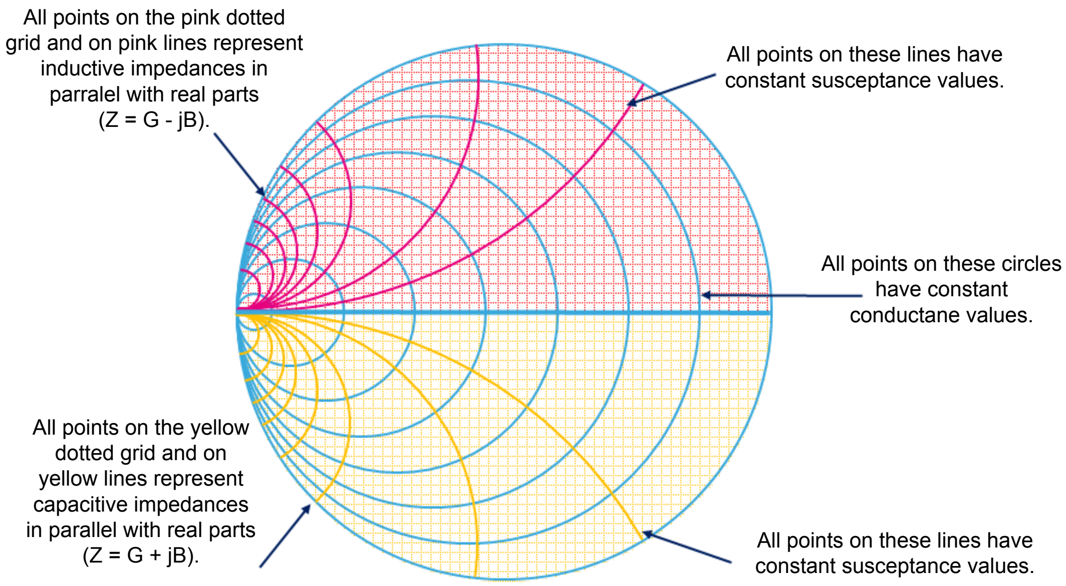
Figure 7. Illustration in Smith chart of how the impedance changes when adding a series capacitor or inductor



On the impedance Smith chart, the impedance is represented in the form: Z = R + jX.

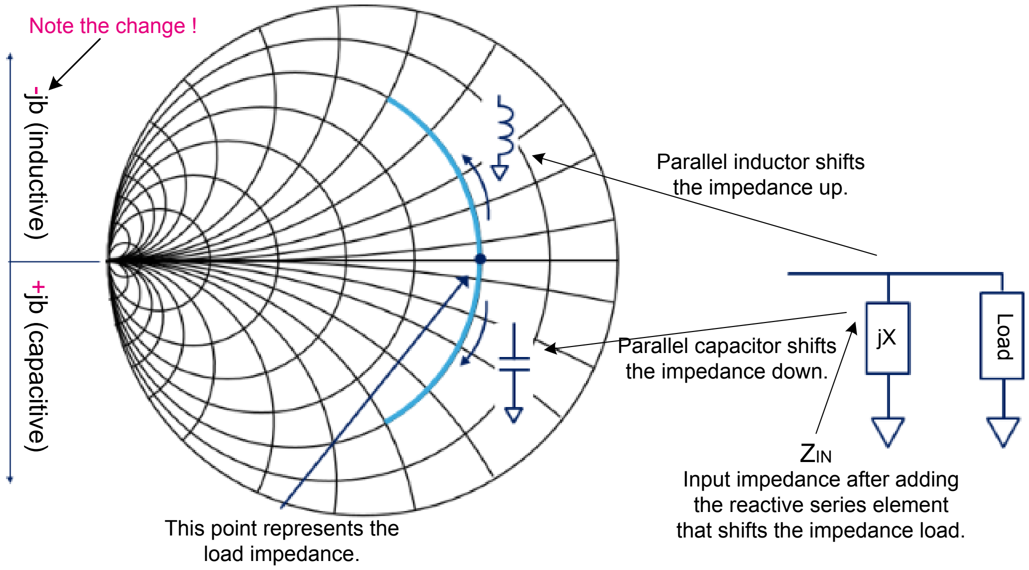
There is another “version” of the Smith chart when using parallel components: the admittance Smith chart. Its construction is like the impedance Smith chart; but “inverted” (see the figure below).

Figure 8. Admittance Smith chart



The figure below shows the result when placing an inductor or capacitor in parallel with the load (or source).

Figure 9. Illustration in Smith chart of how the admittance changes when adding a parallel capacitor or inductor



On the admittance Smith chart, the admittance in the form: $Y = G + jB$.

Remember: The relationship between impedance and admittance is $Z = 1/Y$ or $Y = 1/z$.

3 Choice of RF components

Discrete SMD components are often called "lumped components" in RF due to their behavior regarding the wavelength of the RF signal. On the other hand, there are the distributed components used in microwave engineering. In this application note, lumped components are mentioned, such as SMD inductors and capacitors.

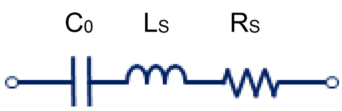
Even if the STM32WL devices operate in the sub-GHz bands, due to the necessity to be compliant with various regulations,spurious and harmonic content must be controlled, up to 10 GHz for some standards such as FCC (federal communication commission). Thus, passive lumped components used in the matching and filtering network, must be selected in order to have the right behavior (such as filter rejection). This section details the frequency limitation of SMD components and how their frequency response can become more complex.

3.1 RF capacitors

A capacitor is a passive electrical component used to store energy in an electrical field and differs from one another in construction techniques and materials used to manufacture. A lot of different types of capacitors exist (such as double-layer, polyester, or polypropylene) with different sizes.

An equivalent high-frequency circuit of a capacitor is represented in figure below.

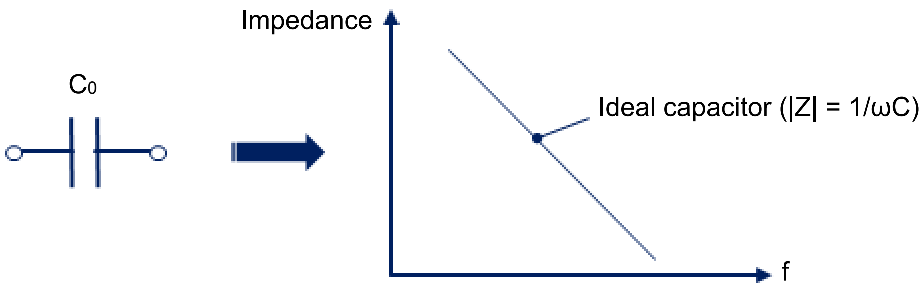
Figure 10. Equivalent high-frequency circuit of a capacitor



The resistor R_S is the equivalent series resistance (ESR) and represents all ohmic losses of the capacitor. The inductor L_S is the equivalent series inductance (ESL) and its value is function of the SRF (self resonant frequency).

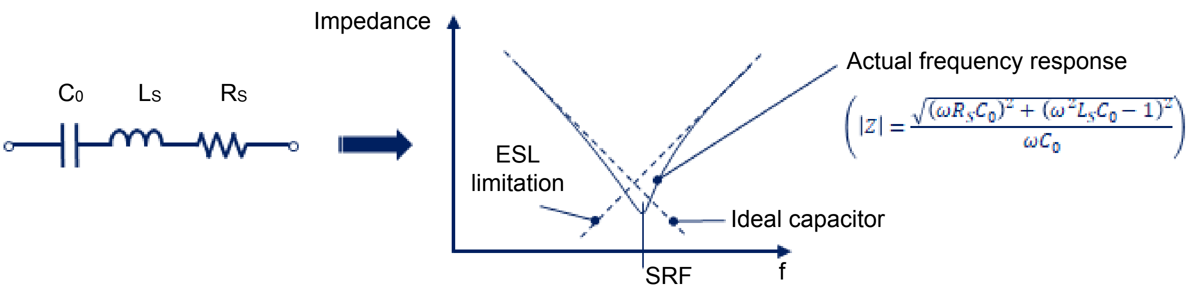
The ideal frequency response of a capacitor is shown in the figure below.

Figure 11. Ideal frequency response of a capacitor



Due to the parasitic effects, the real frequency response of the capacitor is shown in the figure below.

Figure 12. Real frequency response of a capacitor



Capacitors for high-frequency applications must have very small L_S and R_S to maintain the expected frequency behavior, otherwise the design may fail. For RF applications, it is important to know the frequency response of the capacitor before choosing it. For a very good capacitor, the parasitic L_S and R_S elements must be very small.

Note: Avoid capacitors close to the SRF.

For high-frequency applications, ceramic SMD capacitors Class I C0G/N0P with a high-quality factor are better (quality factor = Im(Z)/Re(Z)).

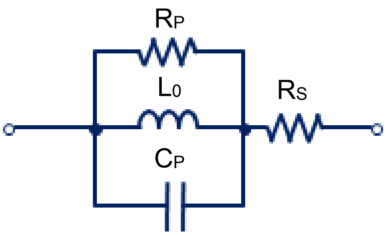
3.2 RF inductors

An inductor is a passive electrical component used to store energy in its magnetic field. Inductors differ from each other for construction techniques and materials used to manufacture.

For high-frequency applications where a high-Q factor is required in order to reduce insertion loss, it is generally recommended to use air-core inductors. Those inductors do not use a magnetic core made of ferromagnetic material, but coil wound on plastic, ceramic, or another nonmagnetic form.

The equivalent circuit of an inductor is represented below.

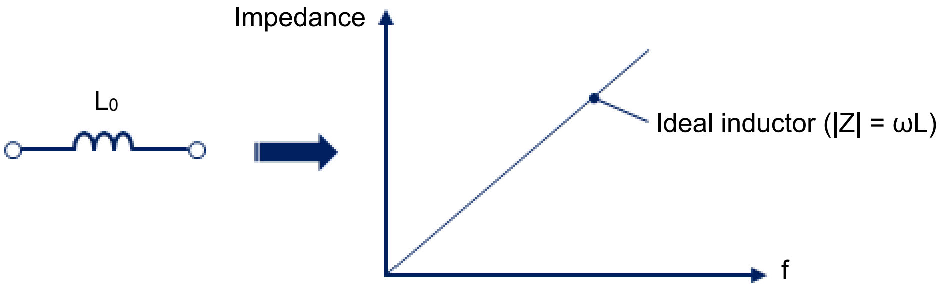
Figure 13. Equivalent circuit of an inductor



The resistor R_S represents the resistance due to the winding wire and terminations, and increases with temperature. The resistor R_P represents the magnetic core losses and varies with frequency, temperature and current. The capacitor C_P represents the capacitance due to winding of the inductor.

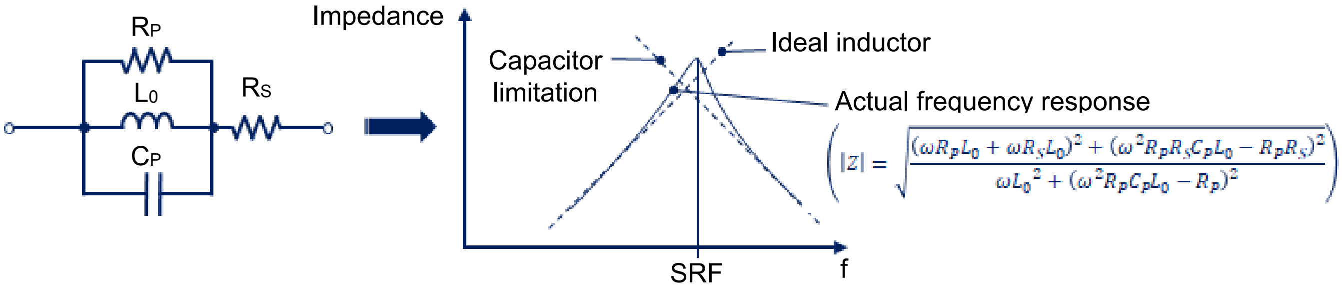
The ideal frequency response of an inductor is shown in the figure below.

Figure 14. Ideal frequency response of an inductor



Due to the parasitic effects, the real frequency response of the inductor is shown in the figure below.

Figure 15. Real frequency response of an inductor



For a very good inductor, the parasitic R_S and C_P elements must be very small, and R_P must be very high.

Note: *Avoid using inductors close to the SRF.*
For high-frequency applications, wire-wound SMD core less inductors with a high-Q factor are better.

4 STM32WL RF description

In this section, the Tx path (RF output) and Rx path (RF input) are described. The functionality of each part of the RF circuitry, plus how to build each part, are detailed.

4.1 Transmitter

The STM32WL transmitter includes a high-efficiency RF PA with two outputs (RFOs):

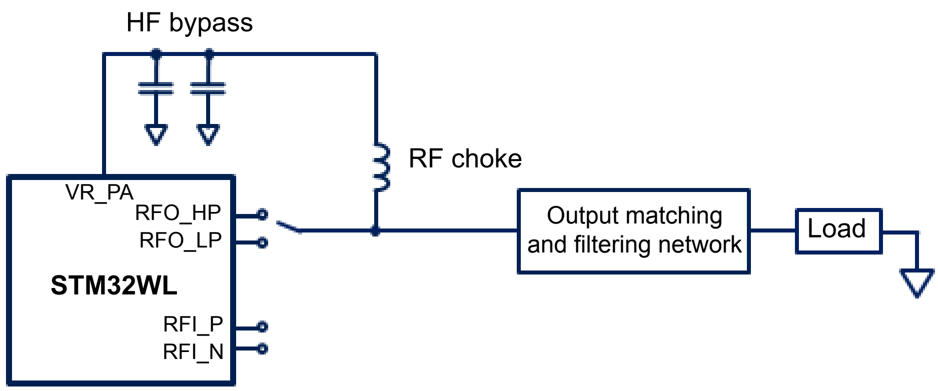
- high output power, programmable up to + 22 dBm (RFO_HP)
- low output power, programmable up to +15 dBm (RFO_LP)

In an application, the customer can choose to use an RF output (RFO) or both RFOs, using a DC switch for biasing circuit.

Note: Only one RFO can be used at a time.

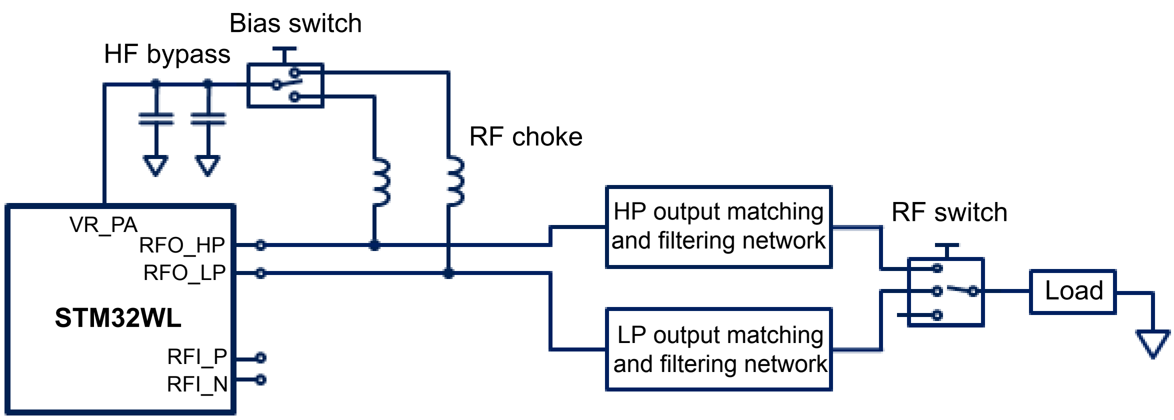
When using one RFO, only one RF Tx matching circuit is necessary as shown in the figure below. The matching network must be chosen for RFO_LP or RFO_HP configuration.

Figure 16. Example of choosing between RFO_HP or RFO_LP when the application is designed for only one RF output



When using the two RFOs, two RF Tx matching circuits are necessary as shown in the figure below.

Figure 17. Example of matching networks needed when the two RF outputs are used

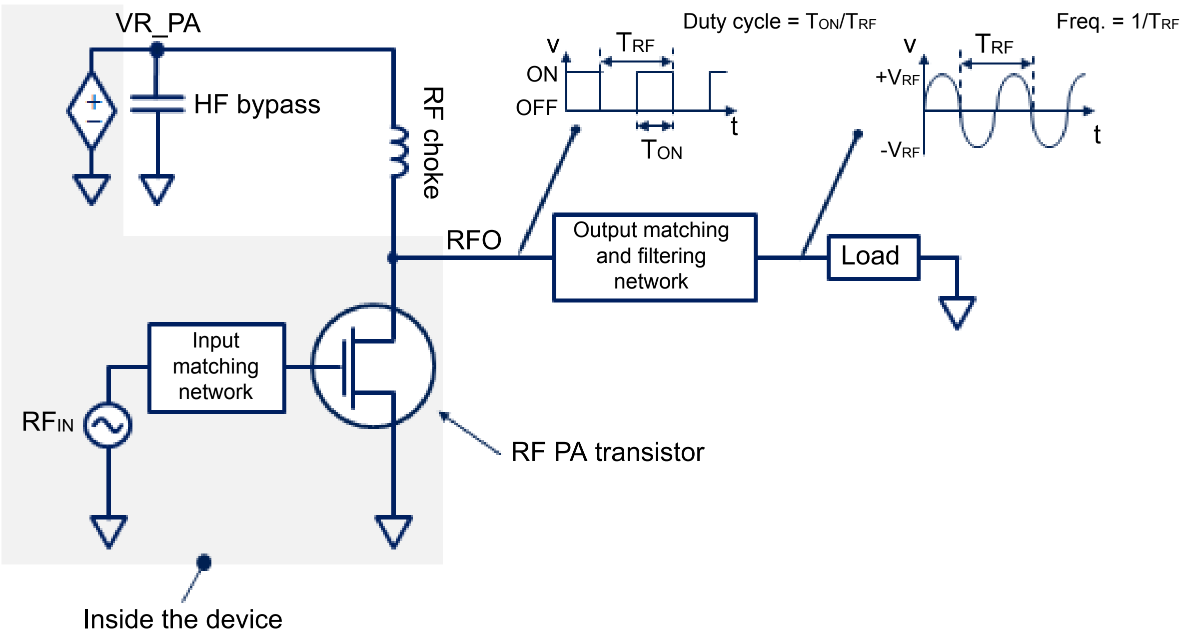


Another switch is necessary when using the two RF outputs for the bias circuit. This switch must ensure that, when using one RFO path, the other does not interfere. The RF choke or bias-feed inductor is always connected to the RFO that is being used, in order to provide the necessary voltage level and current to the RF circuit from VR_PA pin (regulated power amplifier supply). The RF PA must be always supplied by the VR_PA connection. One of the roles of the RF choke is to avoid that RF noise goes into the DC regulated PA supply inside the device (VR_PA pin). Since this RF choke impedance is never high enough (not ideal component), an amount of RF noise goes through this component into the VR_PA circuit. To “absorb” this leaking energy, high-frequency (HF) bypass capacitors are added between the VR_PA pin and the RF choke inductor.

The RF PA inside the device is made using a CMOS technology. The power amplifier acts more like a power-supply converter rather than a real amplifier. Since the PA MOS transistor is used as a switch, its output is connected to V_{DD} (ON state) or GND (OFF state), depending on the input-control signal generated by the amplifier control circuit. The PA output is a PWM high-frequency voltage signal, with its fundamental frequency being the RF sine waveform the user looks for.

The figure below illustrates this operation.

Figure 18. Top level representation of an RF PA inside the device (with the output waveforms)

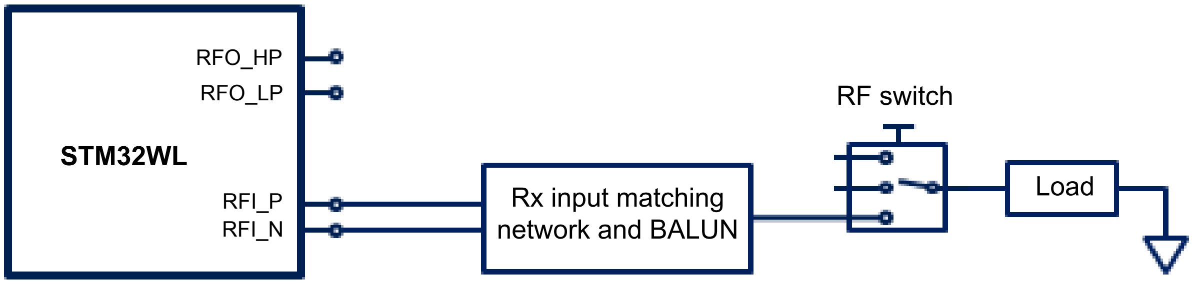


4.2 Receiver

The STM32WL receiver includes a high-performance differential LNA (low-noise amplifier) supporting LoRa, (G)MSK and (G)FSK modulations. The differential inputs (RFI_P and RFI_N) of this receiver support a maximum RF power of 0 dBm, with a sensitivity down to -148 dBm (see the product datasheet for more information).

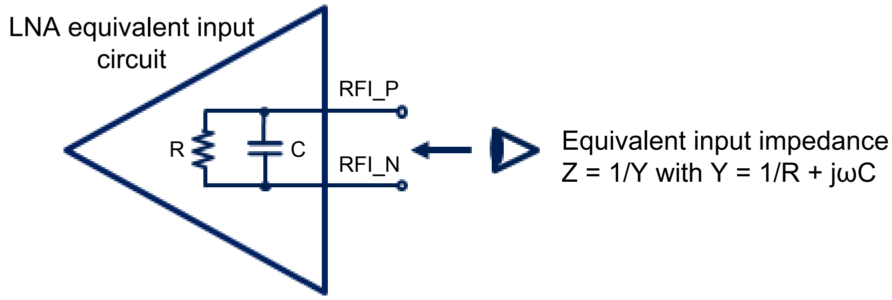
The interface between the LNA high input impedance and the 50 Ω circuit from the antenna side, is done by a matching network circuit, that, in addition, must convert a single-ended input to a differential output. The single-ended (referenced to a GND) circuit is often called unbalanced circuit and the differential circuit is often called balanced circuit. The circuit that converts a balanced circuit into an unbalanced circuit is called BALUN. Thus, the Rx matching network also plays the BALUN role.

Figure 19. **Diagram of Rx circuit with load**



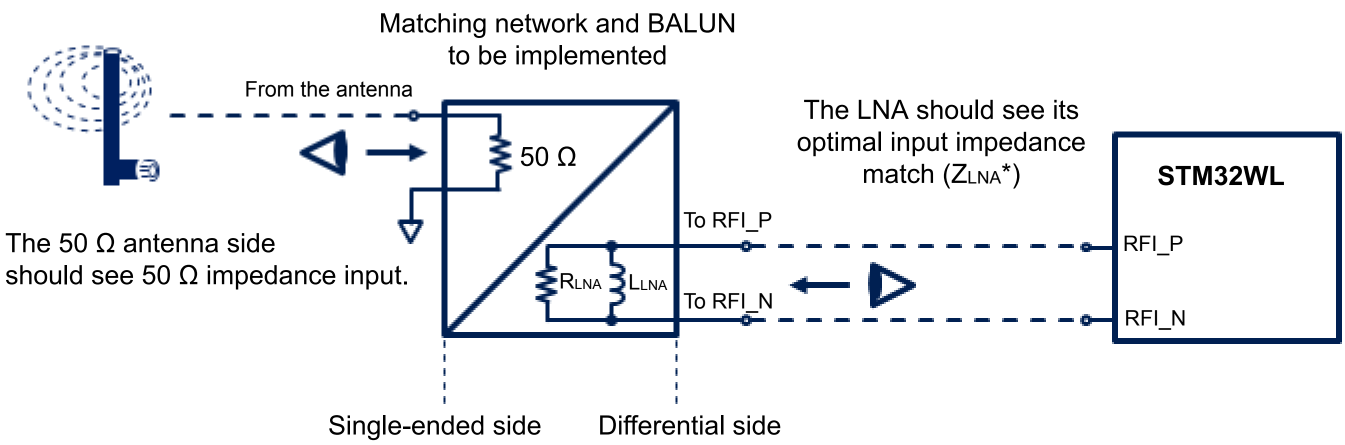
The equivalent input circuit of the LNA is represented in the figure below.

Figure 20. **Equivalent input circuit of the receiver**



The Rx matching network and BALUN that are described in this document, have the characteristics represented in the figure below.

Figure 21. **Matching network and BALUN characteristics to be implemented with lumped components on PCB**

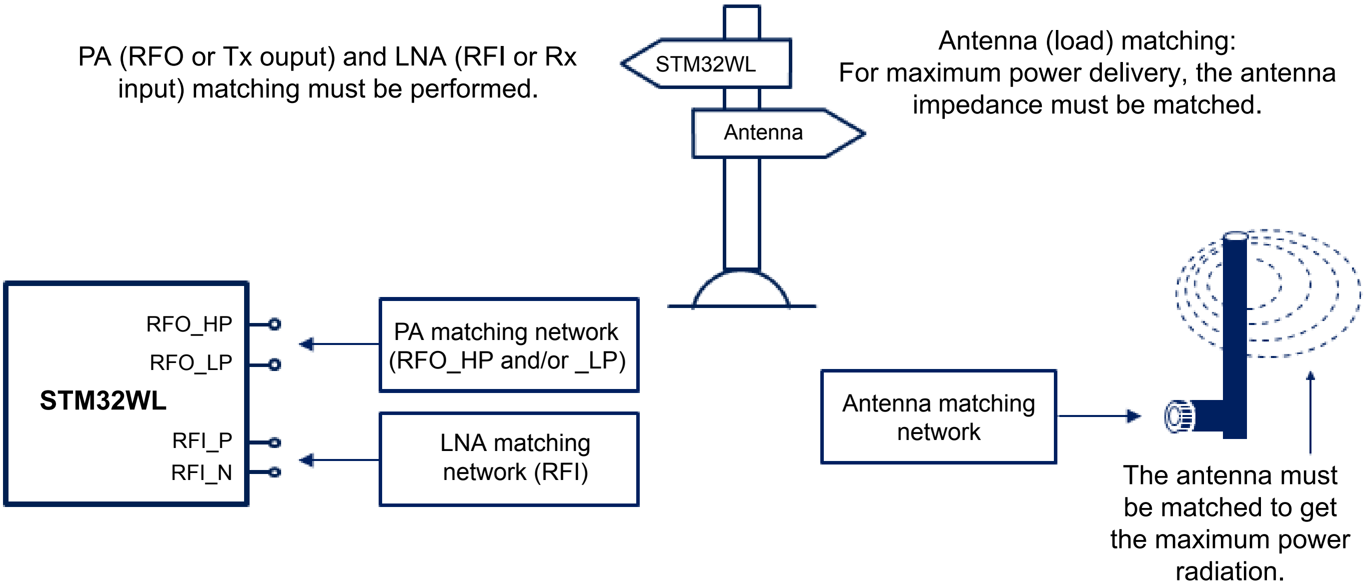


5 STM32WL matching and filtering network

The STM32WL works in half-duplex mode and, for better RF performances, an RF switch is used to isolate the T_X and R_X paths. The RF switch can be with two ports, to switch between one RFO (transmitter output) or RFI (receiver input), or three ports to switch between both RFO_HP (high power), and RFO_LP (low power) or RFI.

Two different impedance matching networks (in electrical engineering “network” is just a fancy name to say “circuit”) may be needed. One of them corresponds to the impedance matching network for the STM32WL PA and LNA. Another impedance matching network corresponds to the antenna. The antenna impedance matching network needs to be performed by the customer from the chosen antenna impedance. This document explains how to build the matching network for RFO (PA output) and RFI (LNA differential input). Using the same principle the customer can perform the impedance matching of the selected antenna.

Figure 22. **Illustration of the two possible matching networks to be implemented**



5.1 Power amplifier network

5.1.1 Equivalent output circuits

There are two different equivalent circuits to represent the PA output impedance. The figures below represent these two possibilities of equivalent output circuit. the equivalent output circuits of the PA is necessary to build the correct matching network.

Figure 23. **PA output equivalent circuit when its impedance is purely resistive**

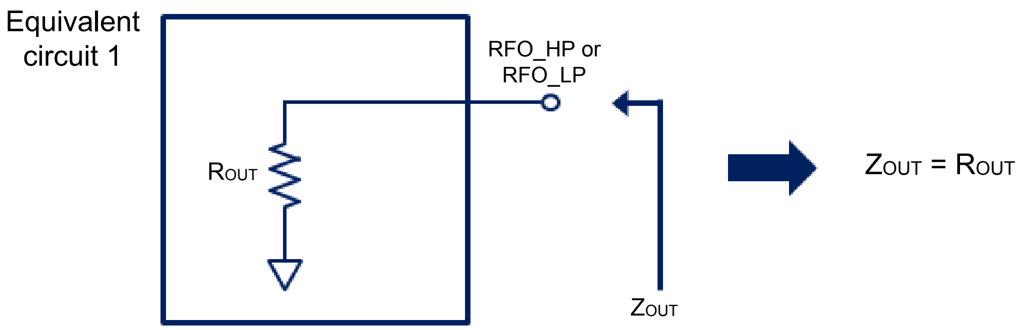
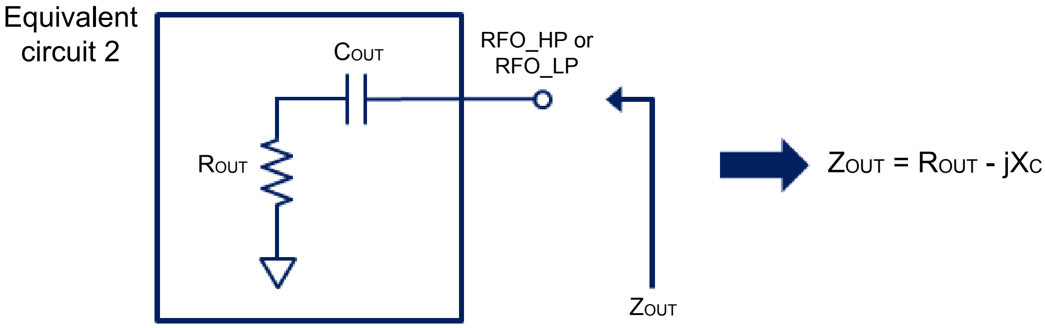


Figure 24. **PA output equivalent circuit when its impedance is resistive with a capacitive reactance**



The PA equivalent output circuit can be determined from the output impedance measurements provided in Appendix A.

Note: The PA output impedance depends on the operating frequency, power and the `PaDutyCycle`, `HpMax` and `PaSel` parameters passed through the `Set_PaConfig ()` command.

5.1.2 Optimal settings

There are some RF power amplifier (PA) configurations that maximize the efficiency of the PA when the maximum output power is different than the nominal power values (+22 dBm (when using RFO_HP) or +14 dBm (when using RFO_LP)). The impact on power consumption is detailed in the product datasheet.

In that case, to benefit from these optimal settings, the following steps are needed:

1. Firmware: apply the RF PA configurations as described in the table below.
2. Hardware: determine a dedicated RF matching network with the RF PA configuration corresponding to the selected optimal setting.

This is because the RF PA output impedance values change with the RF PA settings.

To determine the RF matching network to a specific optimal setting, follow the procedure described in Section 5.1 .

For example, if the required maximum RF output power in the application is +10 dBm or +17 dBm, there is:

- an optimal setting to apply in order to increase the efficiency of the RF PA (reducing current consumption)
- a dedicated RF matching network

Table 2. **RF PA optimal settings**

Mode	Output power (dBm)	`Set_PaConfig()`				`SetTxParams` value (dBm)
		`paDutyCycle`	`hpMax`	`deviceSel`	`paLut`	
Low power (RFO_LP)	+15	0x06	0x00	0x01		+14
	+14	0x04				+14
	+10	0x01				+13
High power (RFO_HP)	+22	0x04	0x07	0x00	0x01	+22
	+20	0x03	0x05			
	+17	0x02	0x03			
	+14		0x02			+14

Caution: To avoid exceeding the maximum ratings that may cause irreversible damage to the device, some restrictions must be followed to prevent overstress on the RF PA:
- low-power mode:
  - For frequencies above 400 MHz, the `PaDutyCycle` must not be higher than `0x07`.
  - For frequencies below 400 MHz, the `PaDutyCycle` must not be higher than `0x04`.
- high-power mode:
  - For any frequency, the `PaDutyCycle` must not be higher than `0x04`.

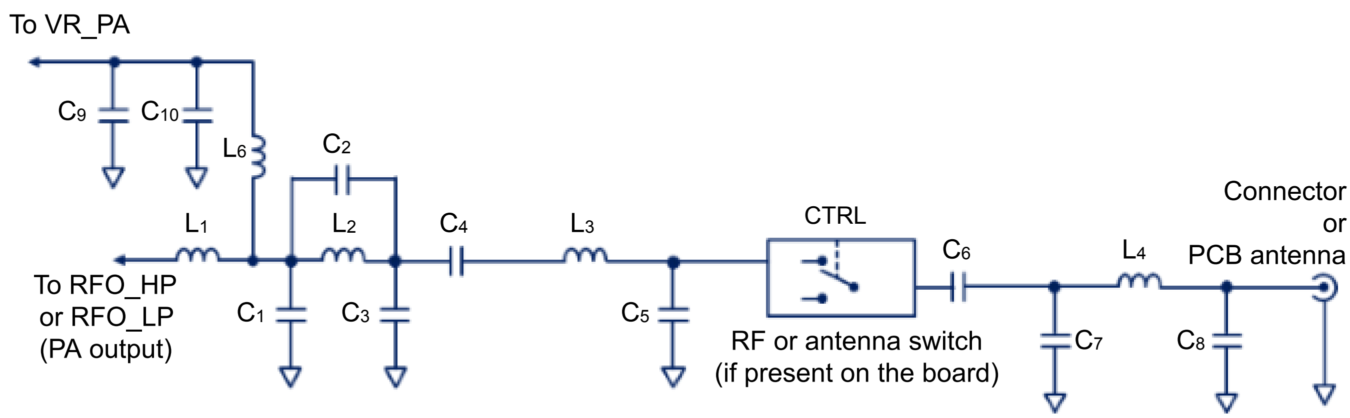
Note: For a given optimal setting, using a different power value makes this value either sub-optimal or unachievable.

The impedance values reported in this application note are measured with the RF PA optimal settings. If the impedance value for the user application is not provided,contact the ST local sales office.

5.1.3 Typical Tx application network

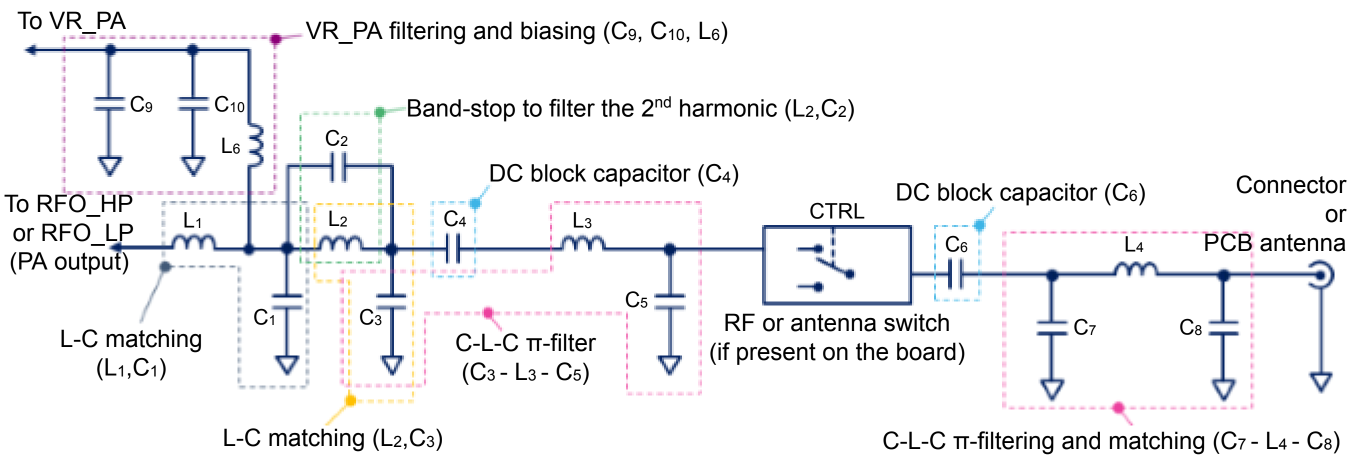
The typical Tx matching and filtering application network is shown in the figure below. The PA output impedance to match depends on frequency and power. Then, for each power and frequency configuration, there is a different BOM when high efficiency is required (higher power with lower current consumption).

Figure 25. Typical Tx application network



Each function of the typical Tx application network is described in the figure below. The reference of the RF switch used are Infineon SP3T BGS13SN8 and SPDT Infineon BGS12SN6.

Figure 26. Description of each part of the typical Tx application network



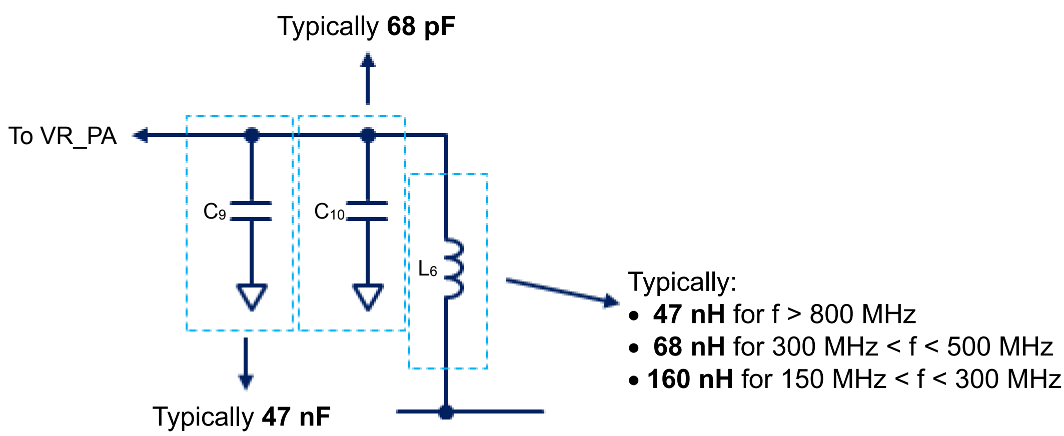
Note: For some RF switches, a DC block capacitor (series-low-impedance capacitor) is mandatory to block DC currents on its input and output (refer to the switch datasheet).

5.1.4 VR_PA biasing and filtering

In RF amplifiers, a high-impedance component is used to ensure the RF signal passes through the device and not back to DC source. For this purpose, RF chokes (RFC) are used (also called biasing inductor or DC feed). RFC are ideally high-impedance (~10x the input matching impedance) components for RF signals and low-impedance for DC. This “high-impedance” is not perfect, allowing some RF leakage to go back to the source: this is the reason why capacitors are added to “absorb” this leaking energy. The RFC is represented by L6 in the figure below and the HF bypass capacitors by C9 and C10:

- The capacitor C9 is typically **47 nF** (Murata GCM155R71E473KA55).
- The capacitor C10 is typically **68 pF** (Murata GCM1555C1H680JA16).
- The RFC (RF choke or DC bias inductor) is typically:
  - **47 nH** for frequencies above 800 MHz (Murata LQW15AN47NG00)
  - **68 nH** for frequencies between 300 MHz and 500 MHz (Murata LQW15AN68NG00)
  - **160 nH** for frequencies between 150 MHz and 300 MHz (Murata LQW18CAR16J0)
- The RFC must have a high-Q factor to reduce losses. An RFC with a poor ESR (equivalent series resistance) reduces the RF output power due to voltage drop on ESR.

Figure 27. VR_PA typical application circuit



5.1.5 PA output matching

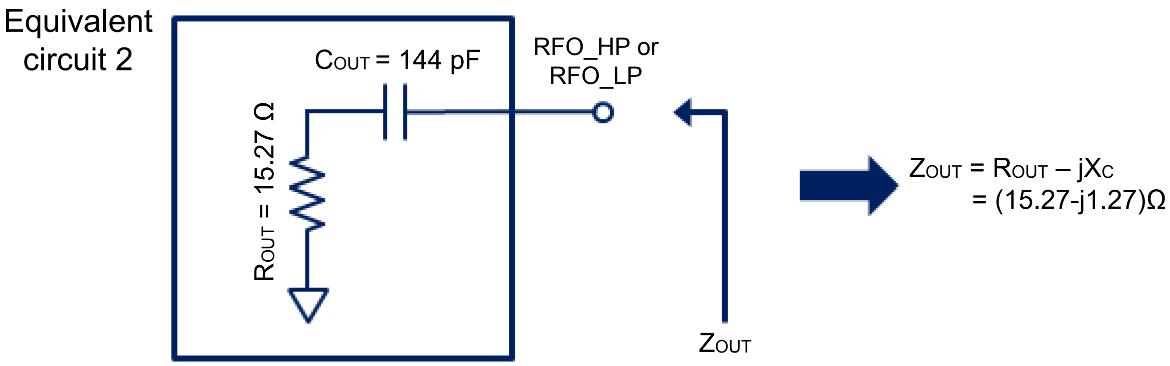
The methodology for the PA matching network is based on an example considering the impedances measured by load-pull analysis (reported in Section A.1.7 Example 7 (UFQFPN48, 14 dBm, 868 MHz)).

The first L-C cell (L1, C1) is used to match the PA optimal impedance (the impedance for which the required output power is reached with the lowest current consumption). From the results below, extracted for 14 dBm @ 868 MHz, the optimal impedance (Point 2) is about (15.27 + j1.27) Ω. The corresponding measured power for this impedance is 14 dBm (+ 0.5 dB to add as explained in Appendix A due to RF cables, connectors and tuner losses).

If the impedance presented to the PA output to get 14 dBm is (15.27 + j1.27) Ω, its output impedance is the complex conjugated of this value. Therefore, the PA output impedance is (15.27 - j1.27) Ω and corresponds to the equivalent circuit 2 presented earlier, with R_{OUT} = 15.27 Ω and:

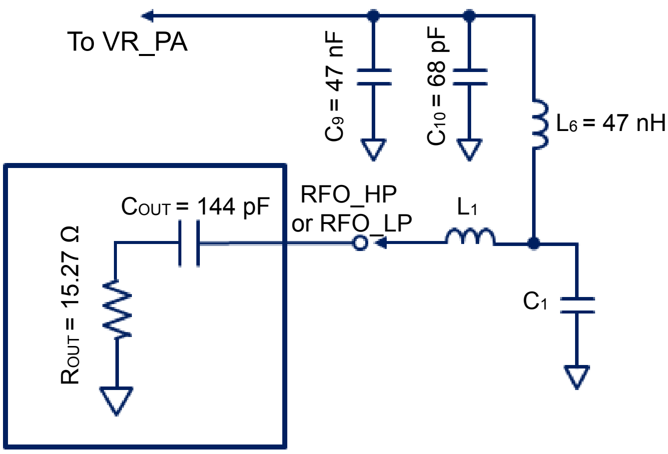
$$C_{OUT} = \frac{1}{2\pi \times 868\,MHz \times 1.27} = 144pF$$

Figure 28. **Equivalent output circuit for UFQFPN48, 14 dBm, 868 MHz**



This equivalent output circuit is matched with an L-C cell (L1, C1) as shown below.

Figure 29. **Placing the first LC matching network cell**



Note: *In order to skip all the formulas presented below, some free Smith chart tool available on internet can be used to help (such as SimSmith at www.ae6ty.com, Smith at www.fritz.dellsperger.net or Online Smith Chart Tool at www.will-kelsey.com/smith_chart/). These tools give the same values than calculating with the formulas below.*

The theoretical values of L1 and C1 are calculated as follows:

1. Calculate m.

$$m = \sqrt{\frac{50}{R_{out}} - 1} = \sqrt{\frac{50}{15.27} - 1} = 1.508$$

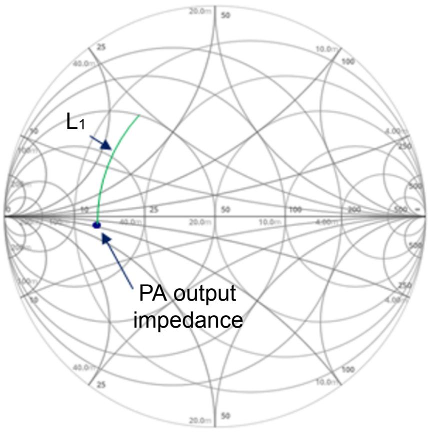
2. Calculate the value for the matching inductor L1.

$$L1 = \frac{1}{2\pi f} \times \left(\frac{50m}{m^2 + 1} + X_C \right)$$

$$\Rightarrow \; L1 = \frac{1}{2\pi \times 868MHz} \times \left(\frac{50 \times 1.508}{1.508^2 + 1} + 1.27 \right) = 4.45 \; nH$$

The result on the Smith chart is shown in the figure below.

Figure 30. L1 used to match the RF PA reactive part and to reach the 20 ms circle



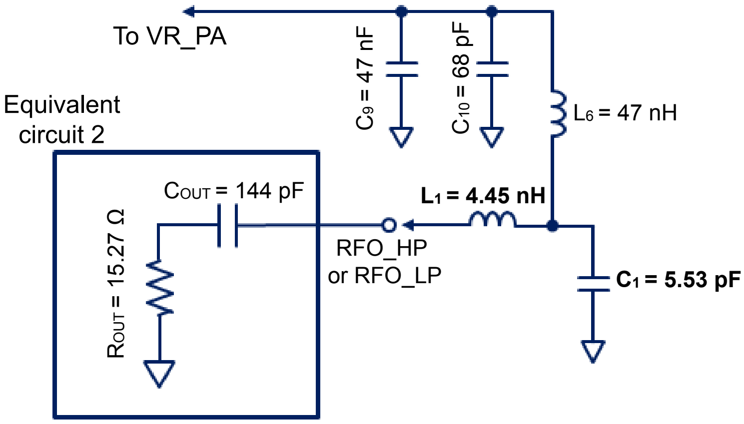
3. Determine the value of the matching capacitor C1 (module of the following formula):

$$C1 = \left| \frac{1}{2\pi f} \times \frac{\sqrt{\frac{R_{out}}{50}\left(1+m^2\right) - 1} + m}{R_{out}\left(1+m^2\right)} \right|$$

$$\Rightarrow C1 = \left| \frac{1}{2\pi \times 868MHz} \times \frac{\sqrt{\frac{15.27}{50}\left(1+1.508^2\right) - 1} + 1.508}{15.27\left(1+1.508^2\right)} \right| = 5.53\,pF$$

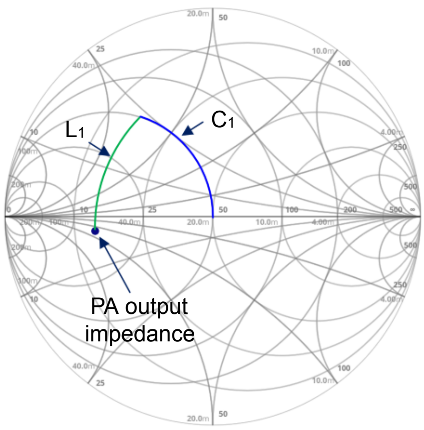
The network with these values becomes as follows.

Figure 31. First LC matching cell with calculated values



The result on the Smith chart is shown in the figure below.

Figure 32. Illustration on Smith chart of the addition of the first matching LC cell



4. Measure the output power to see if this L-C implemented on PCB corresponds to the necessary L-C matching. Be aware that the PCB may add a big impact on those values. If the output power is far from the expected value, try to adjust the values of L1 and C1 and see the impact on the output power. The user may have to tweak these values for the user specific PCB.

Note:
- *The component values must be rounded up to nearest existing SMD value.*
- *For some frequencies, output power configuration and/or PCBs, the first L-C matching cell can be implemented directly with L2 and C3, leaving L1 and C1 unpopulated. The procedure to be applied is the same.*

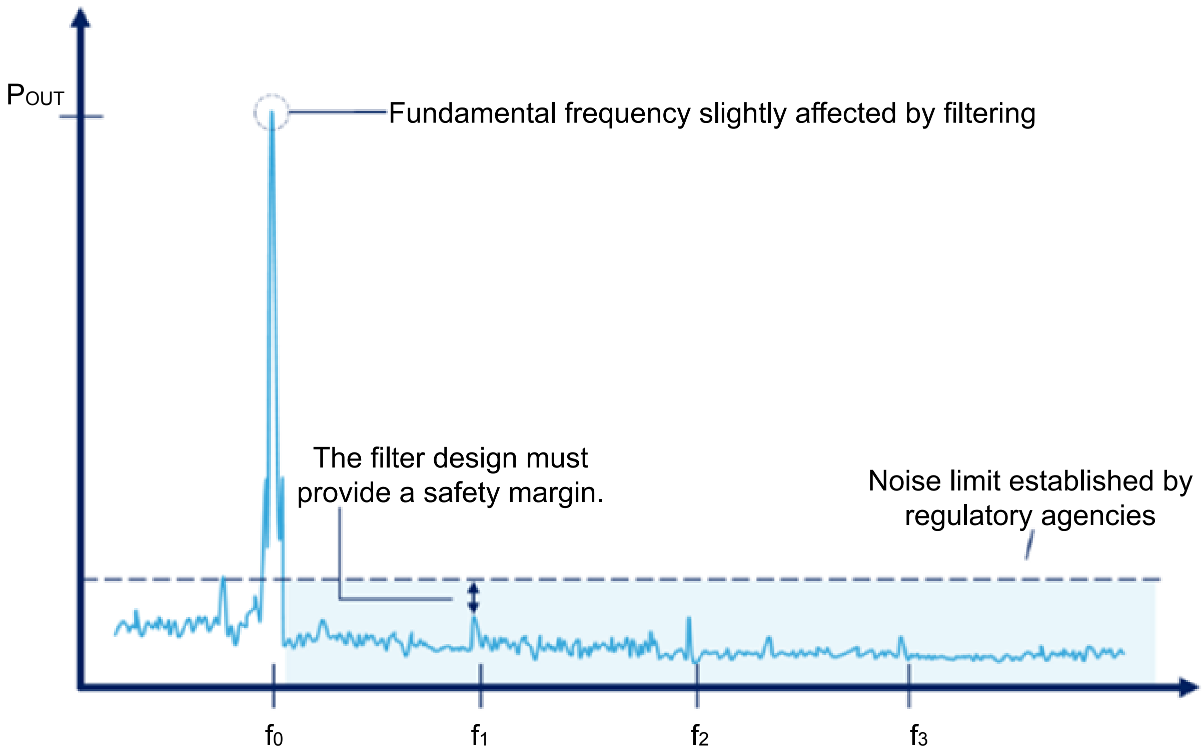
5.1.6 PA output filtering

An RF PA is always a non-linear system, resulting in spurious signals due to non-linear distortion of the input RF signal and/or harmonic contents of output signal. For an RF PA, the main purpose of filters is to eliminate spurious and harmonic contents from the frequency of interest.

Before filtering, the output power in the RF spectrum looks like in Figure 3.

After implementing the filtering stages, the result expected is like in the figure below.

Figure 33. Example of an output spectrum with controlled harmonic and parasite emissions



Determining the notch filter values

1. Calculate the values for the notch filter components (L2, C2) to reject the second harmonic (H2).

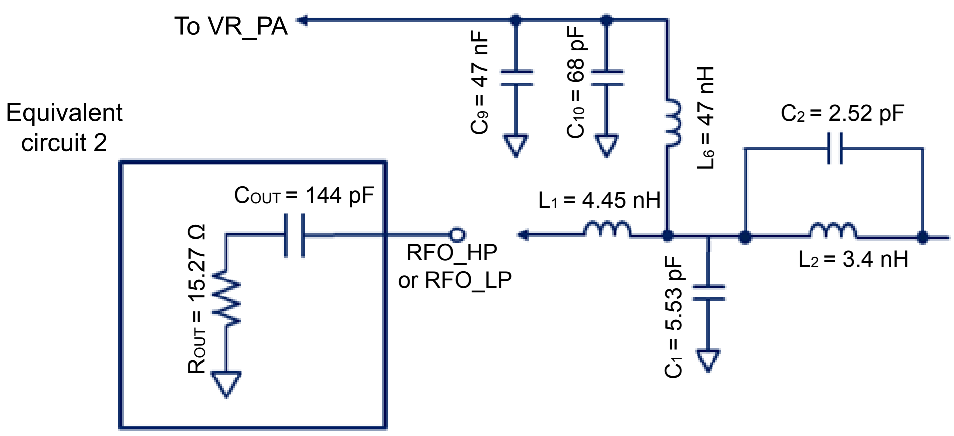
$$H2 = 868\,MHz \times 2 = 1.736\,GHz \quad and \quad 2\pi \times H2 = \frac{1}{\sqrt{L2 \times C2}}$$

As a thumb of rule, L2 is selected as 3/4 of L1 = 3.34 nH.

$$C2 = \frac{1}{(2\pi \times H2)^2 \times L2} = \frac{1}{(2\pi \times 1.736)^2 \times 3.34} = 2.52\,pF$$

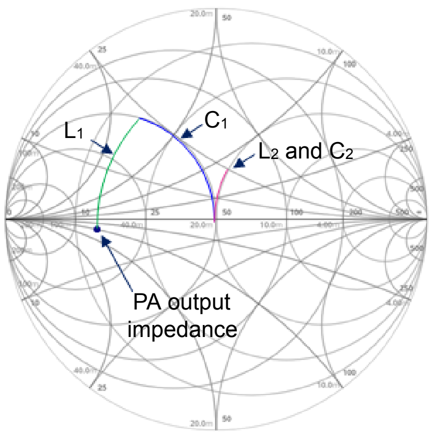
The network with these values becomes as follows.

Figure 34. Network with calculated notch filter values for the previous example



The result on the Smith chart is shown in the figure below.

Figure 35. Illustration of the impedance change on the Smith chart when adding the notch filter component

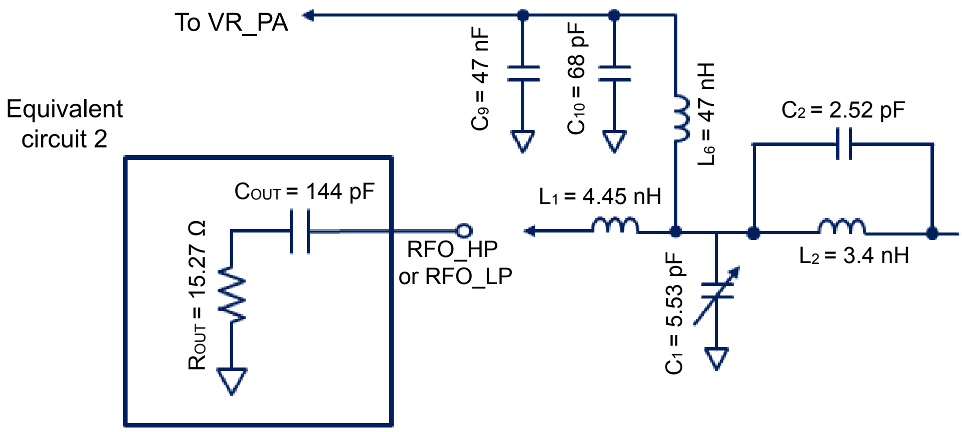


Measure the output power at this point and keep this value. Measure the H2 rejection and try to fine tune the notch filter as explained below.

Note: *Due to parasitic effects of PCB,the user may have to tweak the notch filter values. For example, taking the previous example on a PCB, a practical implementation of the notch filter can have the values 3.4 nH and 2.0 pF (instead of 3.4 nH and 2.5 pF).*

2. Correct the mismatch introduced by the notch filter, by increasing slightly, with increments of 0.3 pF, the value of the capacitor C1, and see the impact on the output power. Try also to decrease its value and see the impact on the output power. Refer to next step if this does not give correct results.

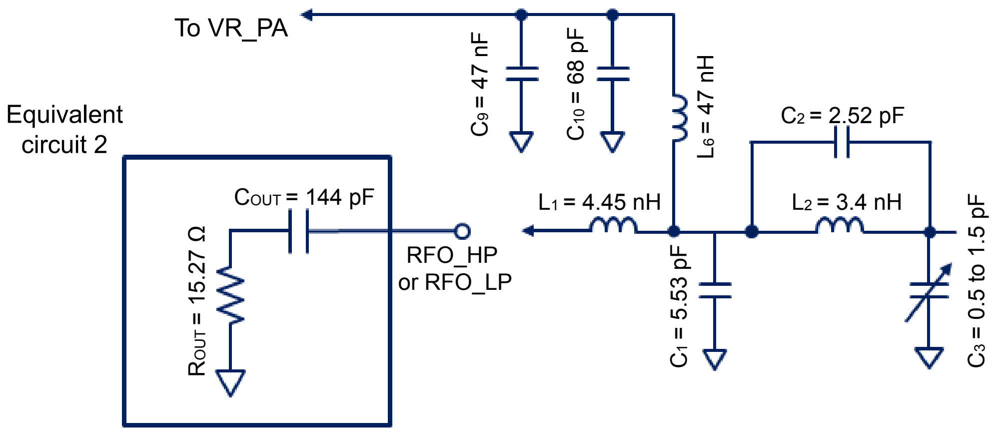
Figure 36. Tweaking C2 value to compensate the mismatch introduced by the notch filter



Note: The same procedure can be done to the value of L1 (starting with ± 0.2 nH), in order to obtain the real values to be implemented on the PCB.

3. If the previous step does not give the expected results, return to the initial values and put a parallel capacitor (C3) after the notch filter, with a value between 0.5 pF and 1.5 pF, and see the impact on the output power and H2 rejection.

Figure 37. Adding the capacitor C3 may reduce the mismatch introduced by the notch filter



Note: If the PA output impedance is purely resistive (equivalent circuit 1), the same steps can be used, with the value X_C equal to zero in the equations above.

How to implement the low-pass filter

This harmonic filter (for example for H3, H4or H5) is implemented by using a π-ladder network (fewer inductors than a T-ladder). The low-pass filter response is of the Chebyshev type: complex zero can be set at H1 with a good roll-off in the stopband.

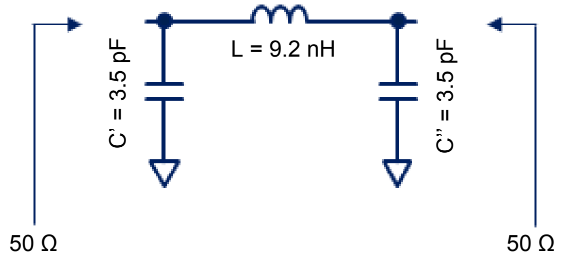
1. Determine the values of the low-pass filter with the following parametric equations.

$$L = \frac{50}{2\pi f} \; and \; C' = C" = \frac{0.95}{50 \times 2\pi f}$$

With values of the previous matching network example for 14 dBm@868 MHz, the filter values become:

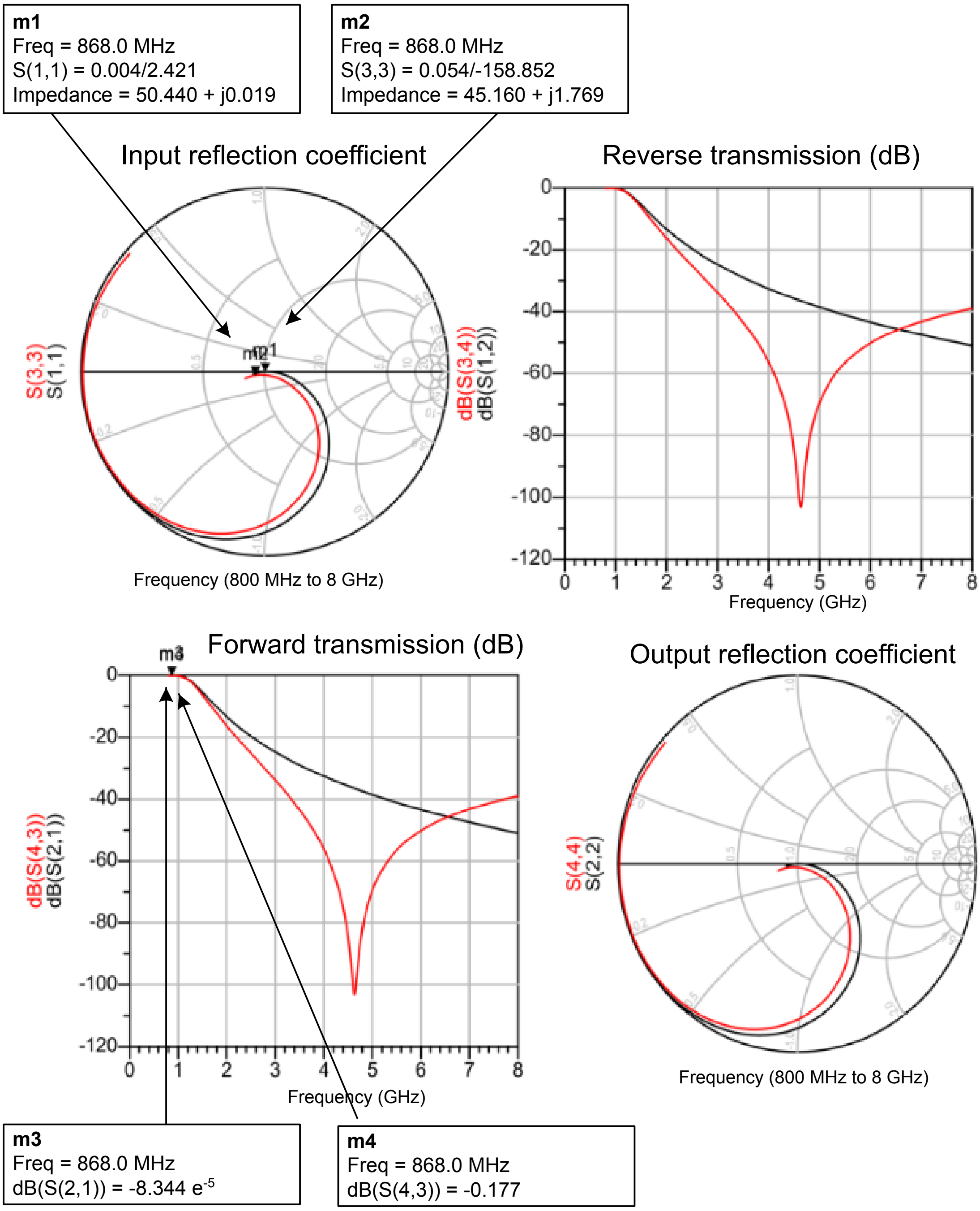
$$L = \frac{50}{2\pi \times 868} = 9.2 \; nH \; and \; C' = C" = \frac{0.95}{50 \times 2\pi \times 868} = 3.5pF$$

Figure 38. Low-pass Pi filter with 50 Ω input and output impedances



The simulation with these values is given below. In black (Ports 1 and 2) with ideal components and in red (Ports 3 and 4) with S-parameters of real components.

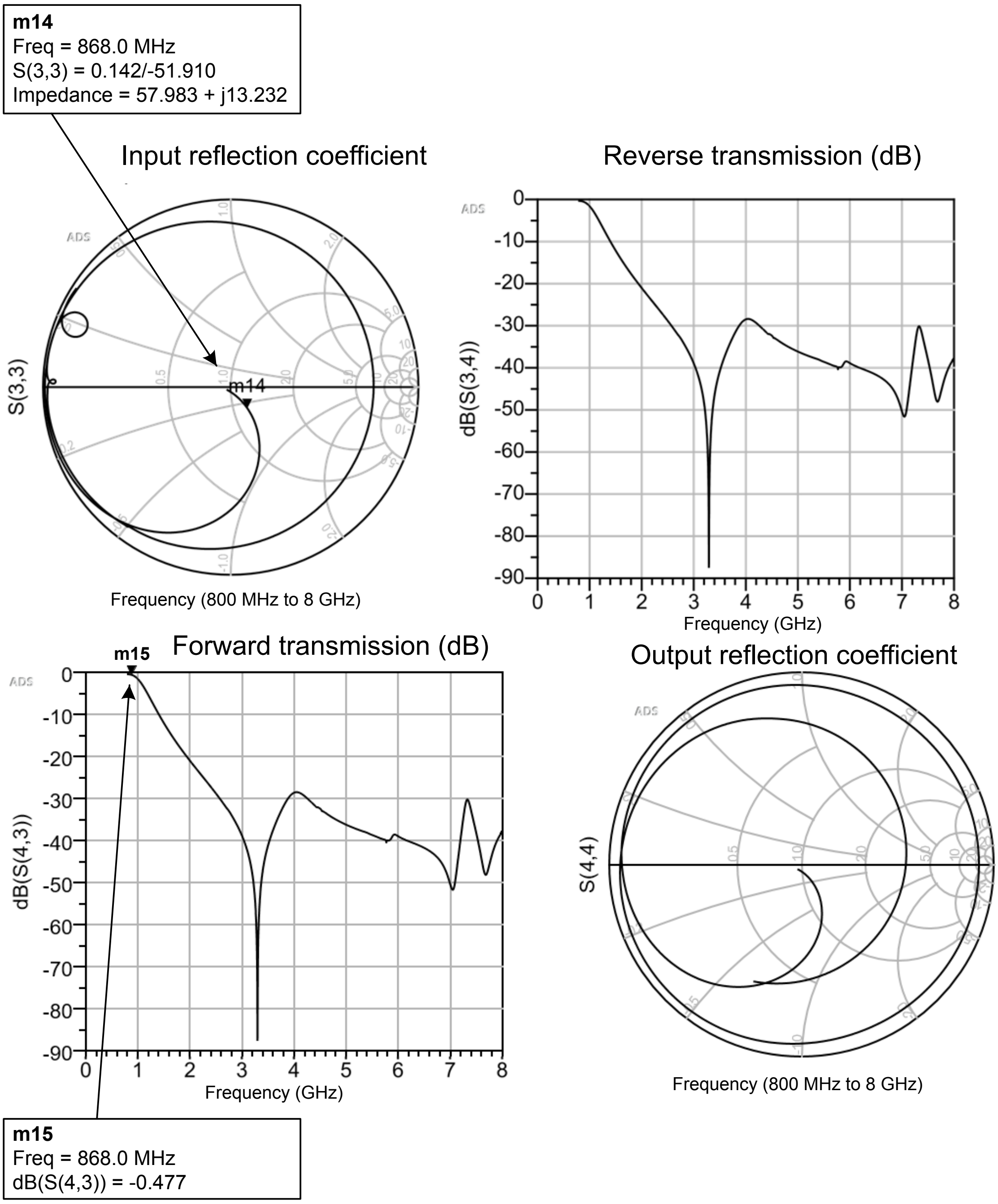
Figure 39. Low-pass Pi filter simulation of S-parameters vs frequency for ideal (black) vs real component s-parameters (red)



Note: *At 868 MHz, the impedance is in the center of the chart, with a forward transmission coefficient equal to -0.1 dB for the simulation with S-parameters of real components.*

The same filter implemented on a PCB gives the below results.

Figure 40. Low-pass Pi filter S-parameters vs frequency for implementation on PCB



The input reflection coefficient is not in the center of the chart. This is due to some parasitic effects introduced by the PCB and effects of real lumped components. In such cases, the user can slightly change the value of one capacitor and/or the other, and see the impact on harmonic rejection and output power. After adjusting the capacitor and inductor values to consider the PCB effects, the results become:

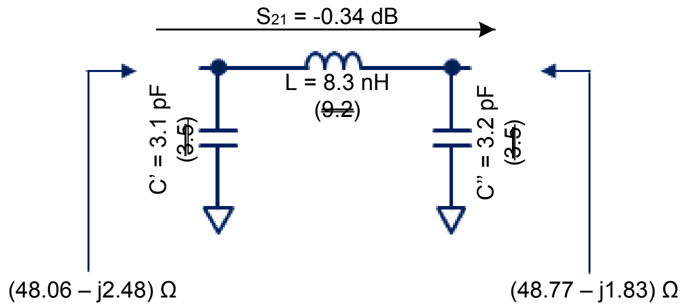


Figure 41. Example of calculated (in parentheses) vs implemented values for the low-pass Pi filter with insertion loss (S21).

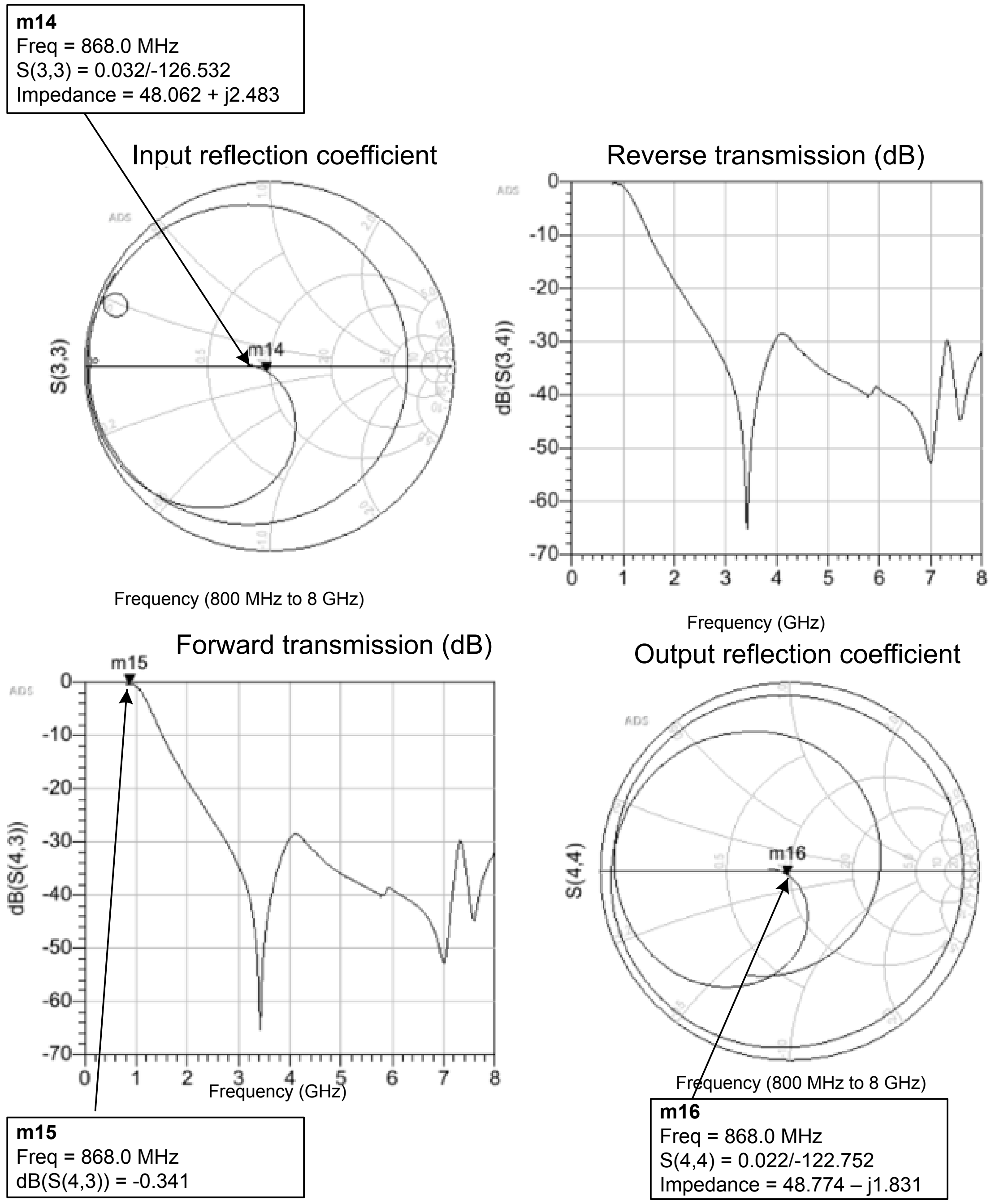
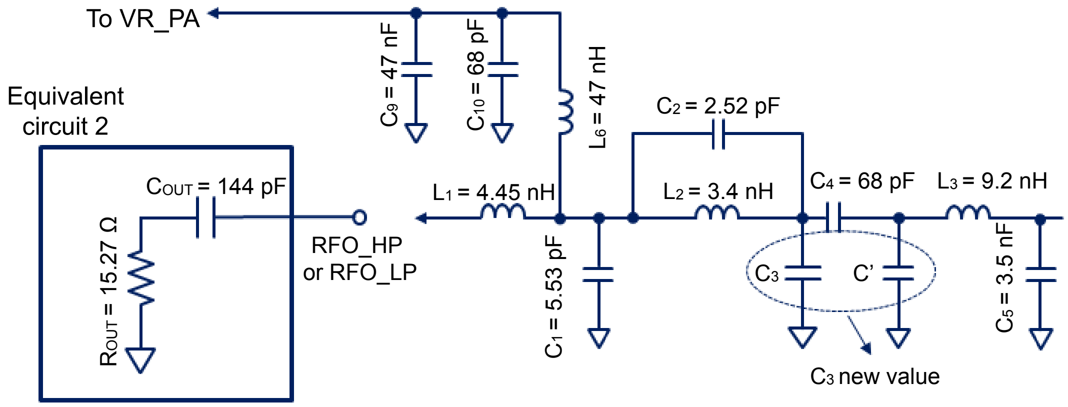


Figure 42. Low-pass Pi filter S-parameters vs frequency for implementation on PCB after tweaking component values

2. Combine the C3 additional capacitance with the PI filter.
If a capacitance C3 has been added to correct the effect on the impedance introduced by the notch filter (see the end of Determining the notch filter values), C3 must be combined with the capacitor of the low-pass filter:

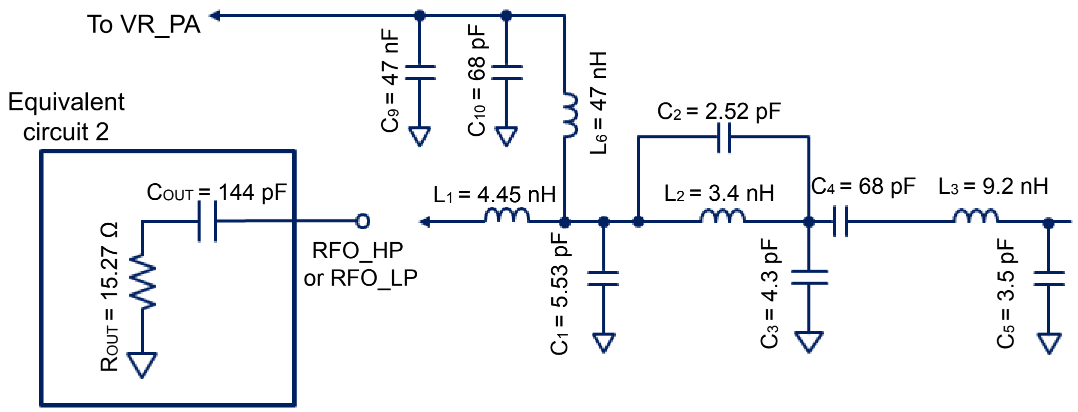
$$C3\ new\ value = C' + C3$$

Figure 43. Recombination of parallel capacitors in the network after adding the low-pass Pi filter



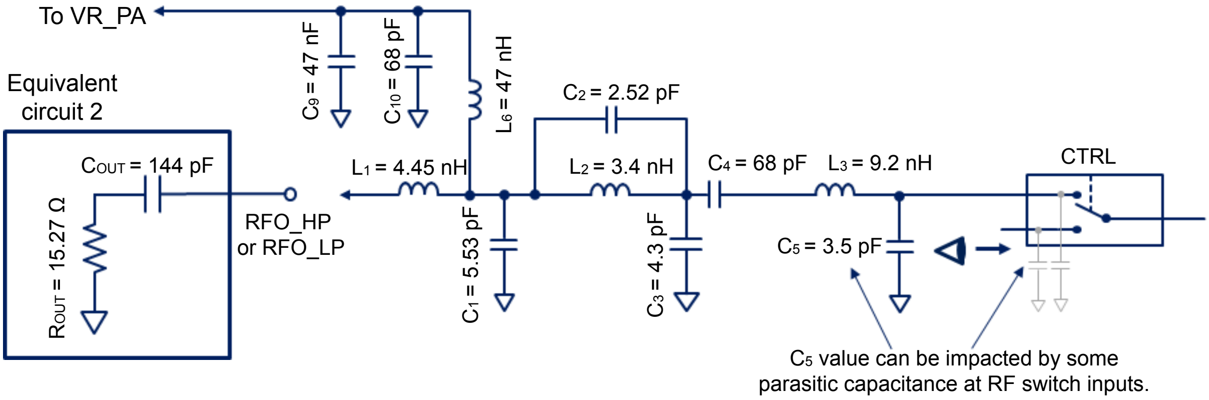
For example, if C3 = 0.8 pF and C' = 3.5 pF, than the new C3 value is 4.3 pF.
The complete network becomes as shown in the figure below.

Figure 44. Parallel capacitors recombined in the network



Note: Some RF switches have a sort of parasitic input capacitance that must be considered in the value of C5. For example, the C5 value may have to be decreased by some pF to get the right output power. This hypothesis can be confirmed by doing a test with and without the switch, and checking the impact on the output power value (see the figure below).

Figure 45. **C5 value may need to be modified to incorporate the parasitic input capacitance of the switch**



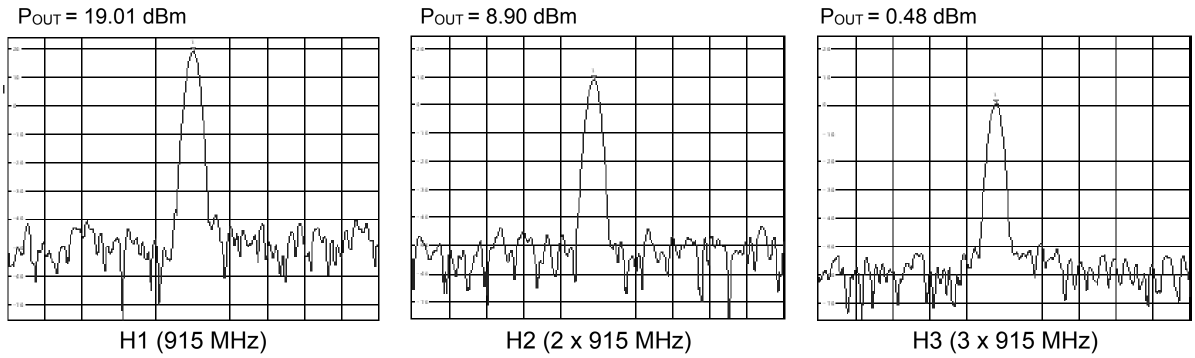
When using the high-power RF output (RFO_HP) in an application, another filter may be needed between the RF switch and the antenna or sma in order to reduce the harmonic emission levels and perform the antenna matching. In such cases, use the steps detailed in How to implement the low-pass filter.

5.1.7 Fundamental frequency power and harmonic levels

The power level of the harmonic frequencies has an impact in the output power of the fundamental frequency and current consumption. Decreasing harmonic levels, the power of the fundamental frequency can be increase and current consumption can be decreased (sometimes slightly). The level of the second (H2) and the third (H3) harmonics can have a significant impact on the fundamental frequency output power.

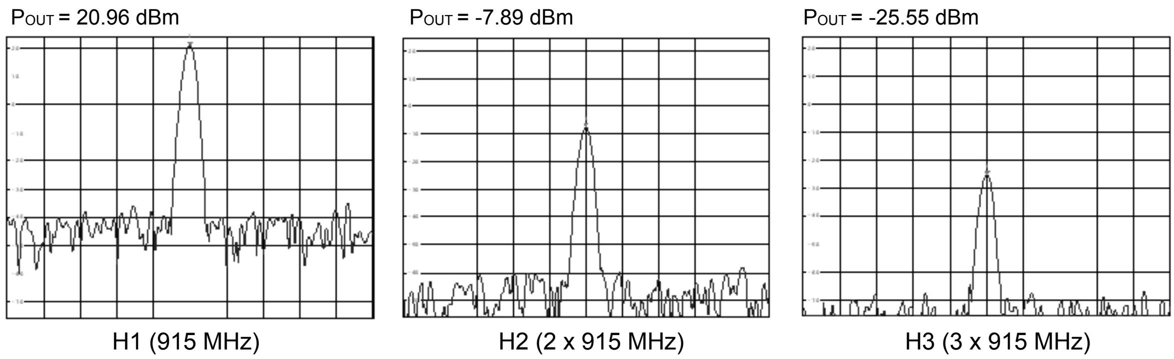
The power level of H2 and H3 depends on the module and phase of the reflection coefficient associated with these harmonics. The figure below is given as an example: captured using a spectrum analyzer without any matching L-C cell.

Figure 46. **Output power (conducted mode) values for H1, H2 and H3 without L-C matching cell**



The same measurement, but now matching with an L-C cell, gives the result in the figure below.

Figure 47. Output power (conducted mode) values for H1, H2 and H3 with an L-C matching cell



Note: The L-C matching cell works also as a low-pass filter. Continue with the matching and filtering network on the same board, the following values are obtained (conducted mode).

Table 3. Power versus frequency

I_{DD} = 117.6 mA. Measurement made on a UFQFPN48 mounted on the reference design board.

Frequency (H1 = 915 MHz)	Power (in dBm)
H1	21.79
H2	-63.1
H3	-60.6
H4	-55.1
H5	-52.6
H6	-65.0
H7	-61.9
H8	-68.3
H9	-65.6
H10	-59.9

5.1.8 PCB impact on impedances

As discussed earlier, the PCB can add a significant impact to the matching and filtering network. To illustrate this, two different impedance extractions are presented in the figure below, done with two different boards.

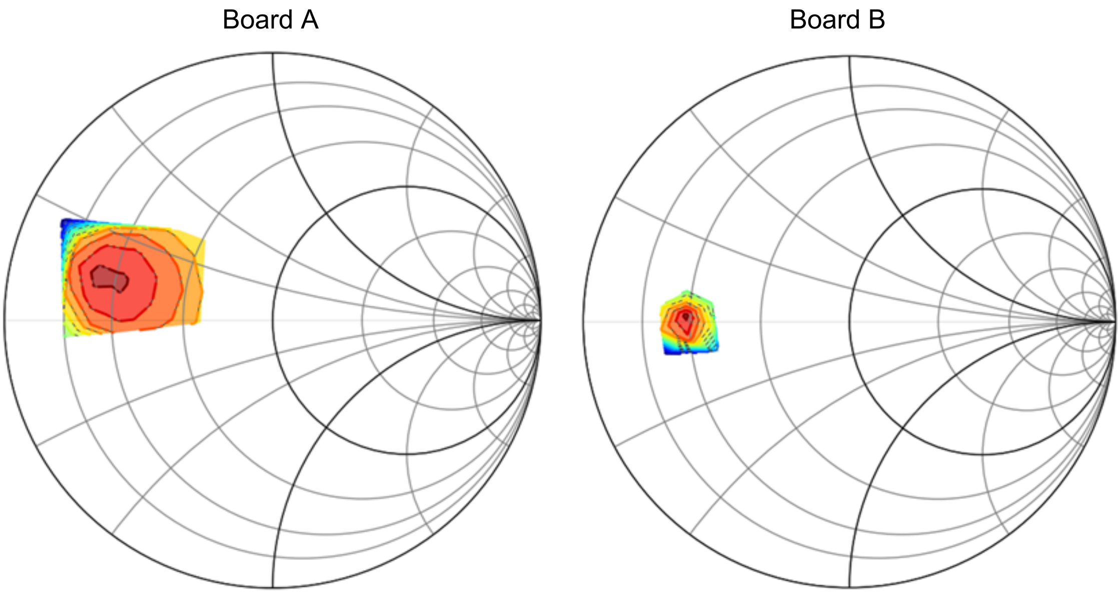


Figure 48. **PCB impact on impedance seen by the RF PA**

The hotspot (impedance for the highest power value) on the Smith chart can be in different regions. The figure below illustrates how it can be moved.

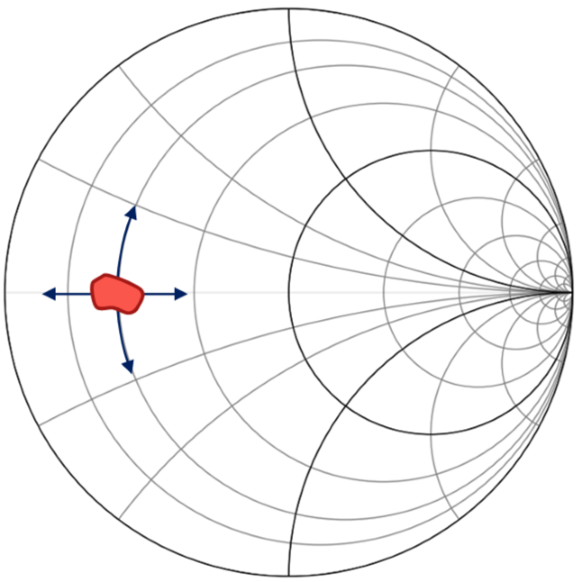


Figure 49. **Illustration of how the hotspot can be move with different PCBs**

For this reason, it may be necessary to fine tune the SMD component values (calculated with the previous formulas) used in the RF network .

Understanding the impact of the TLine on the impedance matching

To save time during impedance matching work, we must be aware of the impact of the planar PCB transmission line (here called TLine) on the impedance matching, understanding how the transmission line changes the impedance seen by the device in order to proceed with the determination of the values for the matching network components. The impact of the transmission line on impedance matching network is described below.

The impedance seen at the beginning of a transmission line terminated with a load is defined as (*lossy line*):

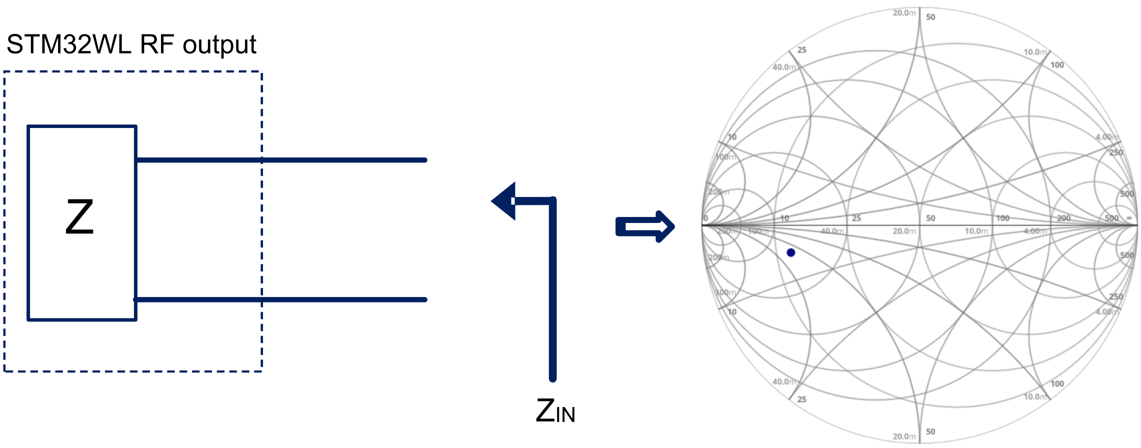
$$Z_{in} = Z_0 \left(\frac{Z_L + Z_0 \tanh(\gamma l)}{Z_0 + Z_L \tanh(\gamma l)} \right)$$

where ɣ is the propagation constant and l is the length of the line.

The TLine impedance formula show that when a TLine (or some PCB track) is added between the package RF output pin and the matching network reference plane, the device see that the TLine rotates the observed reflection coefficient clockwise centered on the characteristic impedance of the TLine.

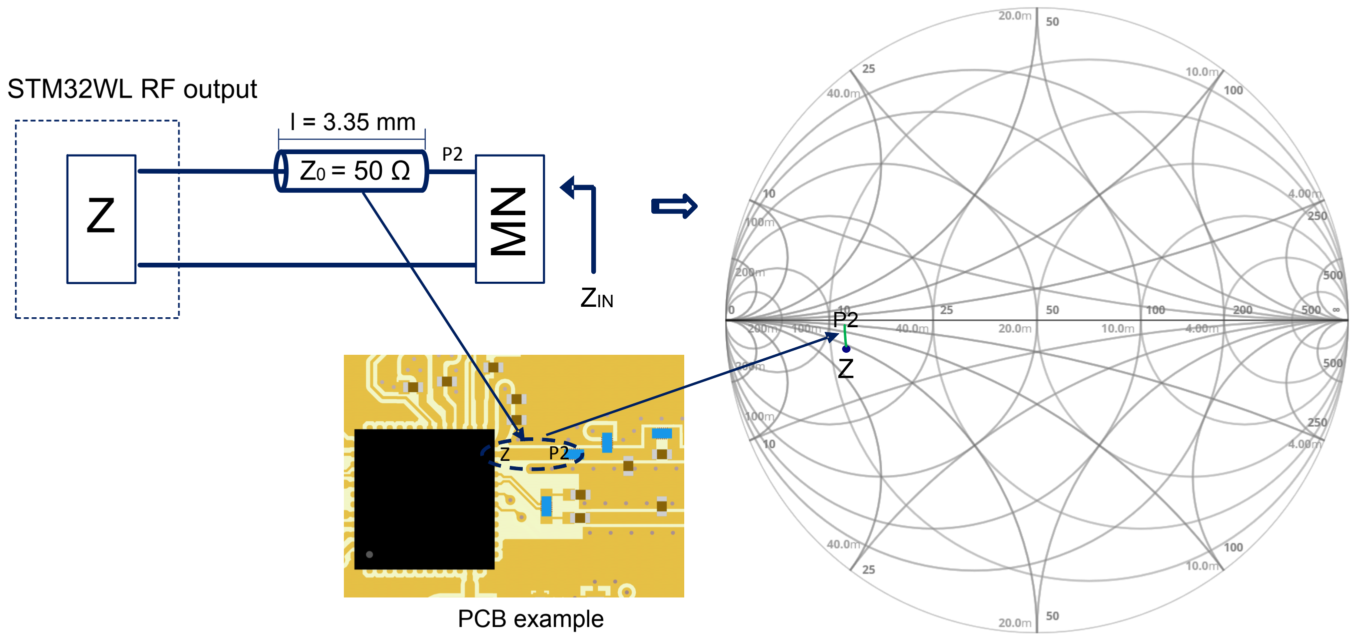
In the example below, the output impedance of the device is the load. The goal is to match the device output impedance to a 50 Ω system. As the device output impedance is Z_{868MHz} = (12 - j5) Ω, this impedance is represented on the Smith chart as shown below:

Figure 50. Impedance of the previous example represented on the Smith chart



As mentioned earlier, placing some length of TLine (PCB track) between the first LC matching cell and the device RF output, causes the reflection coefficient to rotate clockwise centered on the characteristic impedance of the TLine. For example, with a, added 3.35 mm of PCB track between the device and the first LC matching network cell, and considering the velocity factor of the TLine on the PCB equal to 0.58 with a simplified model, the result is shown in the figure below:

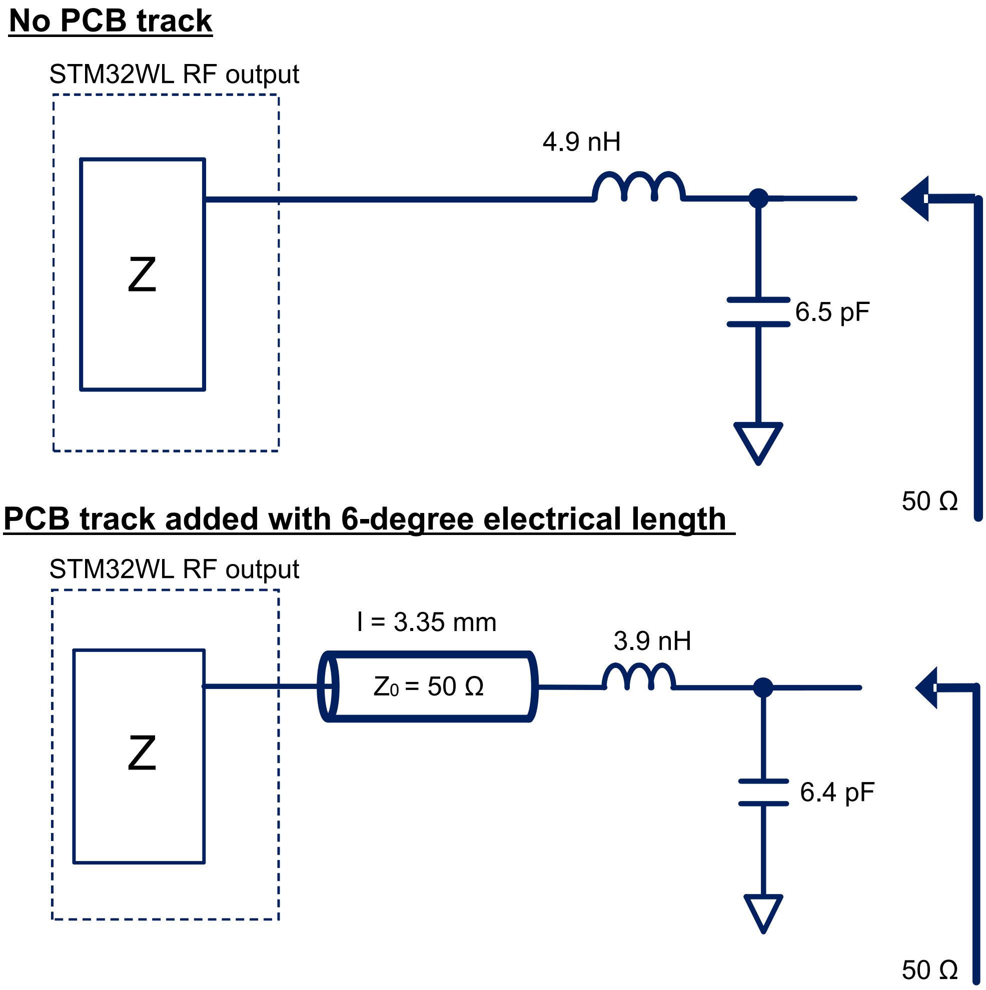
Figure 51. Impact on impedance after adding 3.35 mm of TLine between device RF output and matching network (MN)



As shown in the previous figure, adding this short TLine cancels out the imaginary part of the impedance.

Note: *For this example, the electrical length was only 6 degrees. The same exercise can be done with the free CAD tool SimSmith by AE6TY.*
With the matching network of the previous example, only 3.9 nH of inductance is needed instead of 4.9 nH in case this short PCB track does not exist.

Figure 52. Difference between the inductor value without PCB track versus PCB track with 6-degree electrical length



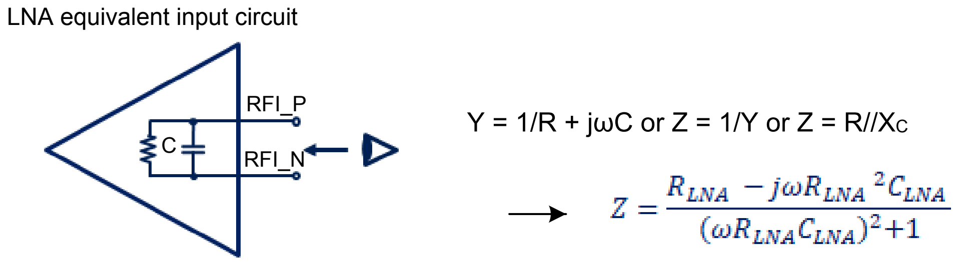
Note: *For this example, the TLine has an inductive behavior, but some substrates may also have some capacitive behavior. .*

5.2 LNA matching network

As mentioned earlier, the LNA equivalent input circuit is a parallel resistor with a parallel capacitor.

Note: The LNA equivalent input impedance has always a negative imaginary part (reactance).

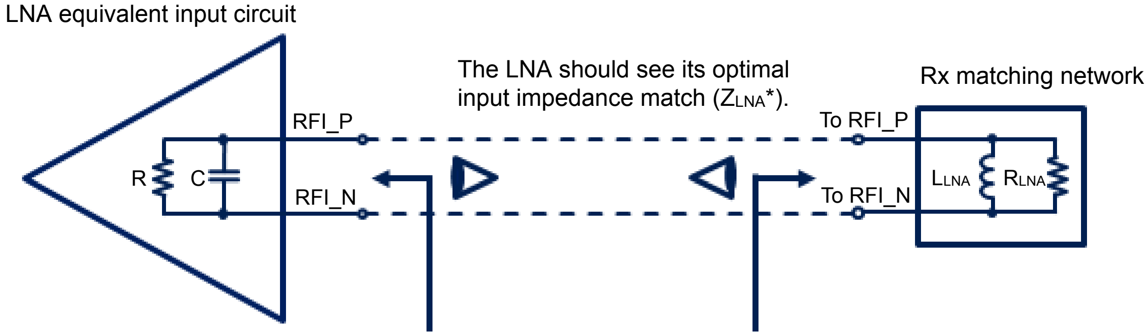
Figure 53. **Equivalent input circuit and impedance of the low-noise amplifier**



$$Z = \frac{R_{LNA} - j\omega R_{LNA}{}^{2} C_{LNA}}{(\omega R_{LNA} C_{LNA})^{2} + 1}$$

The impedance that matches the LNA optimal impedance is the complex conjugated of its own impedance as shown in the figure below (symbols highlighted in yellow).

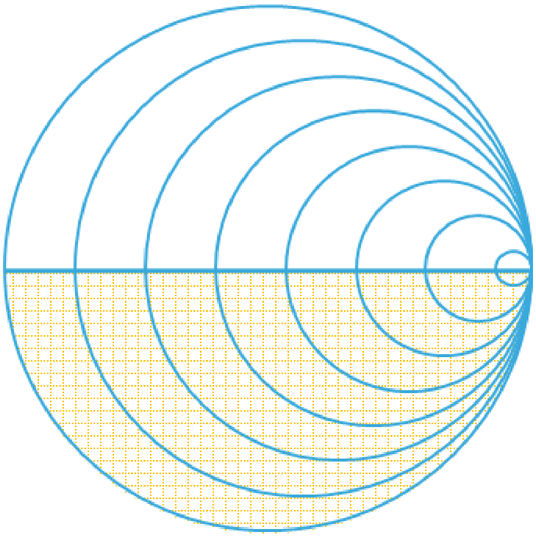
Figure 54. **LNA equivalent input circuit and impedance with matching network needed**



$$Z = \frac{R - j\omega R^{2} C}{(\omega R C)^{2} + 1} \qquad Z = \frac{R + j\omega R^{2} C}{(\omega R C)^{2} + 1}$$

The LNA optimal input impedance is represented on the bottom of the Smith chart as illustrated below.

Figure 55. LNA equivalent input impedance at the bottom of the Smith chart



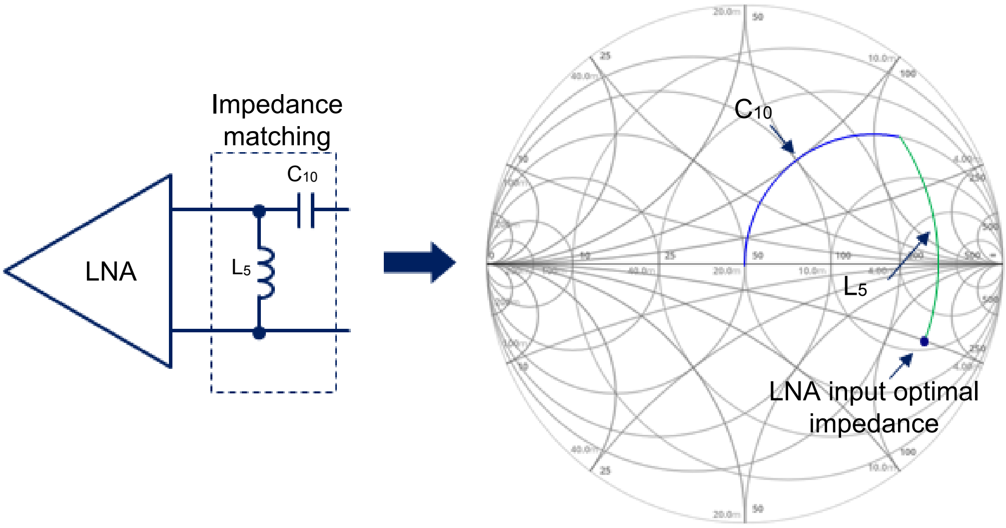
LNA matching methodology

The first step is to match the imaginary part of the LNA input impedance. The methodology is based on an example, such as the LNA optimal impedance for the BGA package at 915 MHz. This corresponding impedance, as reported in A.2, is the complex conjugated of Z_{OPT} = (62 **+** j112) Ω.

It means Z_{LNA} =Z_{OPT}* = (62 **-** j112).

The figure below illustrates the principle of matching the LNA optimal impedance: a parallel inductor with a series capacitor, that both match the LNA reactance and rotate its input impedance further the center of the chart.

Figure 56. Components needed to match LNA impedance to 50 Ω system

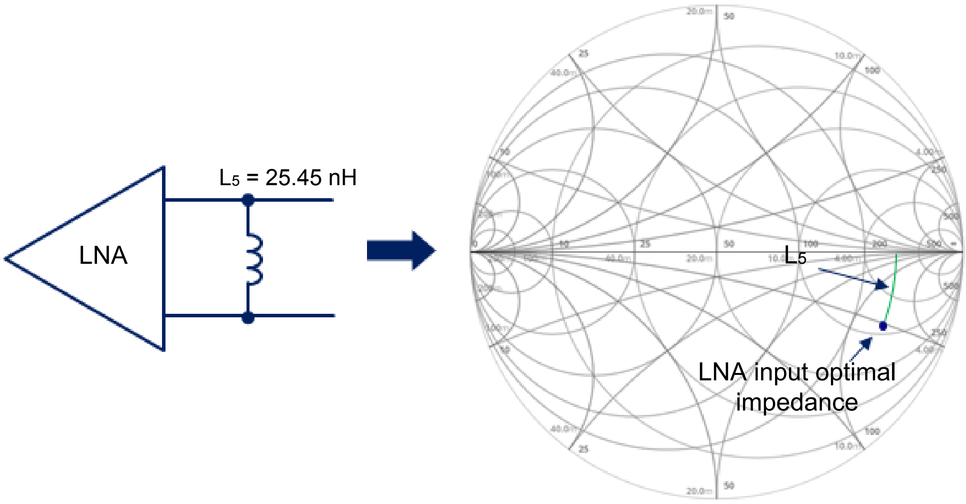


1. Match the LNA input capacitor reactance.
   Calculate the first value of the parallel inductor.

$$L5 = \frac{1}{2\pi f\sqrt{\frac{1}{R^2 + X^2} - \left(\frac{R}{R^2 + X^2}\right)^2}}$$

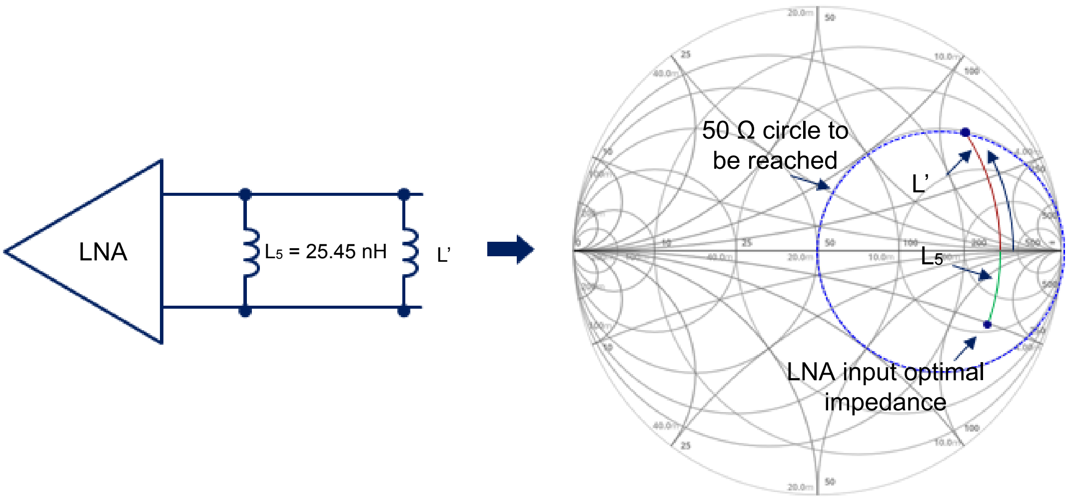
   For the BGA example, f = 915 MHz, R = 62 and X = 112. Then L5 = 25.45 nH.
   With this inductance value, the reactive part of the LNA optimal impedance is matched. The result on the Smith chart is given in the figure below.

Figure 57. **Matching the reactive part of the LNA impedance**



2. Impedance transformation
   The value of the matching inductor L5 is increased to make the impedance transformation between the high impedance LNA side and the antenna side that is a 50 Ω network. Another parallel inductor is added to reach the 50 Ω circle on the Smith chart, as illustrated in the figure below.

Figure 58. **Reaching the 50 Ω circle after the matching of the reactive part of the LNA impedance**

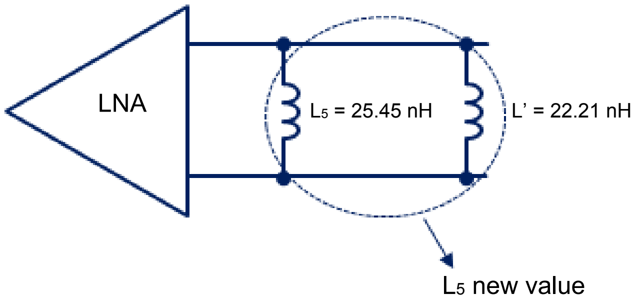


$$L' = \frac{1}{2\pi f\sqrt{\frac{1}{50}\left(\frac{R}{R^2 + X^2}\right) - \left(\frac{R}{R^2 + X^2}\right)^2}}$$

For the BGA example, f = 915 MHz, R = 62 and X = 112. Then L' = 22.21 nH.

3. Combine the two values of the parallel inductors.
The two parallel inductors can be combined into one inductor value, to save BOM and surface on the PCB.

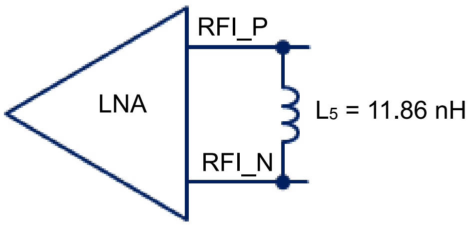
Figure 59. Values of the previous case



$$L5\ new\ value = \frac{L5 \times L'}{L5 + L'}$$

For the BGA example, L5 = 25.45 nH and L' = 22.21 nH. Then the new value of L5 = 11.86 nH.

Figure 60. Combining the two inductors into one



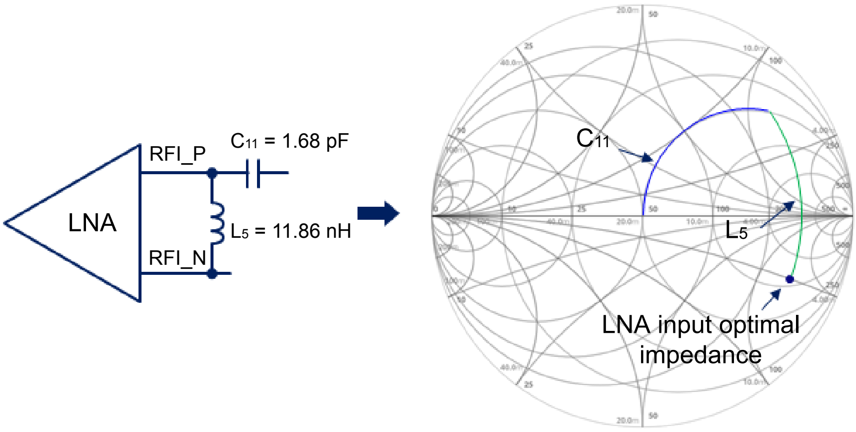
Note: As discussed earlier for the T_X matching network, the value of the inductor L5 can be impacted by parasitic effects of the PCB. For example, in a practical implementation, the L5 value can be 11.00 nH, instead of 11.80 nH.

4. Calculate the value of the series capacitor to reach the center of the Smith chart.

$$C10 = \frac{1}{2\pi f \times 50\sqrt{\frac{1}{50}\left(\frac{R^2 + X^2}{R}\right) - 1}}$$

For the BGA example, f = 915 MHz, R = 62 and X = 112. Then C10 = 1.68 pF.
The result on the Smith chart is give in the figure below.

Figure 61. Reaching the center of the chart with a series capacitor



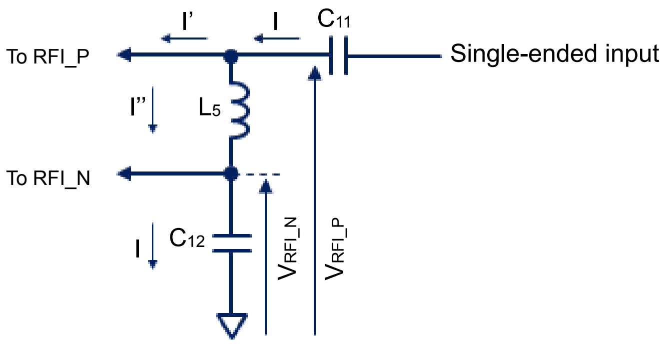
As the receiver has a differential input, a circuit must be built to convert the signal from the antenna side (single-ended signal, referred to as GND), into a differential signal. Normally, this is done using a balun that is a circuit that converts a balanced signal to an unbalanced signal, and vice versa. A balun with lumped components is implemented with four or six elements that ensure a voltage phase difference of 180° with equal amplitude between the lanes.

5. Define the circuit that generates a differential voltage on RFI_N and RFI_P.
Due to the high values of inductors (balun inductors plus matching inductors), a real balun with four or six elements can introduce losses (inductors with high ESR) that decrease the reception performance. The user must then build a "balun-like" circuit with only three elements that makes a good comprise between performance and cost.

Note: Since the LNA input impedance is not infinite, there will be a phase imbalance between RFI_N and RFI_P voltages that does not produce a phase difference of exactly 180°.

The circuit analysis is given in the figure below.

Figure 62. Rx matching network analysis



The voltage on RFI_P must be equal to minus RFI_N.

$$Condition\,1:\ V_{RFI\_N} = -V_{RFI\_P}$$

From the circuit above:

$$V_{RFI\_P} - V_{RFI\_N} = V_{RFI\_P} - \left(-V_{RFI\_P}\right) = 2V_{RFI\_P}$$

and

$$V_{C12} = I \times jX_{C12} = V_{RFI\_N} = \frac{V_{L5}}{2}$$

Starting with condition 1, the voltage in capacitor C12 is half the voltage on inductor L5:

$$I \times jX_{C12} = \frac{I'' \times jX_{L5}}{2}$$

But,

$$I'' = I - I'$$

Then,

$$I \times X_{C12} = \frac{(I - I') \times X_{L5}}{2}$$

If $X_{C12} = X_{L5}$, the previous formula becomes $I = \frac{(I - I')}{2} \Rightarrow \quad I' = -I$

This does not correspond with the actual functioning of this circuit. Therefore, the only solution is the one below:

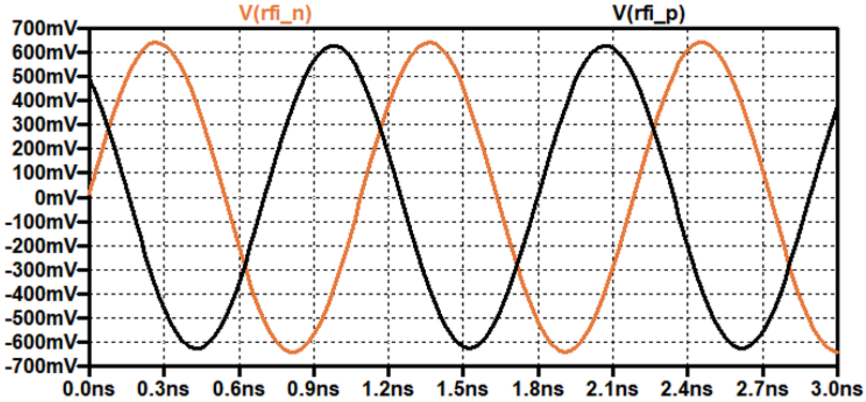
$$I \times X_{C12} = \frac{I'' \times X_{L5}}{2} \quad \Rightarrow \quad X_{C12} = \frac{X_{L5}}{2}$$

It means that the reactance of C12 is the half of L5, but as discussed before, a portion of the L5 value is used to cancel the capacitive reactance of the LNA. Then, the value of L5 that must be used in the previous result, is this one used to reach the 50 Ω circle on the Smith chart found in Step #3 (called L').
Thus C12 is calculated as follows:

$$C12 = \frac{2\sqrt{\frac{1}{50}\left(\frac{R}{R^2 + X^2}\right) - \left(\frac{R}{R^2 + X^2}\right)^2}}{2\pi f}$$

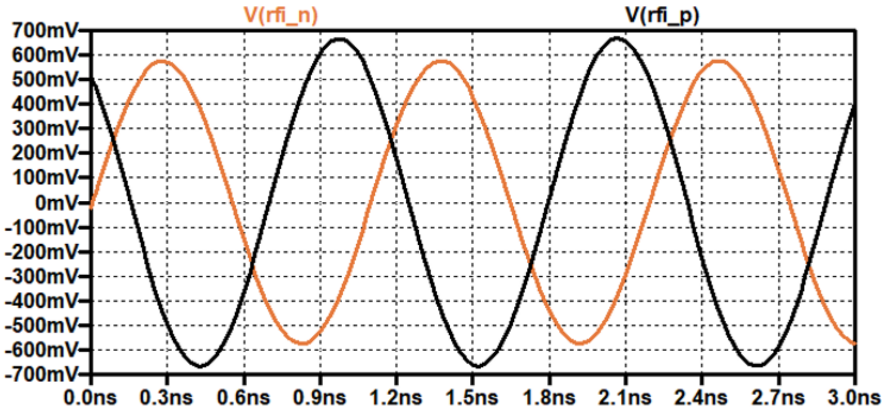
For the BGA example, f = 915 MHz, R = 62 and X = 112. Then C12 = 2.7 pF.
With L5, C11 and C12 values, an SPICE transient simulation with a sinusoidal waveform at 915 MHz as input, gives the result shown in the figure below.

Figure 63. Simulated waveforms showing phase imbalance when using Zoptimal



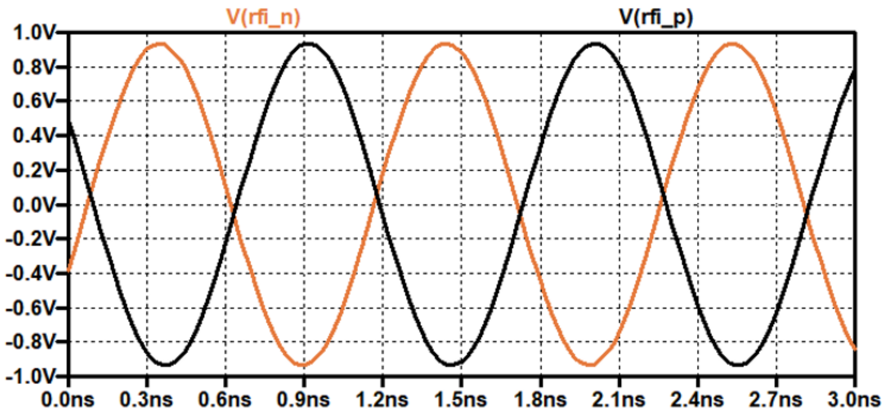
With a wrong C12 value, 3 pF instead of 2.7 pF for example, the result is different.

Figure 64. Amplitude mismatch when using a wrong C12 value



If the RLNA is 10x its reported value, the results are shown below.

Figure 65. RFI_N and RFI_P waveforms showing the phase difference for a large value of the LNA input equivalent parallel resistance



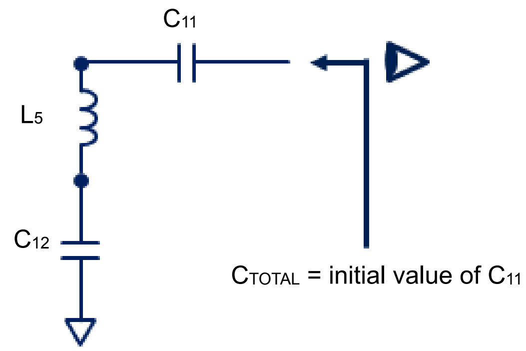
The phase imbalance is strongly proportional to the RLNA when using this three-element BALUN-like. In a practical case, the phase imbalance is less than the one showed in Figure 63, due to RLNA value higher than Roptimal.

Note: The above voltage waveforms are simulated using a transient analysis with the LTspice® software from Analog Devices.

6. Recalculate the value of C11 due to the mismatch introduced by C12.

Note: C11 and C12 capacitors are in series and the result must be equal to the initial value of C11.

Figure 66. Total capacitance seen from 50 Ω side



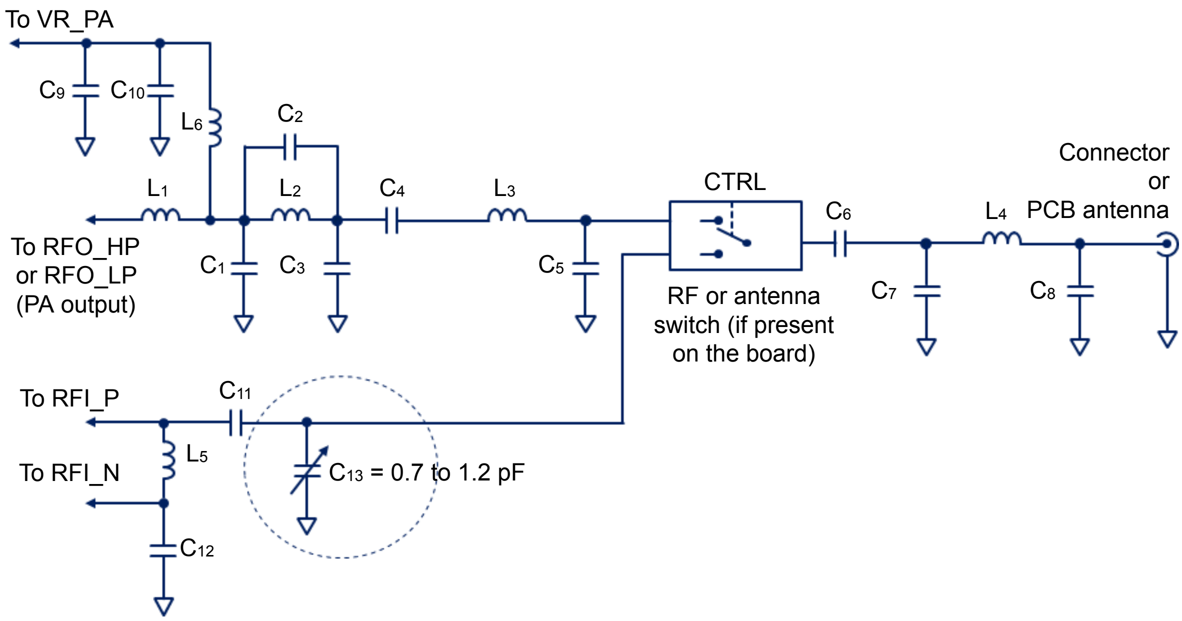
$$\frac{1}{C_{TOTAL}} = \frac{1}{C_{11}} + \frac{1}{C_{12}}$$

For the BGA example, C_{TOTAL} = 1.68 pF and C12 = 2.7 pF, it gives:

$$\frac{1}{1.68pF} = \frac{1}{C_{11newvalue}} + \frac{1}{2.7pF} \Rightarrow C_{11newvalue} = 4.45\ \text{pF}$$

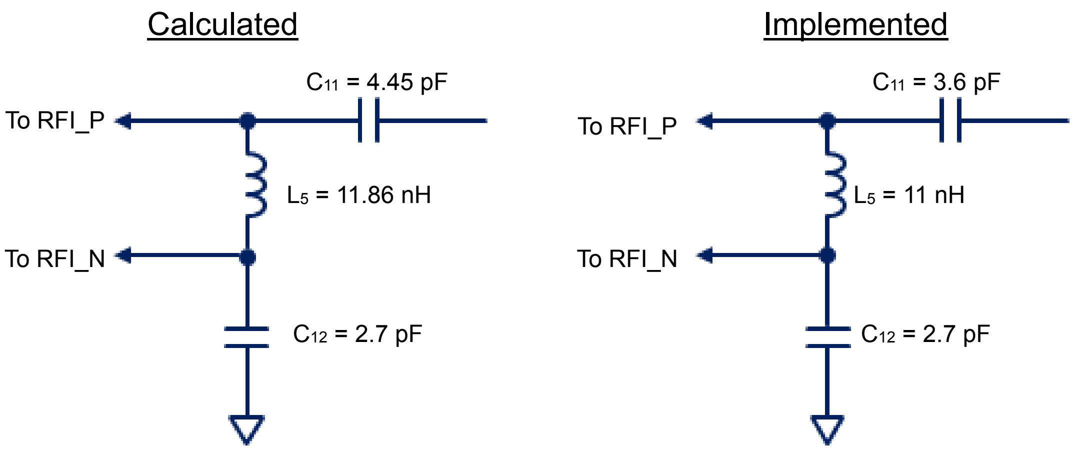
For some RF switches, it is necessary to add an additional capacitor before the RF switch on the R_X path, in order to reduce the amount of harmonic energy that reaches the antenna. If nothing changes in terms of harmonic output power after placing this capacitor, then this capacitor can stay unpopulated (see the figure below).

Figure 67. Additional capacitor on Rx path may reduce the amount of harmonic energy coupled between Tx and Rx paths



The figure below gives the values compared to the calculated ones, on an example of the previous R_X matching circuit implemented on a PCB.

Figure 68. Comparison between calculated and PCB implemented values of the Rx impedance matching network



5.3 RF BOM of calculated components

The whole circuit of the previous example is given in Figure 67.

An RF BOM for the previous calculated component values is given below, using Murata high-Q components series LQW15AN for inductors, GJM1555C for matching network capacitors, and GRM1555 for bypass and DC block capacitors.

Table 4. RF BOM for the previous example

Component name	Murata part number
L1	LQW15AN4N4G80
L2	LQW15AN3N4G80
L3	LQW15AN9N2G80
L5	LQW15AN12NG80
L6	LQW15AN47NG80
C1	GJM1555C1H5R5WB01
C2	GJM1555C1H2R5WB01
C3	GJM1555C1H4R3WB01
C4	GRM1555C1E680JA01
C5	GJM1555C1H3R5WB01
C6	GRM1555C1E680JA01
C9	GRM155C71H473KE19
C10	GRM1555C1E680JA01
C11	GJM1555C1H4R5WB01
C12	GJM1555C1H2R7WB01

Important: *Use components with a high precision (low tolerance) in the first time when performing the matching network on the user PCB, otherwise some additional difficulty due to PCB parasitic effects plus component variation may occur.*

6 Conclusion

RF applications require a certain level of knowledge in theory and practical implementation. This task can be more easily performed using appropriate EDA software. This application note gives an analytical description of the matching and filtering network components that can also be done using an EDA software. Another important point to highlight is the influence of the PCB in all component values. PCBs can add a significant influence due to impedance mismatch introduced by transmission lines not correctly designed and/or manufactured.

Appendix A

A.1 PA matching impedance measurements

Plot overview

The matching impedances come from load-pull analysis done for each package and power/frequency configuration. The results are plotted on the Smith chart with:

- circles colored that represents the regions for constant values of output power (in dBm)
- colored contours that represent the constant current consumption

The objective is to find an impedance output value for which the required power value is reached with the lowest current consumption (highest efficiency). This impedance value is called the optimal impedance. When presenting the value read on the charts, the PA output impedance is matched. See below an example of how the results are presented (zoomed plot on the right).

Figure 69. Example of impedance extraction (by load-pull analysis) results from RF PA plotted on Smith chart

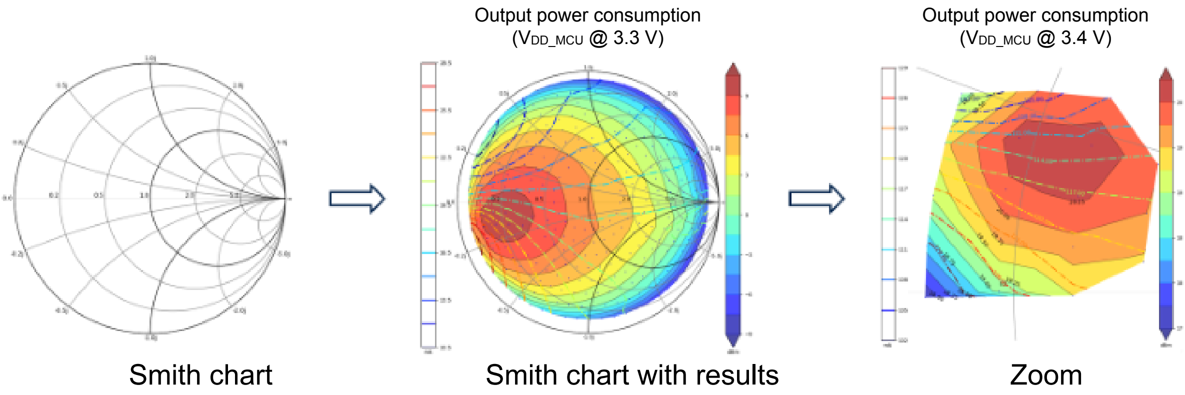
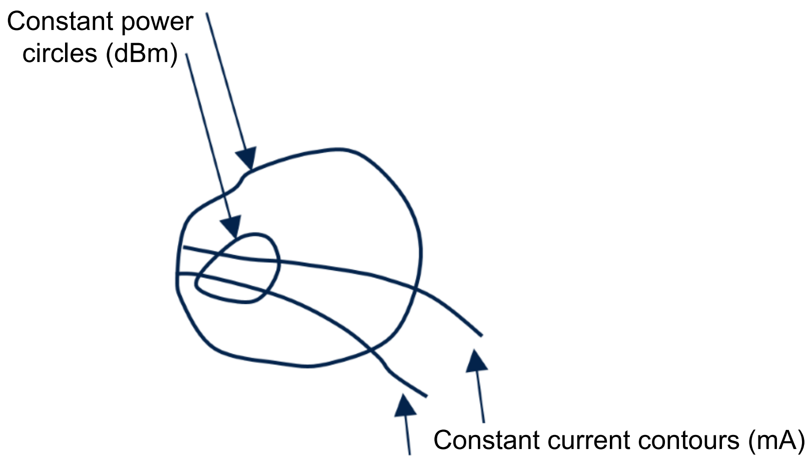


Figure 70. Example of constant power circles and constant current contours of a typical impedance extraction by load-pull analysis



Results

Important:

- *The results are obtained using the "PA optimal setting and operation modes" (see the product reference manual for more information).*
- *Add **0.5 dB** to the results below, due to losses in the RF cables, connectors and tuners used in the measurement.*
- *When operating with high current values (> 100 mA), a voltage drop (about tens of mV) may happen on the V_{DD_MCU}/V_{DDRF}, due to cable or board traces. In such cases, the user must correct the voltage drop or slightly increase the $V_{DD\ MCU}$ by 100 or 150 mV.*
- *The impedance values reported in the tables below are the values from the plot but de-embedded from test fixtures.*
- *The PA output impedance is the complex conjugated of the impedance values reported in the next pages. For example, if the read value from the plot is (15.27 **+** j1.27) Ω, it means that it was the impedance presented to the PA. The PA output impedance is therefore (15.27 **–** j1.27) Ω.*

A.1.1 Example 1 (UFBGA73, 22 dBm, 868 MHz)

UFBGA73 package, 22 dBm @ 868 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 868 MHz
- PA mode: HP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x7
- `PaSel`: 0
- `Power`: 0x16

For each example below, when doing the impedance matching, change L and C to move between the points of the figure as described in Section 2.2.2 . The goal is to have good RF output power and low current consumption.

Use AT_Slave or STM32Cube RF Monitor to perform the matching network.

Figure 71. **Output power consumption (UFBGA73, 22 dBm @ 868 MHz, VDD_MCU = 3.3 V)**

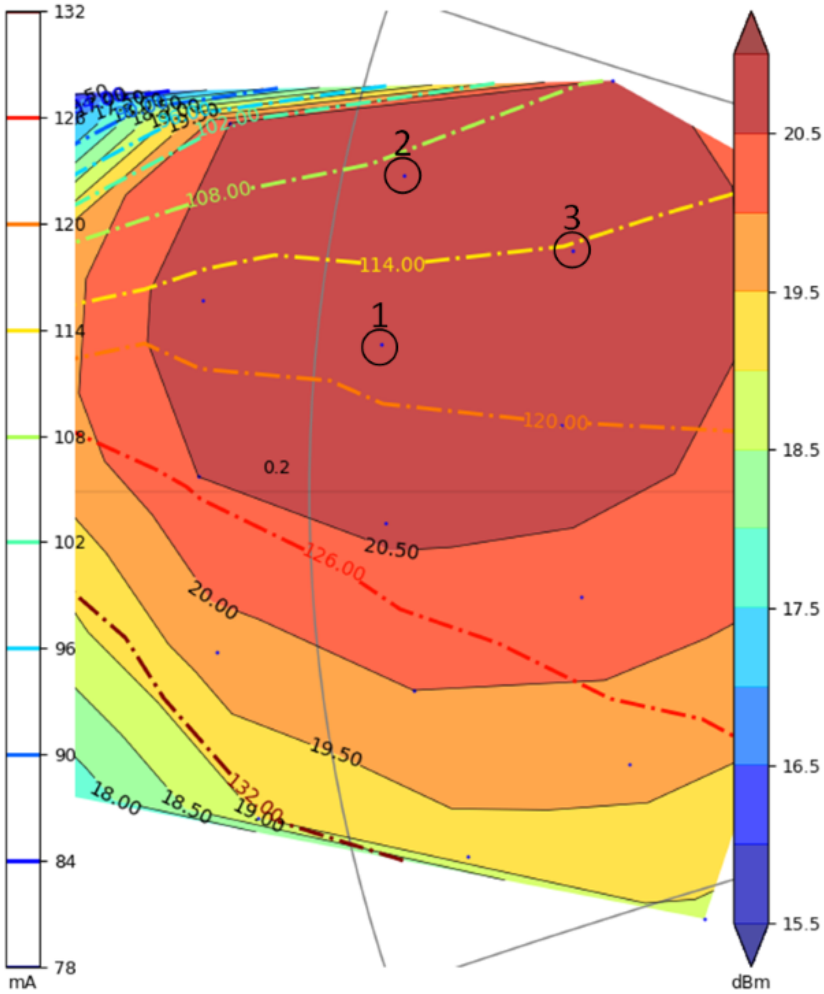


Table 5. **Results for example 1**

	Impedance (Ω)	Current (mA)	Power (dBm)
1	11.83 + j4.55	117.94	21
2	12.37 + j8.25	109.44	20.9
3	16.26 + j6.51	114.24	20.9

A.1.2 Example 2 (UFBGA73, 14 dBm, 868 MHz)

UFBGA73 package, 14 dBm @ 868 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 868 MHz
- PA mode: LP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x0
- `PaSel`: 1
- `Power`: 0x0E

Figure 72. Output power consumption (UFBGA73, 14 dBm @ 868 MHz, VDD_MCU = 3.3 V)

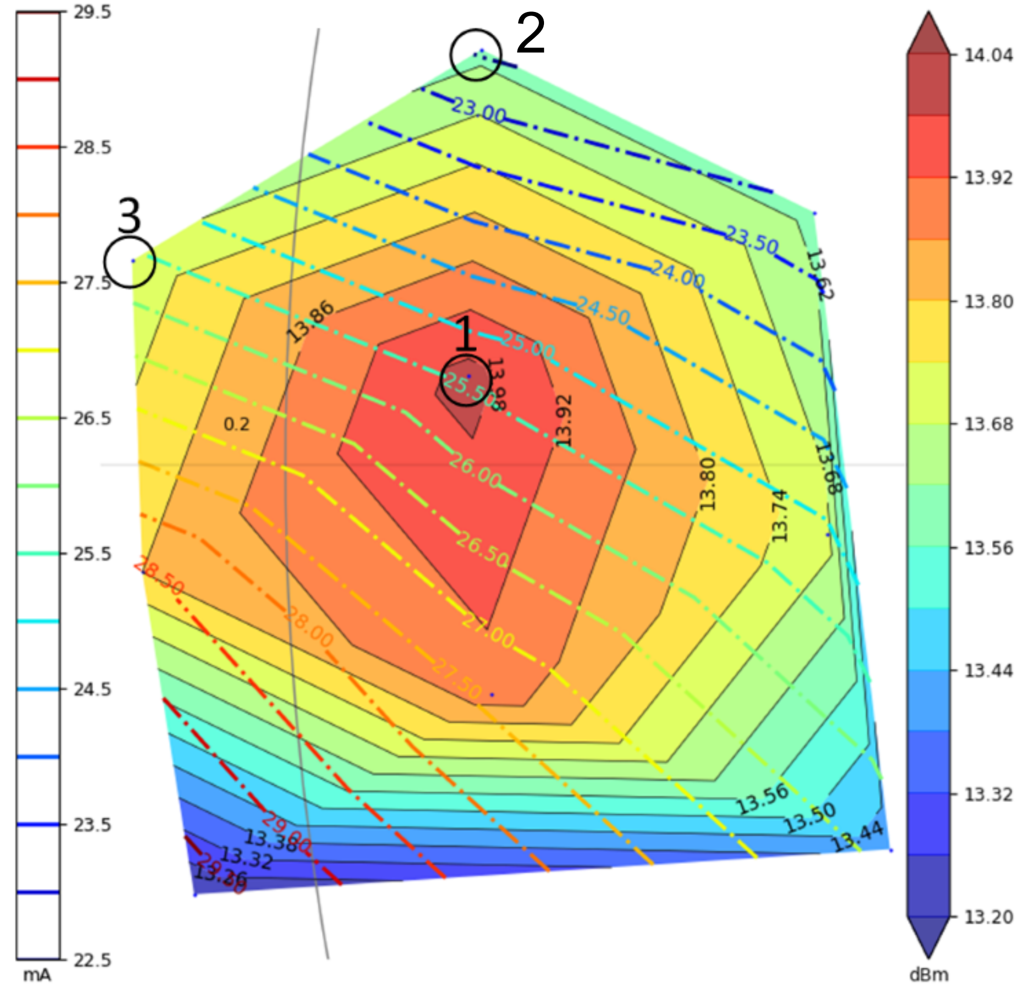


Table 6. Results for example 2

Impedance (Ω)		Current (mA)	Power (dBm)
1	11.92 + j1.00	25.36	14.0
2	11.75 + j4.65	22.44	13.6
3	8.38 + j2.08	25.58	13.7

A.1.3 Example 3 (UFBGA73, 22 dBm, 900 MHz)

UFBGA73 package, 22 dBm @ 900 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 900 MHz
- PA mode: HP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x7
- `PaSel`: 0
- `Power`: 0x16

Figure 73. Output power consumption (UFBGA73, 22 dBm @ 900 MHz, VDD_MCU = 3.3 V)

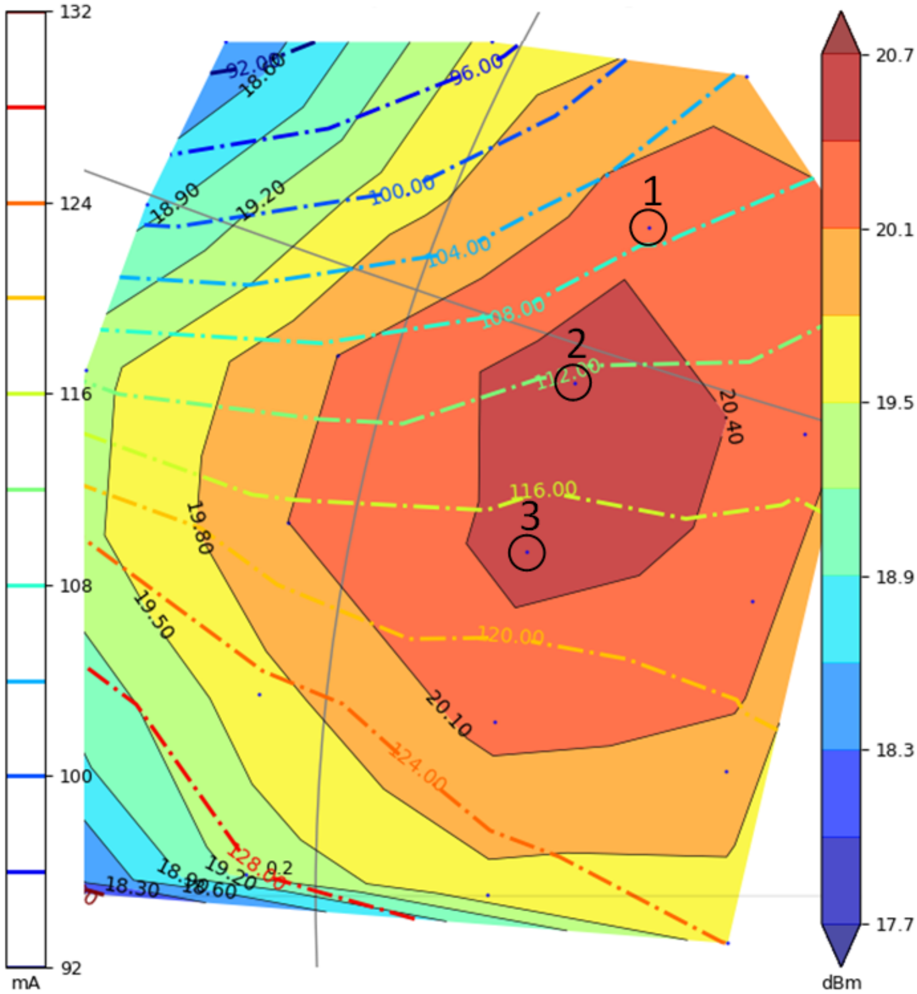


Table 7. Results for example 3

Impedance (Ω)		Current (mA)	Power (dBm)
1	16.32 + j14.50	107.43	20.3
2	15.14 + j10.92	112.56	20.6
3	14.32 + j7.48	117.88	20.5

A.1.4 Example 4 (UFBGA73, 22 dBm, 915 MHz)

UFBGA73 package, 22 dBm @ 915 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 915 MHz
- PA mode: HP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x7
- `PaSel`: 0
- `Power`: 0x16

Figure 74. Output power consumption (UFBGA73, 22 dBm @ 915 MHz, VDD_MCU = 3.3 V)

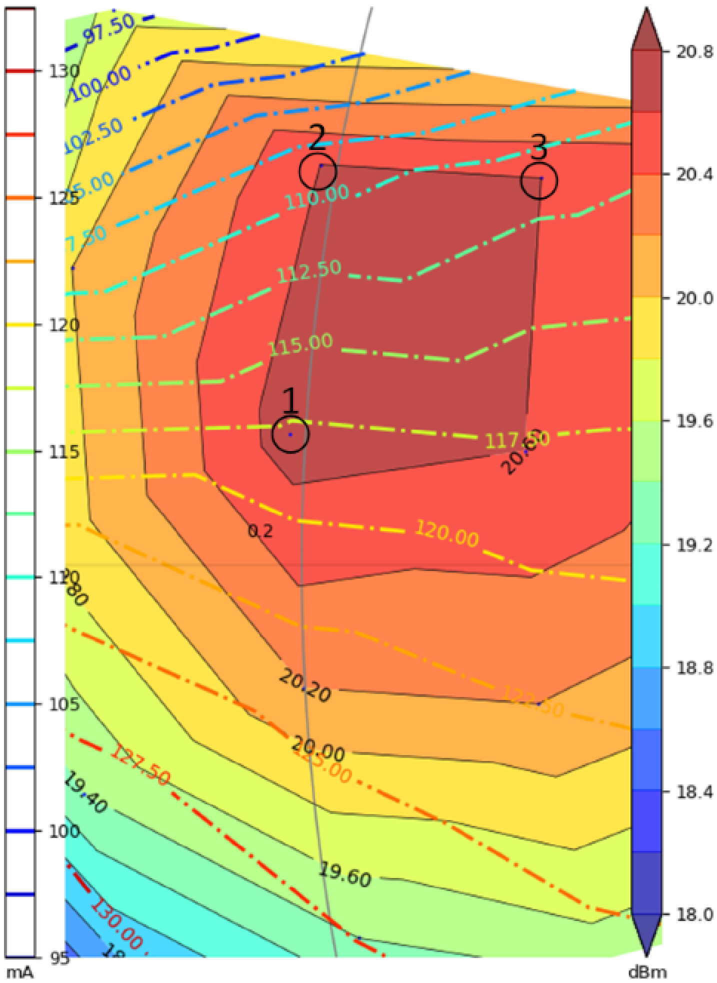


Table 8. Results for example 4

	Impedance (Ω)	Current (mA)	Power (dBm)
1	10.13 + j3.52	117.96	20.7
2	10.73 + j7.23	108.87	20.6
3	14.01 + j7.00	111.57	20.6

A.1.5 Example 5 (UFBGA73, 14 dBm, 915 MHz)

UFBGA73 package, 14 dBm @ 915 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 915 MHz
- PA mode: LP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x0
- `PaSel`: 1
- `Power`: 0x0E

Figure 75. **Output power consumption (UFBGA73, 14 dBm @ 915 MHz, VDD_MCU = 3.3 V)**

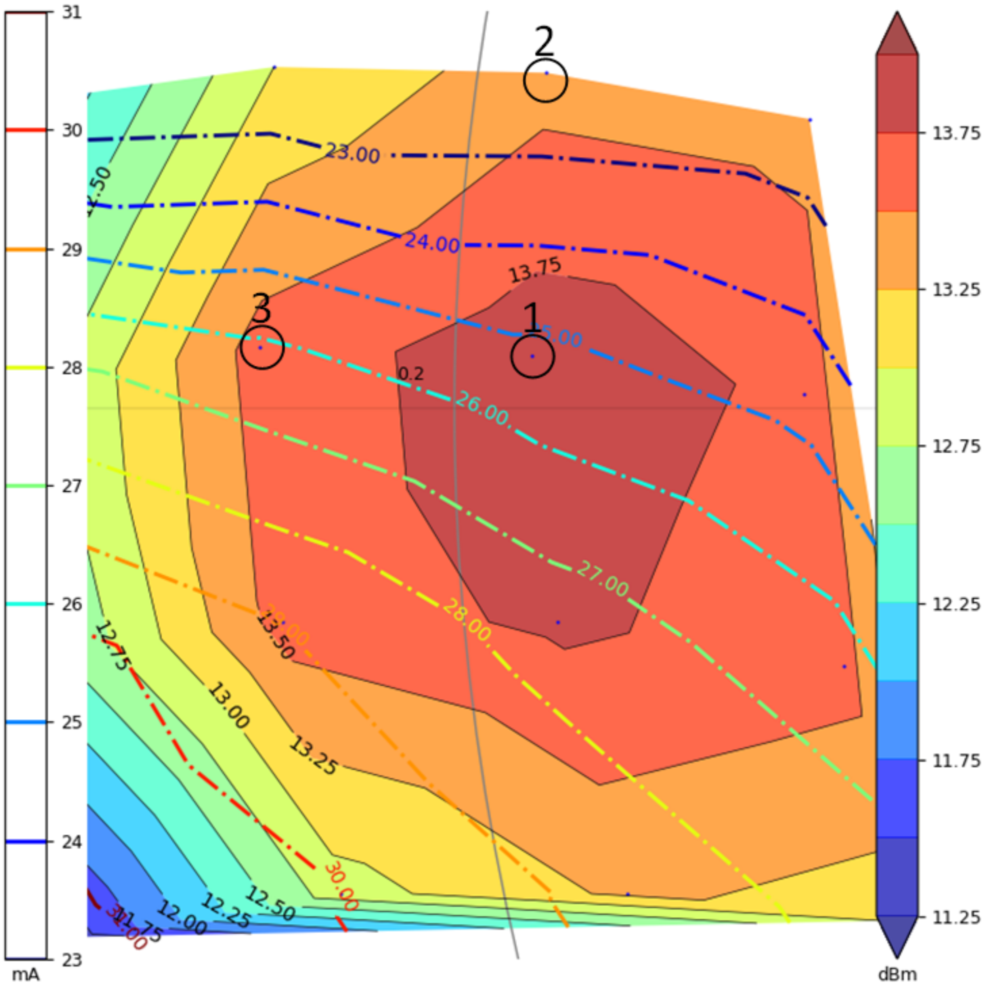


Table 9. **Results for example 5**

	Impedance (Ω)	Current (mA)	Power (dBm)
1	10.97 + j0.66	25.24	13.9
2	10.85 + j4.27	22.06	13.4
3	7.67 + j0.70	26.14	13.6

A.1.6 Example 6 (UFBGA73, 22 dBm, 923 MHz)

UFBGA73 package, 22 dBm @ 923 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 923 MHz
- PA mode: HP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x7
- `PaSel`: 0
- `Power`: 0x16

Figure 76. Output power consumption (UFBGA73, 22 dBm @ 923 MHz, VDD_MCU = 3.3 V)

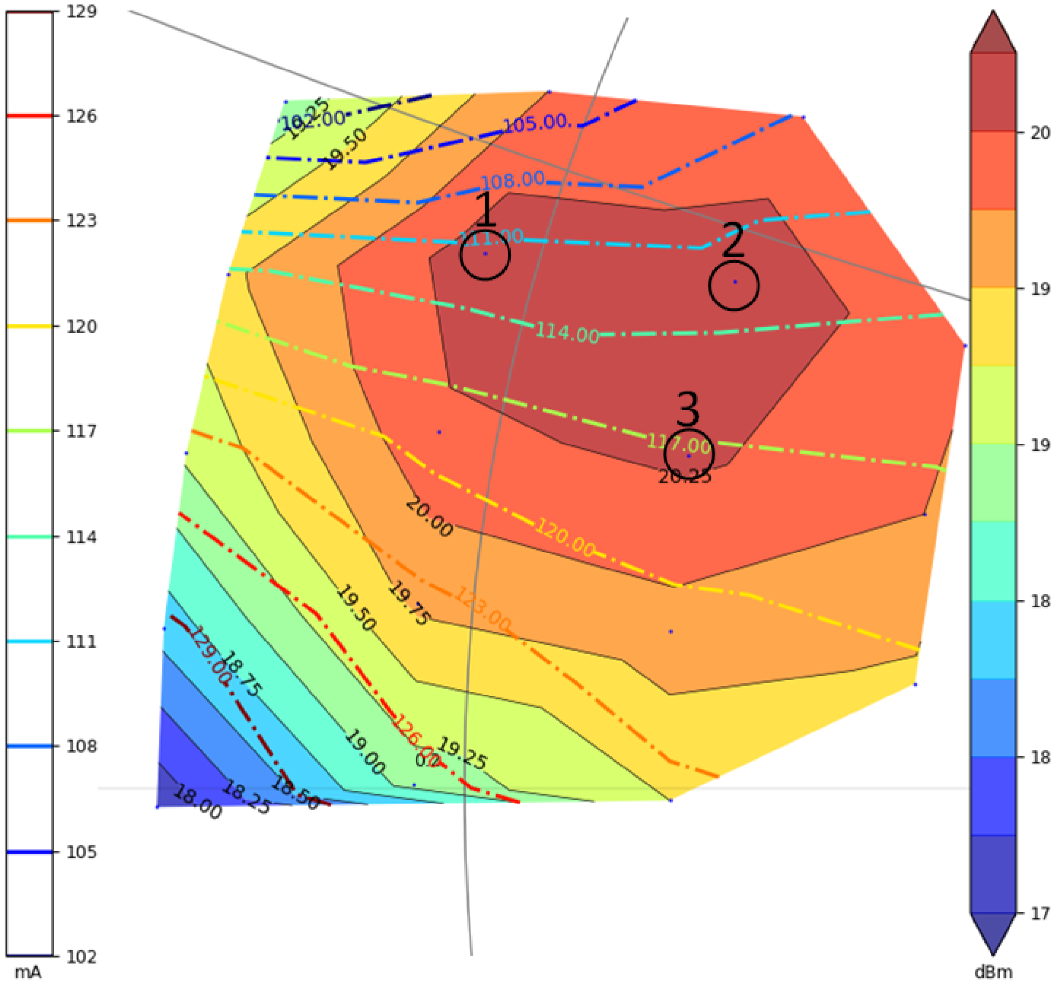


Table 10. Results for example 6

	Impedance (Ω)	Current (mA)	Power (dBm)
1	10.58 + j10.71	111.8	20.4
2	15.48 + j10.60	112.63	20.4
3	14.475 + j7.189	117.26	20.3

A.1.7 Example 7 (UFQFPN48, 14 dBm, 868 MHz)

UFQFPN48 package, 14 dBm @ 868 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 868 MHz
- PA mode: LP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x0
- `PaSel`: 1
- `Power`: 0x0E

Figure 77. Output power consumption (UFQFPN48, 14 dBm @ 868 MHz, VDD_MCU = 3.3 V)

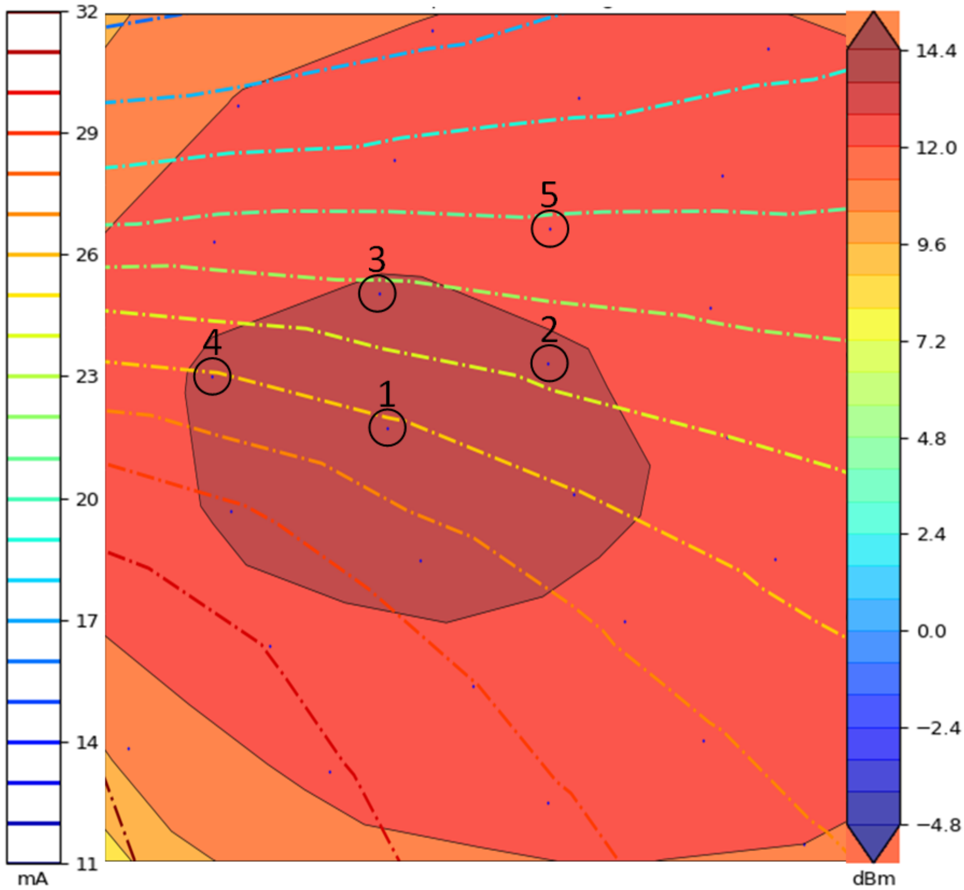


Table 11. Results for example 7

	Impedance (Ω)	Current (mA)	Power (dBm)
1	11.36 + j0.37	25.74	14.0
2	15.27 + 1.27	23.58	13.6
3	11.58 + j3.67	22.78	13.6
4	7.924 + j1.97	25.60	13.7
5	15.80 + j5.16	21.22	13.2

A.1.8 Example 8 (UFQFPN48, 15 dBm, 868 MHz)

UFQFPN48 package, 15 dBm @ 868 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):
- Frequency: 868 MHz
- PA mode: LP
- `PaDutyCycle`: 0x6
- `HpMax`: 0x0
- `PaSel`: 1
- `Power`: 0x0E

Figure 78. Output power consumption (UFQFPN48, 15 dBm @ 868 MHz, VDD_MCU = 3.3 V)

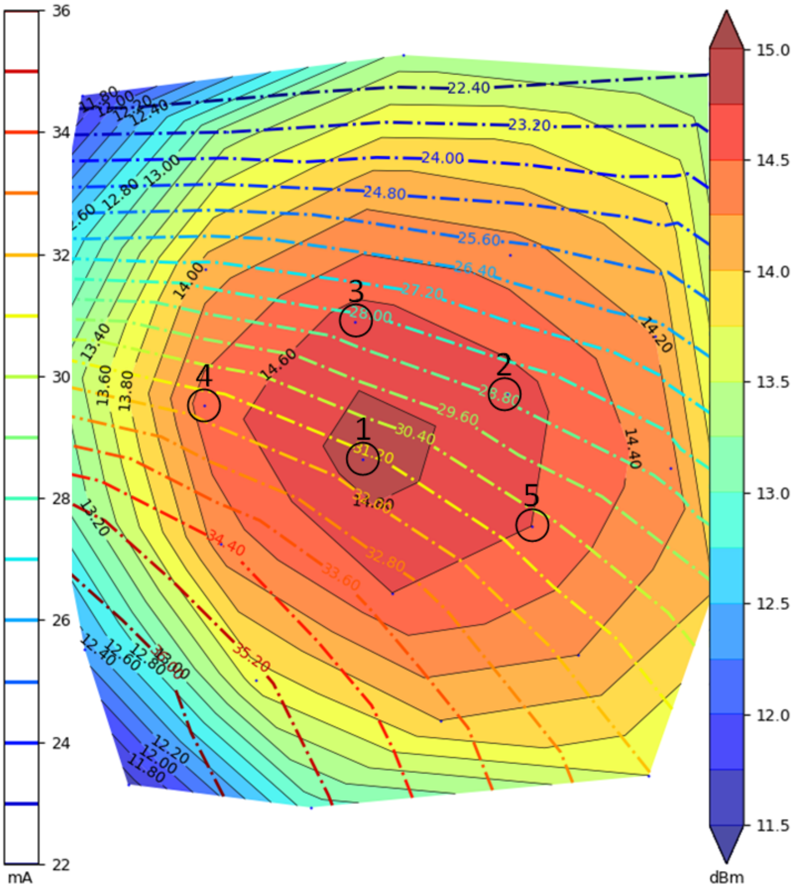


Table 12. Results for example 8

	Impedance (Ω)	Current (mA)	Power (dBm)
1	11.30 + j0.08	31.41	14.9
2	15.27 + j1.25	28.63	14.7
3	11.65 + j3.64	28.23	14.7
4	7.88 + j1.97	31.68	14.5
5	14.86 – j2.65	30.7	14.6

A.1.9 Example 9 (UFQFPN48, 22 dBm, 868 MHz)

UFQFPN48 package, 22 dBm @ 868 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 868 MHz
- PA mode: HP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x7
- `PaSel`: 0
- `Power`: 0x16

Figure 79. **Output power consumption (UFQFPN48, 22 dBm @ 868 MHz, VDD_MCU = 3.3 V)**

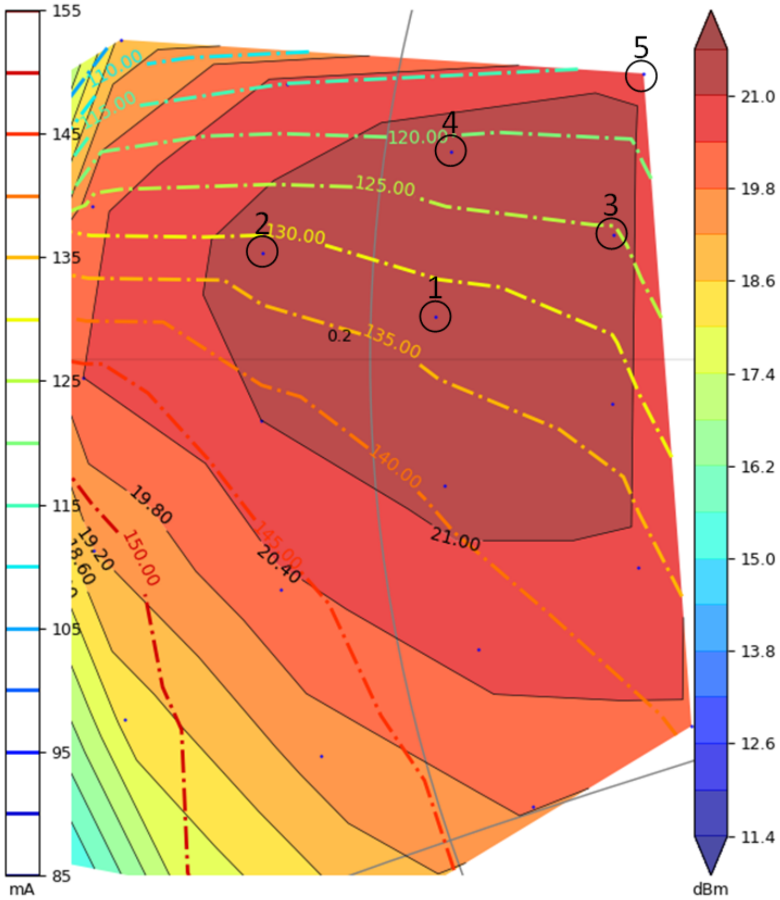


Table 13. **Results for example 9**

	Impedance (Ω)	Current (mA)	Power (dBm)
1	11.31 + j0.91	132.57	21.5
2	7.85 + j2.04	131.77	21.3
3	15.26 + j3.00	125.54	21.4
4	11.39 + j4.43	121.24	21.3
5	15.29 + j6.91	116.22	20.9

A.1.10 Example 10 (UFQFPN48, 14 dBm, 915 MHz)

UFQFPN48 package, 14 dBm @ 915 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 915 MHz
- PA mode: LP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x0
- `PaSel`: 1
- `Power`: 0x0E

Figure 80. Output power consumption (UFQFPN48, 14 dBm @ 915 MHz, VDD_MCU = 3.3 V)

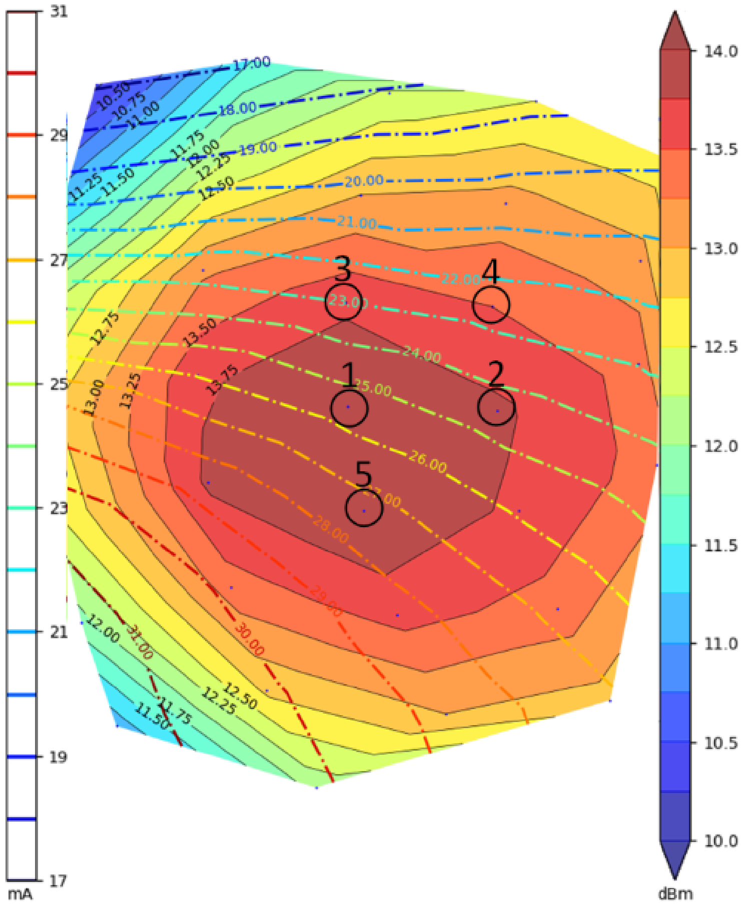


Table 14. Results for example 10

	Impedance (Ω)	Current (mA)	Power (dBm)
1	10.80 + j2.026	25.51	14.0
2	14.25 + j1.24	24.46	13.8
3	11.09 + j4.90	23.01	13.7
4	14.65 + j4.37	22.54	13.5
5	10.59 – j0.82	27.38	14.0

A.1.11 Example 11 (UFQFPN48, 15 dBm, 915 MHz)

UFQFPN48 package, 15 dBm @ 915 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 915 MHz
- PA mode: LP
- `PaDutyCycle`: 0x6
- `HpMax`: 0x0
- `PaSel`: 1
- `Power`: 0x0E

Figure 81. Output power consumption (UFQFPN48, 15 dBm @ 915 MHz, VDD_MCU = 3.3 V)

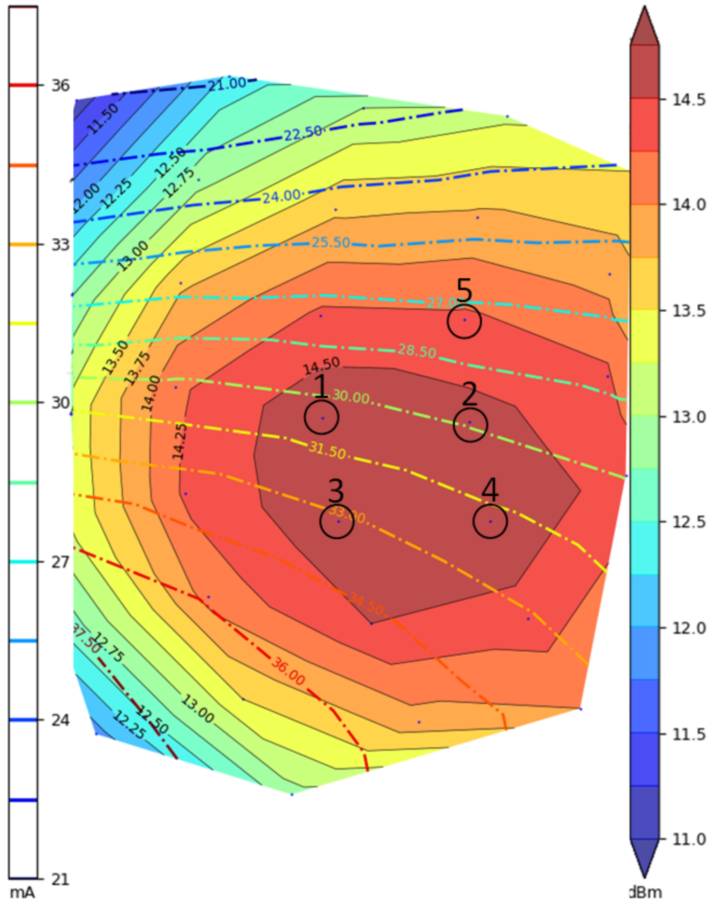


Table 15. Results for example 11

	Impedance (Ω)	Current (mA)	Power (dBm)
1	10.83 + j2.01	30.65	14.7
2	14.18 + j1.20	29.87	14.6
3	10.63 - j0.81	33.22	14.7
4	14.01 - j1.80	31.87	14.7
5	14.62 + j4.44	27.41	14.3

A.1.12 Example 12 (UFQFPN48, 22 dBm, 915 MHz)

UFQFPN48 package, 22 dBm @ 915 MHz, V_{DD_MCU} = 3.3 V.

Configuration (optimal setting):

- Frequency: 915 MHz
- PA mode: HP
- `PaDutyCycle`: 0x4
- `HpMax`: 0x7
- `PaSel`: 0
- `Power`: 0x16

Figure 82. Output power consumption (UFQFPN48, 22 dBm @ 915 MHz, VDD_MCU = 3.3 V)

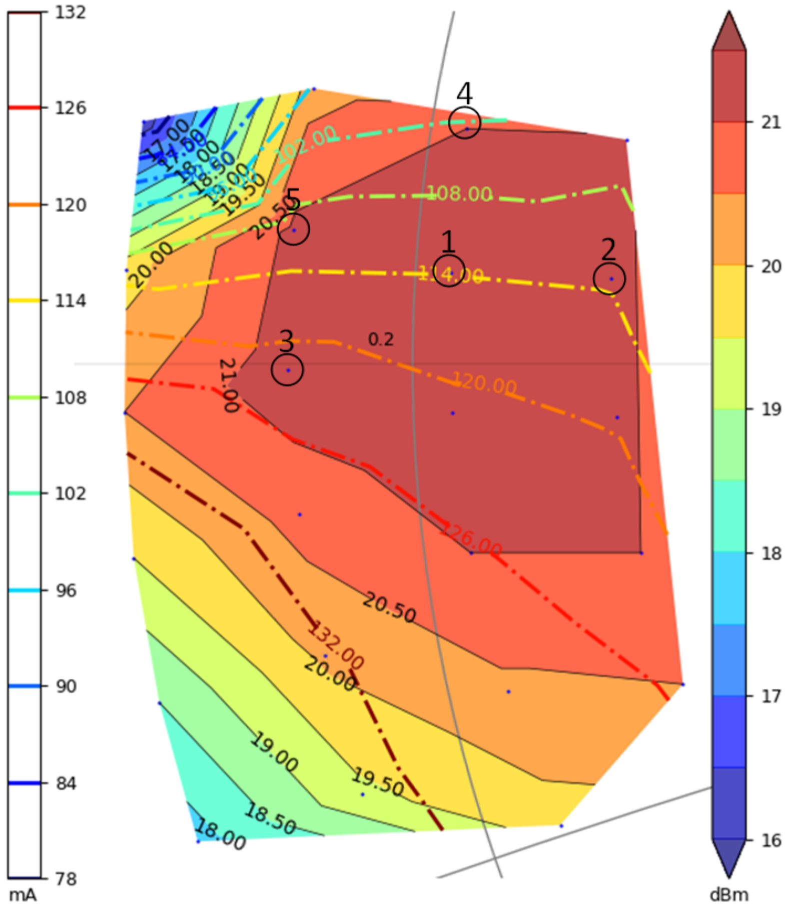


Table 16. Results for example 12

	Impedance (Ω)	Current (mA)	Power (dBm)
1	10.71 + j1.85	113.86	21.5
2	14.13 + j1.96	113.31	21.4
3	7.63 - j0.12	122.48	21.3
4	10.69 + j4.77	102.97	21.0
5	7.65 + j2.47	110.40	21.1

A.2 LNA matching impedance measurements

The optimal impedance is obtained by source-pull analysis, considering the RSSI and noise figure (NF) of the receiver. Measured LNA impedance values are detailed in the tables below, as well as the optimal impedances to be presented to the LNA to obtain the maximum performance of the receiver. Impedances are always reported in ohms in this document.

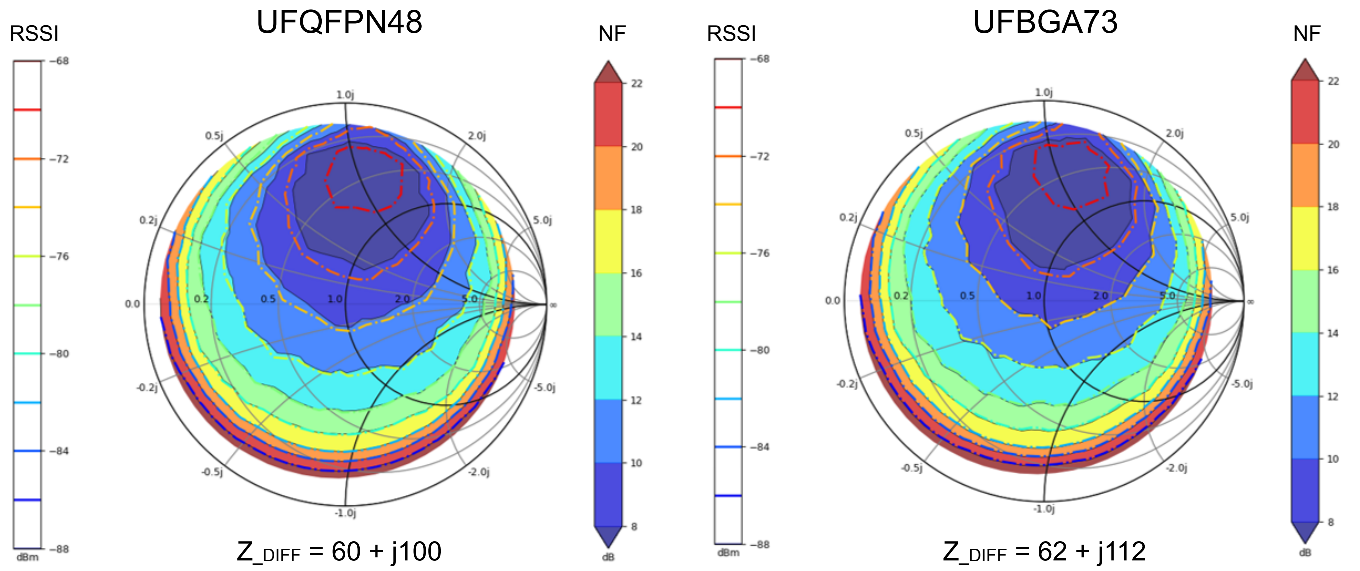
Table 17. **Optimal differential impedance values at device pin level**

Frequency (MHz)	Z_{OPT} (Ω)	
	UFQFPN48	UFBGA73
433	146 + j204	148 + j220
490	142 + j186	144 + j160
868	52 + j102	52 + j104
915	60 + j100	62 + j112

Z_{OPT} illustrations

The graphic below shows an example of a source pull for the packages UFQPN48 and UFBGA73. The lines represent different RSSI values and the circles different noise figures (NF).

Figure 83. **Source-pull analysis results for 915 MHz**



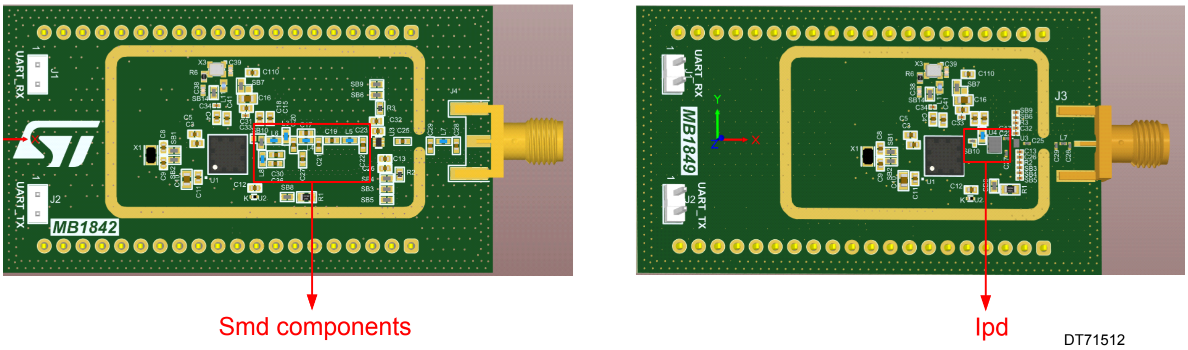
A.3 Integrated passive device (IPD)

When doing RF matching with smd components, the designer must face some aspects of design like difficult matching for maximum output power. He also needs an expensive hardware for the test. The main deviation of values for capacitors and inductors can affect the matching and decrease the transmitted power. A specific value of components is not available in the market.

To avoid these problems, an IPD can be used. IPDs are components that are conceived for a specific application (in this case impedance matching). This component has a low deviation of parameters if compared with smd components. For optimum performance, IPDs are dependent of PCB stack-up, and can simplify the design issue since they are plug-and-play.

The graphic below shows other benefits using IPDs in design such as reduction of bill of materials and system integration.

Figure 84. Board MB1842 solution with smd components and board MB1849 solution with IPD



Appendix B

Table 18. **Rapid conversion table of RF measurements**

Reflection coefficient (Γ)	Return loss (dB)	Mismatch loss (dB)	VSWR	Reflected power (%)	Transmitted power (%)
0.99	0.09	17.01	199.00	98.01	1.99
0.90	0.92	7.21	19.00	81.00	19.00
0.85	1.41	5.57	12.33	72.25	27.75
0.80	1.94	4.44	9.00	64.00	36.00
0.75	2.50	3.59	7.00	56.25	43.75
0.70	3.10	2.92	5.67	49.00	51.00
0.65	3.74	2.38	4.71	42.25	57.75
0.60	4.44	1.94	4.00	36.00	64.00
0.55	5.19	1.56	3.44	30.25	69.75
0.50	6.02	1.25	3.00	25.00	75.00
0.45	6.94	0.98	2.64	20.25	79.75
0.40	7.96	0.76	2.33	16.00	84.00
0.35	9.12	0.57	2.08	12.25	87.75
0.30	10.46	0.41	1.86	9.00	91.00
0.25	12.04	0.28	1.67	6.25	93.75
0.20	13.98	0.18	1.50	4.00	96.00
0.15	16.48	0.10	1.35	2.25	97.75
0.10	20.00	0.04	1.22	1.00	99.00
0.05	26.02	0.01	1.11	0.25	99.75
0.01	40.00	0.00	1.02	0.01	99.99

Table 19. **Main definitions**

Parameter	Definition
Reflection coefficient (Γ)	$\Gamma = \frac{V_-}{V_+} = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_0}{Z_L + Z_0}, \ \text{-}1 \leq \Gamma > 1 \ or \ \ 0 \leq \lvert\Gamma\rvert \ \ \leq 1$
Voltage standing wave ratio (VSWR)	$VSWR = \frac{V_{z\ \max}}{V_{z\ \min}} = \frac{1+\Gamma}{1-\Gamma}, \quad 1 \leq VSWR \ \ \leq \infty$
Return loss (dB)	$RL = 10 \times \log\left(\frac{P_{incident}}{P_{reflected}}\right) = P_{incident\ dB} - P_{reflected\ dB}$ $RL = 10 \times \log\left(\frac{1}{\lvert\Gamma\rvert^2}\right) = \text{-}20 \times \log(\lvert\Gamma\rvert) \quad or \quad RL = -20 \times \log\left(\frac{VSWR-1}{VSWR+1}\right)$
Mismatch loss (dB)	$ML = 10 \times \log\left(\frac{P_{incident}}{P_{incident} - P_{reflected}}\right) = P_{incident\ dB} - P_{delivered\ dB}$ $ML = 10 \times \log\left(1-\Gamma^2\right)$ $Reflectedpower\,(\%) = P_{reflected} = 100 \times \Gamma^2 \quad and$ $Deliveredpower\,(\%) = P_{delivered} = 100 \times \left(1-\Gamma^2\right)$

Figure 85. VSWR versus Γ

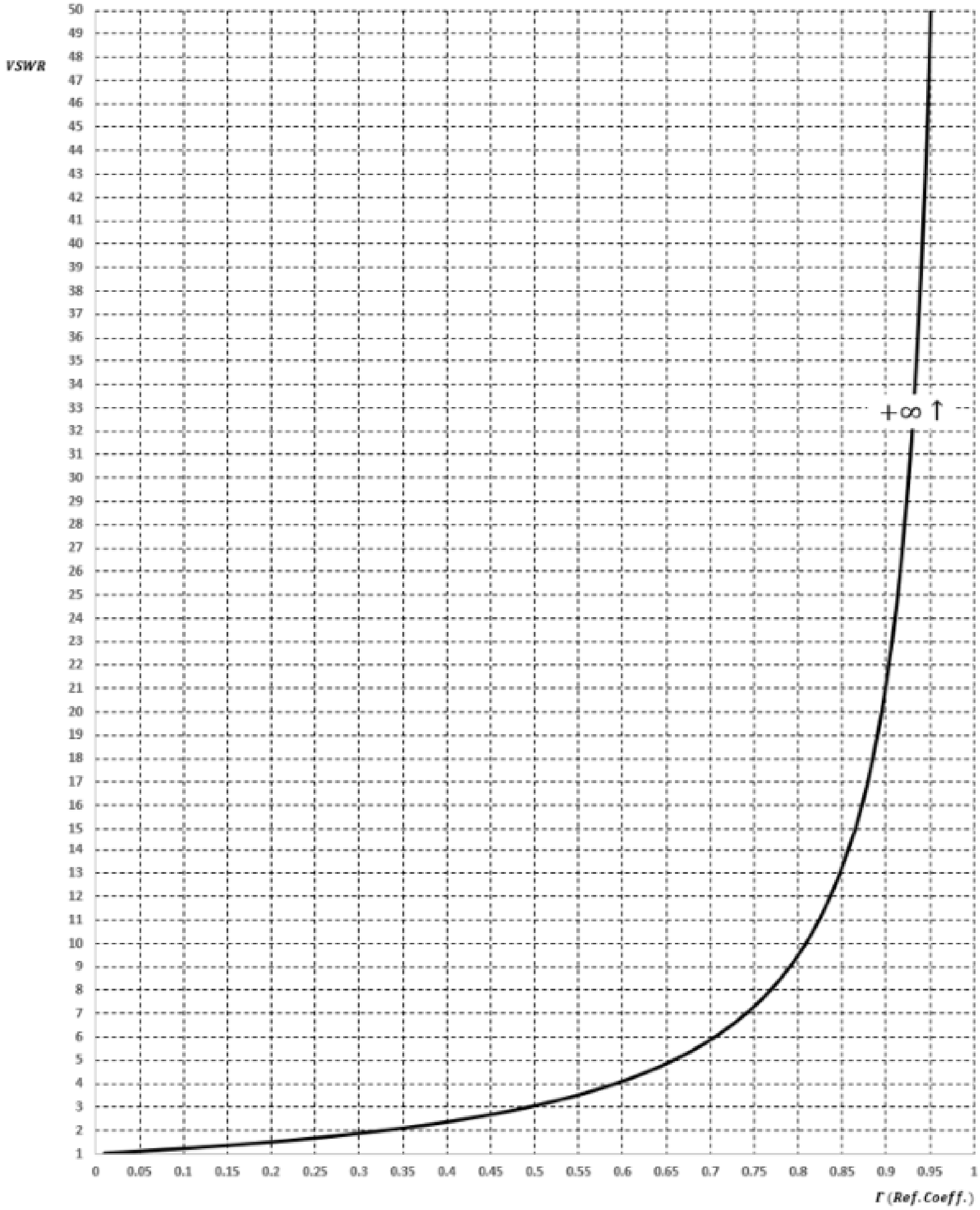


Figure 86. Mismatch loss (-10 log(1-Γ2)) in DB

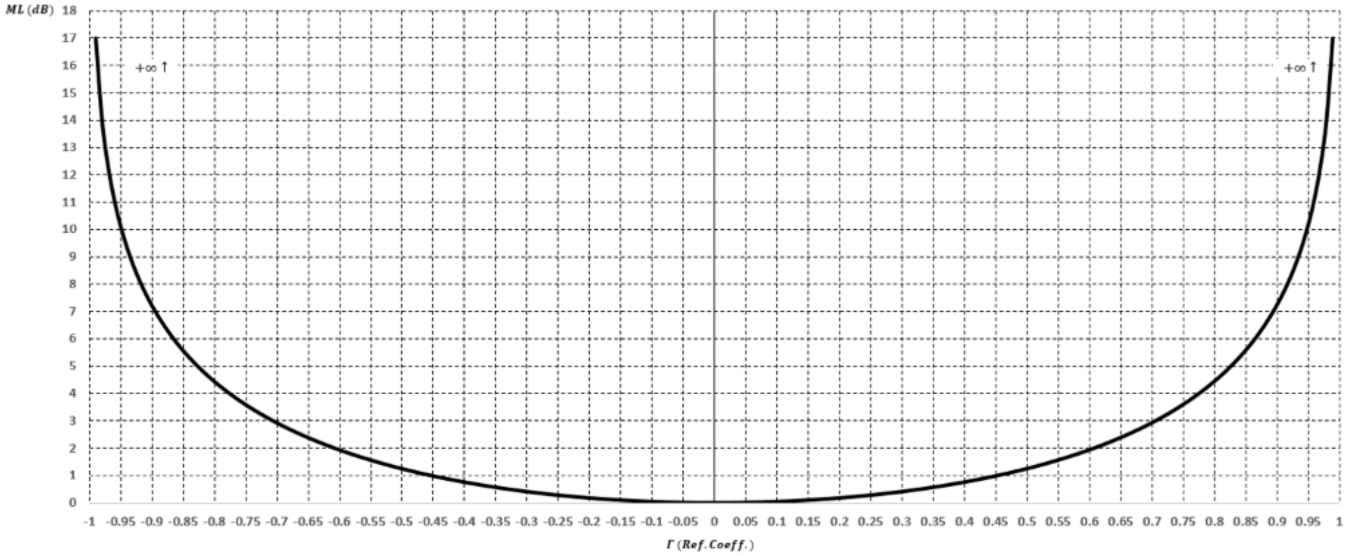
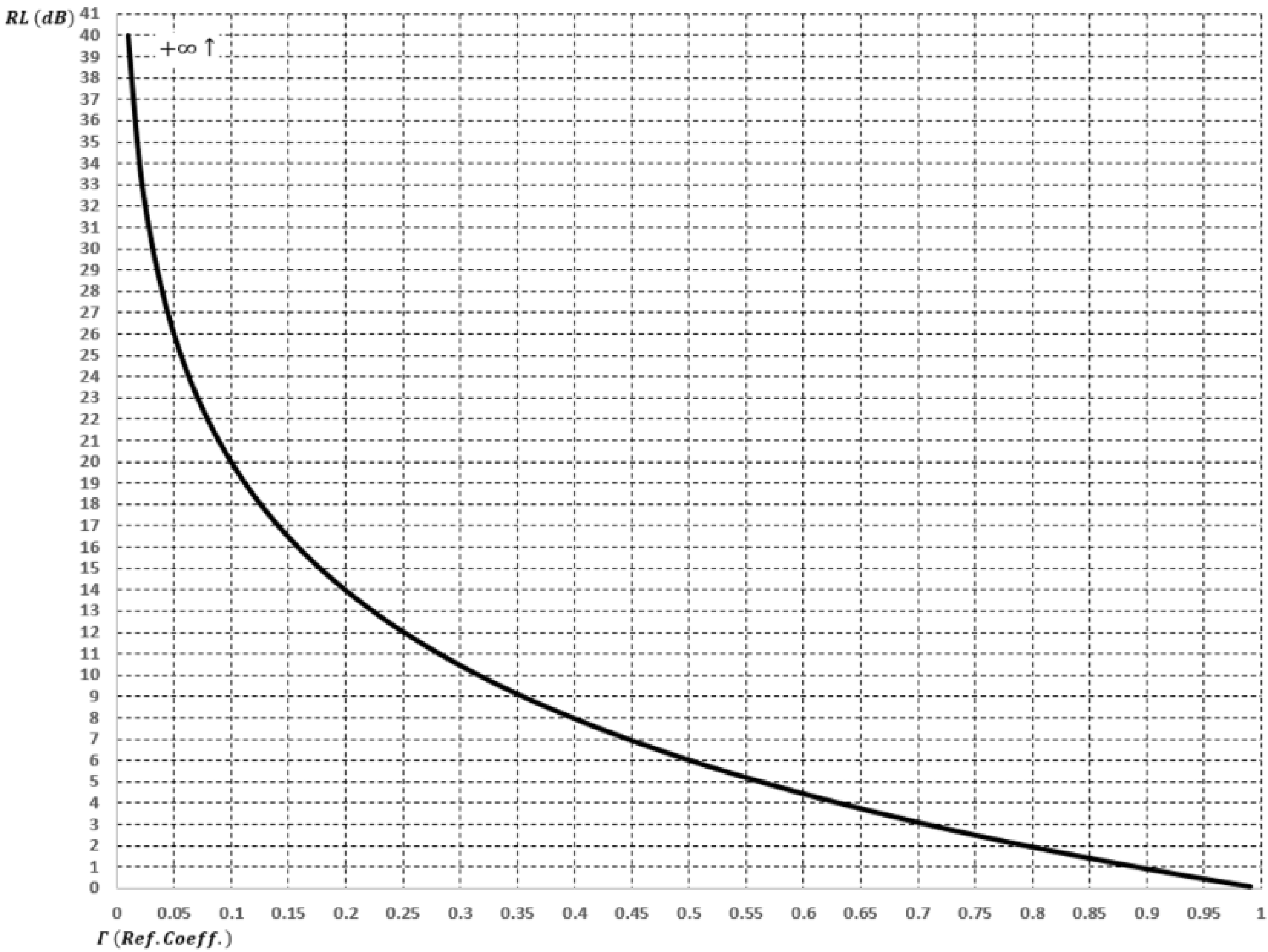


Figure 87. Return loss (-10 log(|Γ|2) in DB



Revision history

Table 20. Document revision history

Date	Version	Changes
8-Dec-2020	1	Initial release.
15-Dec-2020	2	Updated: • Figure 32. Illustration on Smith chart of the addition of the first matching LC cell • Figure 39. Low-pass Pi filter simulation of S-parameters vs frequency for ideal (black) vs real component s-parameters (red) • Figure 40. Low-pass Pi filter S-parameters vs frequency for implementation on PCB • Figure 42. Low-pass Pi filter S-parameters vs frequency for implementation on PCB after tweaking component values • Figure 50. Impedance of the previous example represented on the Smith chart • Figure 51. Impact on impedance after adding 3.35 mm of TLine between device RF output and matching network (MN) • Table 11. Results for example 7 • Figure 80. Output power consumption (UFQFPN48, 14 dBm @ 915 MHz, VDD_MCU = 3.3 V)
12-Dec-2022	3	Updated various typos and graphics. Added Section A.3 Integrated passive device (IPD).

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