AN2626
Application note

MOSFET body diode recovery mechanism in a phase-shifted ZVS full bridge DC/DC converter

Introduction

The ZVS exploits the parasitic circuit elements to guarantee zero voltage across the switching device before turn on, eliminating hence any power losses due to the simultaneous overlap of switch current and voltage at each transition [*1*].

In order to allow the ZVS condition, the intrinsic body diode of the MOSFET has to conduct; in no or low load operation the extremely low reverse voltage, could be not sufficient to guarantee the reverse recovery charge sweep out before turning off the MOSFET. Hence, the body diode could be stressed by high dv/dt that latching the parasitic internal bipolar transistor brings the MOSFET to the failure.

In the market of power applications like telecom power supply, main frame computer-server, welding and steel cutting, the demand of power density is growing each year. Increasing power density means reducing component counts, power losses, heat-sink and reactive component size. The alternative to the hard switched full bridge, typical topology for these applications, was the phase-shifted zero voltage switching (ZVS) full bridge. This ZVS technique guarantees zero voltage across the switching device before turn on, eliminating hence any power losses due to the simultaneous overlap of switch current and voltage at each transition.

By this switching technique also at high frequencies, the switching losses are low; hence it allows the reduction of the components reactive size only. Obviously, by having lower losses lower heat-sink size is allowed. Furthermore, by avoiding the hard-switching condition the EMI/RFI noise is reduced.

The zero voltage condition occurs by the intrinsic MOSFET body diode conduction; an extremely low reverse voltage, occurring at no or low load operation, which could be not sufficient to guarantee the reverse recovery charge sweep out before turning off the MOSFET. In this condition high dv/dt values could turn on the intrinsic bipolar and destroy the MOSFET.

The deep studies of these failure mechanisms have led STMicroelectronics to design new technology in order to develop MOSFETs really suitable for high power phase-shifted ZVS applications. In this technical note we will investigate the possible triggering on of the internal parasitic bipolar.

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1 Topology description

The basic circuit of the phase-shifted converter is composed by four switches; two for each "leg".

The switches, labeled Q1 through Q4 in the *Figure 1* are shunted by their intrinsic body diode (D1 through D4) and intrinsic output capacitance (C1 through C4), shown separately in order to clarify their role in the global functioning.

Figure 1. Phase-shifted ZVS full bridge circuit

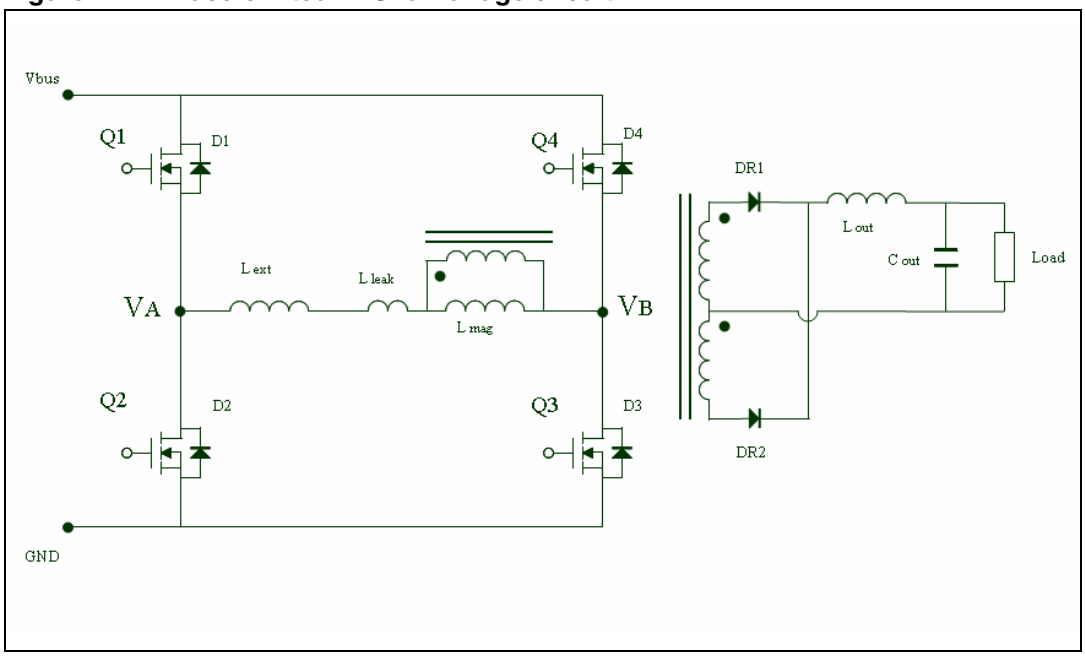
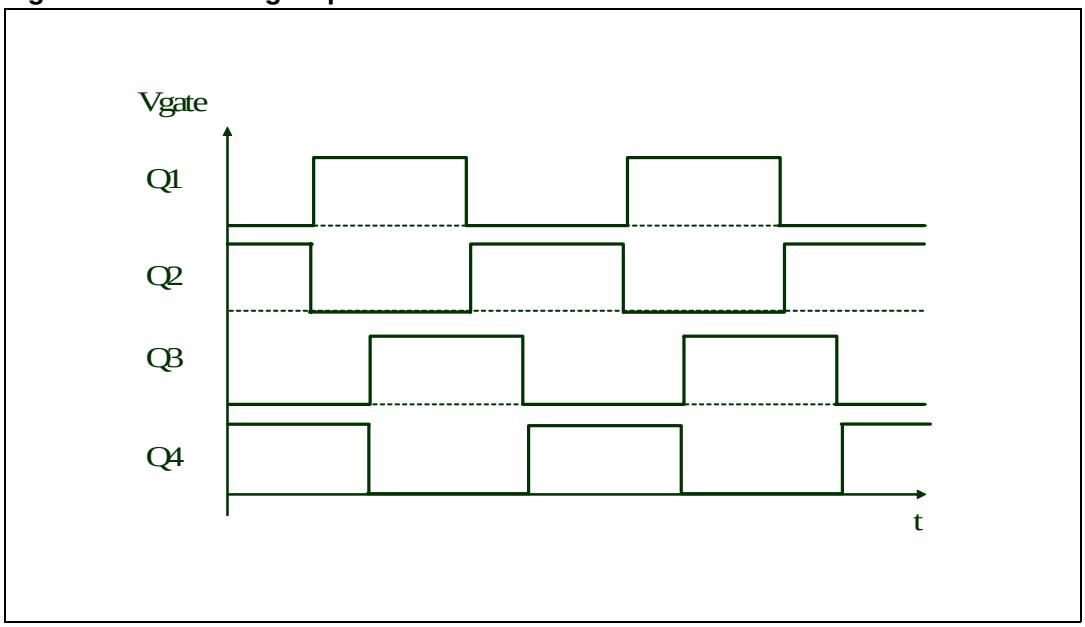


Figure 2. Switching sequence in a P-S ZVS FB converter DC/DC



- Transition t_0-t_1

From the *Figure 3*, at t_0 Q1 and Q3 are in on state and on the primary side there is an energy equal to:

Equation 1

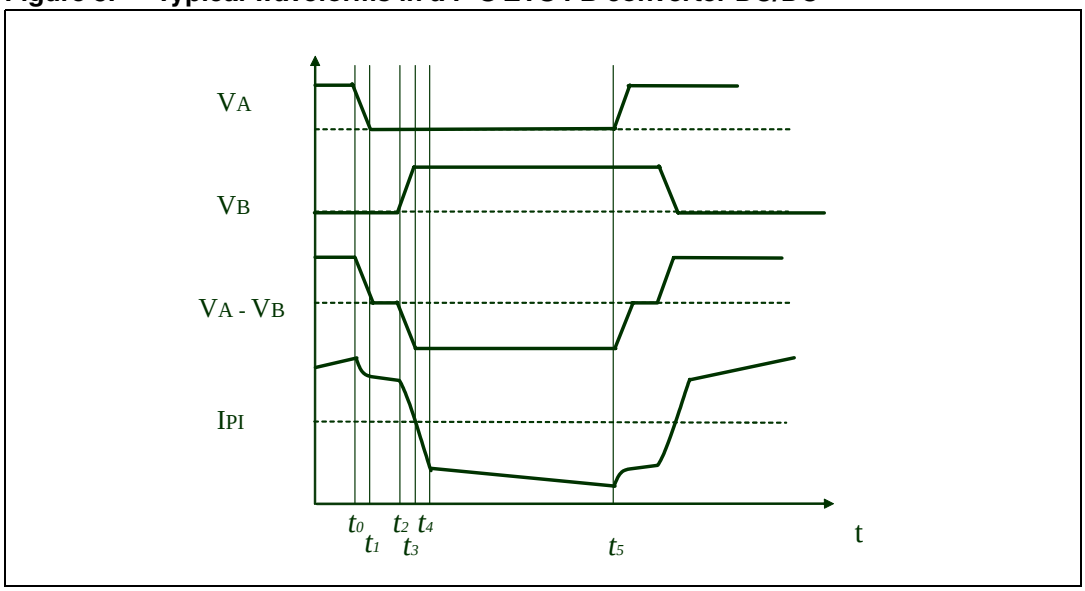
$$E_{t_0-t_1} = E_{mag} - E_{output-reflected} + \frac{1}{2}(L_{leak} + L_{res}) \cdot (I_{mag}(t_0) + NI_{out}(t_0))$$

Instantly, at t_0 the switch Q1 is turned off and the resonant transition begins. The primary current continues to flow, with a like-linear shape (since the current is forced by the output inductor) using the charge stored in the switch output capacitance C2. Simultaneously, the primary current will charge the output capacitance C1 of Q1 from essentially 0 V to the supply voltage V_{dd}, and will discharge the output capacitance C2 from V_{dd} to zero. The transition finishes when the Q2 source voltage exceeds the Q2 drain voltage sufficiently to directly bias the internal body diode D2.

- Freewheeling t_1-t_2

Now D3 is directly biased and the output inductor freewheels. The voltage across the switch Q2 is equal to the drop on its internal body diode D2 hence the ZVS condition is verified. The switch Q3 is turned on and the current, flowing through the primary side, now is shared between the body diode D2 and the channel of MOSFET Q2. During the freewheeling state both output rectifier diodes are forward biased, and hence the reflected voltage to the primary is null.

Figure 3. Typical waveforms in a P-S ZVS FB converter DC/DC



- Transition t_2-t_4

The switch Q3 is turned off, the energy available to complete the transition is:

Equation 2

$$E_{t_2-t_4} = \frac{1}{2}(L_{leak} + L_{res}) \cdot (I_{mag}(t_2) + NI_{out}(t_2))$$

It is much lower than it was in the lead leg, since the magnetizing and output inductance do not contribute [4]. For this reason it is easier to miss the ZVS condition. If the energy stored

is enough, the current will continue to flow into the output capacitances C3 and C4. During the first period the voltage is applied across the leakage and external inductors added in series to the theoretical primary winding of the transformer. The voltage across the theoretical primary winding of the transformer will remain zero, and both output diodes will conduct, until the current flowing through the leakage and external inductors will change direction and reach the reflected output current (t_3-t_4 period).

- Power transfer t_4-t_5

Once the output diode is turned on, the power is transferred from primary to the secondary side of transformer. When the primary current reaches the expected value the circuit is in a condition similar to that reported in the step 1.

2 MOSFET body diode recovery

The cross section of a MOSFET device, illustrated in *Figure 4*, shows an intrinsic diode between body and drain, that is the base-collector junction of the "parasitic" a NPN bipolar transistor source-body-drain. In no or low load conditions this transistor could be turned on and hence brings the MOSFET to the failure, by short circuiting drain and source while high voltages are applied among them. In order to understand this possible failure we must investigate the freewheeling and the ZVS steps. During step 2 the current freewheels into the body-drain diode D2 (see *Figure 4*); since this is directly biased carriers are injected in the N- epi (holes) and P body (electrons) regions of the device. Once Q2 is turned on, a portion of the total current flows through the channel, the parasitic JFET, and the epi region: the MOSFET is conducting in the third quadrant (see *Figure 5*). When the transformer current changes direction the MOSFET Q3 conducts into the first quadrant (see *Figure 6*). The internal body diode D2 now is reverse biased; since it is in parallel with the low resistance channel regions its effective reverse voltage is low. This causes a slow minority carriers extraction, especially from the N- region, since the holes have lower mobility than the electron one. Obviously at low load operation the current flowing through the channel MOSFET is much lower and so is the drop voltage; in this condition the body diode needs more time to complete the reverse recovery, but the powering period is very short and could not be sufficient to remove the minority carriers in the P-N junction.

Figure 4. Current flow into the parallel body diode-channel MOSFET

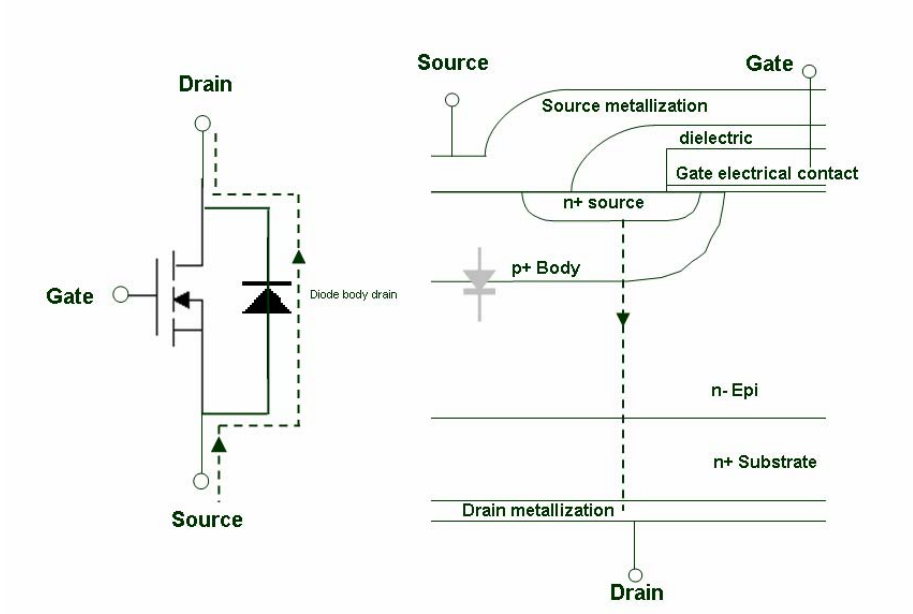
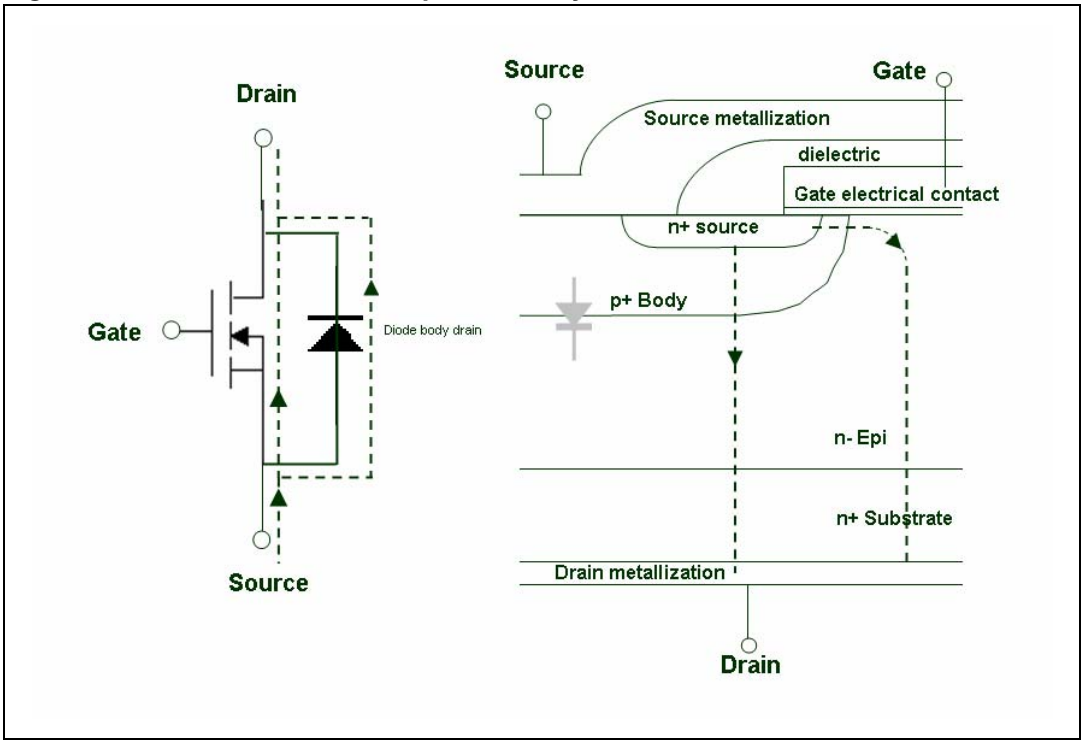
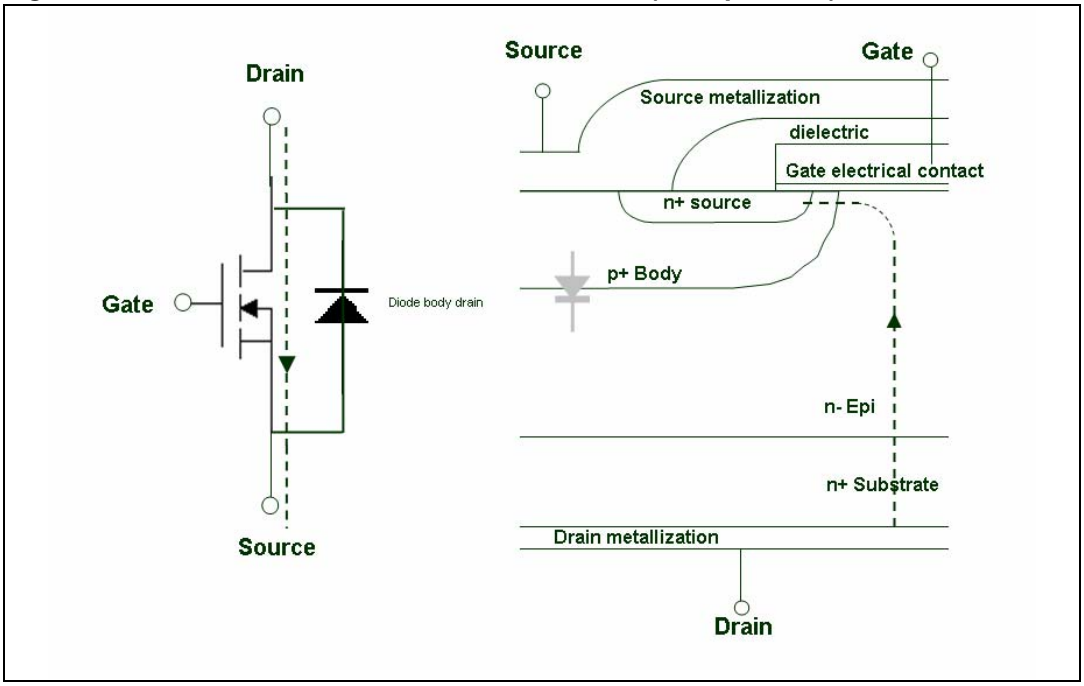


Figure 5. Current flow into the parallel body diode-channel MOSFET



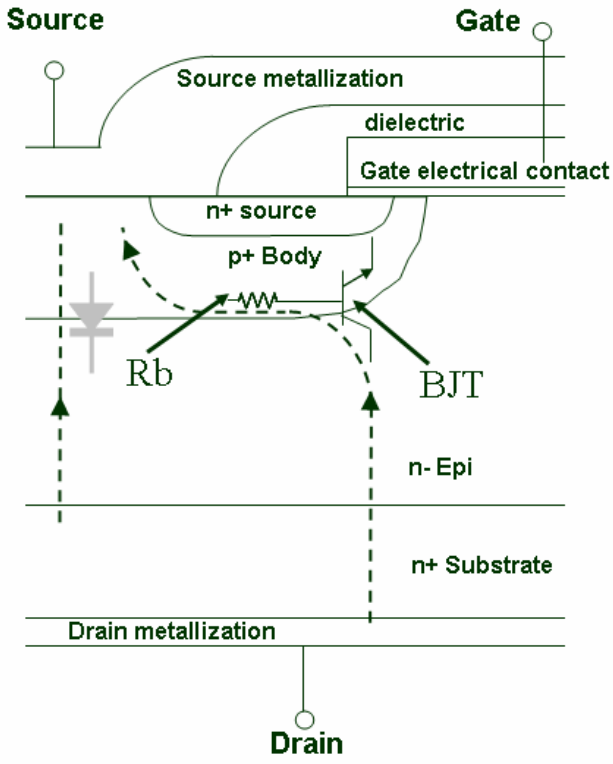
When the Q2 MOSFET is turned off D2 should have yet completely removed its minority carriers, see from both P+ and N- regions, otherwise the high reverse voltage (due to Q1 turning on) results in a fast removal of these carriers. Minority carriers in the N- region are swept towards the P+ body region and this rapid displacement results in a significant current flowing through the P+ body.

Figure 6. Current flow into the channel MOSFET (first quadrant)



In normal condition the source and body regions (that is the emitter and the base of the parasitic bipolar) are shorted via upper source metallization, but by flowing a significant current into the body region below the source region (see *Figure 7*), the intrinsic resistance of this region (shown as Rb) could divert a sufficient current portion able to trigger on the parasitic bipolar; it means creating a short circuit between drain and source pins thus, destroying the device.

Figure 7. Current flow due to the reverse recovery of the body diode



Hence, in order to overcome the previous problems, a MOSFET should have some characteristics:

- The intrinsic body diode with low Trr and low Qrr;
- Ruggedness to the stress due to the trigger on of the parasitic bipolar.

To meet the need related to the body diode a new technology has been developed. The new FD (fast diode) MOSFET has straightforward advantages in terms of Trr, Qrr, Irm and ruggedness in dv/dt.

3 Observations

Choosing to use fast diode technology MOSFETs is a good choice. STMicroelectronics has developed the new Fast diode MD mesh generation that shows excellent performance in these types of topologies. These device families guarantee operation in safe conditions, so far from the triggering on of the parasitic bipolar, so that they are very suitable for the full bridge phase-shift ZVS topologies.

In order to understand these advantages we have compared a standard MOSFET versus a FD MOSFET.

The FD technology device has a lower Qrr than the standard device; meaning that when the diode is reverse biased by the drop voltage on the channel MOSFET, very low in low load condition, it will be faster to complete the recovery and so when it will highly reverse biased by the turn on of the switch in the its same leg it will work in a much more safe condition in term of dv/dt stress (see *Figure 8*).

Figure 8. Comparison between standard and fast diode technology

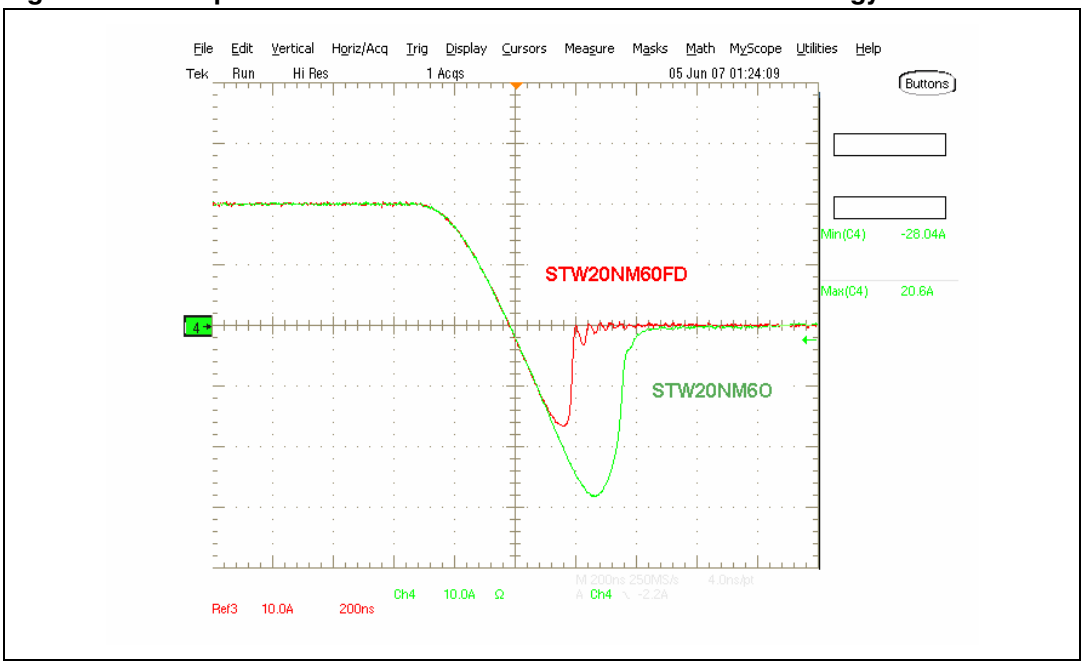


Table 1. Measured dynamic electrical parameters of the devices compared

Device	Irm	Trr	Qrr
	(Di/Dt=100A µs, Isd=20 A, Vdd=100 V, Tj=25°C)		
	(A)	(nS)	(µC)
Standard STW20NM60	25	390	5
Fast diode STW20NM60FD	16	240	1.8

As you can see the ST fast diode technology MOSFET works better, keeping the overall system in a more safe condition.

The fast diode device has worked properly in the application and has shown good performances; report some pictures related to a 1.5 kW DC/DC converter captured on test bench (*Figure 9* and *Figure 10*).

Figure 9. A typical leading leg MOSFET waveforms

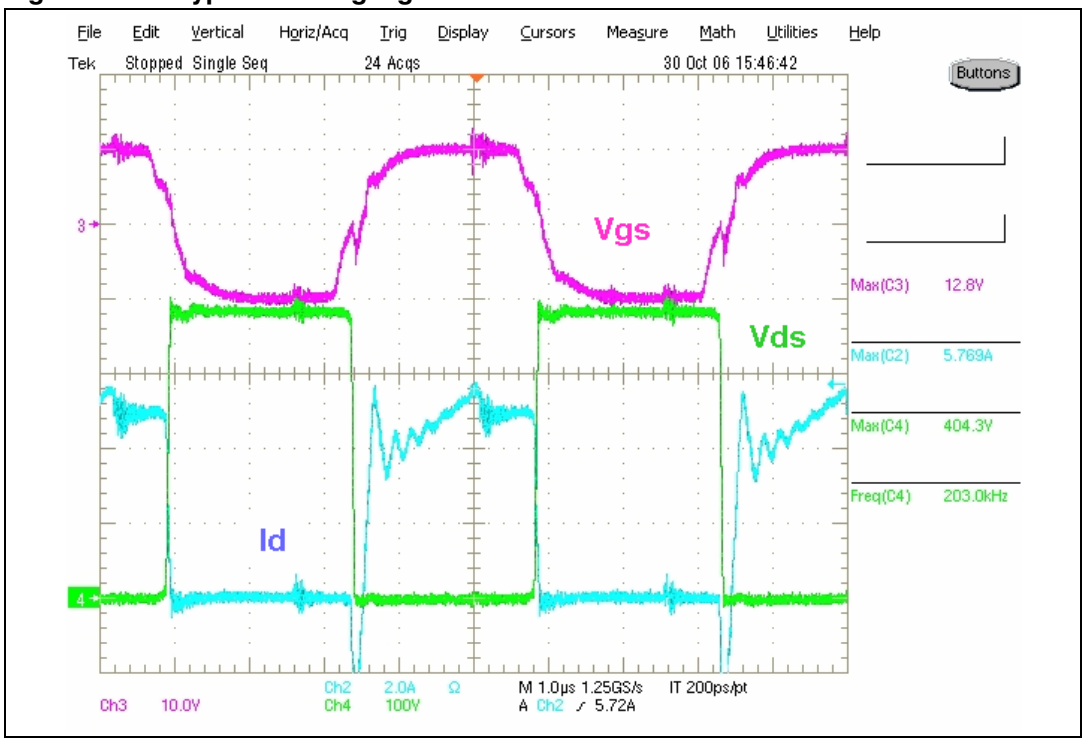
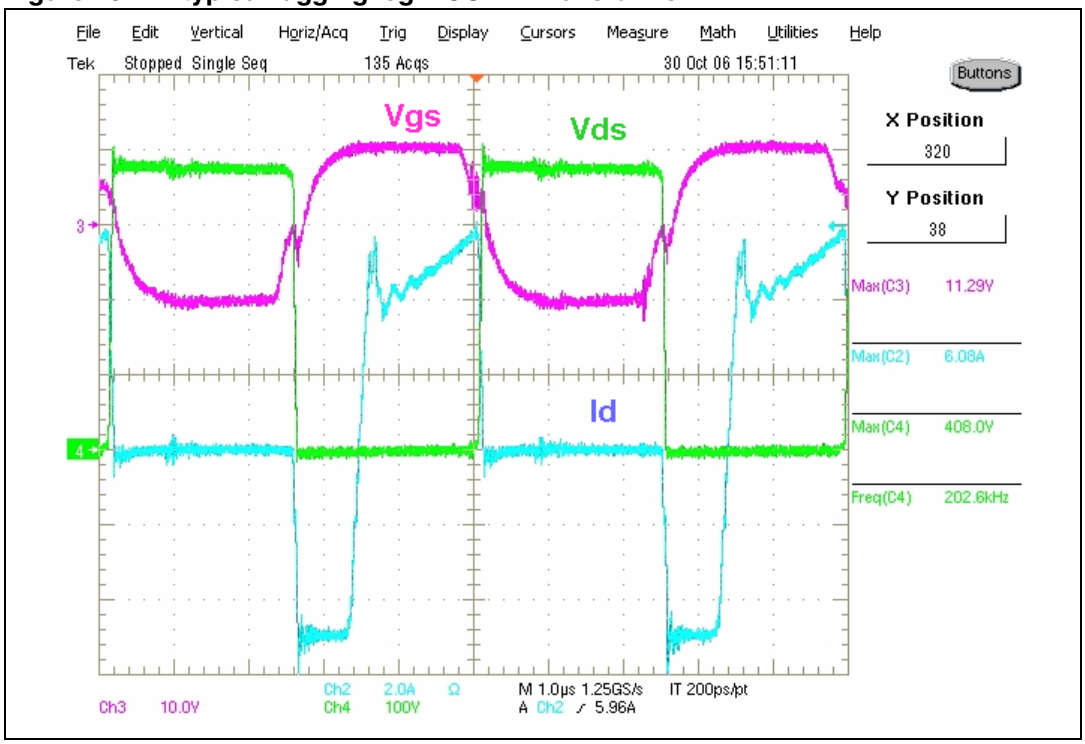


Figure 10. A typical lagging leg MOSFET waveforms



4 References

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2. Alexander Fiel and Thomas Wu International Rectifier Applications Department El Segundo, CA 90245, USA "MOSFET Failure Modes in the Zero-Voltage-Switched Full-Bridge Switching Mode Power Supply Applications"
3. Sampat Shekhawat, Mark Rinehimer and Bob Brockway Discrete Power Group, Fairchild Semiconductor AN-7536 "FCS Fast Body Diode MOSFET for Phase-Shifted ZVS PWM Full Bridge DC/DC Converter"
4. Laszlo Balogh, "Design review:100 W, 400 kHz, DC/DC converter with current doubler synchronous rectification achieves 92% efficiency"

5 Revision history

Table 2. Document revision history

Date	Revision	Changes
21-Sep-2007	1	Initial release

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