AN2989
Application note

LIS331DLM: ±2 *g* /±4 *g* /±8 *g* digital output high performance ultra low-power 3-axis accelerometer

Introduction

This document provides application information for the low-voltage 3-axis digital output linear MEMS accelerometer housed in an LGA package.

The LIS331DLM is a high performance ultra low-power 3-axis linear accelerometer which belongs to the “nano” family of MEMS accelerometers, with digital I^2C/SPI serial interface standard output.

The device features ultra low-power operational modes that allow advanced power saving and smart sleep to wake functions.

The LIS331DLM has dynamically user-selectable full scales of ±2 *g* /±4 *g* /±8 *g* and is capable of measuring acceleration with output data rates from 0.5 Hz to 400 Hz.

The self-test capability allows the user to check the functioning of the sensor in the final application.

The device can be configured to generate interrupt signals in response to inertial wakeup/free-fall events or based on the position of the device itself.

The thresholds and timing of interrupt generators are programmable by the end user “on the fly”. The LIS331DLM is available in a small, thin plastic land grid array (LGA) package and is guaranteed to operate over an wide temperature range of -40 °C to +85 °C.

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1 Register table

Table 1. Register table

Register name	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
WHO_AM_I	0Fh	0	0	0	1	0	0	1	0
CTRL_REG1	20h	PM2	PM1	PM0	DR1	DR0	Zen	Yen	Xen
CTRL_REG2	21h	BOOT	HPM1	HPM0	FDS	HPen2	HPen1	HPCF1	HPCF0
CTRL_REG3	22h	IHL	PP_OD	LIR2	I2_CF1	I2_CF0	LIR1	I1_CF1	I1_CF0
CTRL_REG4	23h	BDU	BLE	FS1	FS0	STsign	0	ST	SIM
CTRL_REG5	24h	-	-	-	-	-	-	TurnOn1	TurnOn0
HP_FILTER_RESET	25h	-	-	-	-	-	-	-	-
REFERENCE	26h	REF7	REF6	REF5	REF4	REF3	REF2	REF1	REF0
STATUS_REG	27h	ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA
OUT_X	29h	XD7	XD6	XD5	XD4	XD3	XD2	XD1	XD0
OUT_Y	2Bh	YD7	YD6	YD5	YD4	YD3	YD2	YD1	YD0
OUT_Z	2Dh	ZD7	ZD6	ZD5	ZD4	ZD3	ZD2	ZD1	ZD0
INT1_CFG	30h	AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
INT1_SRC	31h	-	IA	ZH	ZL	YH	YL	XH	XL
INT1_THS	32h	0	THS6	THS5	THS4	THS3	THS2	THS1	THS0
INT1_DURATION	33h	0	D6	D5	D4	D3	D2	D1	D0
INT2_CFG	34h	AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
INT2_SRC	35h	-	IA	ZH	ZL	YH	YL	XH	XL
INT2_THS	36h	0	THS6	THS5	THS4	THS3	THS2	THS1	THS0
INT2_DURATION	37h	0	D6	D5	D4	D3	D2	D1	D0

2 Startup sequence

Once the device is powered up it automatically downloads the calibration coefficients from the embedded Flash to the internal registers. When the boot procedure is complete (after approximately 5 milliseconds), the device automatically enters power-down mode.

To turn on the device and gather acceleration data, it is necessary to select one of the operating modes through the CTRL_REG1 register, and to enable at least one of the axes. The following general-purpose sequences can be used to configure the device:

1. write CTRL_REG1
2. write CTRL_REG2
3. write CTRL_REG3
4. write CTRL_REG4
5. write Reference
6. write INT1_THS
7. write INT1_DUR
8. write INT2_THS
9. write INT2_DUR
10. read HP_FILTER_RESET (if filter is enabled)
11. write INT1_CFG
12. write INT2_CFG
13. write CTRL_REG5

Register values can be changed at any time, with the device in any operating mode. Modifications take effect immediately.

Note that in case of changes in full scale, ODR or enabling/disabling of self-test, the output of the device requires 3 to 8 samples to settle (see *Table 11*). In cases where the HP filter cut-off frequency is changed, the filter can be reset by reading HP_FILTER_RESET register.

2.1 Reading acceleration data

2.1.1 Using the status register

The device is provided with a STATUS_REG which should be polled to check when a new set of data is available. The reading procedure should be the following:

1. read STATUS_REG
2. if STATUS_REG(3) = 0 then goto 1
3. if STATUS_REG(7) = 1 then some data have been overwritten
4. read OUTX_L
5. read OUTX_H
6. read OUTY_L
7. data processing
7. goto 1

The check performed at step 3 determines whether the reading rate is adequate compared to the data production rate. In cases where one or more acceleration samples have been overwritten by new data due to an excessively slow reading rate, the ZYXOR bit of STATUS_REG is set to 1.

The overrun bits are automatically cleared when all the data present inside the device have been read and new data have not been produced in the meantime.

2.1.2 Using the DataReady signal

The device may be configured to have one HW signal to determine when a new set of measurement data is available for reading. This signal is represented by the XYZDA bit of the STATUS_REG register. The signal can be driven to the INT1 or INT2 pins and its polarity set to active-low or active-high through the CTRL_REG3 register. The interrupt is reset when the higher part of the data of all the enabled channels has been read.

2.2 Output data rate selection and reading timing

The output data rate is user selectable through the DRx bits of the CTRL_REG1 (20h) register. At power-on-reset, the DRx are reset to 0, thus providing a default output data rate of 50 Hz.

The analog signal coming from the mechanical sensor is filtered by a low pass filter before being converted by the internal ADC. The frequency at -3 dB of the low pass filter determines the effective system resolution. The cut-off frequency depends on the DR<1:0> bits in the CTRL_REG1 (20h) register (*Table 2*).

Table 2. Output data rate

DR1, DR0	Output data rate	Analog filter cut-off frequency. (-3 dB)
00	50 Hz	37 Hz
01	100 Hz	74 Hz
10	400 Hz	292 Hz

Note: The precision of the output data rate is related to the internal oscillator; an error of +/- 10% should be taken in account.

A typical reading period is defined which is 616 µs shorter than the output data rate period, in order to prevent the loss of any data produced. During this time period the reading of the data must be performed and the DataReady signal can be used as a trigger to begin the reading sequence. At the end of the complete sequence, the DataReady signal goes down and the rising edge that follows signals that new data are available. If this minimum reading frequency is not observed, some data loss is possible and the DataReady signal no longer signifies a trigger signal. The status register can be used to infer whether an overrun has occurred.

Figure 1. Reading timing

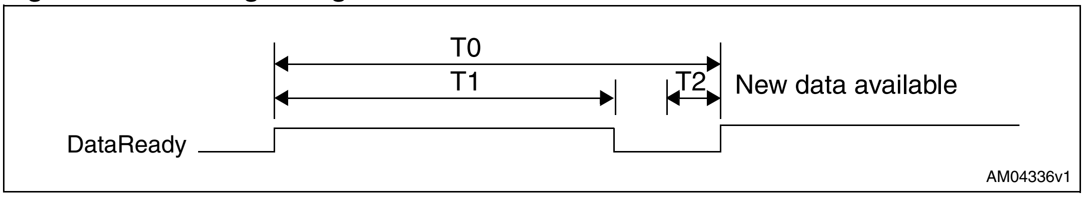


Table 3. Timing value to avoid losing data

Time	Description	Min
T0	Data rate	1/ODR
T1	Reading period	T0-T2
T2	New data generation (typ)	616 µs

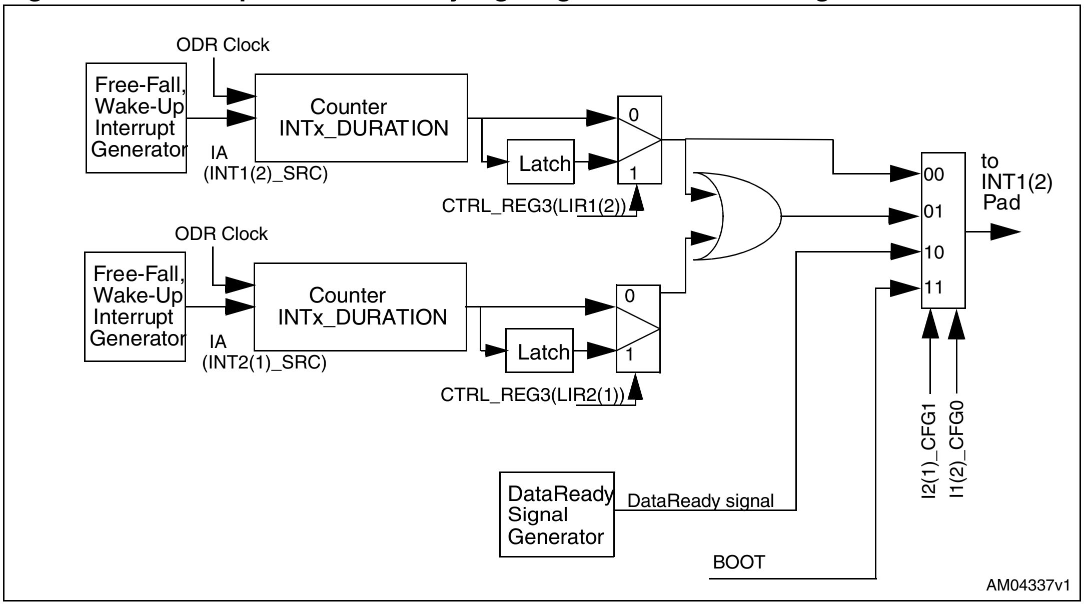
2.3 DataReady vs. interrupt signal

The device is equipped with two pins that can be activated to generate either the DataReady or the interrupt signal. The functionality of the pins is selected acting on bit I1(2)_CFGx bits of the CTRL_REG3 register, according to *Table 4* and with the block diagram given in *Figure 2*.

Table 4. Data signal on INT 1 and INT 2 pads

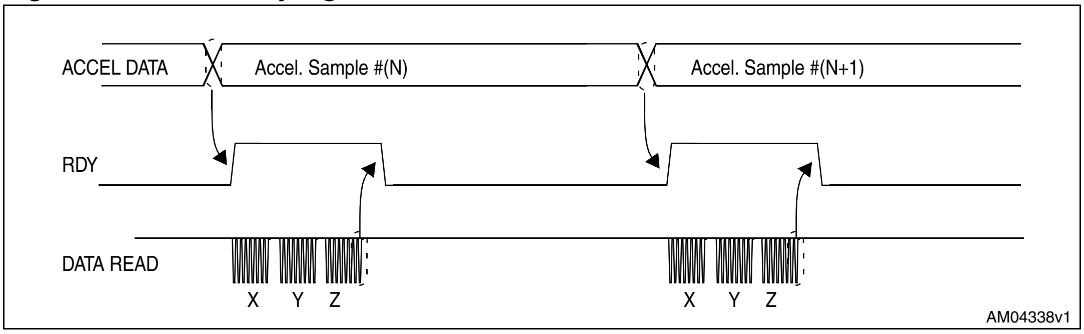
I1(2)_CFG1	I1(2)_CFG0	INT 1(2) pin
0	0	Interrupt 1 (2) source
0	1	Interrupt 1 source OR Interrupt 2 source
1	0	DataReady
1	1	Boot running

Figure 2. Interrupt and DataReady signal generation block diagram



In particular, the DataReady (DR) signal rises to 1 when a new set of acceleration data has been generated and is available for reading. The signal is reset after all the enabled channels are read through the serial interface.

Figure 3. DataReady signal



2.4 Understanding acceleration data

The measured acceleration data are sent into the OUTX, OUTY, OUTZ registers.

Acceleration data for the X (Y, Z) channel is expressed as a 2's complement number.

2.4.1 Data alignment

Acceleration data are represented as 8-bit numbers, two's complement and are right justified.

2.4.2 Example of acceleration data

Table 5 provides a few basic examples of the data that is read in the data registers when the device is subject to a given acceleration. The values listed in the table are given under the hypothesis of perfect device calibration (no offset, no gain error, etc.).

Table 5. Output data register content vs. acceleration (FS = 2 *g*)

Acceleration values	Register address
	29h
0 g	00h
350 mg	15h
1 g	40h
-350 mg	EAh
-1g	C0h

3 Operating modes

The LIS331DLH can operate in the following four modes, which can be selected through the configuration of CTR_REG1 and CTRL_REG5:

- Normal mode
- Power-down
- Low-power
- Sleep to wake

With reference to the datasheet of the device, the power-mode (PM) and data rate (DR) bits of CTRL_REG1 are used to select the basic operating modes (power-down, normal mode and low-power), while the TurnOn bits of CTRL_REG5 are used to enable the advanced mode (sleep to wake) which also involves the interrupt configuration.

Note: The PMx bits are disabled if the Turnonx bits of CTRL_REG5 are not configured as zeros.

Table 6. Power mode and low-power output data rate configurations

PM2	PM1	PM0	Power mode selection	Output data rate [Hz] ODR_{LP}
0	0	0	Power-down	--
0	0	1	Normal mode	ODR
0	1	0	Low-power	0.5
0	1	1	Low-power	1
1	0	0	Low-power	2
1	0	1	Low-power	5
1	1	0	Low-power	10

Table 7. CTRL_REG1 - data rate

DR!	DR0	Data rate generation [Hz] ODR
0	0	50
0	1	100
1	0	400

Table 8. CTRL_REG5 - sleep to wake configuration

TurnOn1	TurnOn0	Sleep to wake status
0	0	Sleep to wake function disabled
0	1	An interrupt event is occurred and system is generating data at ODR
1	0	Not allowed
1	1	Sleep to wake function enabled

Table 9 and *Table 10* show the typical power consumption values for the different operating modes.

Note: Higher data rates correspond to lower device resolution.

Table 9. Power consumption - normal mode (µA)

ODR	50 Hz	100 Hz	400 Hz
Power consumption	250	255	290

Table 10. Power consumption (µA)

$ODR\backslash ODR_{LP}$	0.5 Hz	1 Hz	2 Hz	5 Hz	10 Hz
50 Hz	10	20	30	60	99
100 Hz	10	15	20	40	80
400 Hz	10	15	20	40	80

3.1 Normal mode

In Normal mode data are generated at the data rate (ODR) selected through the DR bits and for the axis enabled through the Zen, Yen and Xen bits of CTRL_REG1. Data generated for a disabled axis is 00h.

Data interrupt generation is active and configured through INT1_CFG and INT2_CFG registers.

3.2 Power-down mode

When the device is in power-down mode, almost all internal blocks of the device are switched off to minimize power consumption. Digital interfaces (I^2C and SPI) are still active to allow communication with the device. Configuration register content is preserved and output data registers are not updated, thus keeping in memory the last data sampled before going to power-down mode.

Typical turn-on time to go back to Normal mode is 1 ms + 1/ODR.

Table 11. Turn-on time

Data rate generation (Hz)	Turn-on time - typical (ms)
50	21
100	11
400	3.5

3.3 Low-power mode

When the device is in low-power mode data are produced at the ODR_{LP} selected by the PM bits of CTRL_REG1.

Turn-on time follows the same rules as for power-down mode (Table 11).

3.4 Sleep to wake

The sleep to wake function, in conjunction with low-power mode, allows further reduction of system power consumption and development of new smart applications.

The LIS331DLM may be set to a low-power operating mode, characterized by lower date rate refreshments. In this way the device, even if sleeping, continues sensing acceleration and generating interrupt requests.

When the sleep to wake function is activated, the LIS331DLM is able to automatically wake up as soon as the interrupt event has been detected, increasing the output data rate and bandwidth. With this feature the system may be efficiently switched from low-power mode to full-performance depending on user-selectable positioning and acceleration events, thus ensuring power saving and flexibility.

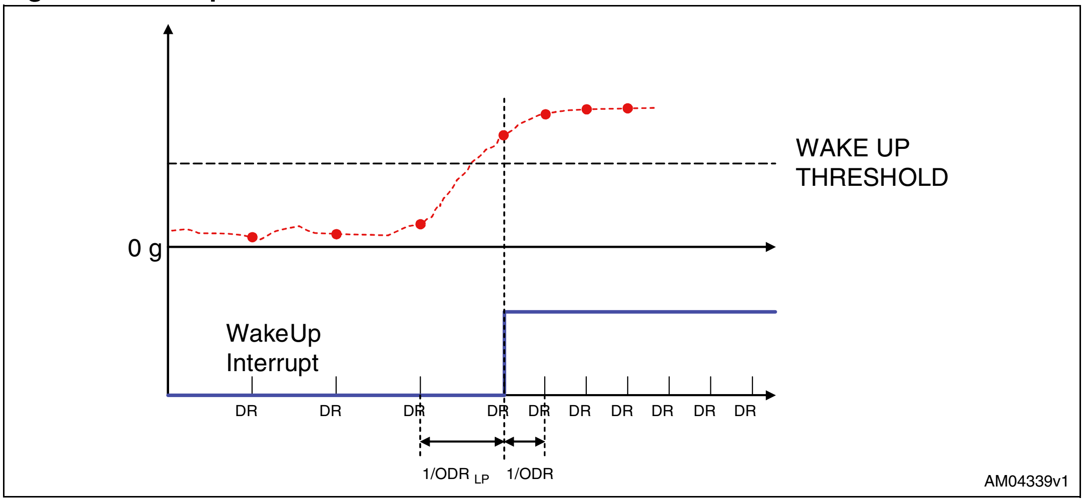
The sleep to wake function is activated through the TurnOnx bits of CTRL_REG5 (Table 8).

When the device is in sleep to wake mode, it automatically samples the acceleration data at ODR_{LP} to verify if interrupt conditions are reached. When an interrupt event occurs, the device goes back to generating data at ODR (Figure 4). If interrupt conditions are not reached, the device remains in low-power mode at ODR_{LP}.

The device is ready to immediately generate valid samples as soon as it exits from sleep to wake mode.

Note: At an interrupt event, the contents of CTR_REG5 changes to 0x01 while the content of CTRL_REG1 is left untouched: PMx bits are ignored. To return to normal mode or low-power-mode, the TurnOnx bits of CTRL_REG5 must be set to zero.

Figure 4. Sleep to wake mode



3.4.1 Entering sleep to wake mode

The sequence to set up the sleep to wake function is:

1. configure the desired interrupt event (free-fall, wakeup, 6D position or 6D movements)
2. select the desired low-power mode (ODR_{LP}) and data rate (ODR) in CTRL_REG1
3. enable sleep to wake through CTRL_REG5 (TurnOn1 = TurnOn0 = 1)

Once an interrupt event occurs, the TurnOn bits change to TurnOn1 = 0 and TurnOn0 = 1 and the system generates data at ODR. The user can re-activate the sleep to wake function by executing step 3 again.

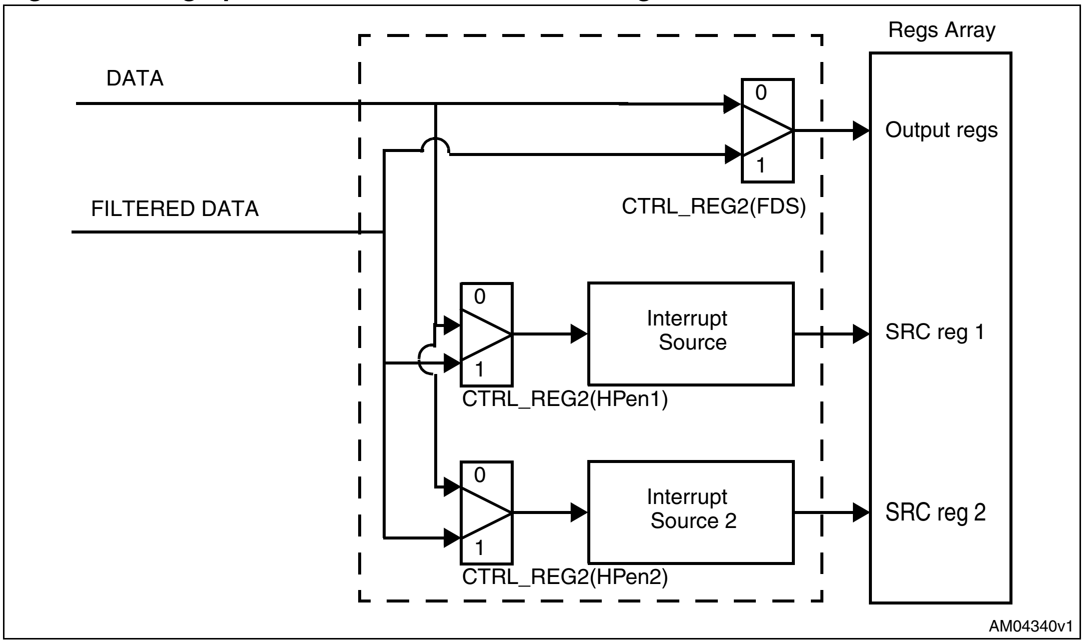
3.4.2 Exiting sleep to wake mode

To return to normal mode or to low-power mode, the user must disable the sleep to wake function by setting TurnOn1 = TurnOn0 = 0.

4 High-pass filter

The LIS331DLM provides embedded high-pass filtering capability to easily delete the DC component of the measured acceleration. As shown in *Figure 5*, it is possible to independently apply the filter on the output data and/or on the interrupts data through the FDS, HPen1 and HPen2 bits of the CTRL_REG2 register configuration. This means that it is possible, for example, to obtain filtered data while interrupt generation works on unfiltered data.

Figure 5. High-pass filter connections block diagram



4.1 Filter configuration

As shown in *Table 12*, two operating modes are possible for the high-pass filter:

:

Table 12. High-pass filter mode configuration

HPM1	HPM0	
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference mode
1	0	Same as configuration 00h
1	1	Not allowed

The bandwidth of the high-pass filter depends on the selected ODR and on the settings of HPCFx bits of CTRL_REG2. The high-pass filter cut-off frequencies (f_t) are shown in *Table 13*.

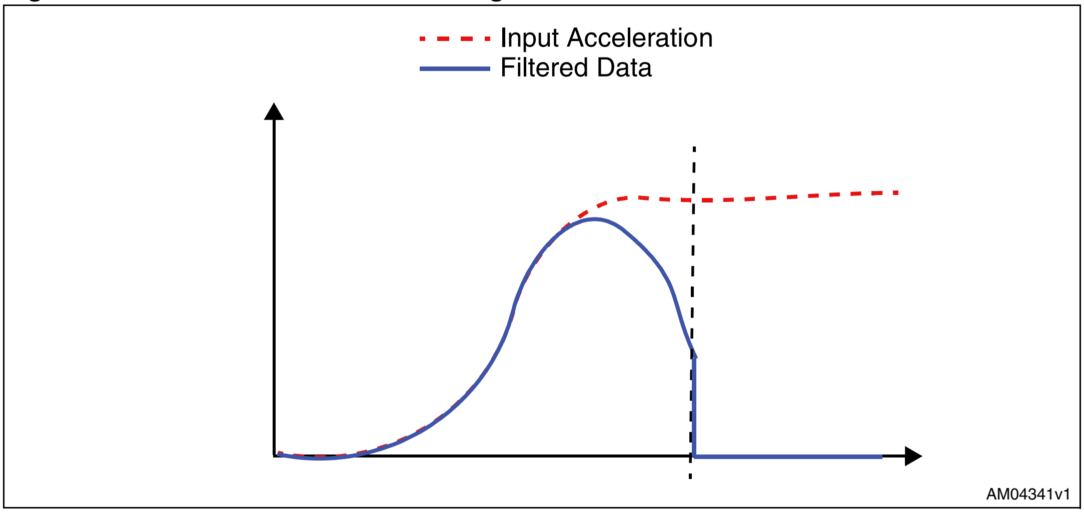
Table 13. High-pass filter cut-off frequency configuration

HPcoeff2,1	f_t [Hz] Data rate = 50 Hz	f_t [Hz] Data rate = 100 Hz	f_t [Hz] Data rate = 400 Hz
00	1	2	8
01	0.5	1	4
10	0.25	0.5	2
11	0.125	0.25	1

4.1.1 Normal mode

In this configuration the high-pass filter can be reset reading the HP_FILTER_RESET register, instantly matching the output data to the input acceleration.

Figure 6. HP_FILTER_RESET readings



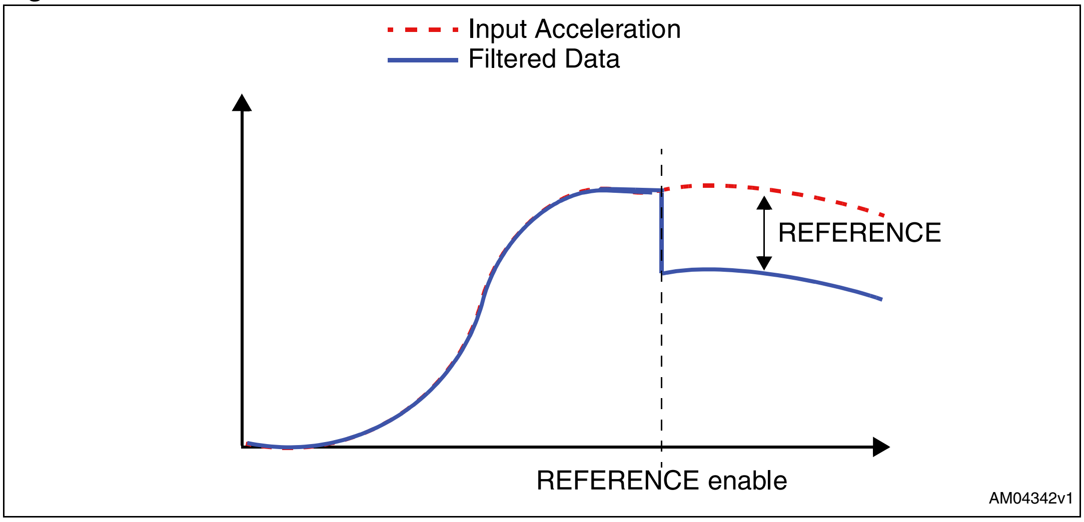
4.1.2 Reference mode

In Reference mode configuration the output data is calculated as the difference between the input acceleration and the content of the REFERENCE register. This register is in 2's complement representation and the value of 1LSB of these 7-bit registers depends on the selected full scale (*Table 14*).

Table 14. Reference mode LSB value

Full scale	Reference mode LSB value (mg)
2	~16
4	~31
8	~63

Figure 7. Reference mode



5 Interrupt generation

The LIS331DLM can provide two interrupt signals and offers several possibilities to personalize these signals. The registers involved in the interrupt generation behavior are CTRL_REG3, INT1_CFG, INT2_CFG, INT1_THS, INT2_THS, INT1_DURATION, INT2_DURATION.

The LIS331DLM interrupt signal can behave as free-fall, wakeup or 6D orientation detection.

Table 15. Interrupt mode configuration

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6 direction movement recognition
1	0	AND combination of interrupt events
1	1	6 direction position recognition

Whenever an interrupt condition is verified, the interrupt signal is generated and by reading the INT1_SRC and INT2_SRC registers it is possible to detect which condition has occurred.

5.1 Duration

The content of the duration registers set the minimum duration of the Interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

When in Normal mode, duration time is measured in N/ODR, where N is the content of the duration register and ODR is 50, 100, 400 Hz.

Table 16. Duration of LSB value in normal mode

ODR (Hz)	Duration of LSB value (ms)
50	20
100	10
400	2.5

When in low-power mode, duration time is measured in N/ODR_{LP}, where N is the content of the duration register and ODR_{LP} is 0.5, 1, 2, 5, 10 Hz.

Table 17. Duration of LSB value in low-power mode

ODR (Hz)	Duration of LSB value (s)
0.5	2
1	1
2	0.5

Table 17. Duration of LSB value in low-power mode (continued)

ODR (Hz)	Duration of LSB value (s)
5	0.2
10	0.1

5.2 Threshold

Threshold registers define the reference accelerations used by the interrupt generation circuitry. The value of 1LSB of these 7-bit registers depends on the selected full scale (*Table 18*).

Table 18. Threshold LSB value

Full scale	Threshold LSB value (m*g*)
2	~16
4	~31
8	~63

5.3 Free-fall and wakeup interrupts

The LIS331DLM interrupt signals can behave as free-fall, wakeup or 6D orientation detection. When an interrupt condition is verified, the interrupt signal is generated and by reading the INT1_SRC and INT2_SRC registers it is possible to determine which condition has occurred.

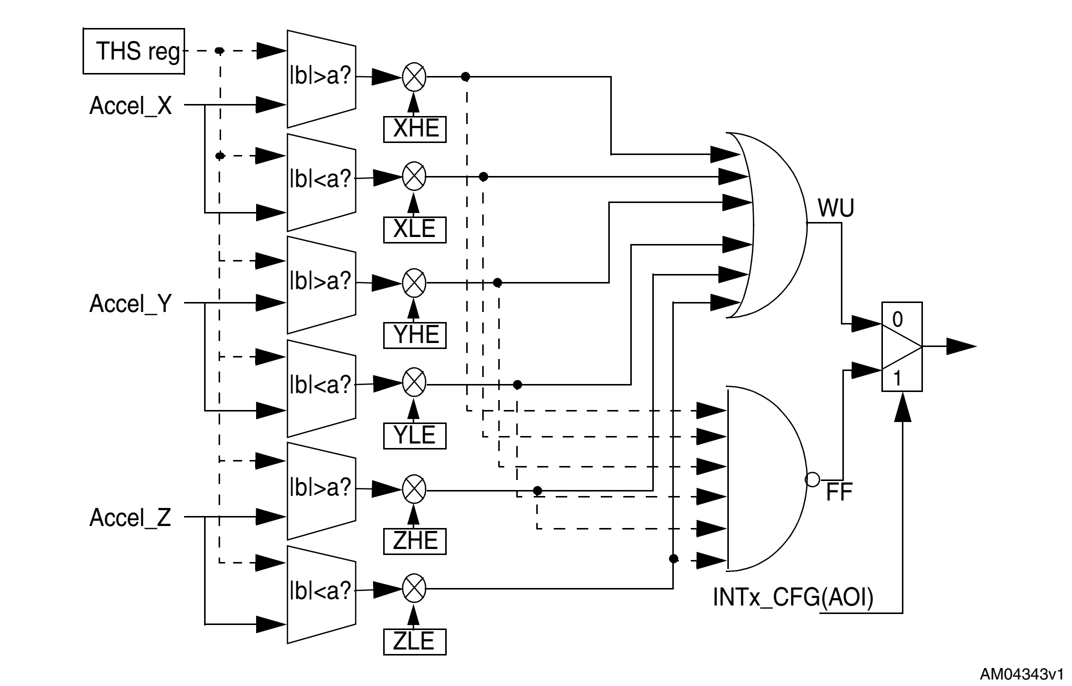
The Free-Fall signal (FF) and wakeup signal (WU) interrupt generation block is represented in *Figure 8*.

FF or WU interrupt generation is selected through the AOI bit in INTx_CFG register. If the AOI bit is ‘0’, signals coming from comparators are put in logical “OR”. Depending on the values written in the INT1_CFG register, every time the value of at least one of the enabled axes exceeds the threshold written in module in INTx_THS registers, a WU interrupt is generated. Otherwise, if the AOI bit is ‘1’, signals coming from the comparators go into a “NAND” port. In this case, an interrupt signal is generated only if all the enabled axes exceed the threshold written in the INTx_THS register.

The LIRx bits of the CTRL_REG3 can be used to determine whether or not the interrupt request must be latched. If the LIRx bit is ‘0’ (default value), the interrupt signal goes high when the interrupt condition is satisfied and immediately returns low if the interrupt condition is no longer verified. Otherwise, if the LIRx bit is ‘1’, when an interrupt condition is applied, the interrupt signal remains high even if the condition returns to a non-interrupt status, until a reading of the INTx_SRC register is performed.

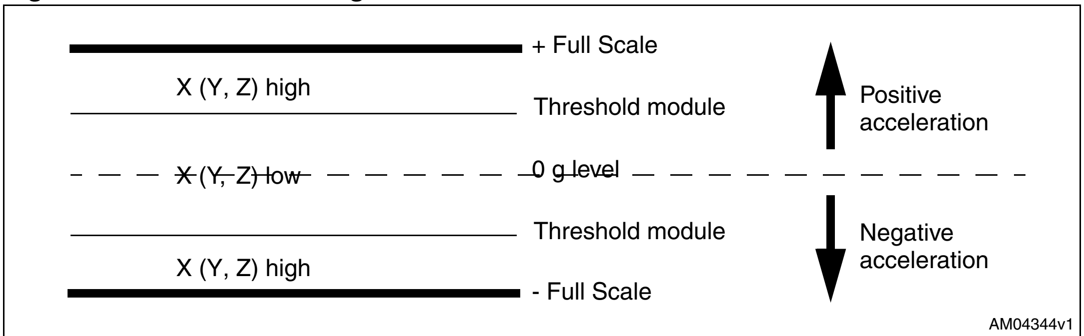
The ZHIE, ZLIE, YHIE, YLIE, XHIE and HLIE bits of the INTx_CFG register select on which axis the interrupt decision must be performed, and in which direction the threshold must be exceeded to generate the interrupt request.

Figure 8. Free-fall, wakeup interrupt generator



The threshold module which is used by the system to detect free-fall or inertial wakeup events is defined by the INTx_THS registers. The threshold value is expressed over 7 bits as an unsigned number and is symmetrical around the zero-g level. XH (YH, ZH) is true when the unsigned acceleration value of the X (Y, Z) channel is higher than INTx_THS. Similarly, XL, (YL, ZL) low is true when the unsigned acceleration value of the X (Y, Z) channel is lower than INTx_THS. Refer to *Figure 9* for additional details.

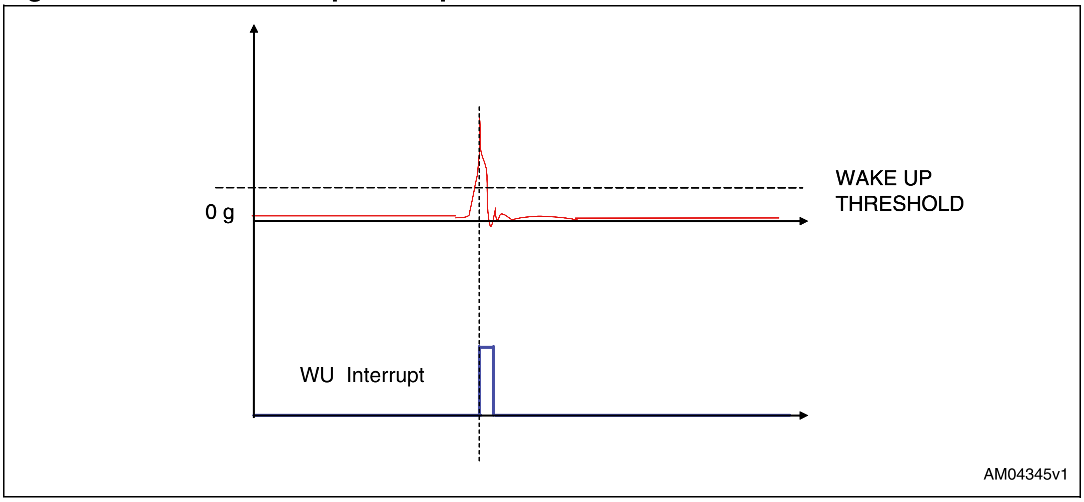
Figure 9. FF_WU_CFG high and low



5.4 Inertial wakeup

The wakeup interrupt refers to a specific configuration of the INTx_CTRL registers that allow the interrupt generation when the acceleration on the configured axis exceeds a defined threshold (*Figure 10*).

Figure 10. Inertial wakeup interrupt



5.4.1 HP filter bypassed

This paragraph provides a basic algorithm which shows the practical use of the inertial wakeup feature. In particular, with the code below, the device is configured to recognize when the absolute acceleration along either X or Y axis exceeds a preset threshold (250 m*g* used in the example). The event which triggers the interrupt is latched inside the device and its occurrence is signaled through the use of the INT1 pin.

1	write 2Fh into CTRL_REG1	// Turn-on the sensor and enable X, Y and Z // ODR = 100 Hz
2	write 00h into CTRL_REG2	// High-pass filter disabled
3	write 00h into CTRL_REG3	// Latched interrupt active high on INT1 pad
4	write 00h into CTRL_REG4	// FS = 2g
5	write 00h into CTRL_REG5	// Sleep to wake disabled
6	write10h into INT1_THS	// Threshold = 250 mg
7	write 00h into INT1_DURATION	// Duration = 0
8	write 0Ah into INT1_CFG	// Enable XH and YH interrupt generation
9	poll INT1 pad; if INT1=0 then goto 8	// Poll RDY/INT pin waiting for the // wakeup event
10	read INT1_SRC	// Return the event that has triggered the // interrupt
11	(Wakeup event has occurred; insert your code here)	// Event handling
12	goto 8	

5.4.2 Using the HP filter

The code which follows provides a basic routine showing the practical use of the inertial wakeup feature performed on high-pass filtered data. In particular, the device is configured to recognize when the high-frequency component of the acceleration applied along either the X, Y or Z axis exceeds a preset threshold (250 m*g* is used in the example). The event which triggers the interrupt is latched inside the device and its occurrence is signalled through the INT1 pin.

1	write 2Fh into CTRL_REG1	// Turn on the sensor, enable X, Y and Z // ODR = 100 Hz
2	write 15h into CTRL_REG2	// High-pass filter enabled on data and interrupt1
3	write 00h into CTRL_REG3	// Latched interrupt active high on INT1 pad
4	write 00h into CTRL_REG4	// FS = 2 *g*
5	write 00h into CTRL_REG5	// Sleep to wake disabled
6	write10h into INT1_THS	// Threshold = 250 mg
7	write 00h into INT1_DURATION	// Duration = 0

8	read HP_FILTER_RESET	// Dummy read to force the HP filter to
		// actual acceleration value
		// (i.e. set reference acceleration/tilt value)

9	write 2Ah into INT1_CFG	// Configure desired wakeup event
10	poll INT1 pad; if INT1 = 0 then goto 9	// Poll INT1 pin waiting for the // wakeup event
11	(Wakeup event has occurred; insert your code here)	// Event handling
12	read INT1_SRC	// Return the event that has triggered the // interrupt and clear interrupt
13	(Insert your code here)	// Event handling
14	goto 9	

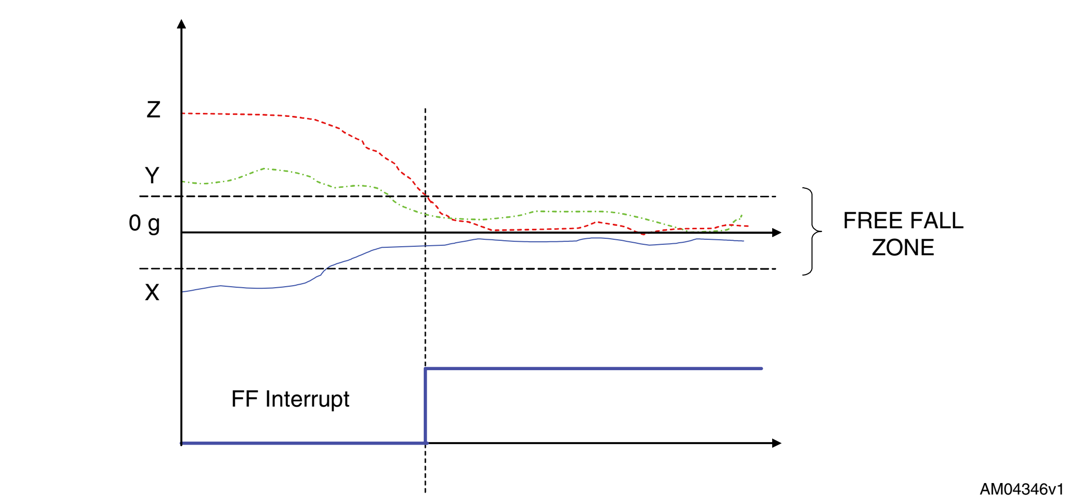
At step 8, a dummy read at the HP_FILTER_RESET register is performed to set the current/reference acceleration/tilt state against which the device performed the threshold comparison.

This read may be performed any time it is required to set the orientation/tilt of the device as a reference state without waiting for the filter to settle.

5.5 Free-fall detection

Free-fall detection refers to a specific configuration of the INTx_CTRL registers that allows the recognition of device free-fall: the acceleration measurements along all the axes go to zero. In real cases, a “free-fall zone” is defined around the zero-g level, where all accelerations are small enough to generate the interrupt (*Figure 11*).

Figure 11. Free-fall interrupt



This paragraph provides the fundamentals for using the free-fall detection feature. In particular, the software routine which configures the device to detect and signal free-fall events is as follows:

1	write 2Fh into CTRL_REG1	// Turn-on the sensor, enable X, Y and Z // ODR = 100 Hz
2	write 00h into CTRL_REG2	// High-pass filter disabled
3	write 04h into CTRL_REG3	// Latched interrupt on INT1
4	write 16h into INT1_THS	// Set free-fall threshold = 350 mg
5	write 03h into INT1_DURATION	// Set minimum event duration
6	write 95h into INT1_CFG	// Configure free-fall recognition
7	poll INT1 pad; if INT1 = 0 then goto 8	// Poll INT1 pin waiting for the free-fall event
8	(Free-fall event has occurred; insert your code here)	// Event handling
9	read INT1_SRC register	// Clear interrupt request
10	goto 7	

The code sample exploits a threshold set at 350 m*g* for free-fall recognition and the event is notified by the hardware signal INT1. At step 5, the INT1_DURATION register is configured to ignore events that are shorter than 3/DR = 3/100 ~= 30 ms in order to avoid false detections.

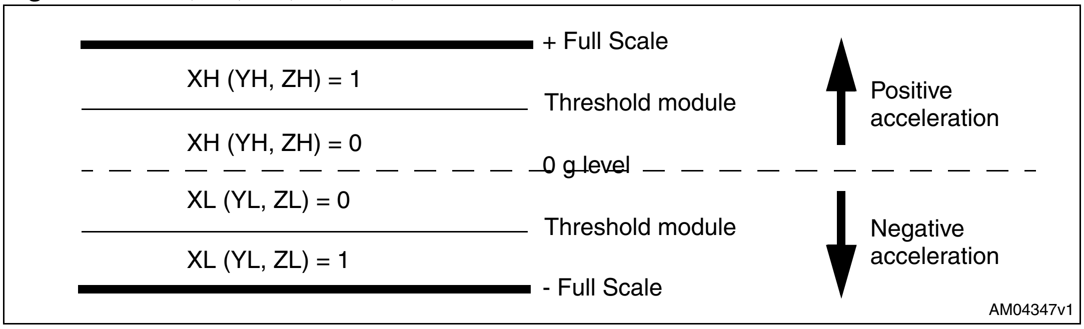
Once the free-fall event has occurred, a read at the INT1_SRC register clears the request and the device is ready to recognize other events.

5.6 6D direction

The LIS331DLM features an advanced capability to detect the orientation of the device in space. The 6D direction function can be enabled through the AOI and 6D bits of the INT1_CFG register (*Table 3*). When configured for the 6D function, the ZH, ZL, YH, YL, XH, XL bits of INTx_SRC send information about the value of the acceleration generating the interrupt when it exceeds the threshold, and whether the acceleration value is positive or negative. More specifically:

- ZH (YH, XH) is 1 when the sensed acceleration is greater than the threshold in the positive direction.
- ZL (YL, XL) is 1 when the sensed acceleration is greater than the threshold in the negative direction.

Figure 12. ZH, ZL, YH, YL, XH, XL behavior



There are two possible configurations for the 6D direction function:

- **6D movement recognition**: In this configuration the interrupt is generated when the device moves from one direction (known or unknown) to a different, known direction. The interrupt is active only for 1/ODR.
- **6D position recognition**: In this configuration the interrupt is generated when the device is stable in a known direction. The interrupt is active as long as the position is maintained, as shown in *Figure 13*, (a) and (b).

In *Figure 13*, the 6D Movement line shows the behavior of the interrupt when the device is configured for 6D Movement recognition on the X and Y axes (INT1_CFG = 0x4Ah), while the 6D Position line shows the behavior of the interrupt when the device is configured for 6D Position recognition on the X and Y axes (INT1_CFG = 0xCAh). INT1_THS is set to 0x21.

With reference to *Figure 14*, the device has been configured for the 6D Position function on the X, Y and Z axes. *Table 19* shows the content of the INT1_SRC register for each position.

Figure 13. 6D movement vs. 6D position

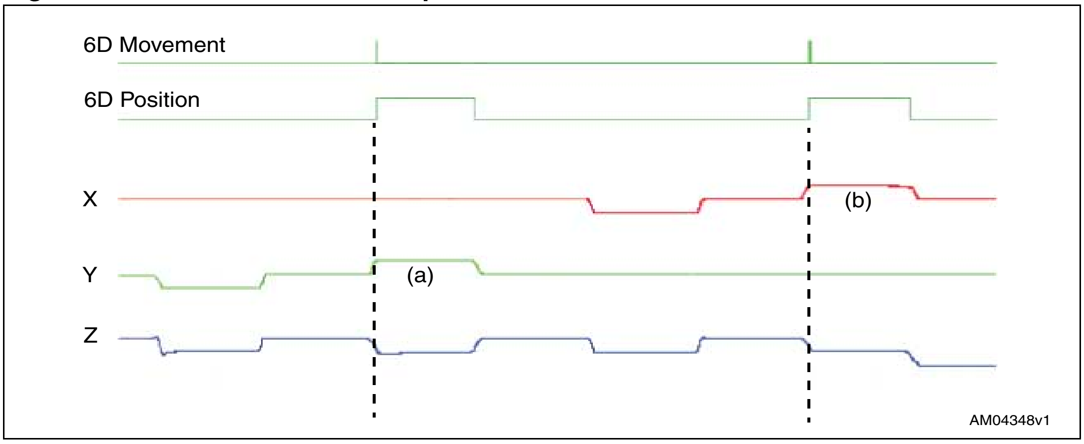


Figure 14. 6D recognized positions

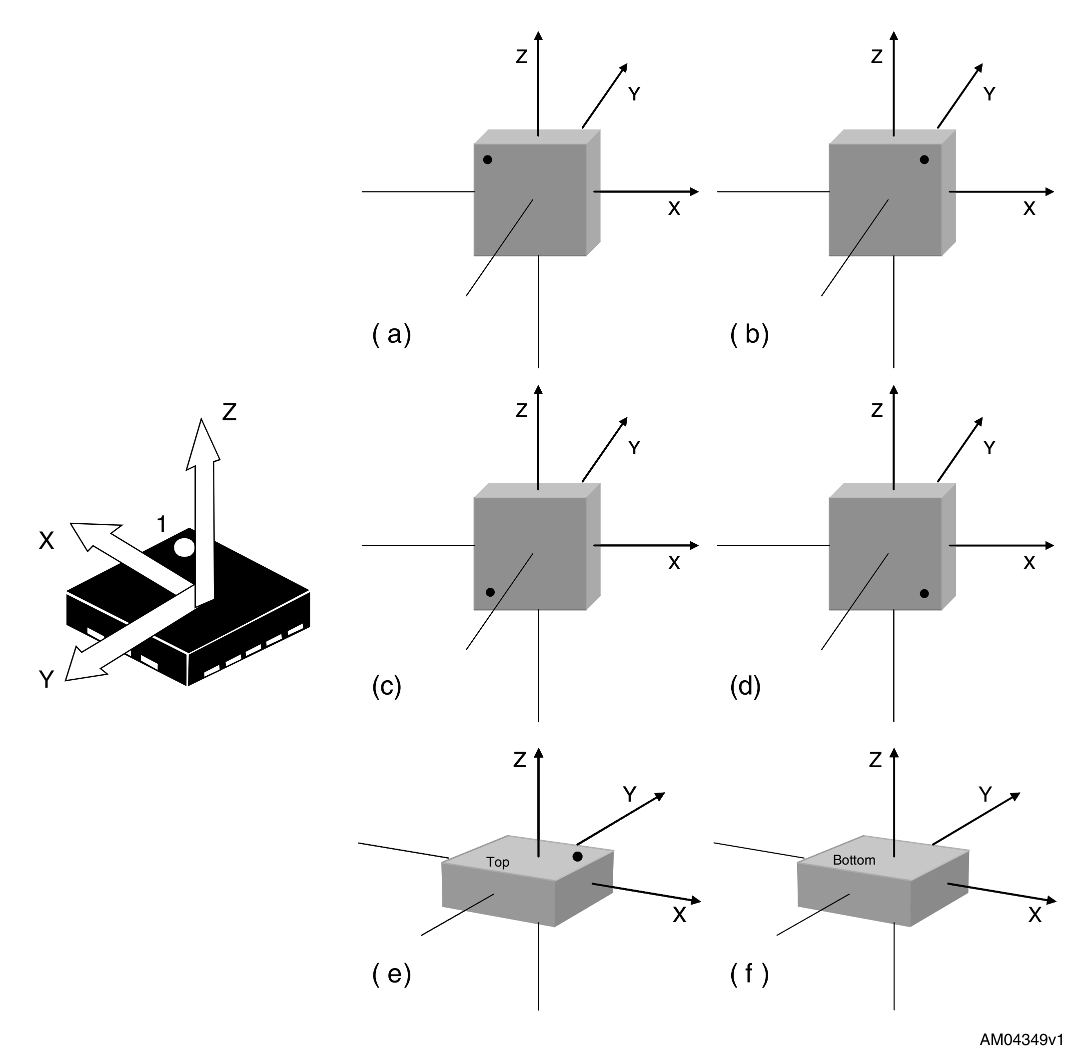


Table 19. INTx_SRC register in 6D position

Case	IA	ZH	ZL	YH	YL	XH	XL
(a)	1	0	0	0	1	0	0
(b)	1	0	0	0	0	1	0
(c)	1	0	0	0	0	0	1
(d)	1	0	0	1	0	0	0
(e)	1	1	0	0	0	0	0
(f)	1	0	1	0	0	0	0

6 Revision history

Table 20. Document revision history

Date	Revision	Changes
24-Jun-2009	1	Initial release.