AN3212
Application note

5 W to 7 W high power factor offline LED driver based on VIPer devices

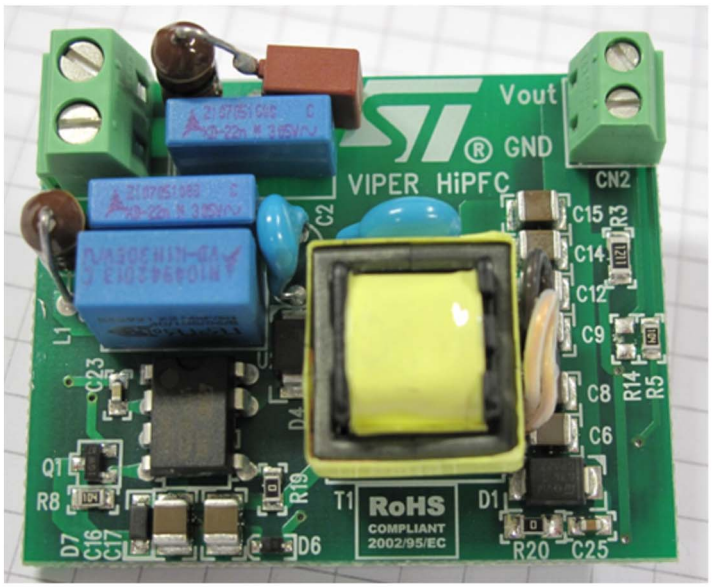
Introduction

The driving idea behind this application note is to exploit the possibility of implementing an LED power supply module characterized by a high power factor, based on devices from the VIPer family in flyback configuration and with a TSM1052 as a constant current controller.

The other key point is to avoid using high voltage electrolytic capacitors, evaluate the influence of the output bulk electrolytic capacitor on overall performance, and consider its replacement with much smaller ceramic components, eventually implementing a non electrolytic configuration.

The STEVAL-ISA120V1 demonstration board has been designed as a platform to perform this evaluation.

Figure 1. STEVAL-ISA120V1 VIPer27 LED driver module



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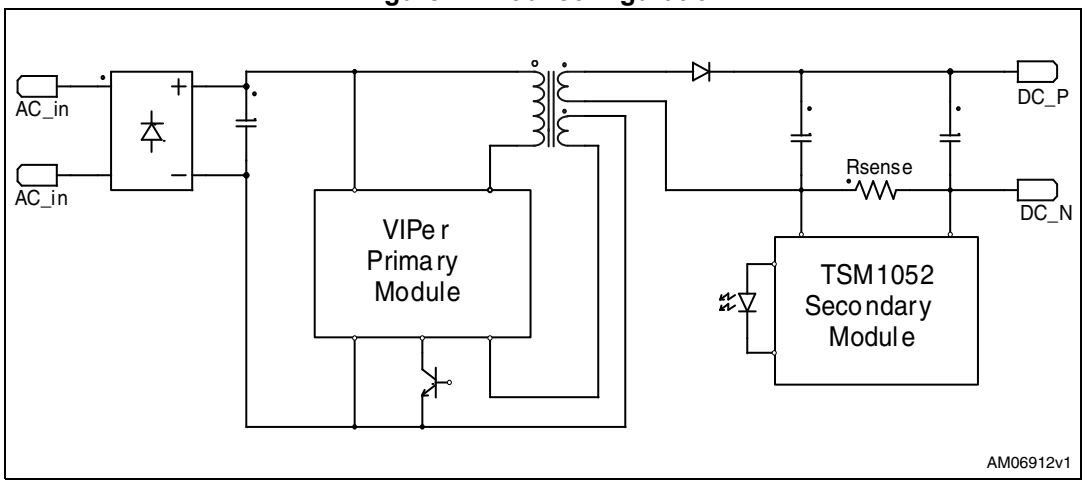
1 Main characteristics

1.1 Initial configuration

Several demonstration boards already exist which accept the mains input voltage, wide or local voltage range, and generate a regulated output current to drive an LED “string” with an output power in the range of 3 W to 7 W, but none are expressly intended to achieve a high power factor and/or avoid the use of electrolytic capacitors.

For this reason a “standard” flyback configuration was developed, based on a VIPer device and with a TSM1052 as the constant current controller, then, some changes were introduced in order to address the key points indicated above.

Figure 2. Initial configuration



1.2 Requirements

The design was started taking the following key points into account:

- Input voltage: 100 to 264 V_{AC}
- Power factor: > 0.9 @ 115 V and 230 V
- Output power: 3.5 W to 7 W (3 x 1 W / 3x 2.5 W LED series)
- Output current (average): 0.35 A to 0.7 A
- Input/output isolation
- No high voltage electrolytic capacitors
- Possibility of no low voltage electrolytic capacitors
- Open/short-circuit protection
- Minimal part count
- No dimming required

2 Circuit description

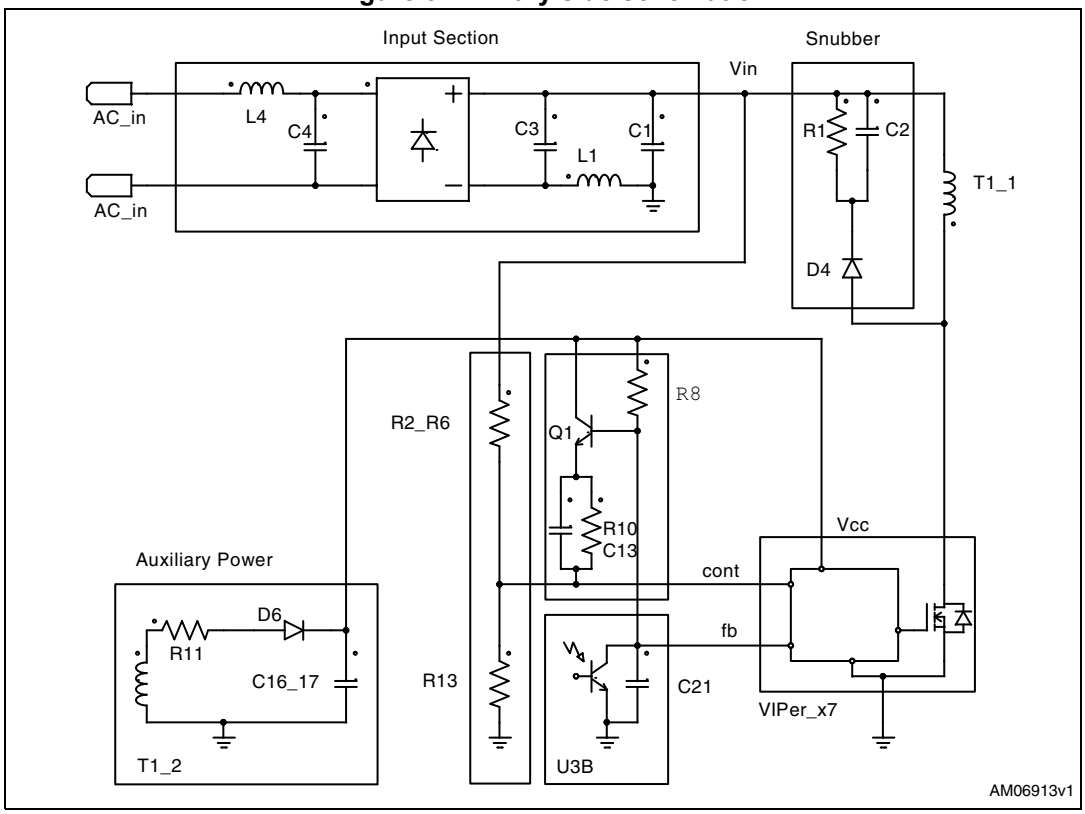
2.1 Primary side

In order to keep the part count to a minimum, the primary side of the converter is based on a device from the VIPer family, a VIPer17 for the 3.5 W and a VIPer27 for the 7 W version.

As can be seen in *Figure 3*, the circuit is similar to a standard flyback, with:

- Input section with X2 capacitor, diode bridge, EMI filter
- RCD snubber in parallel to the primary winding of the transformer
- Auxiliary power supply
- Optocoupler insulated feedback loop
- VIPer converter

Figure 3. Primary side schematic



The more “unusual” points are:

- The relatively small values of the EMI filter capacitors
- The circuitry related to the VIPer “cont” pin

The first is dictated from the high power factor requirement; usually these capacitors have a much higher value in order to get a low output ripple and reduced EMI emissions, but this inevitably leads to a poor power factor. For this reason their value must be set as a compromise starting with usual values and reducing them until the required PF can be reached.

Care should be taken in designing the EMI filter due to the constraints indicated above. In *Section 4: Measurements* two versions are presented, with their different responses.

The main drawback to this configuration is that it lacks a bulk capacitor which stores energy on the primary side, and then the output current is affected by a high ripple, unless a large electrolytic capacitor is used on the secondary side.

The second point is the true way to get a good power factor.

Referring to the VIPer17/27; *Off-line high voltage converters* datasheets, the cont pin is the control that allows reducing the MOS peak current setting from the internally fixed point to about 1/10 of that value. This can be accomplished by means of a resistor Rlim connected between this pin and ground. *Figure 4* and *5* represent the current ratio iDlim/(iDlim @ 100k) as a function of Rlim. As can be seen, changing Rlim from 100 Kohm to a few kohms progressively limits the corresponding MOSFET peak current.

Figure 4. ID_{LIM} vs R_{LIM} - VIPer17

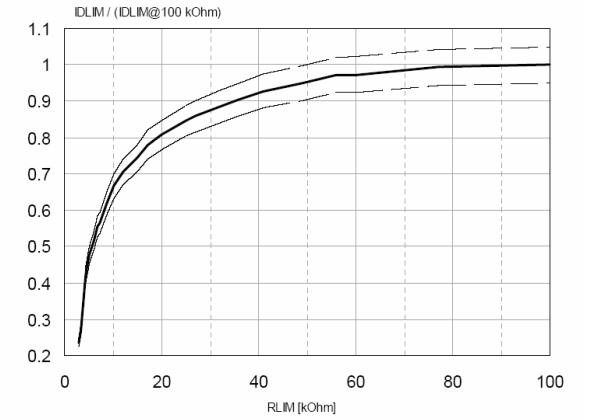
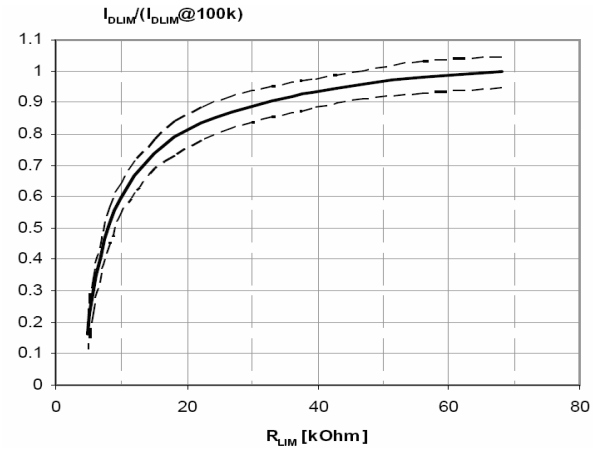


Figure 5. ID_{LIM} vs R_{LIM} - VIPer27



An equivalent function can be implemented connecting the cont pin to a variable voltage through a fixed resistor; in this way the peak current can be modulated simply varying the control voltage: reducing the voltage, lowers the current.

Then, if the rectified mains voltage is scaled and applied to the cont input, the resulting MOSFET peak current, and also the corresponding average input current, are shaped just like Vin, obtaining the required high power factor.

The resistor array made up of R2, R6 and R13 implements this function, where R13 is the lower practical value that fixes the minimum peak current, and R2 + R6 come out as a consequence to guarantee a sufficient power transfer to the output (the lower the value, the higher the output power).

On the other hand, to maintain a constant (average) output current, some kind of regulation is required and for this reason, on the secondary side, there is an error amplifier which senses the LED current and drives an optocoupler (see *Section 2.2*). On the primary section the corresponding phototransistor is connected to the “FB” pin, and through this input the voltage of the VIPer's PWM comparator is modulated.

In this way, the MOSFET peak current envelope follows the shape of Vin until it is somehow limited by the clipping action of the feedback.

It is worth noting that the bandwidth of this loop must be very low, otherwise it would counteract the Vin modulation.

Figure 6 and *7* show the results of a simulation which represent the behavior of the circuit. *Figure 6* is in the case of no feedback on the FB pin: only Vin is applied to the cont pin. The average output current is 1.12A.

Figure 7 represents the condition when also the feedback is forced on the FB pin (Iout_avg = 0.7A). Please note that it is a rough approximation to show how the configuration works.

Figure 6. No feedback on FB pin

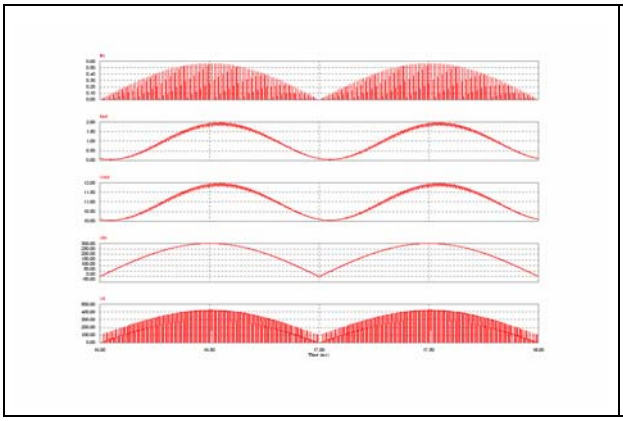
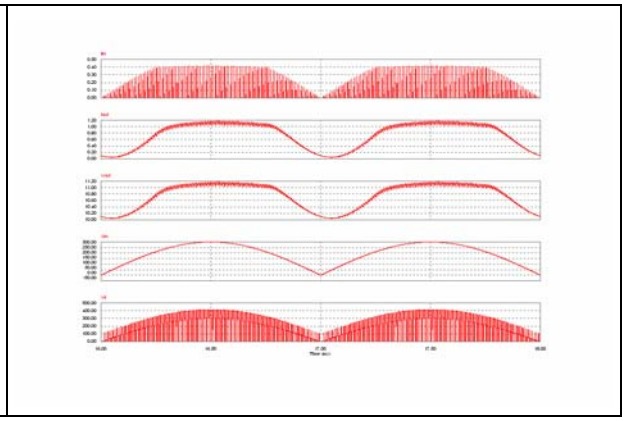


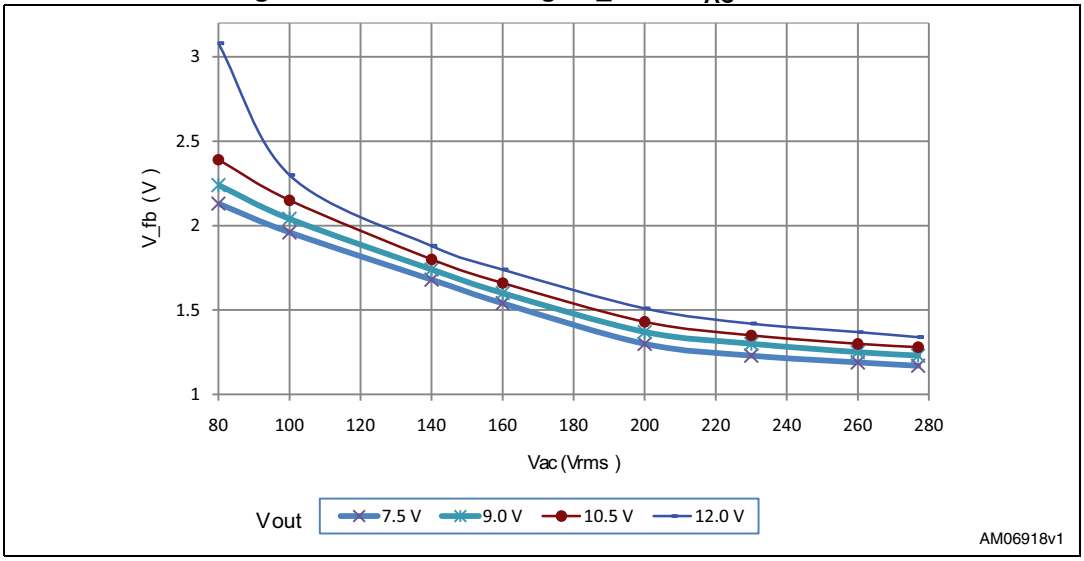
Figure 7. Feedback on FB pin



One limit of this solution is that the voltage applied to the cont pin is directly proportional to the AC input voltage, and then at higher Vin the “clipping” is more evident and the PF is worse.

To overcome this, a possible solution may be to feed part of the FB voltage to the cont pin; in this way an offset voltage that is higher at lower AC input is provided, obtaining a more constant modulation shape, and a better PF.

Figure 8. Feedback voltage V_fb vs. V_{AC} and Vout



Unfortunately it is not possible to simply connect a resistor between the FB and cont pins: to adapt the impedance levels it is necessary to buffer the feedback signal before driving the cont input. To do this, the NPN transistor Q1 is employed in an emitter follower configuration and the R10 resistor provides the correct balancing between the Vin and V_fb actions.

Reducing its value increases the influence of V_fb, obtaining a better control of the output current even at the extreme mains and load values; on the other hand, increasing it makes predominant the influence of Vin optimizing the power factor.

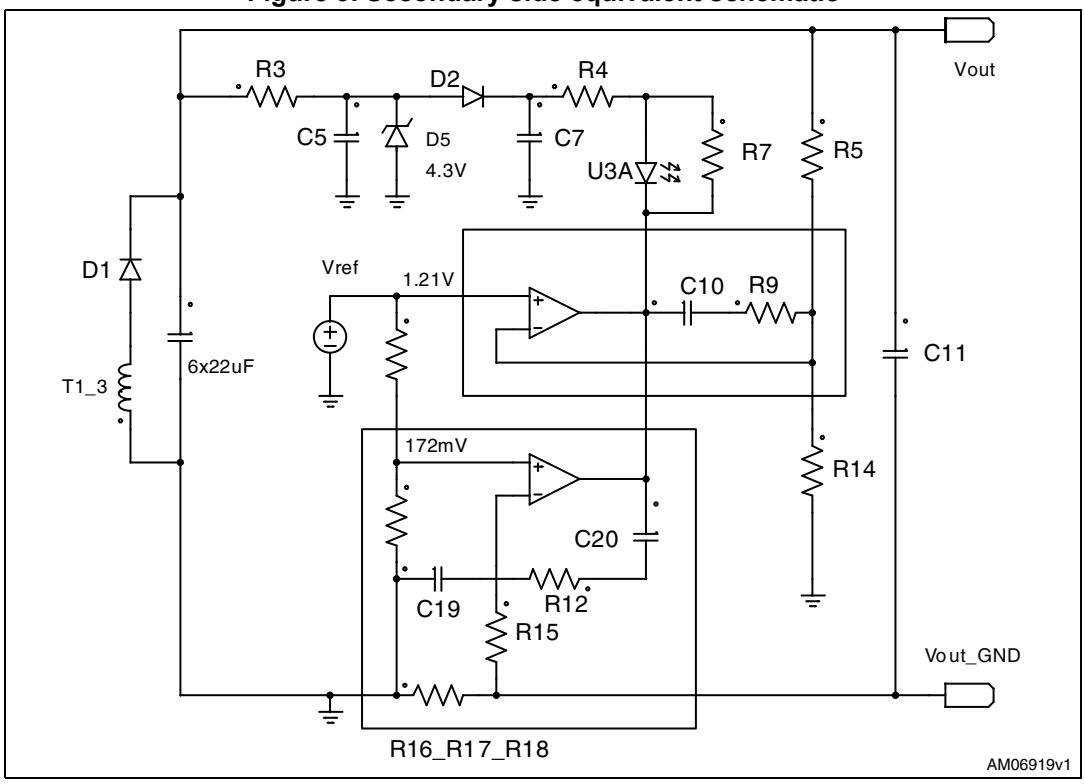
2.2 Secondary side

On the secondary side a TSM1052 is employed as a voltage reference and error amplifier for the constant current control loop, while the CV operational amplifier is simply used as a comparator for output overvoltage protection.

The configuration is quite common, with the two op amp outputs tied in wired_or to drive the optocoupler's photodiode.

The equivalent circuit is represented in *Figure 9*.

Figure 9. Secondary side equivalent schematic



The first point which is worth noting is the decoupling of the supply voltage (R3, D5, C5, C7, etc.) It protects the TMS1052 in the case of overvoltage due to LED “open” fault, and filters the noise that may eventually be picked up from the output wire connection.

Moreover, it avoids that the output voltage and its ripple modulate the photodiode current (while this action can be useful in CV applications, in this case it isn't, because it would introduce a voltage feedback in the current loop path).

The second point is related to the TSM1052 grounding; in this configuration the reference GND is on the left-hand side of the sense resistor (R16, R17, R18 in parallel), the TSM1052 GND pin and the lower side of R14 are connected to this point.

Looking at the component values, it can be noted that:

- The time constant of the voltage op_amp is quite short (R9 = 0 Ω, C10 = 560 pF); this is because the circuit has to react as fast as possible to output overvoltage
- The time constant of the current op_amp is very long (R12 = 5.6 kΩ, C20 = 1 µF), as already stated, the reason for this is in the way in which the current control is implemented; while Vin modulates the cont pin cycle by cycle, the current feedback op_amp simply evaluates the average output current and drives the FB (and cont) pins with a voltage that varies very slowly. For the same reason, also the capacitor C21, on primary side, has a very high value of 10 µF
- The resistor on the optocoupler's photodiode anode (R4) is a mere 220 Ω, this is in order to achieve a high DC loop gain, and so a good current regulation
- The voltage divider, made up of R5 and R14, is dimensioned in order to fix an overvoltage cut-off of:

Equation 1

$$Vout_{coff} = (1.21V) \cdot \left(\frac{R5 + R14}{R14}\right) = 15.97V$$

Slightly higher than the maximum output voltage:

Equation 2

$$Vout_{max} = \left(VLED_{avg} + \frac{1}{2}VLED_{rip} + VRsense_{pk}\right)$$

But not too high, so as to avoid the possibility that Vaux too could reach a critical voltage.

- The sense resistor is implemented with R16, R17 and R18 in parallel. Due to the configuration with GND on the “transformer side” of Rsense, its value must be evaluated taking into account that the threshold level is 172 mV instead of 200 mV.

Equation 3

$$Vsense' = Vsense \cdot \left(\frac{Vref}{Vref + Vsense}\right)$$

Equation 4

$$Vsense' = 0.2 \cdot \left(\frac{1.21}{1.41}\right)V = 0.2 \cdot (0.858)V = 0.1716V$$

Equation 5

$$Rsense = \frac{Vsense'}{I_{LED}}$$

Equation 6

$$Rsense = \frac{0.1716}{0.7} = 0.245\Omega$$

2.3 Circuit variants

Up to now the “basic” 7 W configuration has been referenced, but as indicated in the introduction to the document, the goal was also to investigate the influence of the requirements on the design, with special attention to:

- Output Power: 3.5 W/7.0 W
- Input voltage: wide range (90 V - 277 V_{AC}) / European range (170 V to 277 V_{AC})
- Power factor: > 0.7/>0.9
- Electrolytic capacitors: yes/no (ripple current)

Output power: to change this, it is enough to change the value of some components:

Table 1. Changes

Components/power	3.5 W	7.0 W
Rsense	0.5 Ω	0.25 Ω
Transformer primary inductance	2 mH	1.5 mH
VIPer	VIPer17	VIPer27

Even though, to obtain the best performance also at 3.5 W, some kind of fine tuning may be required in the current shaping circuitry and in the EMI filter section, and probably a smaller transformer would be sufficient.

Input voltage range: this impacts the voltage rating of the devices directly connected to the rectified input voltage. The demonstration board is provided with the indicated components to sustain the max value of Vin = 277 V, and, of course, in the case of a 90 V - 130 V range they can be derated. On the other hand, the max input current occurs at the lower input voltage and then the transformer must be dimensioned as a consequence; for this reason, if the board is targeted to the high line range, the transformer may be reduced (to be carefully verified). That is to say that the wide range is the worst condition, and the demonstration board design reflects this fact.

Power factor: if it is sufficient to reach a PF > 0.7, the transistor Q1, and the associated R8, R10, and C13, can be avoided.

In any case, if this parameter must be optimized, R2+R6, R13, and R10 must be modified, even though it's not a straightforward task, because the best shape of the peak current envelope must be found, as a function of input and output voltage ranges.

Electrolytic capacitors: the question is slightly more complicated; as LEDs have a very long life, also the electronics should have a comparable MTBF, but el_caps with this property, despite being very expensive, are difficult to find, for this reason they should be avoided, but without them, in this configuration, the output current ripple is inevitably high. Therefore, special care must be taken in selecting the LEDs: their max. allowed current must be higher than the output peak current. Moreover, this ripple is almost equivalent to a sort of dimming at twice the line frequency which should be carefully considered from the optical point of view.

In any case the board allows all these variations in order to carry out the tests without any major changes.

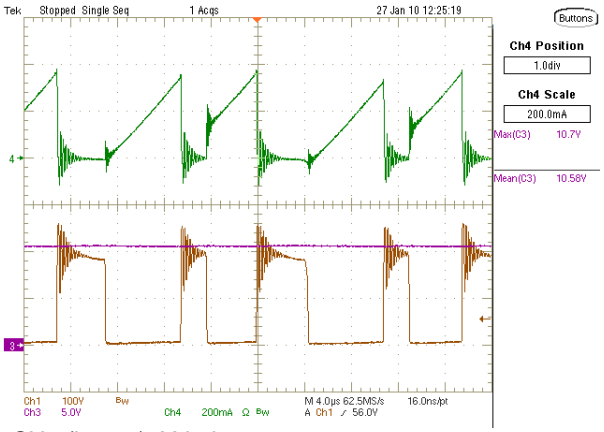
3 Waveforms

To take a look at the behavior of the board, the 7 W configuration has been selected and analyzed in the main characteristic conditions, capturing the relevant signals.

3.1 Input

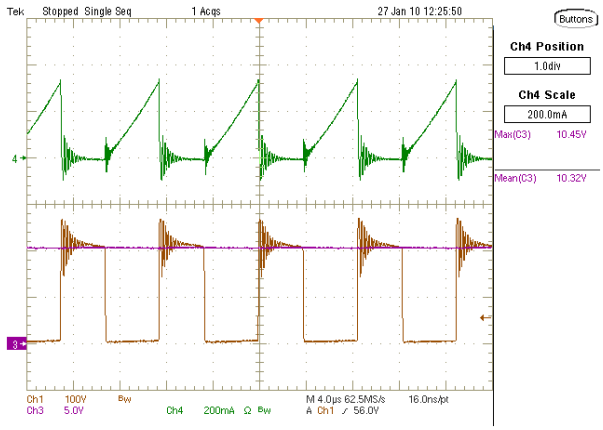
With the first series of waveforms the intention was to give a representation of the VIPer's drain voltage and current at nominal output (10.5 V/0.7 A) with several input voltages. Because of the difficulty of taking a stable snapshot of these measurements with an AC input, use of a DC source was chosen, and the voltage fixed at: 75 V (the minimum level at which the circuit starts switching), 100 V, 120 V, 162 V, 254 V, 325 V, 391 V, and then 50 V (the minimum level at which the converter stops switching.

Figure 10. V_drain, I_drain at Vin= 75 V



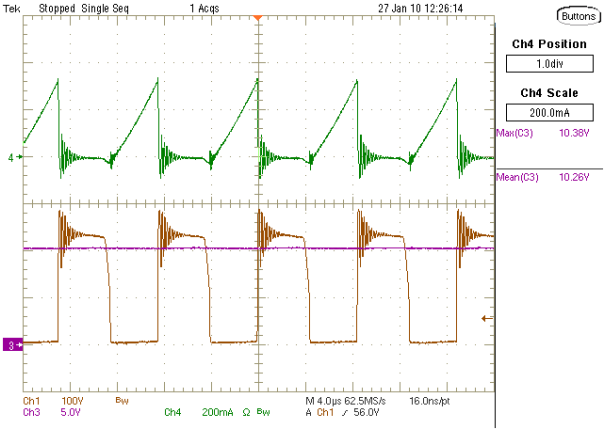
CH1 (brown)=Vdrain, CH3 (red)= Vout, CH4 (green)= Idrain

Figure 11. V_drain, I_drain at Vin= 100 V



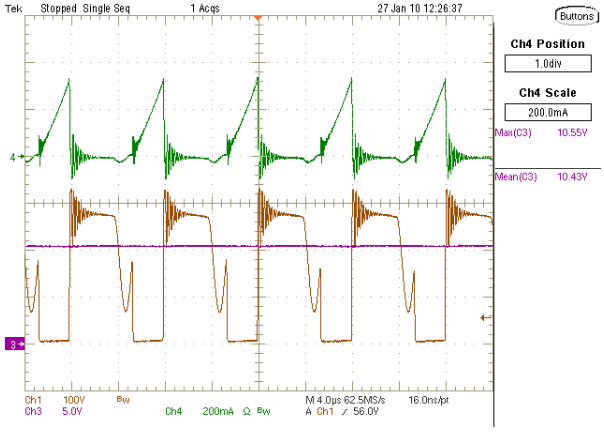
CH1 (brown)=Vdrain, CH3 (red)= Vout, CH4 (green)= Idrain

Figure 12. V_drain, I_drain at Vin= 120 V



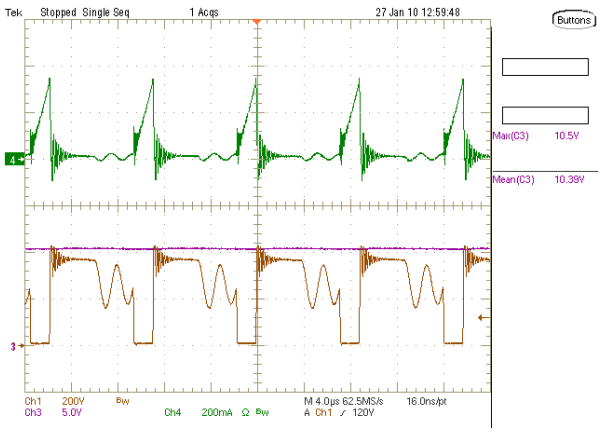
CH1 (brown)=Vdrain, CH3 (red)= Vout, CH4 (green)= Idrain

Figure 13. V_drain, I_drain at Vin= 162 V



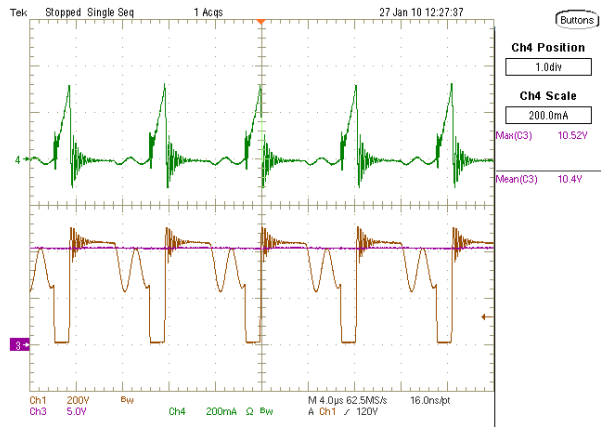
CH1 (brown)=Vdrain, CH3 (red)= Vout, CH4 (green)= Idrain

Figure 14. V_drain, I_drain at Vin= 254 V



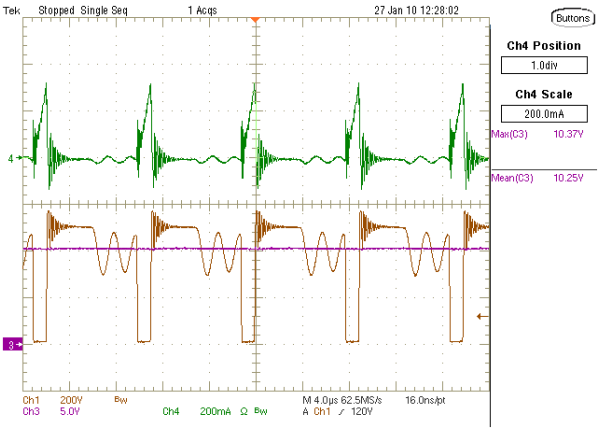
CH1 (brown)=Vdrain, CH3 (red)= Vout, CH4 (green)= Idrain

Figure 15. V_drain, I_drain at Vin= 325 V



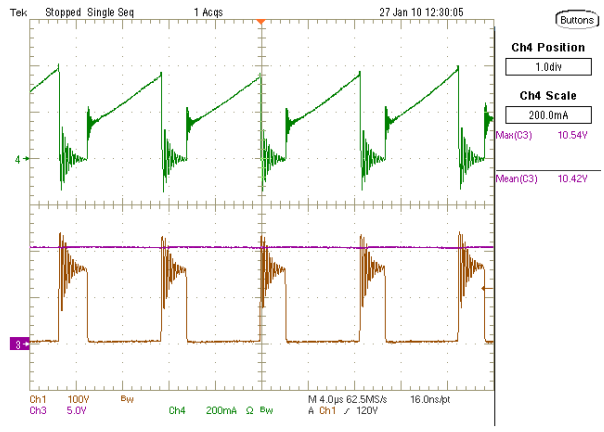
CH1 (brown)=Vdrain, CH3 (red)= Vout, CH4 (green)= Idrain

Figure 16. V_drain, I_drain at Vin= 391 V



CH1 (brown)=Vdrain, CH3 (red)= Vout, CH4 (green)= Idrain

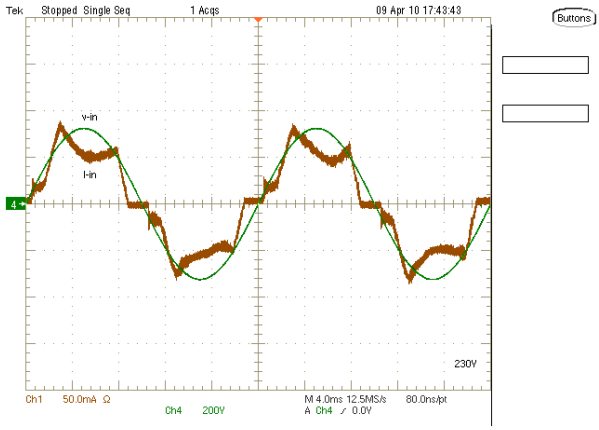
Figure 17. V_drain, I_drain at Vin= 50 V



CH1 (brown)=Vdrain, CH3 (red)= Vout, CH4 (green)= Idrain

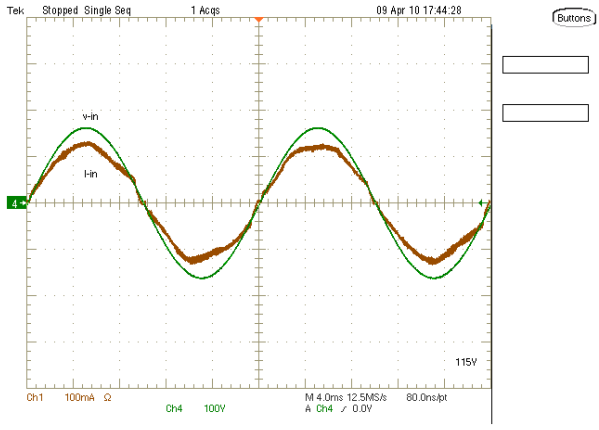
And to give an idea of the AC input voltage and current, *Figure 18* and *19* show the plot of these waveforms.

Figure 18. Vin and Iin at Vin = 230 V_{AC}



CH1(brown)= Iin
CH4 (green)= Vin

Figure 19. Vin and Iin at Vin = 115 V_{AC}



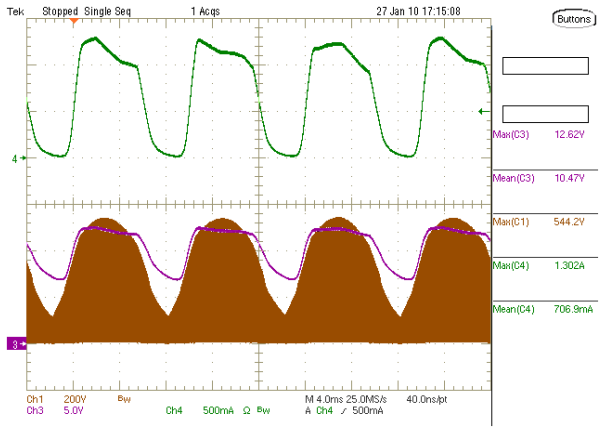
CH1(brown)= Iin
CH4 (green)= Vin

3.2 Output

The following images represent the output current and voltage waveforms at nominal load (10.5 V, 0.7 A) in the case of input voltage of 230 and 115 V_{AC}.

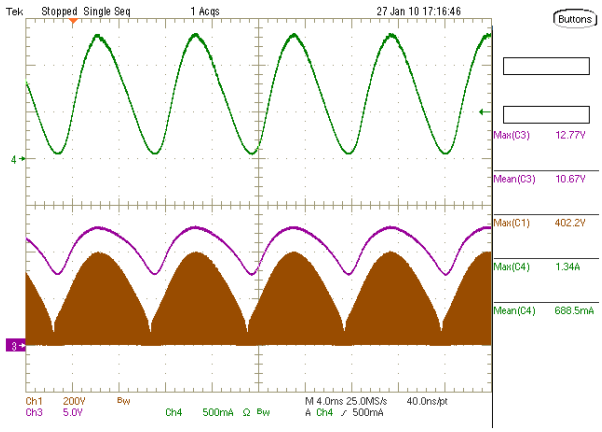
Without an output electrolytic capacitor:

Figure 20. V_out, I_out at Vin = 230 V_{AC}, no El_cap



CH1 (brown)=Vdrain, CH3 (red)= Vout,
CH4 (green)= Iout

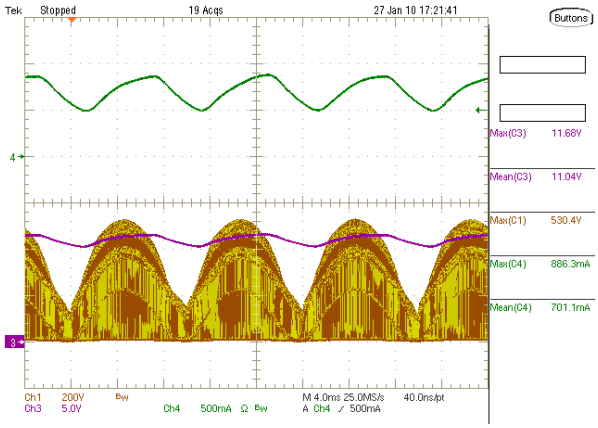
Figure 21. V_out, I_out at Vin = 115 V_{AC}, no El_cap



CH1 (brown)=Vdrain, CH3 (red)= Vout,
CH4 (green)= Iout

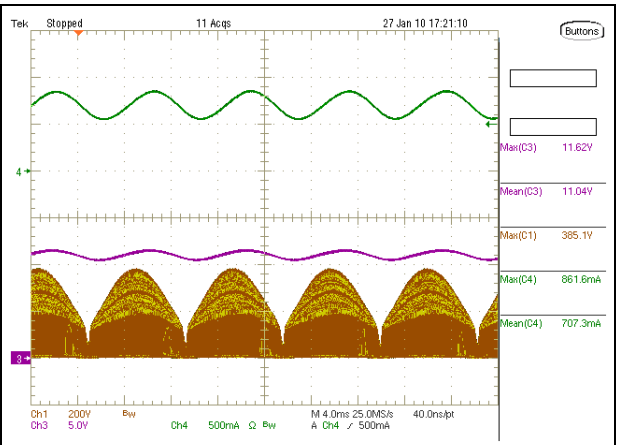
With an output electrolytic capacitor of 1000 µF:

Figure 22. V_out, I_out at Vin = 230 V_{AC}, 1000 µF El_cap



CH1 (brown)=Vdrain, CH3 (red)=Vout
CH4 (green)= Iout

Figure 23. V_out, I_out at Vin = 115 V_{AC}, 1000 µF El_cap



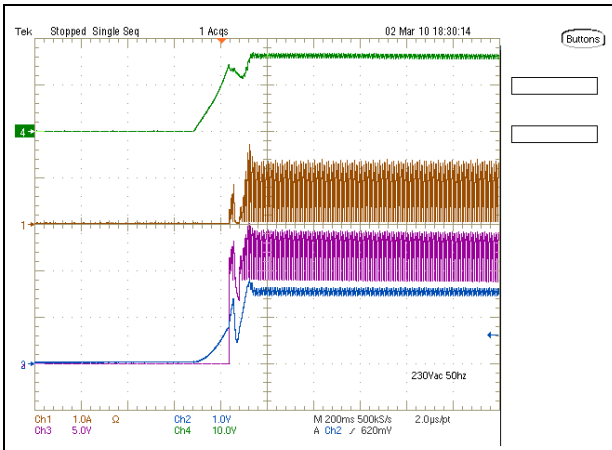
CH1 (brown)=Vdrain, CH3 (red)=Vout
CH4 (green)= Iout

Of course in the case of no el_cap, the ripple current is much higher, it is up to the application to decide if it can be tolerated or a capacitor is required.

3.3 Startup sequence

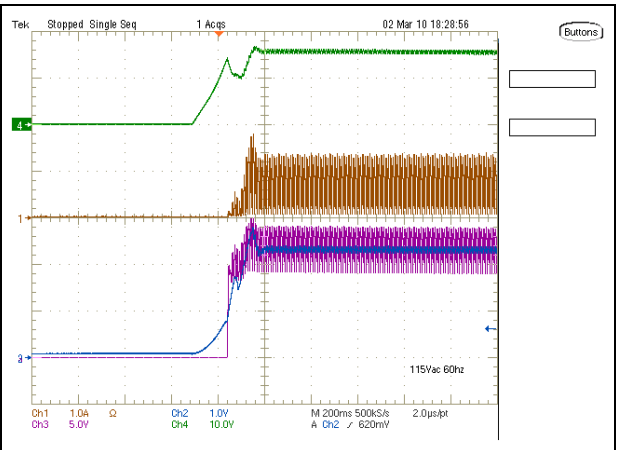
Oscilloscope screenshots were taken at 230 V and 115 V, with the nominal load without and with - a 1000 µF output capacitor.

Figure 24. Startup sequence at Vin = 230 V_{AC}, no El_cap



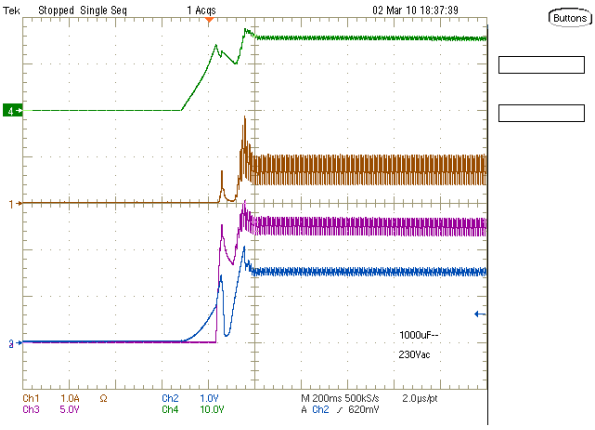
CH1 (brown)=Iout CH3 (blue)= Vfb
CH2 (red)=Vout CH4 (green)=Vdd

Figure 25. Startup sequence at Vin = 115 V_{AC}, no El_cap



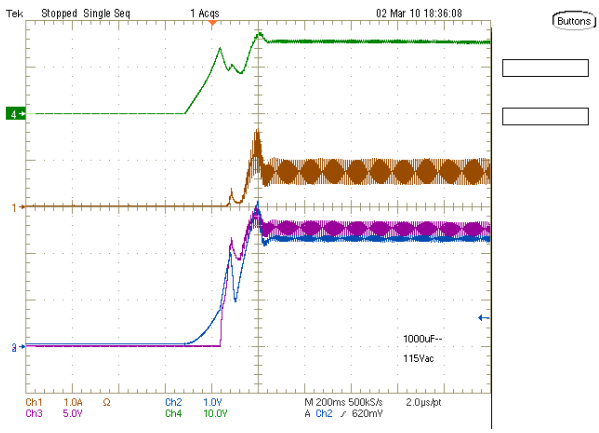
CH1 (brown)=Iout CH3 (blue)= Vfb
CH2 (red)=Vout CH4 (green)=Vdd

Figure 26. Startup sequence at Vin = 230 V_{AC}, 1000 µF El_cap



CH1 (brown)=Iout CH3 (blue)= Vfb
CH2 (red)=Vout CH4 (green)=Vdd

Figure 27. Startup sequence at Vin = 115 V_{AC}, 1000 µF El_cap



CH1 (brown)=Iout CH3 (blue)= Vfb
CH2 (red)=Vout CH4 (green)=Vdd

The circuit is relatively under damped, but this is intentional in order to guarantee a sure startup, while minimizing the short-circuit detection time and providing a good average current regulation.

Increasing R12 leads to a better startup current envelope and lower overshoot, but care should be taken regarding the overload protection and DC current regulation, which slightly worsens.

With output capacitors of very high value, it is possible that the circuit doesn't start at the "first shot", in this case it is enough to increase the Vaux capacitors C16 and C17, but also in this case the short-circuit protection must be evaluated very carefully.

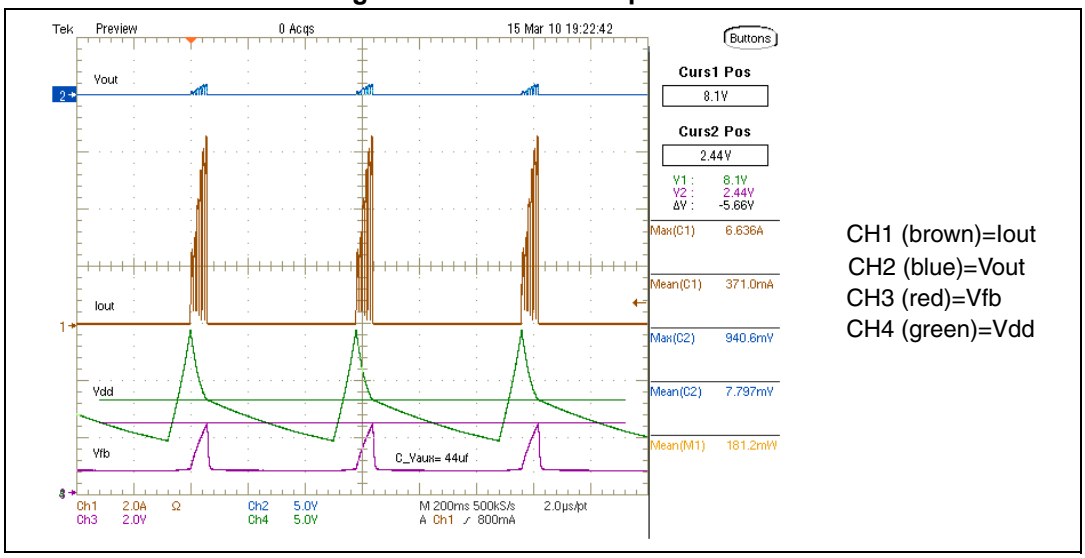
3.4 Short-circuit protection

The primary application of this board is as a "bulb replacement", and therefore short-circuit failure is not critical: provided that the circuit survives without any damage. There are no stringent requirements on maximum output current during shorts, so simplicity and minimal part count are privileged at the expense of higher current pulses.

As the feedback circuit is too slow to react to the short-circuit, the protection is based on the fact that, in case of overload, the output voltage drops, and as a consequence, also the auxiliary power Vdd reaches the shutdown voltage of the controller (8 V nom).

The time required for the intervention is directly proportional to the capacitance of C16 and C17, and then, the lower their value, the shorter the output current pulses. But, on the other hand, it cannot be reduced too much, otherwise the startup sequence becomes critical.

Figure 28. Short-circuit protection



As the most severe condition appears at the highest input voltage, the snapshot is taken with V_{AC} = 277 V, and with a total capacitance value (C16 + C17) of 44 µF.

As can be seen, even though the current pulses are quite high (6.6 A max) the output voltage and the repetition rate are low, for this reason also the power involved is not critical (181 mW average) and therefore, this condition can be sustained indefinitely.

Figure 29 and *30* show the conditions when the short-circuit is applied and removed.

It is worth noting that the very short and high current pulse, which appears when the short circuit is forced, is due to the discharge of the ceramic output capacitors; even though no electrolytic is present this current can reach a very high value.

Figure 29. Short-circuit application

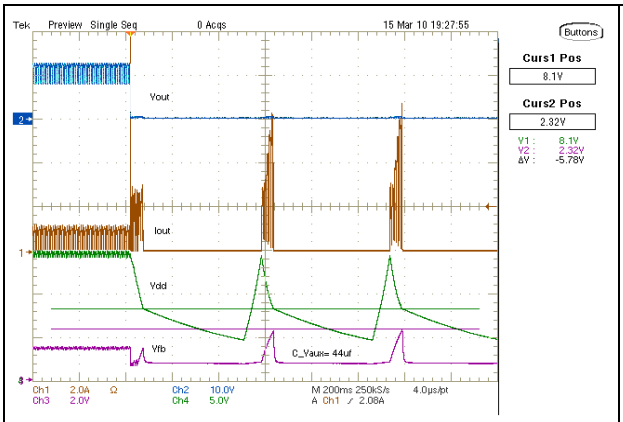
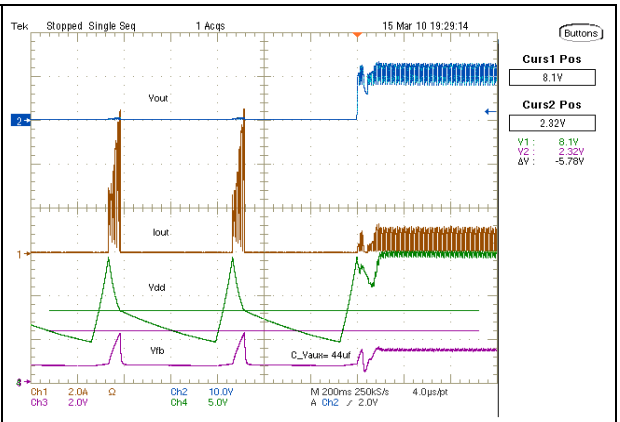


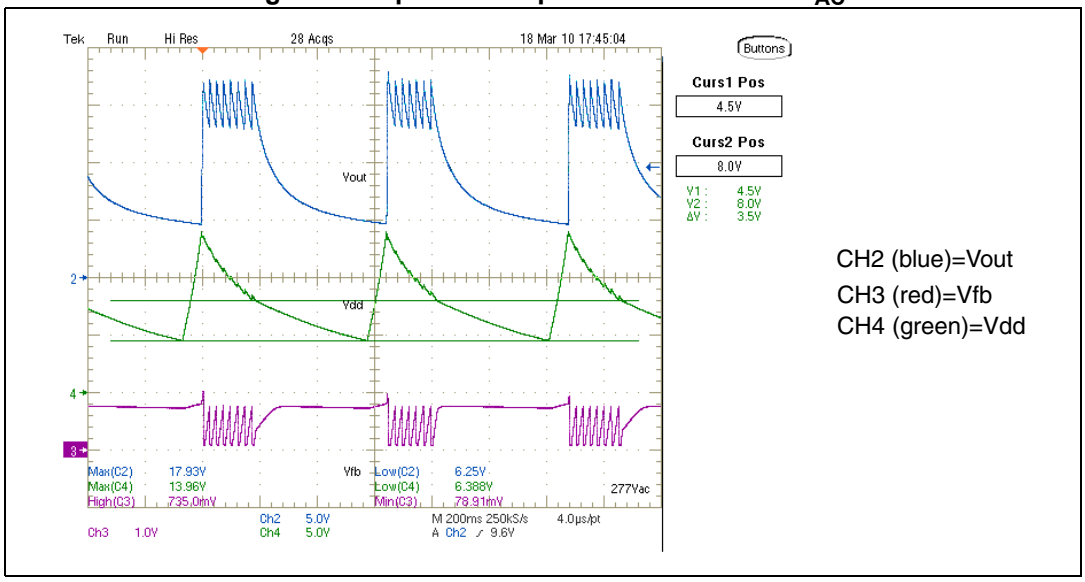
Figure 30. Short-circuit removal



3.5 Open circuit protection

As already indicated, the TSM1052 in the secondary section contains an op amp that senses the output, and in the case of overvoltage, drives the optocoupler photodiode, which in turn forces the VIPer's FB pin to ground. As a result the VIPer stops switching, and enters the burst mode if Vfb drops below the 0.6 V threshold. If Vdd goes under 8 V (V_{AC} higher then 140 V), a restart cycle is initiated.

Figure 31. Open circuit protection Vin = 277 V_{AC}



Otherwise a continuous burst mode is sustained.

Figure 32. Open circuit protection Vin = 90 V_{AC}

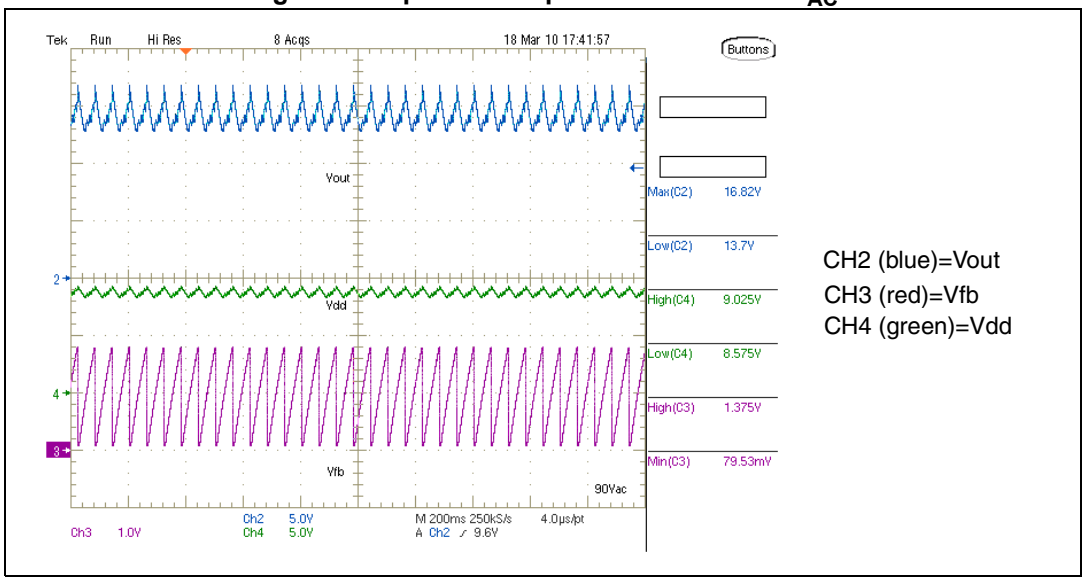
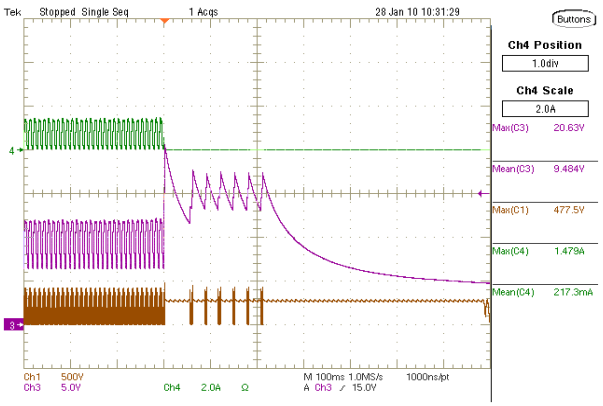
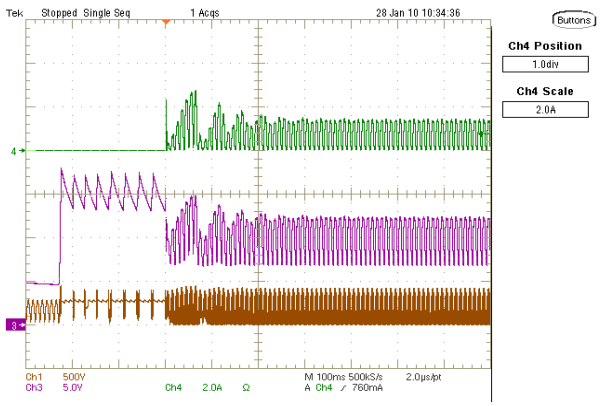


Figure 33. Open circuit application



CH1 (brown)=Vdrain CH4 (green)=Iout
CH3 (red)=Vout

Figure 34. Open circuit removal



CH1 (brown)=Vdrain CH4 (green)=Iout
CH3 (red)=Vout

4 Measurements

For all the board configurations, a common test setup was defined with:

- A HP6812B programmable AC mains voltage source
- A Yokogawa WT210 wattmeter to measure input voltage, current, power, and PF
- A string of several diodes to simulate the LED load
- A couple of Keithley 2000 multimeters to measure output (average) voltage and current, or alternatively, a WT210 Wattmeter to measure output power and efficiency
- An Agilent E7402A spectrum analyzer plus LISN for EMI conducted emission tests

The test procedure consisted of connecting the module output to a string of 10 diodes (STTH108) to emulate an LED load with a forward voltage of approximately 8.75 V, and then taking the measurements while the input voltage was set at several values from 90 to 277 V_{AC}.

The procedure was repeated increasing the number of diodes (12 and 14 devices) in order to simulate an LED load with a voltage of about 10.5 V and 12.0 V.

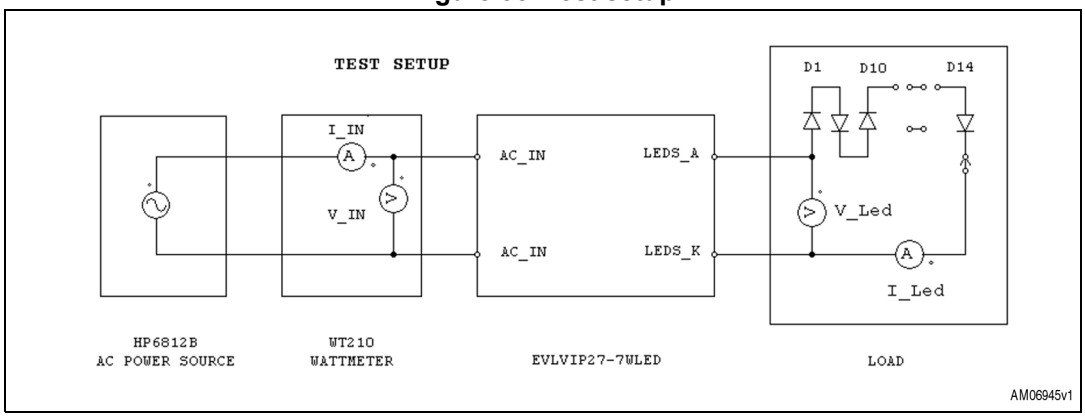
The first run was without any electrolytic, and then the measurements were repeated with a 1000 µF capacitor directly connected to the output.

In both conditions relevant data were collected and the results summarized in the following graphs: the first shows the output voltage as a function of the input AC voltage with the number of load diodes as the parameter, the others represent:

- the output current (average)
- the output current (peak)
- the output power
- the efficiency
- the power factor

as a function of the input voltage and with the output voltage approximately corresponding to 10, 12, and 14 diodes load, as the parameter.

Figure 35. Test setup



Special consideration must be paid to output power and efficiency measurements.

Usually, in making these evaluations on standard power supplies, it is enough to take the average values, as read out from the Voltmeter (V_Led) and Ammeter (I_Led) and simply calculate the output power as their product.

This approach is correct whenever these values are constant, but in this application, due to the high ripple present, especially if no electrolytic capacitor is employed, these waveforms cannot be considered DC values at all. Therefore a more accurate way to take the measurements, at least from the AC-DC converter point of view, is to connect a true wattmeter also to the output.

For this reason, as indicated above, the two Keithley 2000s were replaced with a WT210 then the input/output power measurements were repeated and the efficiency evaluated.

4.1 7.0 W NO EL_CAP configuration

Figure 36. NO_El_Cap output voltage (average)

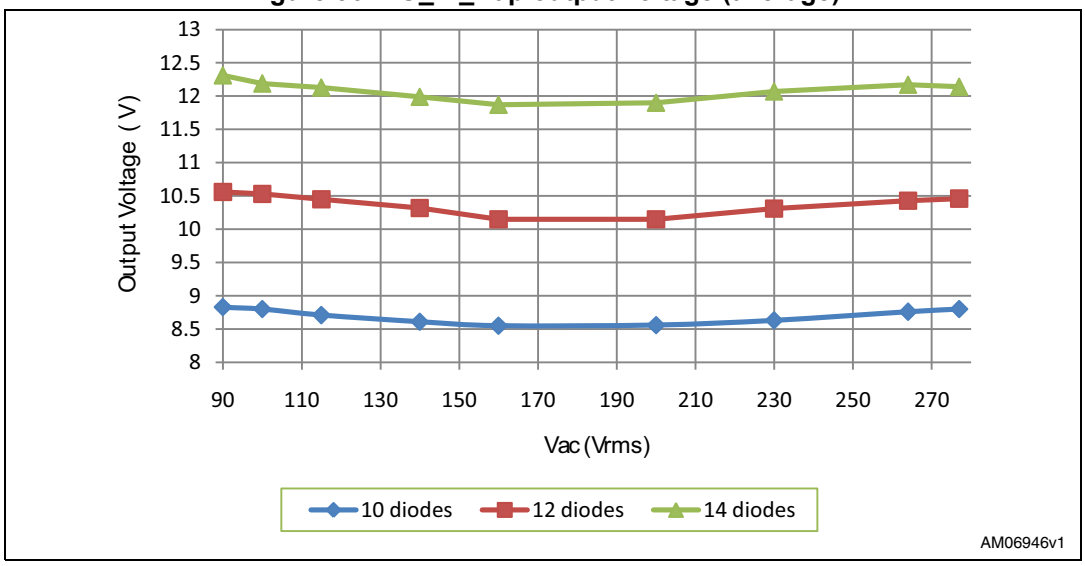


Figure 37. NO_EI_Cap output current (average)

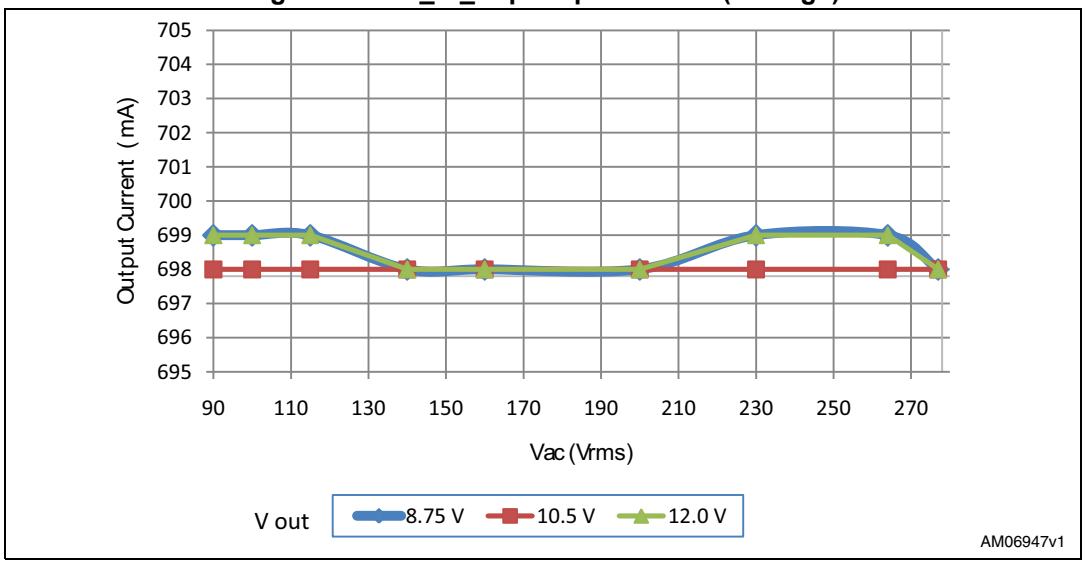


Figure 38. NO_EI_Cap output current (peak)

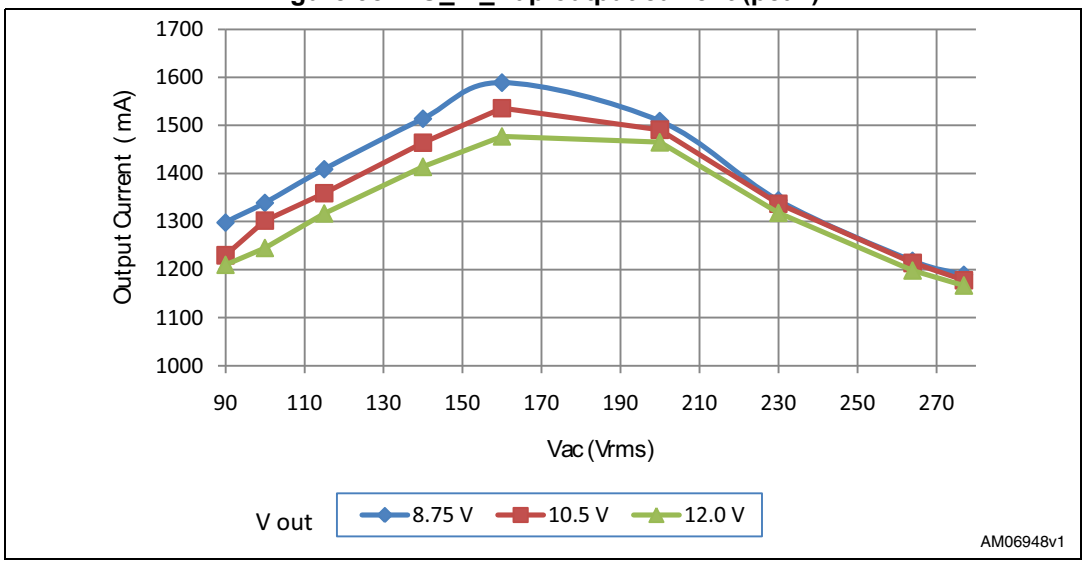


Figure 39. NO_EI_Cap output power

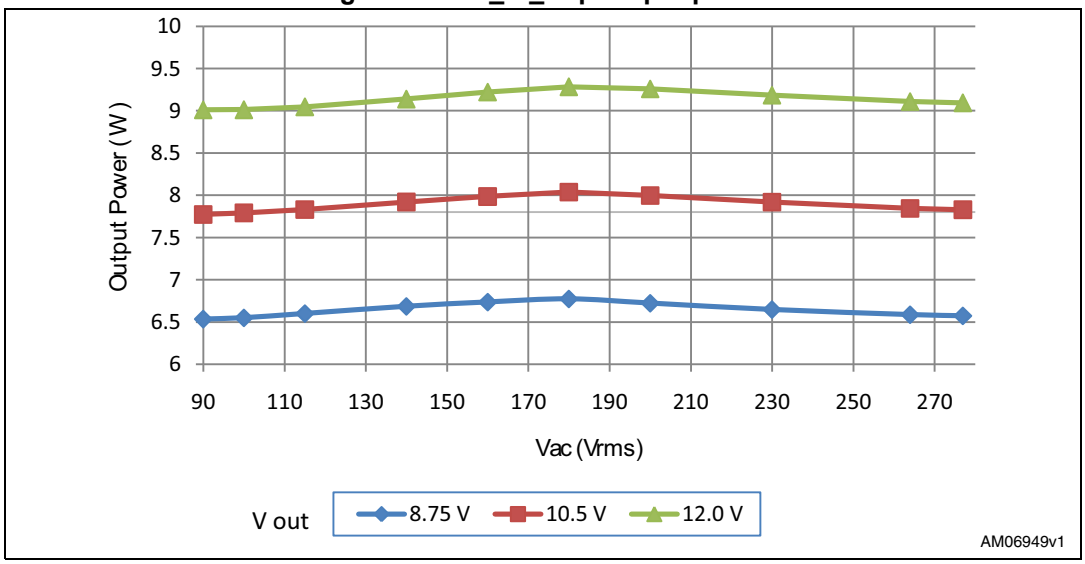


Figure 40. NO_EI_Cap efficiency

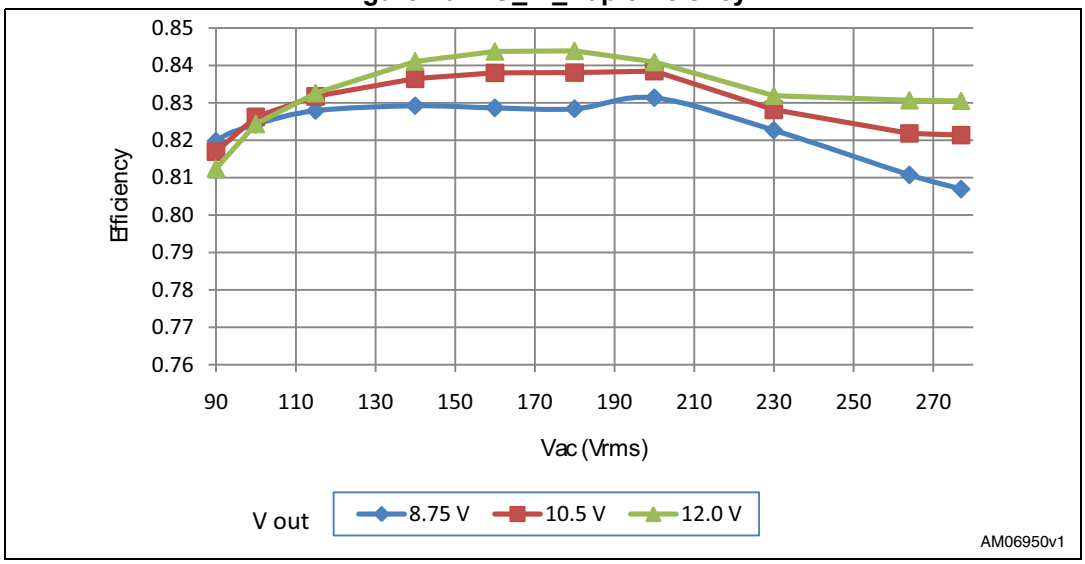
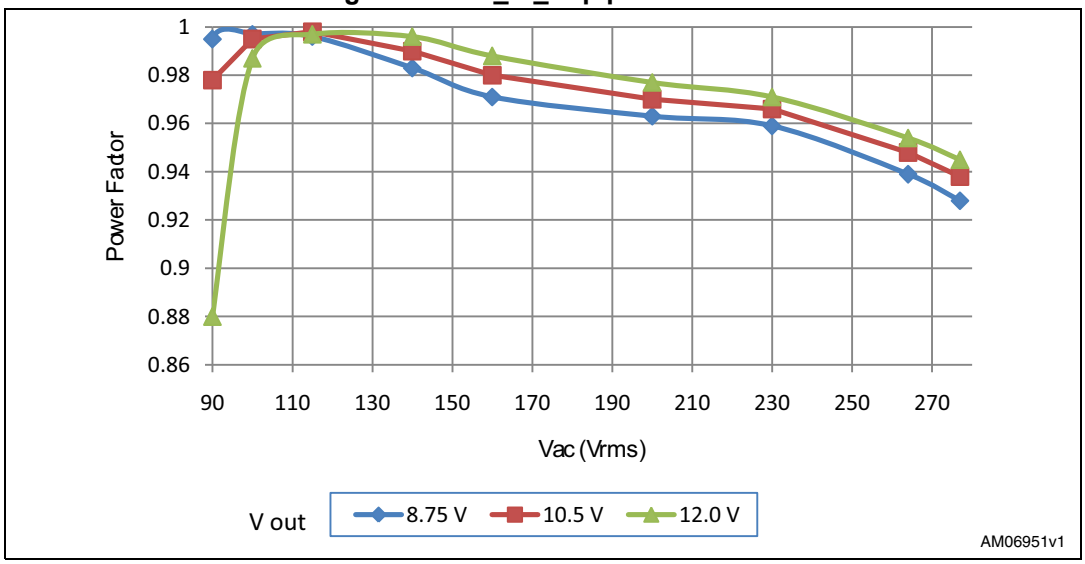


Figure 41. NO_El_Cap power factor



4.2 7.0 W EL_CAP configuration

The following measurements were taken with a 1000 µF electrolytic capacitor connected to the module output.

Figure 42. 1000 µF output voltage (average)

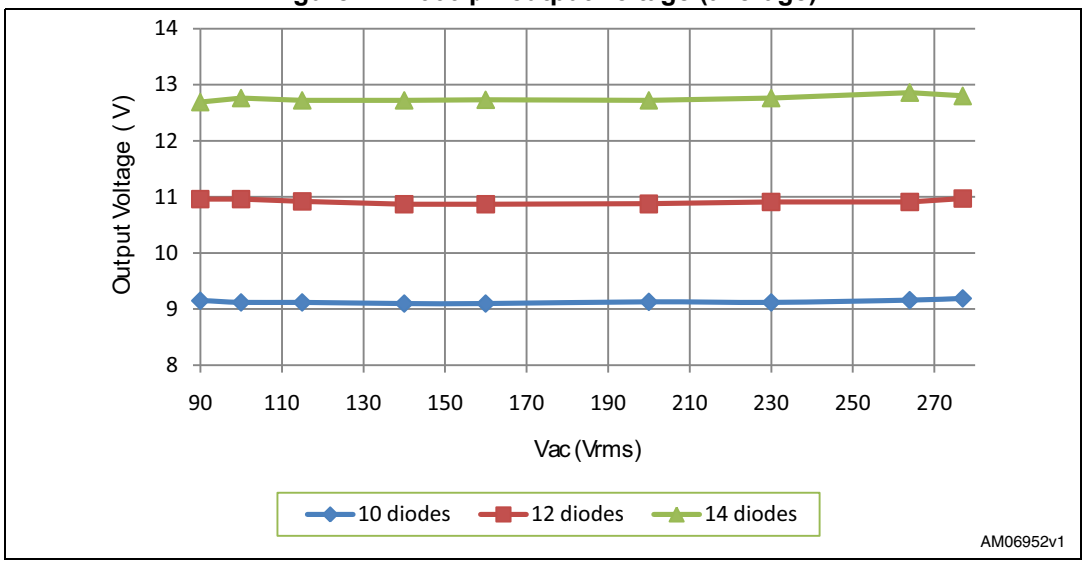


Figure 43. 1000 µF output current (average)

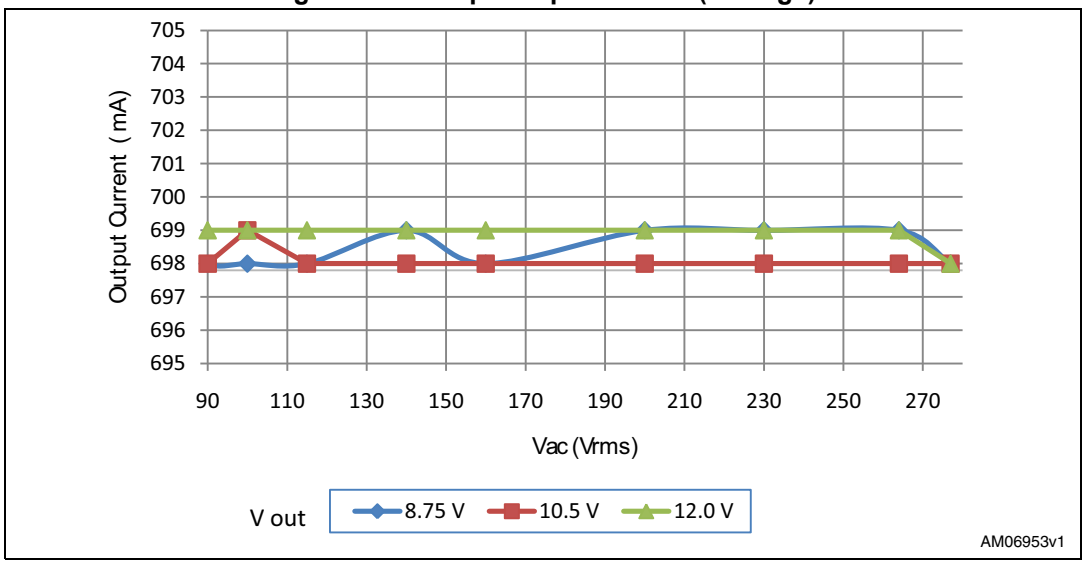


Figure 44. 1000 µF output current (peak)

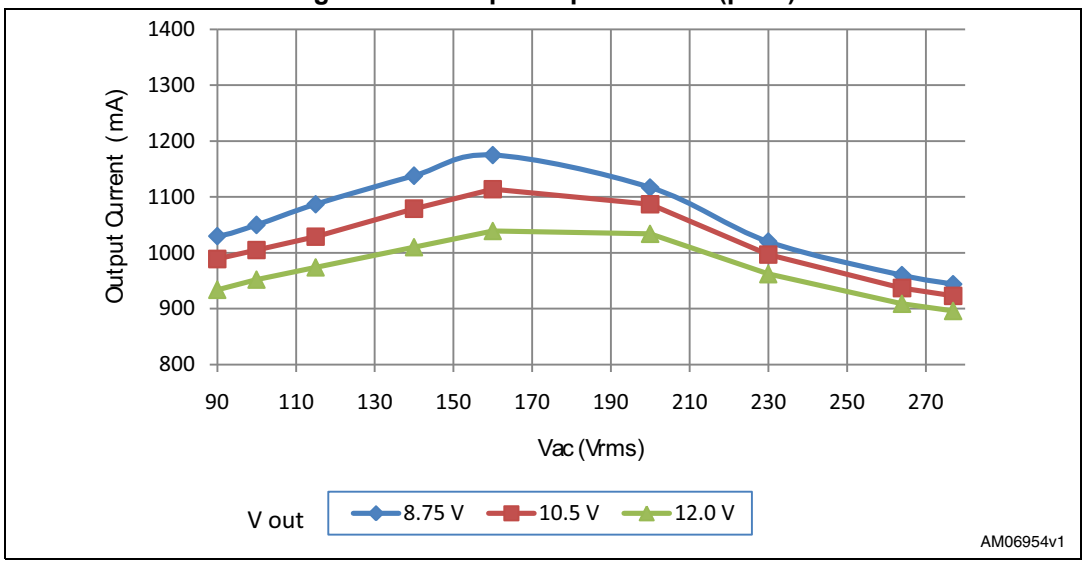


Figure 45. 1000 µF output power

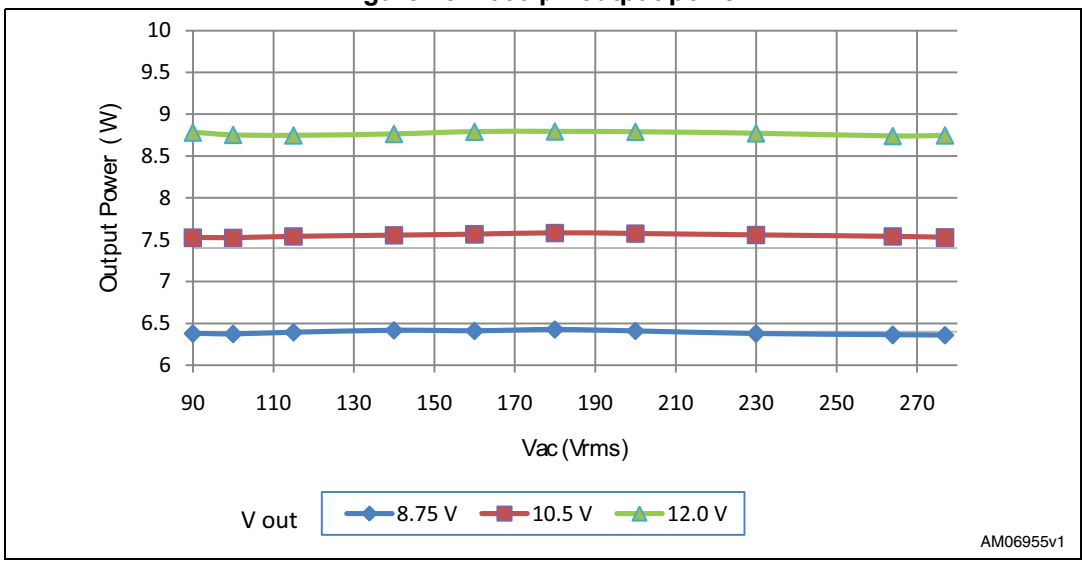


Figure 46. 1000 µF efficiency

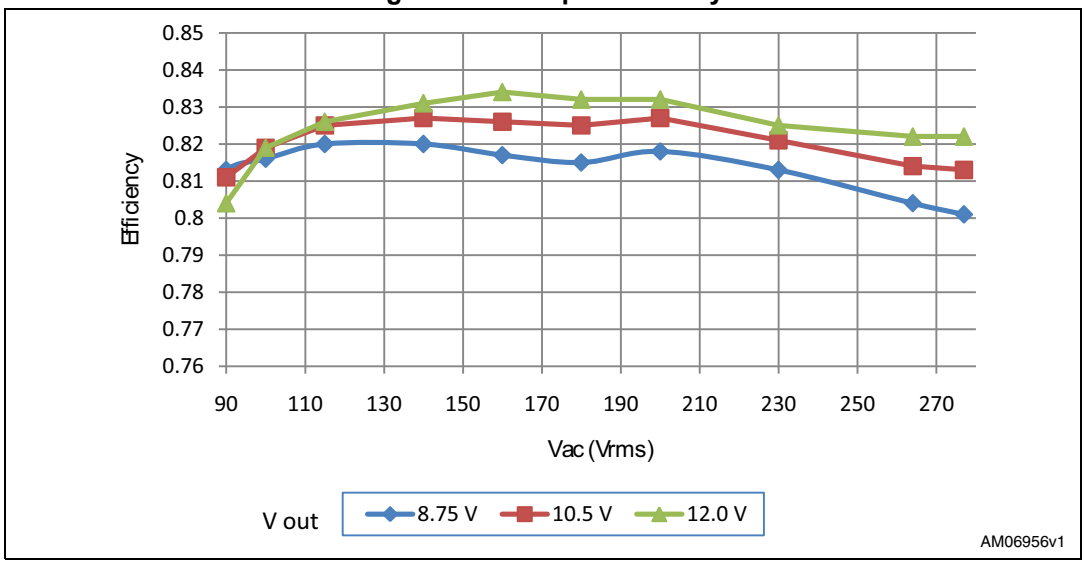
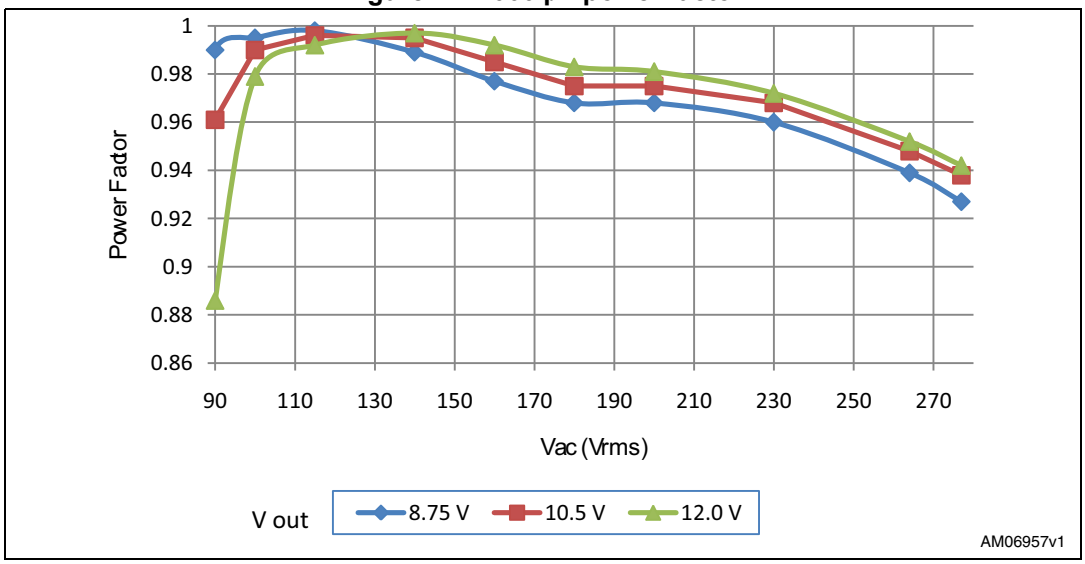


Figure 47. 1000 µF power factor



4.3 EMI filter

The first version of the EMI filter has been implemented with the classic PI cell:

- C4 (22 nF) capacitor before the diode bridge plus C3 (22 nF) capacitor
- L1 coil (1 mH)
- C1 (100 nF) capacitor

Figure 48 and *49* show the plots taken at 230 V and 115 V with an LED load (0.7 A/10.5 V).

Figure 48. EMI (PI filter) 230 V_{AC}

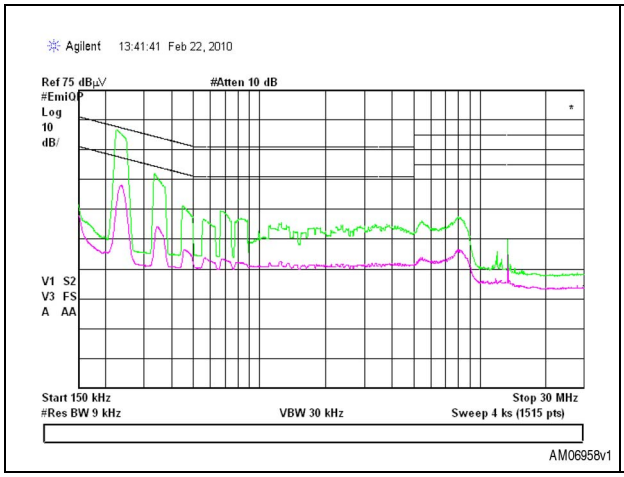
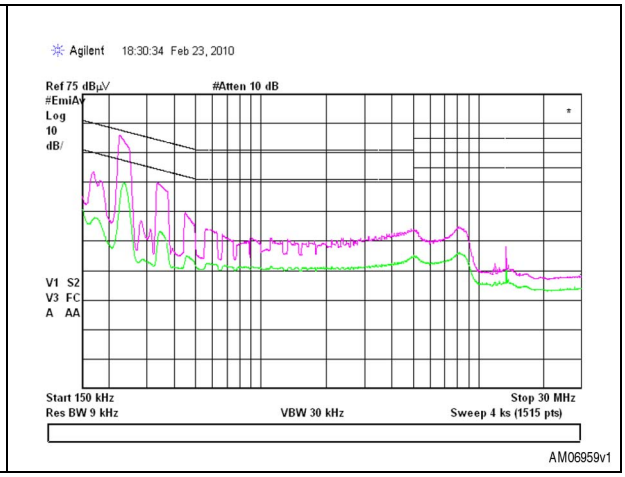


Figure 49. EMI (PI filter) 115 V_{AC}



As can be seen, there wasn't a lot of margin, so the inductance value was increased. It is not possible to increment the capacitances, unless at the expenses of a worse PF, and with limited improvement. Then, to be safe, a second coil (L3 -1 mH) was introduced in the AC path, actually adding an L cell just before the diode bridge and the PI section.

The result obtained is clearly better and is indicated in *Figure 50* and *51*.

Figure 50. EMI (L + PI filter) 230 V_{AC}

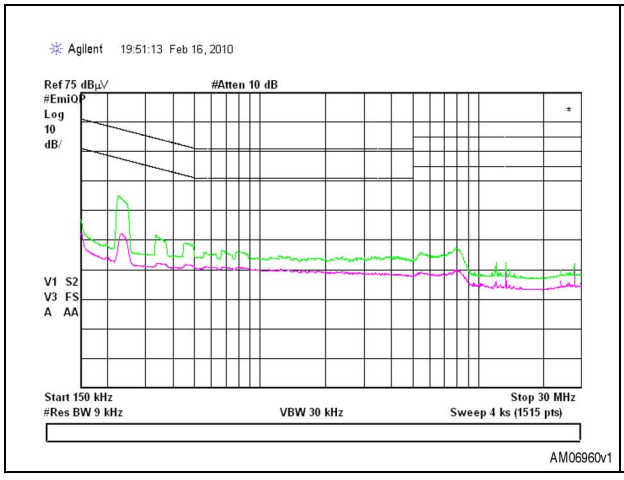
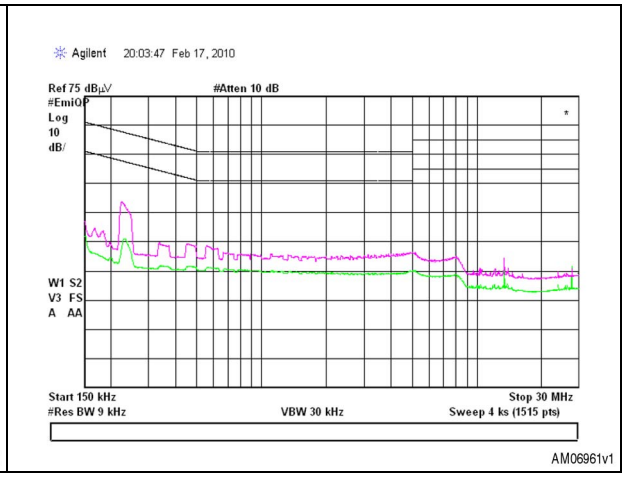


Figure 51. EMI (L + PI filter) 115 V_{AC}



4.4 Thermal maps

The following images were taken with a thermo camera under the following conditions:

- Ambient temperature: 27 °C
- Load: 7 W LED
- AC input voltage: 90 V, 115 V, 230 V, and 277 V

The three highlighted areas correspond to the devices:

1. VIPer27
2. Transformer
3. STPS3L60 output diode

Figure 52. Thermal map at 90 V_{AC}

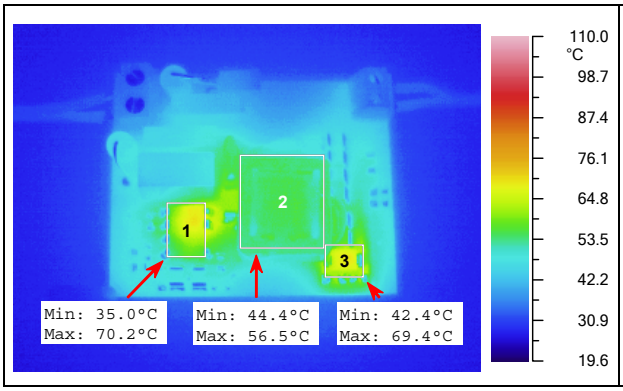


Figure 53. Thermal map at 115 V_{AC}

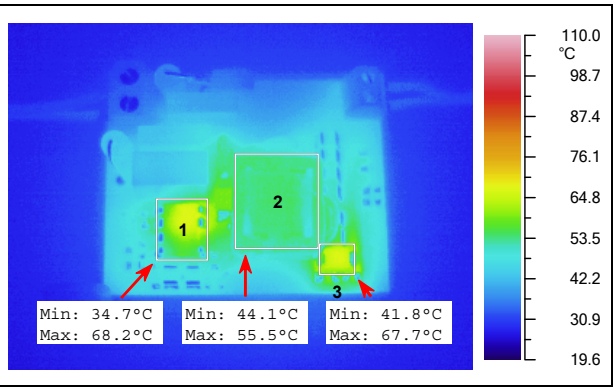


Figure 54. Thermal map at 230 V_{AC}

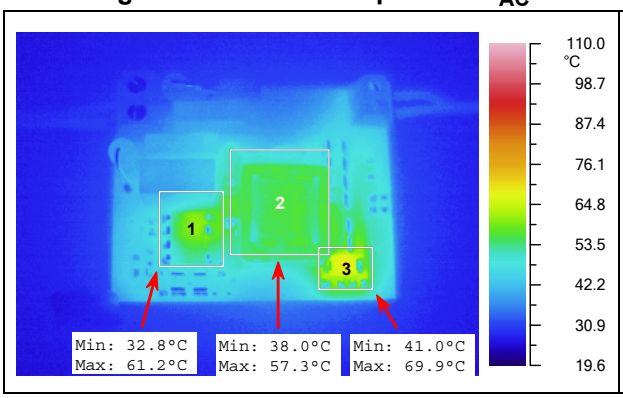


Figure 55. Thermal map at 277 V_{AC}

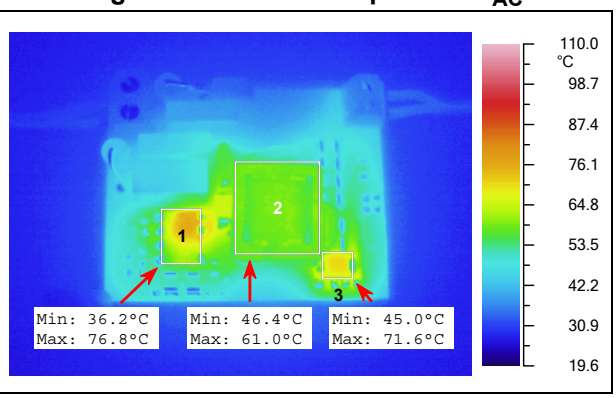


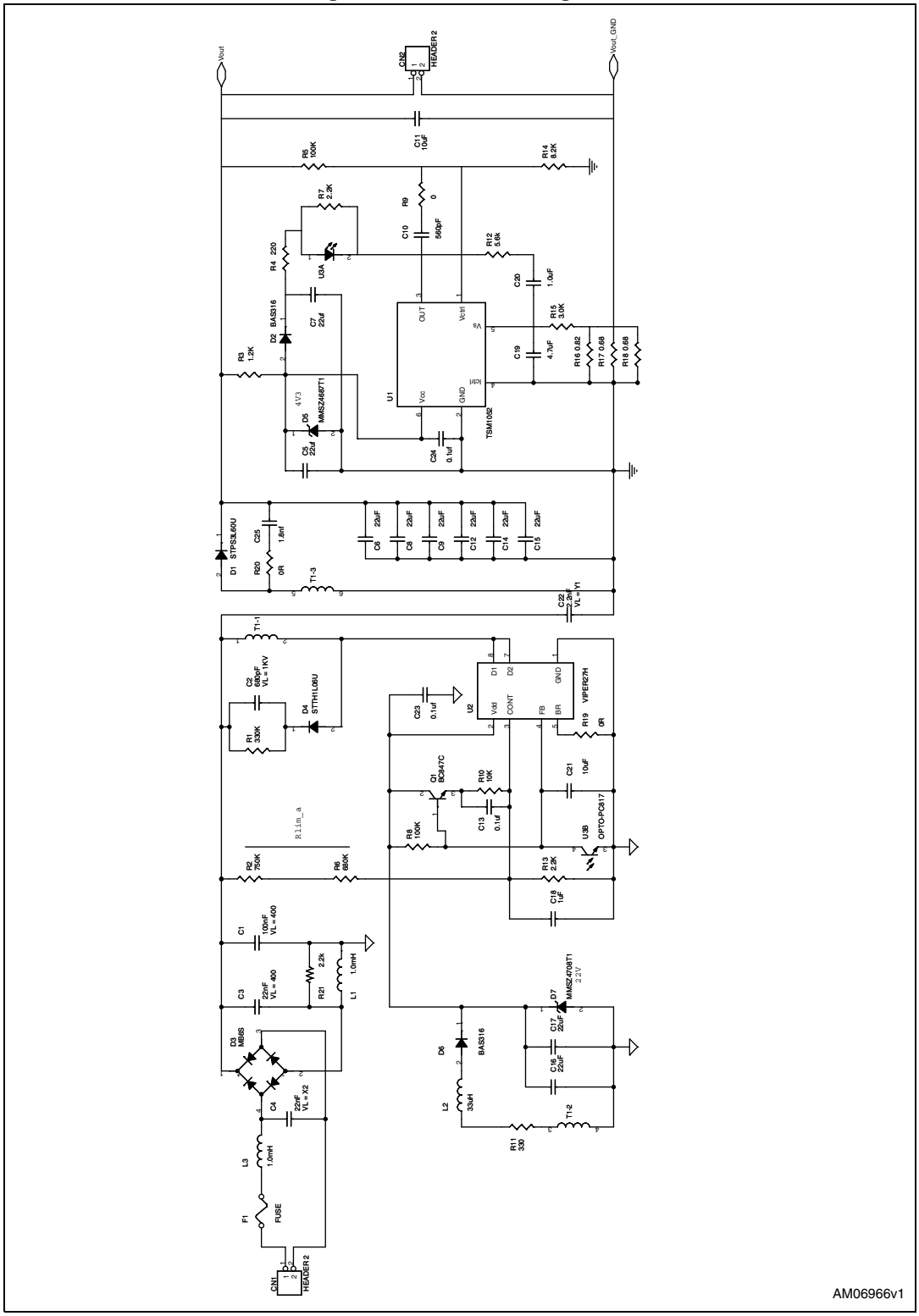
Table 2. Components max. temperature

Device	T[^{0}C]@ 90 V	T[^{0}C]@ 115 V	T[^{0}C]@ 230 V	T[^{0}C]@ 277 V
VIPer27	70.2	68.2	61.2	76.8
Transformer	56.5	55.5	57.3	61.0
STPS3L60	69.4	67.7	69.9	71.6

As can be seen, the circuit is well within safe conditions.

5 Electrical diagram

Figure 56. Electrical diagram



6 BOM list

Table 3. BOM 7.0 W version

Reference	Part	VL	PCB footprint	note
CN1	Header 2		5.08 mm	
CN2	Header 2		3.81 mm	
C1	100 nF	400	5.0x13.0	EPCOS B32921
C2	680 pF	1 kV	5.08 mm	1KV CERCAP DIA. 4x7 mm PITCH 5.08 mm MURATA
C3	22 nF	400	5.0x13.0	EPCOS B32921
C4	22 nF	X2	5.0x13.0	EPCOS B32921
C5,C6,C7,C8,C9,C12, C14,C15,C16,C17	22 µF	25	1210	
C10	560 pF	25	0603	
C11,C21	10 µF	25	1210	
C13,C23,C24	0.1 µF	16	0603	
C18	1 µF	16	0603	
C19	4.7 µF	16	0603	
C20	1.0 µF	16	0603	
C22	2.2 nF	Y1	10 mm	Y1 SAFETY CAP DE1E3KX222M MURATA
C25	1.8 nF	50	0603	
D1	STPS3L60U		SMB	
D2,D6	BAS316		SOD-323	
D3	MB6S		SOIC-4	
D4	STTH1L06U		SMB	
D5	MMSZ4687T1		SOD-123	
D7	MMSZ4708T1		SOD-123	
F1	Fuse	250 V	8.5x4 mm	800 mA
L1,L3	1.0 mH		5.2x12 mm	0.1 A axial lead
L2	33 µH		1206	
Q1	BC847C		SOT-23	
R1	330 kΩ		1206	
R2	750 kΩ		1206	
R3	1.2 kΩ		1206	
R4	220 Ω		0805	

Table 3. BOM 7.0 W version (continued)

Reference	Part	VL	PCB footprint	note
R5,R8	100 kΩ		0805	
R6	680 kΩ		1206	
R7,R13	2.2 kΩ		0805	
R9	0		0805	
R10	10 kΩ		0805	
R11	330 Ω		1206	
R12	5.6 kΩ		0805	
R14	8.2 kΩ		0805	
R15	3.0 kΩ		0805	
R16	0.82 Ω		1206	
R17,R18	0.68 Ω		1206	
R19,R20	0		0805	
R21	2.2 kΩ		AX/RC05	
T1	T1		E16	
U1	TSM1052		SOT23-6	
U2	VIPer27H		DIP-7	
U3	OPTO-PC817-A		4-SMD	

7 7 W transformer specifications

7.1 Mechanical specifications

Figure 57. Coil former mechanical drawing

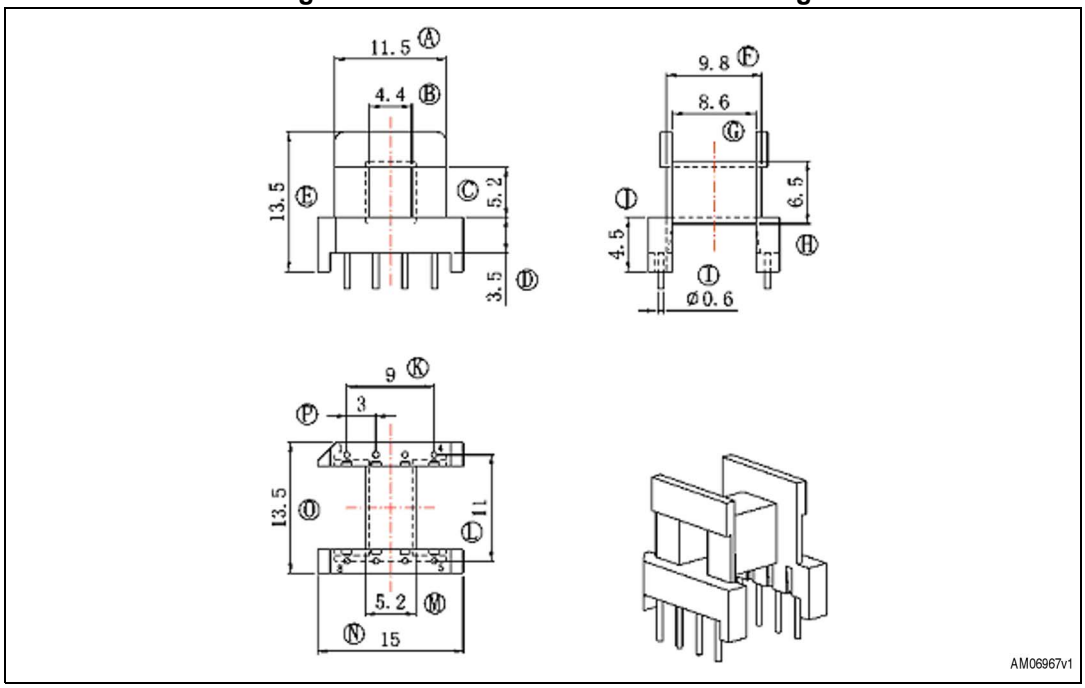
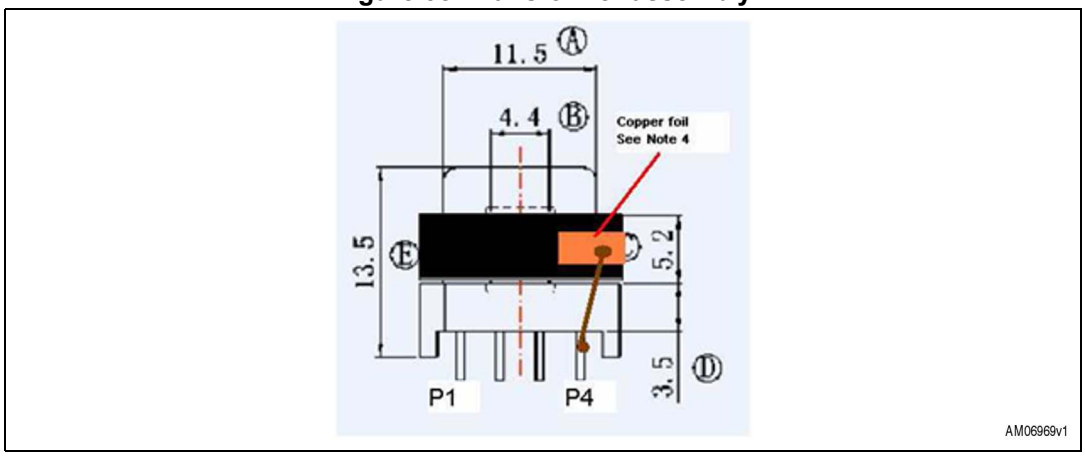


Figure 58. Transformer assembly



7.2 Electrical specifications

1. BOBBIN: EE16 (4 +4 pin)
2. CORE: EE16 AL:1140 +/-25%nH/N*N (TDK PC40 MATERIAL or equivalent)
3. Primary inductance (P1 - P2): 1.5 mH +/- 10% (at 100 kHz, 1 V)
4. Leakage inductance (P1 - P2): < 50 µH (at 100 kHz, 1 V) with other pins shorted

Figure 59. Transformer electrical drawing

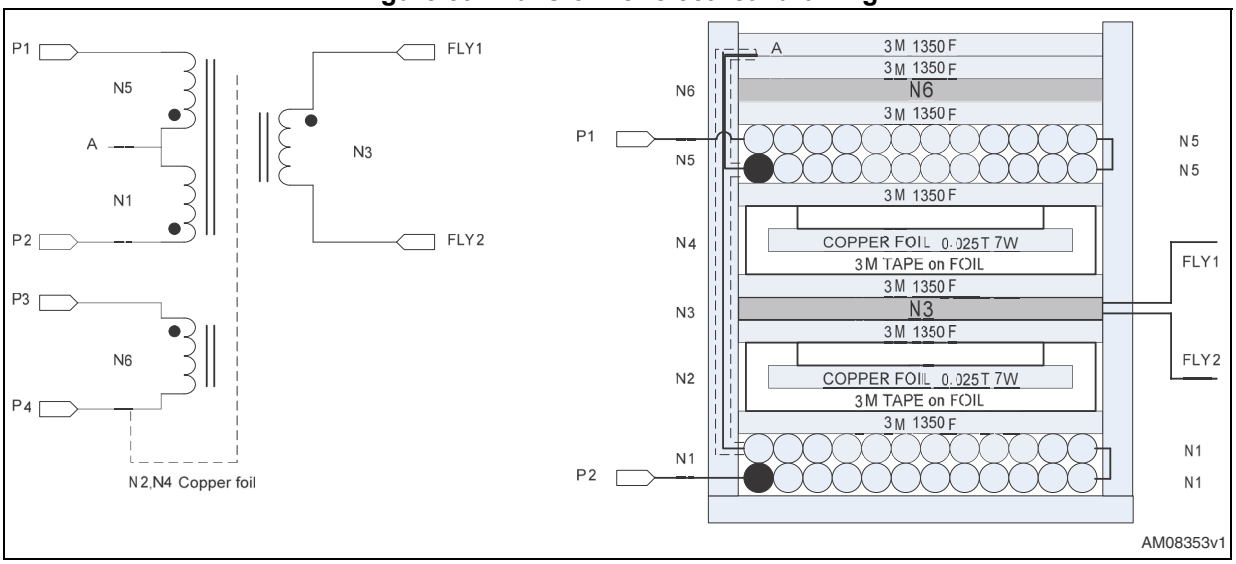


Table 4. Transformer winding data

Winding	Pins	Wire type	Wire size	# turns
N1	P2----A	2UEW	Φ 0.15 mm * 2	54T 2Layer
N2	P4	Copper foil	0.025 mmT * 7 mmW	
N3	FLY1 ---- FLY2	Triple insulation winding wire Totoku TIW-3 UL FILE no. E66483 or equivalent	Φ 0.55 mm	10T
N4	P4	Copper foil	0.025 mmT * 7 mmW	
N5	A----P1	2UEW	Φ 0.15 mm * 2	54T 2Layer
N6	P3----P4	2UEW	Φ 0.22 mm	14T

Note: 1 HIPOT: 3 KV_{AC} primary to secondary 1 min. 10 mA

2 Start winding from the pin marked "·" (especially for N5 and point A)

3 Cut off pin 5, 6, 7, 8

*4 Attach a copper foil 3M #1245 tape (4 mm width*10 mm length) to the Core,*

5 Make sure the foil maintains good contact with the ferrite core, and solder a UL xpvc wire to pin 4 as short as possible.

8 Revision history

Table 5. Document revision history

Date	Revision	Changes
19-Oct-2010	1	Initial release.
15-Mar-2013	2	Replaced part number EVLVIP27-7WLED with STEVAL-ISA120V1.