AN3258
Application note

STM8AF and STM8S series HSI oscillator calibration using LIN automatic resynchronization

Introduction

Local interconnect network (LIN) is a widely used standard for communication between various nodes present inside the electronic control unit (ECU) of a vehicle. LIN sync frame, which is defined by LIN standard, is used as a reference by the LIN slave nodes for clock synchronization. Using this technique, LIN slave nodes can calibrate the variable internal RC oscillator and use it as the system clock source. Therefore, the LIN slave node application can save the cost of using crystal or resonator oscillators.

This application note describes a method to calibrate the STM8AF and STM8S series high-speed internal (HSI) oscillator using the LIN automatic resynchronization feature of the LINUART peripheral. The calibration method is also provided with a software routine. It can be downloaded from *www.st.com*.

The user must be familiar with the LIN bus standard, STM8AF and STM8S series architecture, and the basics of C language. Detailed information about the STM8AF and STM8S series microcontroller peripheral features, hardware registers, and electrical characteristics are available in STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016) and the product datasheets.

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1.1 HSI trimming bits

STM8AF and STM8S series microcontrollers have an HSI oscillator with a nominal frequency (f_{HSI}) of 16 MHz which is factory calibrated at an ambient temperature (T_A) of 25°C and a supply voltage (V_{CC}) of 5 V. The accuracy for overall temperature and voltage range is ±5% (please refer to the device specific datasheet) which is sufficient for many applications. For a given voltage and temperature condition, the HSI oscillator frequency can be calibrated to ±1% or ± 0.5% by using calibration bits as described below and in *Figure 1*.

After a device reset, the factory calibration value at T_A = 25 °C and V_{CC} = 5 V is automatically loaded into the internal calibration register. The HSI frequency can be fine-tuned by writing the calibration bits present in the HSI clock calibration trimming register (*CLK_HSITRIMR*). The maximum number of calibration bits present is either three or four depending on the device. The calibration bits provide an additional trimming value which is added to the factory calibration value to fine-tune the HSI output frequency. The additional trimming value, written in the trimming bits, is interpreted as a signed value with two's complement representation (*see Table 1*). In the case of three trimming bits, this additional trimming value can vary from -4 (100b) to 3 (011b) and in the case of four trimming bits, this additional trimming value varies from -7 (1001b) to 7 (0111b). Thus, the additional trimming value can be added or subtracted to the factory calibration value. An increase in the trimming value causes a decrease in the HSI frequency. The frequency change per step is ±1% or ±0.5% depending on the device and number of trimming bits used (three or four). Some devices can use either three or four trimming bits which are programmable via the HSITRIM option byte.

Figure 1. STM8AF and STM8S series HSI trimming principle

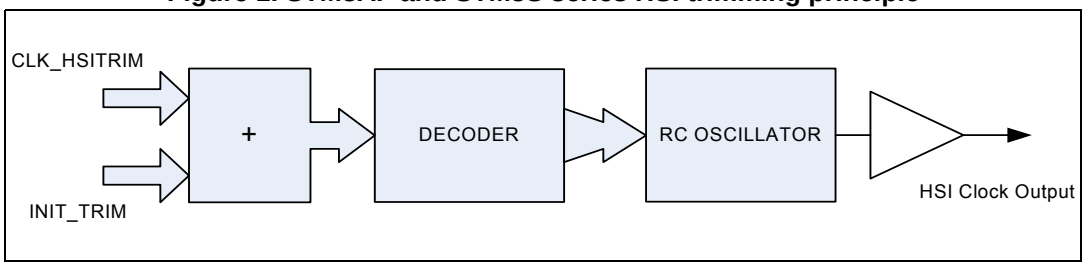


Table 1. CLK_HSITRIMR values and binary two's complement representation

3-bit trimming value		4-bit trimming value	
Decimal value	Binary two's complement value	Decimal value	Binary two's complement value
3	011b	7	0111b
2	010b	6	0110b
1	001b	5	0101b
0	000b	4	0100b
-1	111b	3	0011b
-2	110b	2	0010b
-3	101b	1	0001b
-4	100b	0	0000b
-	-	-1	1111b
-	-	-2	1110b
-	-	-3	1101b
-	-	-4	1100b
-	-	-5	1011b
-	-	-6	1010b
-	-	-7	1001b

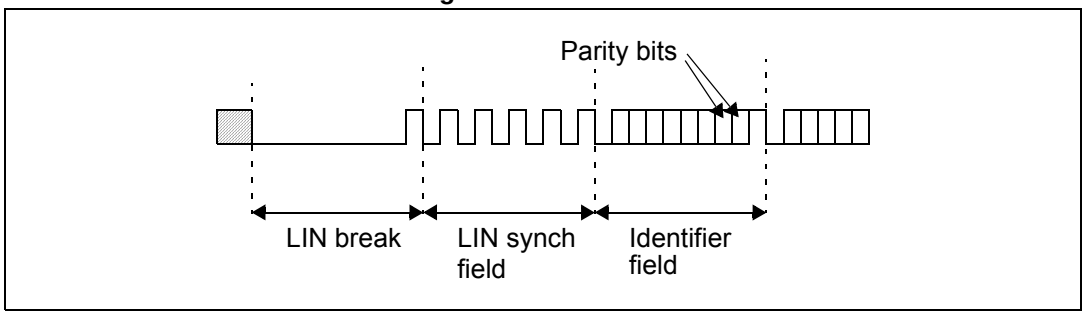
1.2 LIN automatic resynchronization

In the LIN standard, the master node initiates the communication by sending a LIN message header to the slave node. The LIN message header sent by the master node comprises three fields (see *Figure 2*):

- Break field
- Sync field
- Identifier field
  - frame identifier
  - parity

The break field is at least 13 nominal bit times the dominant value followed by a break delimiter. The sync field is a byte with a data value of 0x55. The identifier field consists of two subfields: the frame identifier and the parity. Bits 0 to 5 are frame identifier and bits 6 to 7 are the parity.

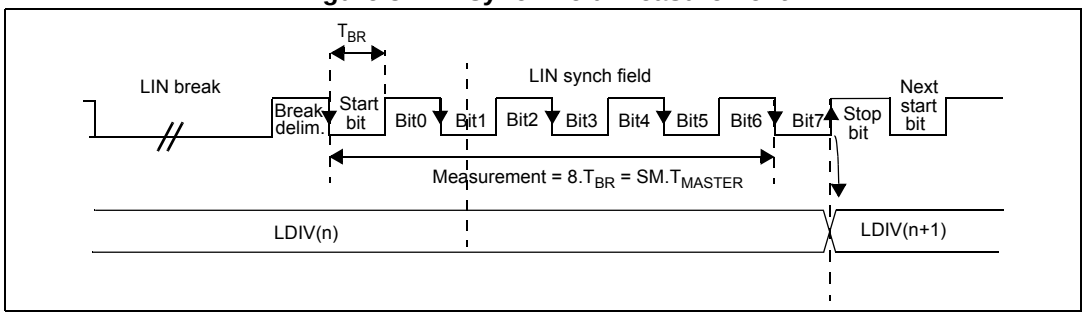
Figure 2. LIN header



Usually, the master node uses a crystal or resonator oscillator to generate the correct baud rate. The sync field byte is used by the slave node to synchronize with the master clock.

The STM8AF and STM8S series LINUART peripheral has an automatic resynchronization feature which makes use of the sync byte field to synchronize with the master baud rate. The automatic resynchronization feature measures the sync byte field and automatically adjusts the slave baud rate generator after each LIN sync field reception from the master node (see *Figure 3*).

Figure 3. LIN synch field measurement



After each LIN break reception, the time duration between five falling edges on the LIN Rx pin is sampled on the f_{MASTER} clock. The result of this measurement is stored in an internal 19-bit register called SM which is not user accessible. Then, the LIN baud rate divider (LDIV) is automatically updated at the end of the fifth falling edge.

Note: f_{MASTER} and T_{MASTER} are the respective system clock frequency and time period of the STM8AF and STM8S series slave node (please refer to the clock tree figure in STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016)) and should not be considered as the frequency of the master node.

1.3 HSI calibration method

This section explains how to calibrate the HSI oscillator using the LIN automatic resynchronization feature described above. The automatic resynchronization feature updates the LIN baud rate divider (LDIV) after each LIN sync field reception. The calibration method uses the updated LDIV factor to calculate the HSI frequency variation, under current conditions, using the equations below.

Equation 1

$$f_{HSIDIV""} = \frac{f_{HSI}}{HSIDIV}$$

Where, f_{HSI} = nominal HSI frequency of 16 MHz and HSIDIV is the HSI prescaler factor programmed in the CLK_CKDIVR register.

The LIN baud rate is programmed by software after writing the LDIV_NOM value into the BRR1 and BRR2 registers.

Equation 2

$$Baudrate = \frac{f_{MASTER}}{LDIV\_NOM}$$

As slave node uses the HSI clock as f_{MASTER}, $f_{MASTER} = f_{HSIDIV}$.

Equation 3

$$LDIV\_NOM = \frac{f_{MASTER}}{Baudrate}$$

Equation 4

$$f_{MESASURED} = LDIV\_MEAS \times Baudrate$$

After the LIN sync field reception, the LIN baud rate divider is measured by the automatic resynchronization (LDIV_MEAS) and it is automatically loaded into the BRR1 and BRR2 registers. These actions keep the same baud rate under varying HSI oscillator frequency conditions. The LDIV_MEAS factor multiplied by the baud rate gives the current HSI frequency ($f_{MEASURED}$).

Where, LDIV_MEAS = LDIV measured after automatic resynchronization.

The difference between the $f_{REFERENCE}$ and $f_{MEASURED}$ gives the variation of HSI oscillator frequency.

Equation 5

$$\Delta_{FREQUENCY} = f_{MASTER} - f_{MEASURED}$$

Where, $\Delta_{FREQUENCY}$ is the HSI oscillator frequency variation.

1.4 HSI calibration routine

The calibration routines are written in C language. They include STM8S/AF standard peripheral library (STSW-STM8069) functions.

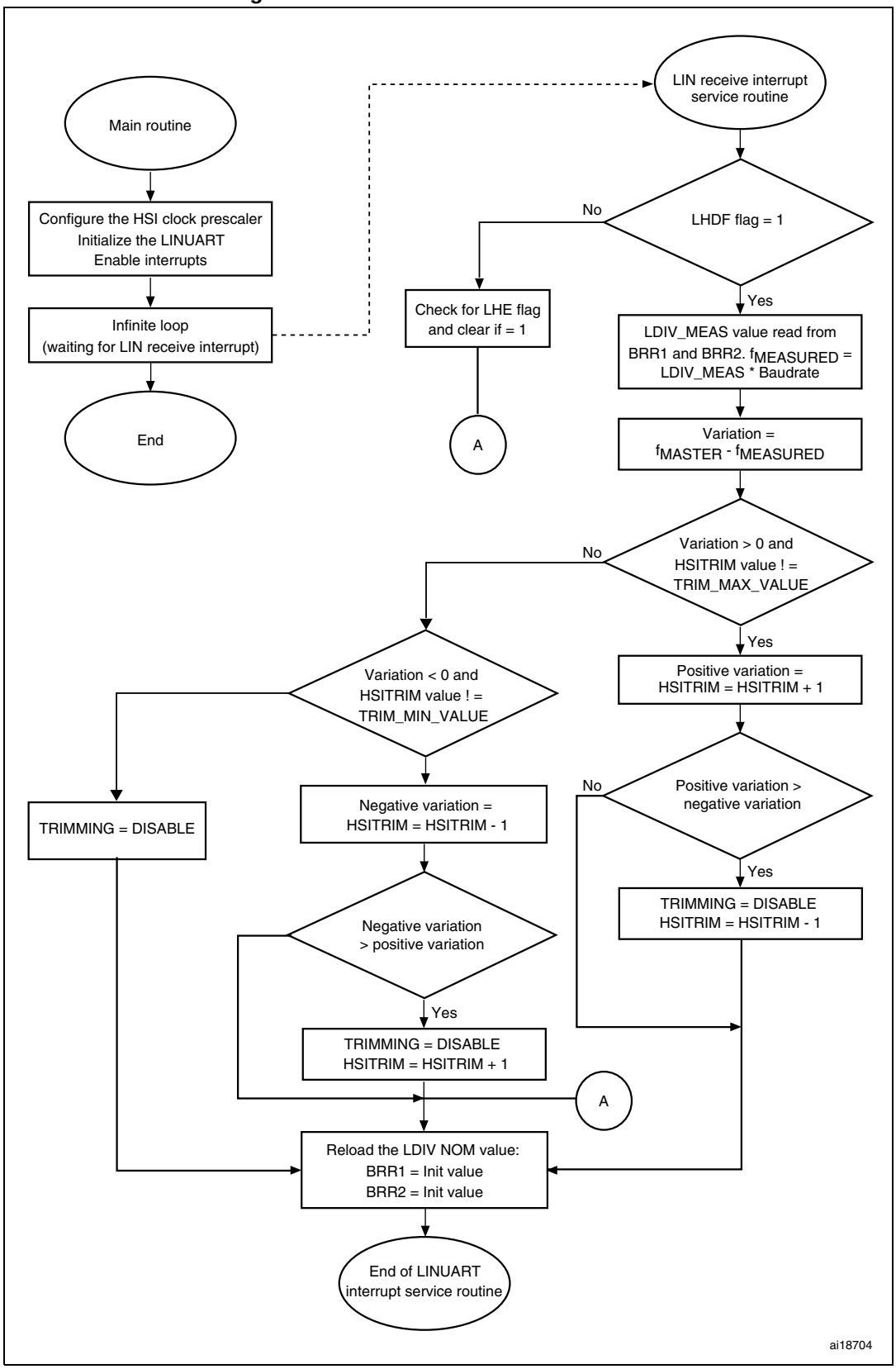
The calibration routine starts with the configuration of the HSI clock prescaler value bits, HSIDIV[1:0], in the CLK_CKDIVR register. The value programmed in the software example is HSIDIV[1:0] = 00 which means, $f_{HSIDIV} = f_{HSI/1}$ = 16 MHz. The HSI trimming bits, HSITRIM[3:0] or HSITRIM[2:0], in the CLK_HSITRIMR register are kept at reset value.

The LINUART peripheral is initialized at baud rate 19200 bps, 8 data bits, 1 stop bit and no parity. LINUART is configured in slave mode (LSLV bit =1) with the automatic resynchronization feature enabled (LASE bit = 1) and the LIN divider update method (LDUM) bit = 0. Both LIN header detection (LHDIEN) and LIN receiver (RIEN) interrupts are enabled. The LINEN bit is set to enable the LIN mode.

When a valid LIN header is received by the LIN slave, the LIN receive interrupt is generated. Inside the interrupt service routine, if the LIN header detection flag (LHDF) is set, LDIV_MEAS is read from the BRR1 and BRR2 registers (see *Figure 4*). Using *Equation 4*, $f_{MEASURED}$ is calculated. The variation of the HSI oscillator frequency ($\Delta_{FREQUENCY}$) is calculated by using *Equation 5*.

Depending on whether the $\Delta_{FREQUENCY}$ is positive or negative, the trimming value (as described in *Section 1.1: HSI trimming bits*) is written to increase or decrease the HSI oscillator frequency by one trimming step. When the next sync frame is received, the procedure is repeated to check and calibrate the HSI oscillator until the trimming value reaches the upper/lower limit or until the measured $\Delta_{FREQUENCY}$ is greater than the value measured with the previous trimming value. The maximum number of valid LIN headers required to calibrate the HSI oscillator is four if three trimming bits are used and eight if four trimming bits are used.

Figure 4. HSI calibration routine flowchart



1.5 LIN header error handling

It is possible that slave node receives an invalid LIN header or a LIN header with an error. In this case, the LIN header detection flag (LHDF) is not set and the corresponding LIN header detection interrupt does not occur but, the LIN header error (LHE) flag is set.

A LIN header error may occur under the following conditions:

1. The break delimiter is too short.
2. The sync field is not equal to 0x55 or the deviation error in the sync field is outside the LIN specification which allows a clock deviation of up to 14% between the slave and master oscillators.
3. The framing error occurs in the sync field or the identifier field.
4. A LIN header reception timeout occurs.

In the case of a LIN header error detection (LHE bit set), the LHE bit is cleared inside the interrupt service routine and the software waits for the new valid LIN header.

1.6 LIN divider update method

Three registers are managed internally by the LINUART peripheral for the automatic update of the LIN divider (LDIV). They are:

1. LDIV_NOM which stores the value written by software in the LINUART_BRR1 and LINUART_BRR2 registers.
2. LDIV_MEAS which stores the value of the LIN sync field measurement.
3. LDIV which stores the value which is used to generate the baud rate.

The LDIV can be updated from the LDIV_MEAS register after the LIN sync field measurement or from the LDIV_NOM register after a software write in LINUART_BRR1.

If LASE =1, the LDIV_MEAS is loaded automatically into LDIV after each LIN sync field measurement. The loading from LDIV_NOM into LDIV depends on the LDUM bit setting.

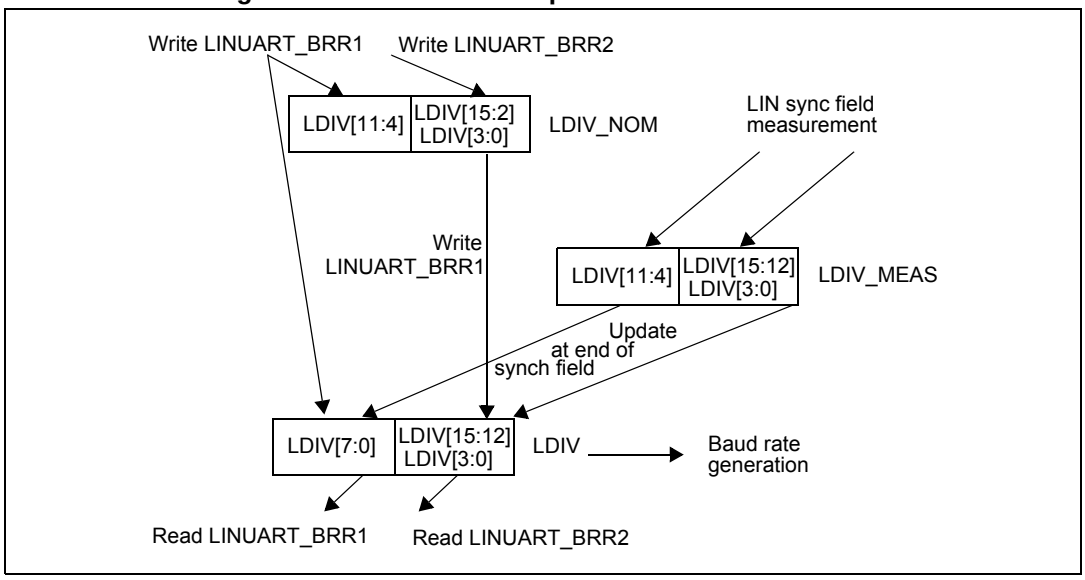
If LDUM = 1, the LDIV_NOM value is loaded automatically into LDIV register at the end of character reception (RXNE =1).

If LDUM =0, the LDIV_NOM value is loaded into LDIV after a software write into LINUART_BRR1.

If the loading from LDIV_MEAS and LDIV_NOM into LDIV occurs at the same time, LDIV_NOM has the priority.

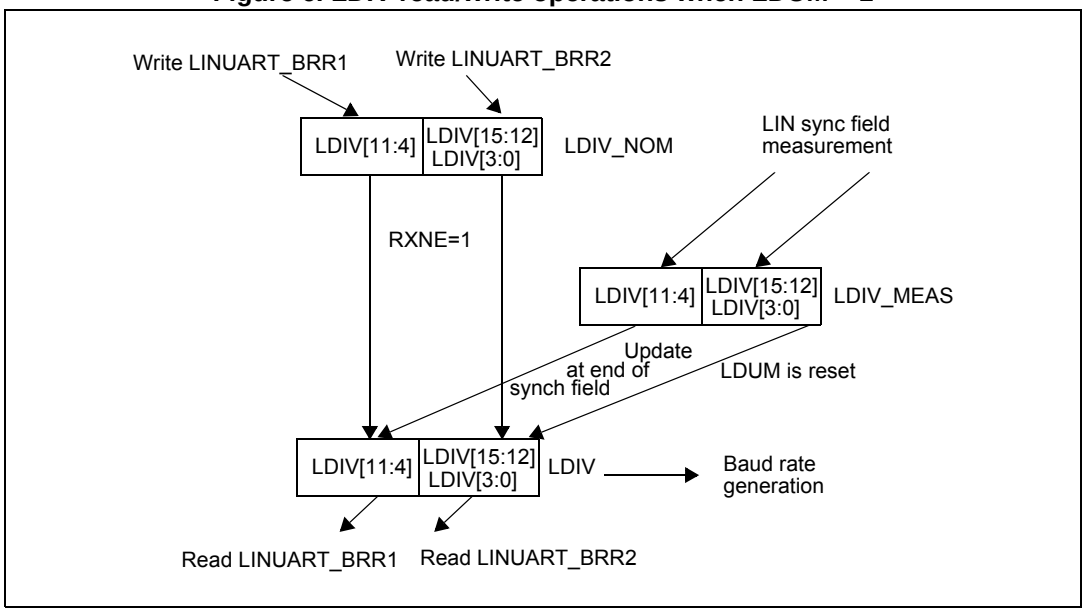
In *Figure 5*, the software example has been implemented with (LDUM = 0). After the LIN reception of the LIN header interrupt and the execution of the calibration routine, the LDIV is loaded with LDIV_NOM by writing the LINUART_BRR1.

Figure 5. LDIV read/write operations when LDUM = 0



In the case of LDUM = 1 (see *Figure 6*), the LDUM bit has to set by software before the LIN checksum reception. In this way, the LDIV_NOM is loaded into LDIV at the end of character reception.

Figure 6. LDIV read/write operations when LDUM = 1



1.7 LIN clock deviation

LIN clock deviations may be caused by the following sources:

1. Deviation due to transmitter error (DTRA): The transmitter can be either a master or a slave (in the case of a slave listening to the response of another slave).
2. Error due to the LIN synch measurement performed by the receiver (DMEAS).
3. Error due to the baud rate quantization of the receiver (DQUANT).
4. Deviation of the local oscillator of the receiver (DREC): This deviation can occur during the reception of one complete LIN message assuming that the deviation was compensated at the beginning of the message.
5. Deviation due to the transmission line (DTCL) which is generally due to the transceivers.

Total clock deviation = DTRA + DMEAS + DQUANT + DREC + DTCL

If the LINUART is to receive a character correctly, the total deviation should be <3.75%. For more details, please refer to STM8S series and STM8AF series 8-bit microcontrollers reference manual (RM0016).

2 Conclusion

The calibration method described in this application note allows the LIN slave nodes to calibrate and operate with the HSI internal oscillator (16 MHz) under variable temperature and voltage conditions.

3 Revision history

Table 2. Document revision history

Date	Revision	Changes
05-Oct-2010	1	Initial release
11-Sep-2015	2	Extended the document applicability to STM8AF and STM8S series and updated the document references accordingly. Replaced LINUART/UART1 occurrences with LINUART.