Gate to cathode capacitor, impact on triac immunity and reliability

Introduction

Triacs and SCRs are power semiconductors, which are usually directly connected to the grid line. As it is well known, the AC grid voltage can be highly perturbed by important voltage variation during very short times, for example, mechanical relay contact bounce, universal motor disturbances. Several electromagnetic standards describe how appliances have to be tested to check their immunity to such events. For example, the IEC 61000-4-4 standard gives the test procedures and immunity requirements respectively for fast transient voltages.

To increase power-semiconductor device immunity, most designers add a capacitor across the power device control terminal (the gate for SCRs or triacs) and its reference terminal (K or A1 respectively for SCRs and triacs). This capacitor helps stabilize the control terminal potential and so is believed to help increase resistance to fast voltage rises (dV/dt). As this capacitor is also placed between the power device and the control circuit, which could be a logic gate or a microcontroller unit (MCU), it acts as a filter on the path from the line to the sensitive control circuit, and helps filter the noise coming from line disturbances.

This paper demonstrates why a gate to the cathode capacitor is not efficient to improve triac immunity to fast voltage transients, especially for nonsensitive devices. This application note demonstrates that such capacitors can increase the risk of failure for repetitive or accidentally high dI/dt.

The results presented in this application note have been produced over a considerable period of time. Some products, which are used as examples to present these results, may no longer be available. However, the results presented apply to all classes and types of product, and thus are equally applicable to similar products available in the market.

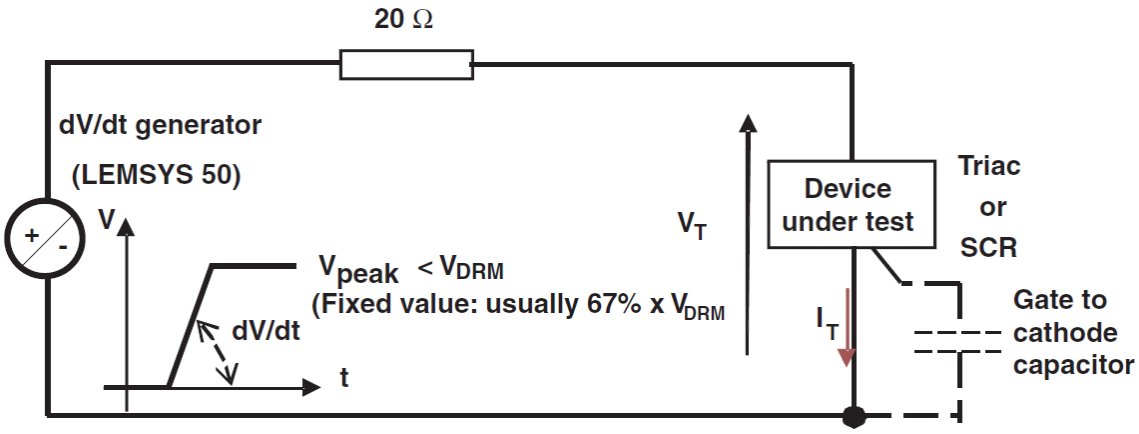
1 Gate to cathode capacitor, impact on dV/dt immunity

1.1 dV/dt test method

To characterize device immunity, semiconductor companies give the maximum dV/dt rate that can be applied across a device without a risk of triggering it.

The test schematic features a dV/dt generator, which applies a voltage-versus-time linear slope (see Figure 1). The test equipment detects if the voltage across the DUT (device under test) decreases below a given threshold. For a given dV/dt level, if the device voltage drops below this threshold, this means that the device has switched on. The DUT capability is then lower than this dV/dt rate. The dV/dt parameter specified in the device datasheet is then the minimum rate that all devices were able to withstand during the tests.

Figure 1. dV/dt test simplified schematic



The dV/dt parameter is usually measured under the following conditions:

- Peak applied voltage = 67% of V_{DRM}
- Maximum junction temperature (125 °C most of the time)
- Gate open

These test conditions are the worst case, as the dV/dt immunity decreases if both the junction temperature and the impedance between G and K increase. The following figures give an example of a 600 V SCR dV/dt measurement. A 402 V peak voltage is applied, as it represents 67% of the specified V_{DRM}. In Figure 2, the device remains off. There is no current increase. In Figure 3, the same device switches on approximately 2 µs after the voltage reaches its peak and stable level. According to these two results, it could be said that the tested SCR is able to withstand a 150 V/µs rate.

Figure 2. **600 V SCR test with a 150 V/µs slope**

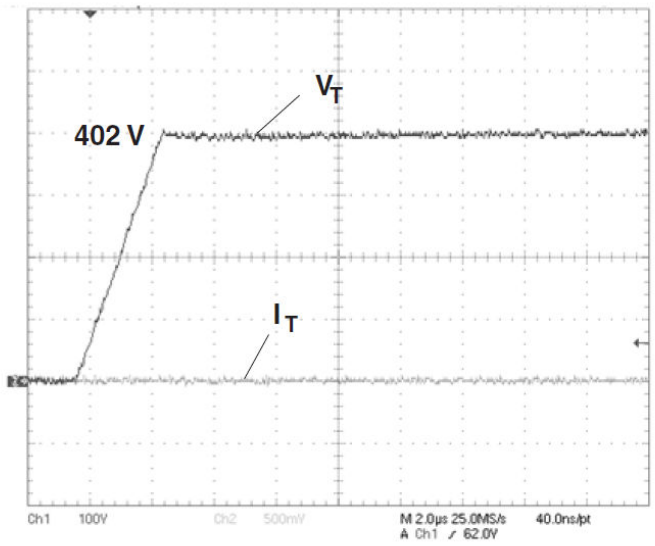
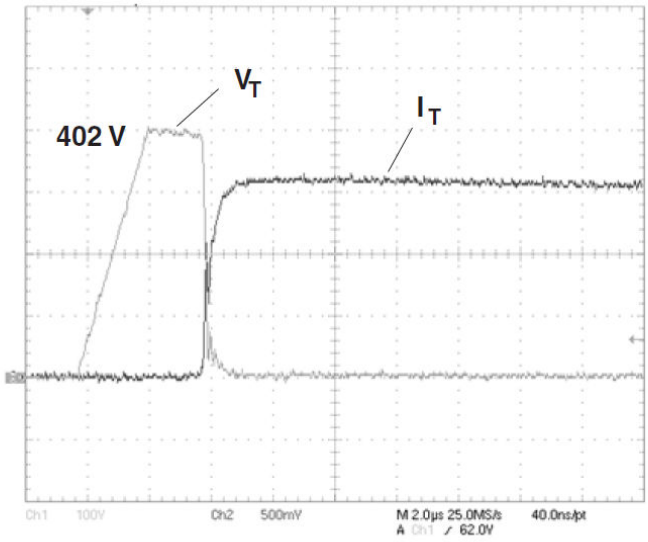


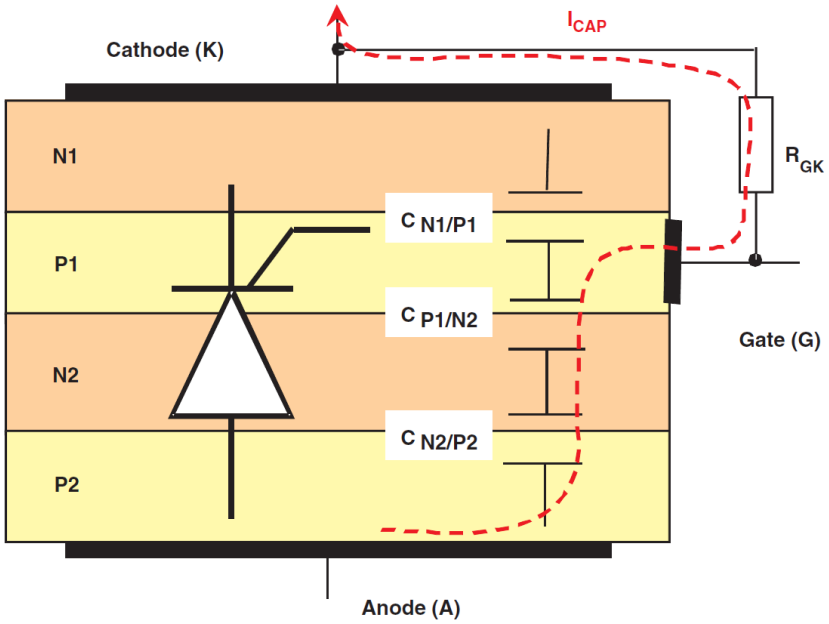
Figure 3. **600 V SCR test with a 160 V/µs slope**



1.2 dV/dt improvement for SCR

To understand why a semiconductor can be triggered by a dV/dt slope applied across its terminals, it should be kept in mind that semiconductor devices are composed of several silicon layers. An SCR features four layers, alternatively doped by holes (P area) or by electrons (N area). Each PN junction presents a spurious capacitance (see Figure 4). When a voltage slope is applied, a spurious capacitive current (I_{CAP}) is induced by these capacitances. This current can then flow to the cathode through the P1-N1 junction and cause the device switch-on. To solve this issue, an impedance, for example a resistor (refer to gate to cathode resistor in Figure 4), could be added between the gate and cathode terminals. The spurious capacitive current is then shunted and avoids the device being triggered.

Figure 4. **SCR simplified silicon structure and spurious capacitive current**



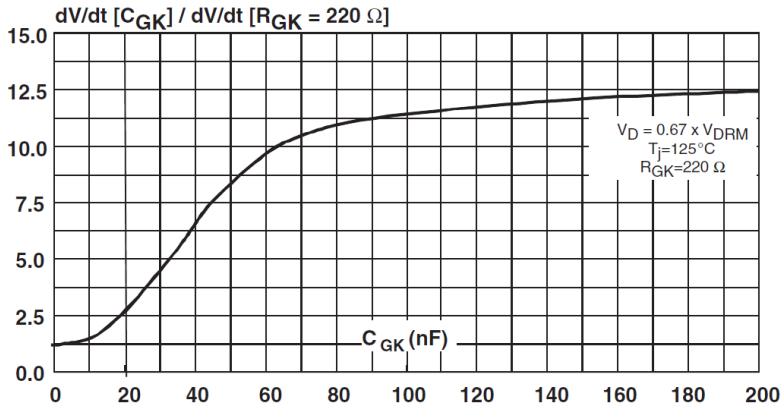
A better solution could be found if a capacitor is used instead of a resistor. A high-voltage gate to the cathode capacitor is not necessary because only a low voltage (V_{GK} is around 1 V typically) is applied across this capacitor.

Figure 5 shows the typical relative dV/dt increase versus gate-cathode capacitance for an 8 A sensitive SCR series (I_{GT} max = 0.2 mA). The SCR dV/dt could be improved more than ten times with a 100 nF gate to the cathode capacitor.

It should be noted that a gate to cathode resistor is still used in parallel with the gate to cathode capacitor to discharge it after gate current removal.

For non–sensitive SCRs (I_{GT} above around 5 mA), a gate to the cathode capacitor does not improve dV/dt immunity a lot. Indeed, these devices already feature a very low internal gate to the cathode resistor. So, adding any external component is not very efficient to shunt the spurious capacitive current.

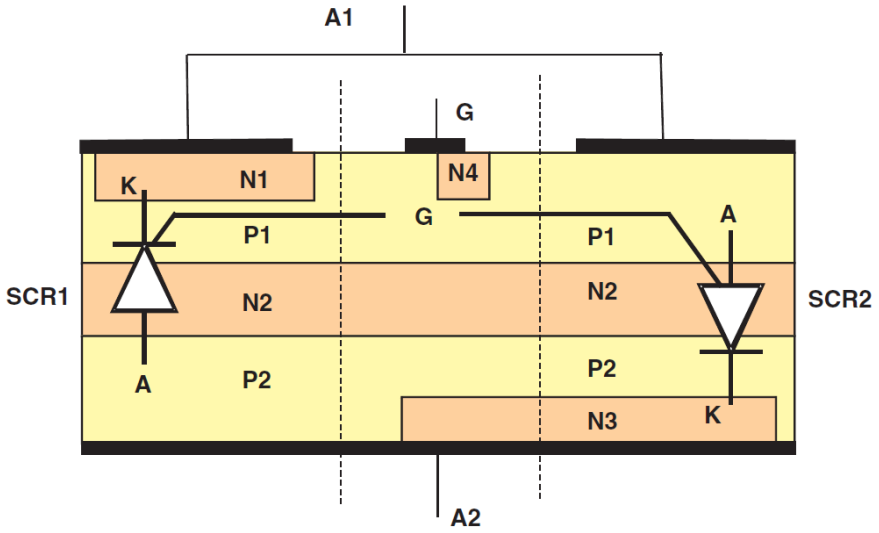
Figure 5. **SCR dV/dt increase versus added gate to cathode capacitor**



1.3 Behavior of triacs regarding dV/dt

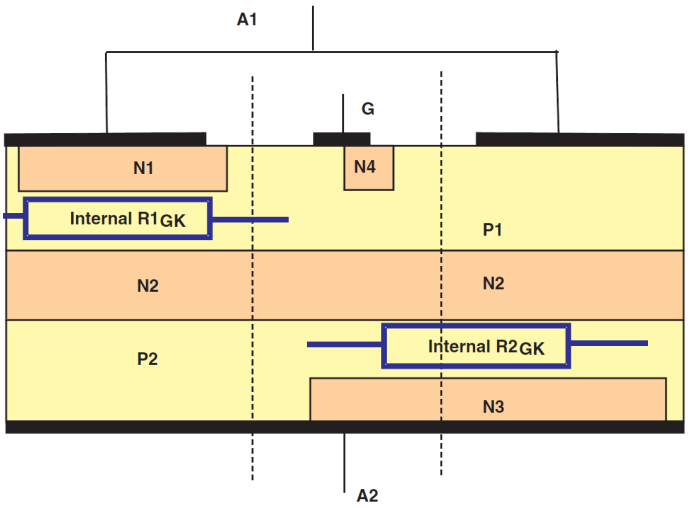
A triac silicon structure differs from an SCR structure. First, triacs can conduct current in both directions. A triac is equivalent to two SCRs back-to-back with a common gate. The real gate area of the reverse SCR is on the opposite side of the gate terminal connection (see Figure 6).

Figure 6. Triac simplified silicon structure



This device can turn on with dV/dt slope in direct or in reverse. When a positive dV/dt static is applied on A2, the device SCR1 can improve its immunity with a gate to cathode capacitor or gate to cathode resistor. With this polarity, the device is equivalent to an SCR. It is really efficient for a sensitive triac, which has a high value internal $R1_{GK}$ (see Figure 7). The external gate to cathode capacitor or gate to cathode resistor is then in parallel and improves immunity. When the positive dV/dt slope is applied on A1, there is no possibility to reinforce this immunity. The gate electrode is on the opposite side and there is no possibility to add an external component in parallel with the internal $R2_{GK}$.

Figure 7. Triac simplified silicon structure with internal gate to cathode resistor shown



The gate to the cathode capacitor thus has a totally different impact according to the bias voltage. Table 1 and Table 2 give, for example, some dV/dt characterization results respectively for one triac (16 A, 600 V, 10 mA I_{GT} device) and for another triac (16 A, 600 V, 35 mA I_{GT} device).

For the more sensitive device (I_{GT} = 10 mA), a 100 nF gate to the cathode capacitor improves the dV/dt capability by a factor of 10, but only for positive voltage bias. For the other devices (I_{GT} = 35 mA), the 100 nF gate to the cathode capacitor does not have any impact on the dV/dt capability.

So, a gate to the cathode capacitor could be useful only for sensitive devices, but only for half the time for appliances working on AC voltage. Experiments have shown that a gate to the cathode capacitor could improve the immunity level during IEC 61000-4-4 standard tests for the more sensitive device (I_{GT} = 10 mA) but not for the 35 mA I_{GT} device, as shown in Section 1.4.

Table 1. dV/dt characterization at 125 °C and V_{peak} = 402 V for sensitive triac device (I_{GT} = 10 mA)

		Without gate to cathode capacitor		With gate to cathode capacitor (100 nF)	
		Sample 1	Sample 2	Sample 1	Sample 2
dV/dt (V/µs)	Direct	360	450	2260	1900
	Reverse	800	760	800	760

Table 2. dV/dt characterization at 125 °C and V_{peak} = 402 V for less sensitive triac device (I_{GT} = 35 mA)

		Without gate to cathode capacitor		With gate to cathode capacitor (100 nF)	
		Sample 1	Sample 2	Sample 1	Sample 2
dV/dt (V/µs)	Direct	2350	1850	2350	1850
	Reverse	2750	1950	2750	1950

1.4 Behavior of triacs to EFT (electrical fast transient)

To compare immunity between several triacs (Snubberless and logic level) with and without gate to cathode capacitor, tests have been carried out in the following conditions (see Figure 8):

- An X2 1 nF capacitor is connected at the line input
- The PCB is 10 cm above the reference plane
- The triac A2 terminal is linked to a 25 W light bulb (resistive loads are chosen to reduce dI/dt rates in case of firing).
- The gate could be left open, or connected to the A1 terminal through an external gate to the cathode capacitor or connected to A1 through a 100 Ω R_G in series with a gate to the cathode capacitor
- No snubber circuits are added across the triacs
- Ambient temperature: 25 °C
- The burst generator is programmed as required in the IEC 61000-4-4 standard (15 ms burst duration, 3 Hz burst frequency, 5 kHz spike frequency, one second test duration).

Figure 8. IEC 61000-4-4 test configuration

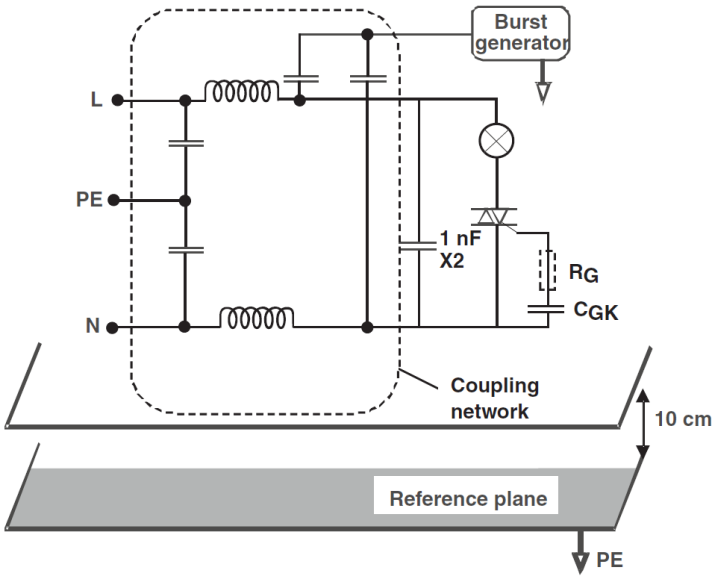


Table 3 and Table 4 give the test results for the two previous sample triacs (logic level and Snubberless) with and without gate to cathode capacitor. A burst test is carried out for each coupling mode (to line, to neutral, and to line and neutral). Only the minimum burst level before turn-on, for all coupling modes, is recorded in these two tables.

Table 3. IEC 61000-4-4 tests results with logic level triac - sensitive device (I_{GT} = 10 mA)

	Without gate to cathode capacitor		With gate to cathode capacitor (100 nF)		With R_G (100 Ω) and C_{GK} (100 nF)	
	Sample 1	Sample 2	Sample 1	Sample 2	Sample 1	Sample 2
Minimum held burst level (kV)	1.3	1.3	3.6	3.5	3.3	3.2

Table 4. IEC 61000-4-4 tests results with Snubberless triac - less sensitive device (I_{GT} = 35 mA)

	Without gate to cathode capacitor		With gate to cathode capacitor (100 nF)		With R_G (100 Ω) and C_{GK} (100 nF)	
	Sample 1	Sample 2	Sample 1	Sample 2	Sample 1	Sample 2
Minimum held burst level (kV)	> 4.5	> 4.5	> 4.5	> 4.5	> 4.5	> 4.5

These experimental results show that there is no immunity improvement if a gate to the cathode capacitor is added to Snubberless triacs. Indeed, the immunity level is very high and above our burst generator capability (4.5 kV).

On the other hand, logic level triacs withstand a lower immunity level compared to Snubberless devices. This level is lower without the gate to the cathode capacitor. A 100 nF gate to the cathode capacitor improves almost by 3 the triac immunity. But gate to cathode capacitor lowers triac reliability (refer to Section 1: Gate to cathode capacitor, impact on dV/dt immunity).

To keep the gate to the cathode capacitor benefits without lowering system reliability, one solution is then to add a resistor (R_G) in series with the gate to the cathode capacitor. The immunity level is then similar to that with the single gate to the cathode capacitor. Such a resistor comes for free, since the gate resistor, used to limit the control circuit output current, can be used as R_G.

Usually, logic-level triacs are driven directly by a microprocessor. MCU 4-4 immunity behavior is improved by adding an RCR filter. A comparison with and without filter has been performed with an ACST (I_{GT} max = 10 mA, 6 A on-state rms current) and an STMicroelectronics MCU. A capacitor is connected between two resistors and A1. One of these resistors (240 Ω) is connected to the output of the MCU and the other one (50 Ω) to the ACST gate. This can improve the level of immunity up to 600 V according to coupling, polarity, and MCU output configuration. For instance, with an MCU open drain output configuration, the negative voltage applied on line 4-4 immunity is 3.9 kV with a filter compared to 3.3 kV without a filter.

2 Gate to cathode capacitor, impact on dI/dt capability

As well as being almost ineffective in improving triac immunity, a gate to the cathode capacitor has a major drawback when operating with triacs. A gate to the cathode capacitor significantly decreases the triac dI/dt capability. For example, Table 5 gives the experimental results obtained in repetitive operation for a standard triac (1 A, 600 V, 5 mA I_{GT}). Table 5 clearly shows that the lifetime of the device is drastically reduced when a 100 nF or 10 nF gate to the cathode capacitor is added. On the other hand, the triac dI/dt capability remains if a resistor is added in series with a gate to the cathode capacitor.

Table 5. Repetitive dI/dt tests results with a standard 1 A triac

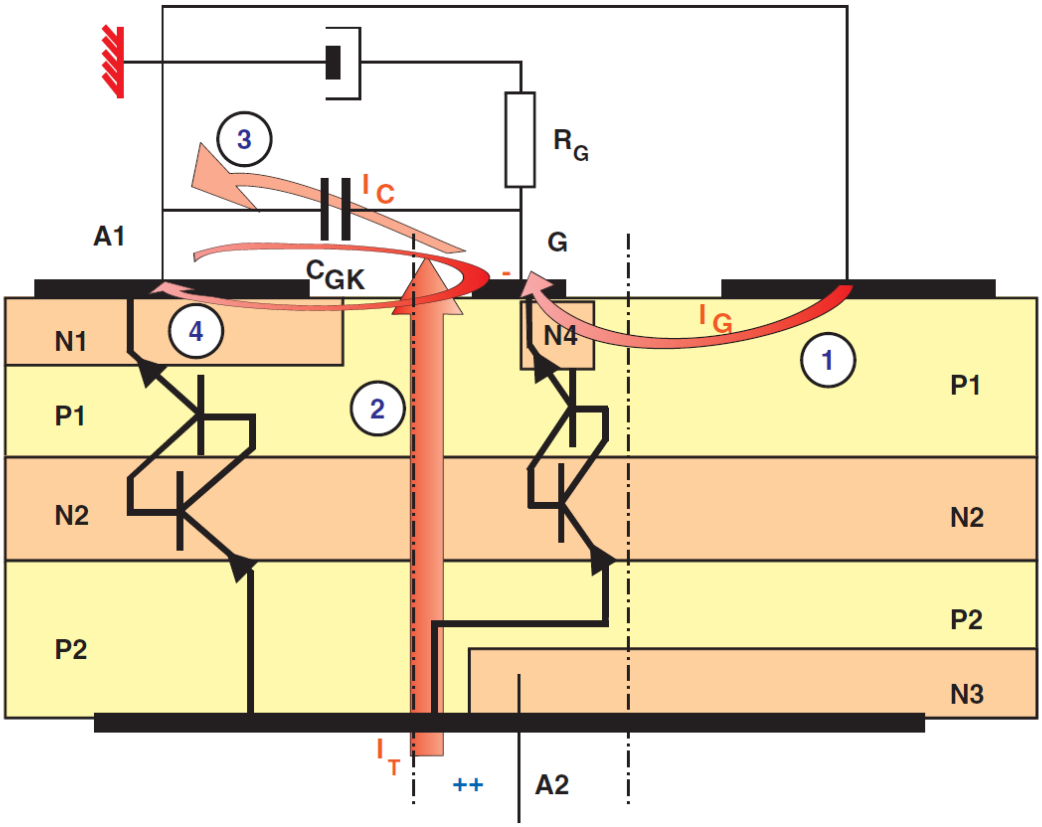
	Without a gate to cathode capacitor	With gate to cathode capacitor (100 nF)	With R_G (50 Ω) and C_G (100 nF)
dI/dt (A/µs)	30	30	30
I_{peak} (A)	3.5	3.5	3.5
Number of cycles (millions of cycles)	50	0.1	50
Results	0 failed / 20	8 failed / 10	0 failed / 10

The high density current during charge and discharge of the capacitor explained the poor life time with a gate to the cathode capacitor. In the case of an R_G-C_G circuit, the resistor in the series limited this density of current. Triac dV/dt immunity is improved with this circuit and dI/dt capability is not decreased.

The Figure 9 gives the different operating steps when a triac is switched on in quadrant 2 (V_T > 0 and I_G < 0) with a gate to the cathode capacitor. The event sequence is as follows:

1. The triggering current is first sunk from the gate by the control circuit
2. The pilot SCR is turned on. This pilot SCR is implemented by the P2-N2-P1-N4 layers. It is not the same SCR that is on at the end of this switching-on process
3. A high inrush current circulates through the gate to cathode capacitor due to the pilot SCR turn on (without a gate to cathode capacitor, the gate current would be limited by the gate resistor R_G)
4. The gate to the cathode capacitor is discharged after the main SCR turn-on. This SCR is implemented by the P2-N2-P1-N1 layers. This causes a high peak gate current and can damage the triac.

Figure 9. **Sequence of events during triac switch-on in quadrant 2**



Even if the triac is driven in zero voltage switch mode, a spurious turn-on could appear and a high dI/dt could run through the pilot SCR. A gate to the cathode capacitor could increase the failure rate as explained above. For example, for the sensitive logic level triac described in Section 1.4: Behavior of triacs to EFT (electrical fast transient), non-repetitive dI/dt capability robustness in Q2 is divided by around 2 with a gate to the cathode capacitor: 360 A/µS with C_{GK} = 200 nF and 670 A/µs without gate to cathode capacitor.

This behavior is not linked to the triac technology but directly linked to the internal device. So, whatever the technology, a gate to the cathode capacitor decreases dI/dt capability in repetitive or in accidental mode.

3 Conclusion

To increase power semiconductor device immunity to fast transient voltages it is quite common to add a capacitor between the control terminal (gate or base) and the drive reference terminal (source, emitter, cathode, or A1 terminal). For SCRs, the drive reference is the cathode, K. A gate to the cathode capacitor is then usually added with very sensitive devices and could be very useful to increase SCR immunity to dV/dt.

This application note shows that as well as being almost ineffective in improving triac immunity, a gate to the cathode capacitor has a major drawback when operating with triacs. Such a capacitor increases the failure rate when repetitive dI/dt rates are applied at turn-on or in the case of spurious turn-on with high dI/dt.

Explanations of silicon structure behavior during turn-on show the supplementary stress due to a gate to the cathode capacitor irrespective of technology choice. This shows that such capacitors should be removed from triac designs.

Revision history

Table 6. **Document revision history**

Date	Revision	Changes
27-Mar-2012	1	Initial release.
17-Jan-2024	2	Minor text changes.

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