Power MOSFET technology gate current needs in a synchronous buck converter

Introduction

High frequency converters and applications require the best driver-MOSFET trade-off in terms of dynamic parameters to optimize the turn-on and turn-off transients. Power MOSFET technology also plays an important role in minimizing dynamic losses and improving system efficiency.

In this document, the full characterization of Power MOSFET gate current is realized by bench tests and OrCAD® simulation results, focusing on the impact of Power MOSFET technology on gate current behavior.

Ever increasing system switching frequency pushes designers and converter engineers to optimize semiconductor technology, improving device switching behavior and system efficiency. In fact, the higher the switching frequency, the larger the switching and dynamic losses; in these conditions, the best trade-off between the driver and Power MOSFET is mandatory to enhance the overall converter performance.

Power MOSFET gate current behavior during switching transients plays an important role in establishing a good trade-off between Power MOSFET and driver performance.

In this document, Power MOSFET gate current characterization is performed through bench tests and simulations (by Cadence® OrCAD Capture) on a single-phase synchronous buck converter, allowing a full understanding of the impact of the silicon technology on device gate current.

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1 Synchronous buck converter description

1.1 Topology and theory of operation

The platform used for the gate current characterization is a single-phase synchronous buck converter. In *Figure 1*, the basic schematic is depicted, where S1 is the control FET (or high-side FET) and S2 is the synchronous FET (or low-side FET). In the same image, it is also shown that the Power MOSFET gate signals are provided by the "control unit" in a synchronous way: S1 and S2 cannot be in an ON state simultaneously, avoiding the creation of a low-resistance path between the input voltage (V_{IN}) and G_{ND} (shoot-through or cross-conduction), generating a spurious power dissipation worsening overall efficiency. L and CO form the output filter (low-pass filter), which generates a DC voltage from a square-wave signal on the low-side drain (so-called phase node).

Figure 1. Single phase synchronous buck converter topology
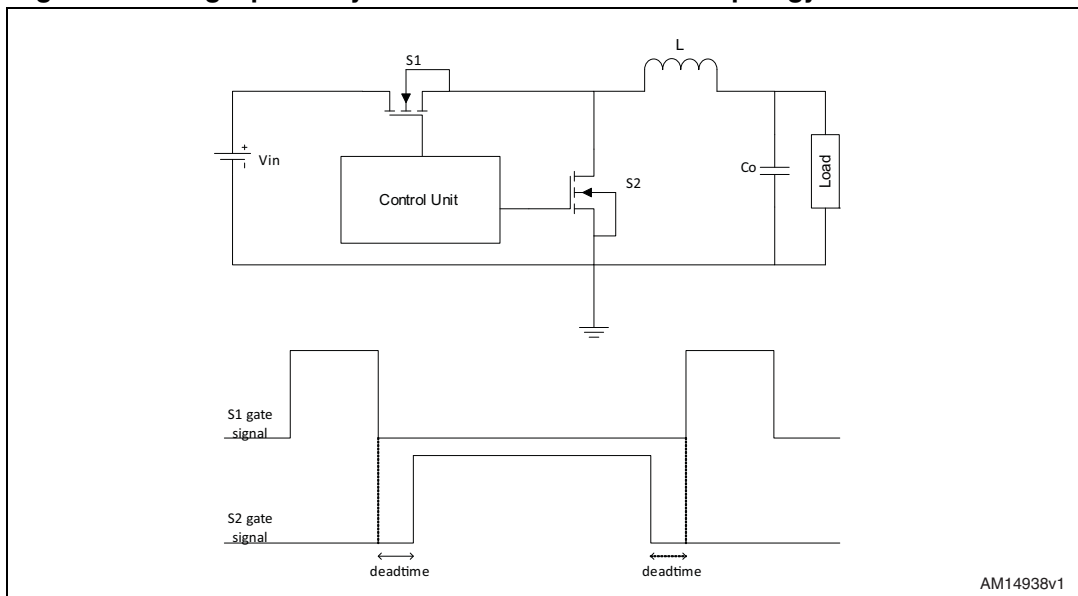
The synchronous buck converter is a closed-loop topology as the output voltage is compared firstly with a reference voltage, producing an error signal; this voltage is then compared to a sawtooth signal, at the desired switching frequency (fSW) (integrated in the control unit) to switch on and off the Power MOSFETs. In this way, the output voltage is regulated when line or load changes occur.

Together with the output voltage regulation, the control unit provides complete logic control and protection (overcurrent, overvoltage, undervoltage, etc.…).

When S1 is on, the current in the output coil increases linearly:

$$\left(\frac{dI}{dt} = \frac{V_{IN} - V_{OUT}}{L}\right)$$

and $V_L = V_{IN} - V_{OUT}$. During the deadtime (t_{df}), the energy store in L discharges through the body-drain diode of S2 till its gate-source signal becomes high. Therefore, the load current diverts from the body-drain diode to the channel ($V_{DS,ON} \ll V_{F,DIODE}$). Finally, both gate signals are low and the body-drain diode is forward-biased, allowing the load current flow.

During the deadtime and before the HS turn-on, the LS device must remove the charge stored in the LS body-drain diode (reverse recovery charge process) before sustaining drain-source voltage. Therefore, the body-drain characteristics, in terms of reverse recovery current and charge, seriously impact the Power MOSFET switching behavior and converter power losses, especially when the converter switching frequency rises up.

In a synchronous buck converter, the low-side drain is subjected to fast positive/negative slopes and high voltage spikes, which can exceed the low-side absolute maximum voltage, degrading the Power MOSFET reliability up unto its failure. Therefore, the right Power MOSFET choice and system configuration, device placement on the board, and the optimization of the stray inductances and parasitic, allow an important phase node spike reduction, improving the converter performance.

If t_{ON} is the HS conduction time and T_S the switching period, the converter duty cycle is defined as:

Equation 1

$$D = \frac{t_{ON}}{T_S}$$

So, the input-output relationship of a buck converter is given by:

Equation 2

$$V_{OUT} = D \bullet V_{IN}$$

1.2 Low-side switching transients analysis

The low-side device works as a "synchronous rectifier" because its on-time interval is synchronized to the high-side FET on-time; moreover, it works alternatively in an OFF state (body-drain diode forward biased during deadtime) or in third quadrant ($V_{DS} < 0$, $I_D < 0$), as the load current flows from source to drain.

Figure 2. HS/LS waveforms during LS turn-off
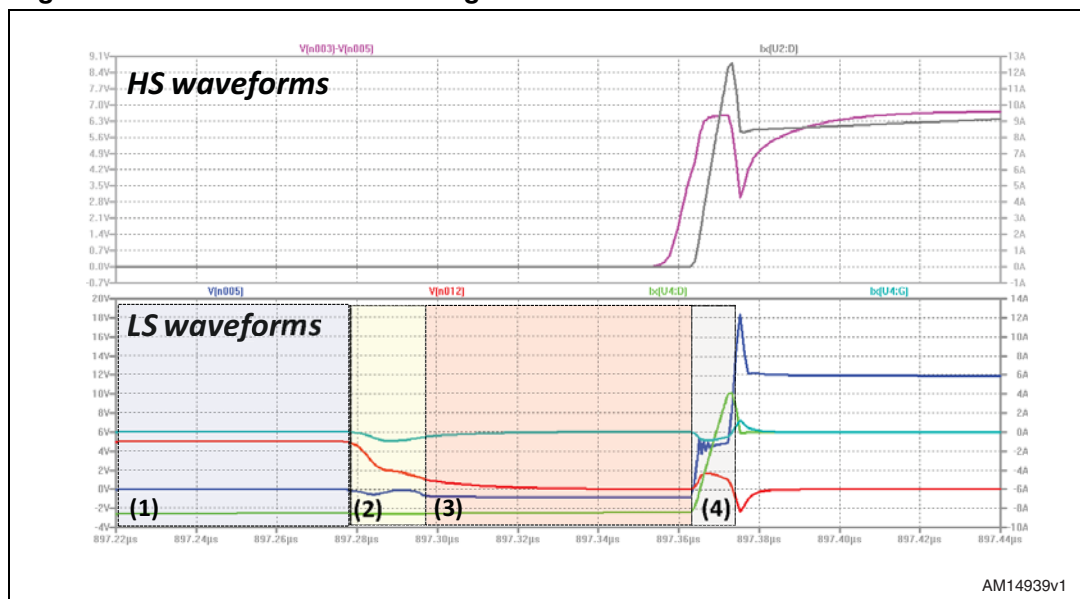
In these conditions, it is interesting to analyze the switching transients.

In *Figure 2*, the HS and LS waveforms during LS turn-off are reported. The top half of the image shows HS V_{GS} (purple trace) and I_D (grey trace), while the bottom half shows LS V_{GS} (red trace), V_{DS} (blue trace), I_G (light blue trace) and I_D (light green trace).

The main LS turn-on steps are analyzed in detail, as follows:

1. Low-side FET is in an ON state (in this case, $V_{GG} = 5$ V), with load current flowing from source to drain (green trace). At the end of (*1*), the driver begins to turn off the FET.

2. V_{GS} goes down from V_{GG} to V_{th} and the gate current becomes negative and starts to remove the charge stored in the device intrinsic capacitances. At the end of (*2*), the gate-source voltage becomes equal to the threshold voltage ($V_{GS} = V_{th}$): so, the gate current is dropped to low values (intrinsic caps are discharged) and the load current diverts from the Power MOSFET channel to the body-drain diode.

3. During deadtime, the LS FET is in an OFF state ($V_{GS} = 0$), V_{DS} becomes negative ($V_{DS} = -V_{F,DIODE}$) and the load current flows through the body-drain diode. As a consequence, minority excess charge in both diode regions is created.

4. The LS current decreases linearly, while the HS current increases linearly in direct proportion to the fall of the LS FET current. To completely turn off the LS device, the excess stored charge in its body diode must be removed: so, the reverse recovery process generates an extra-current (I_{RR}), which adds to the HS current. The maximum HS current peak is, therefore, given by:

    $I_{D,HS} = I_{LOAD} + I_{RR}$
    The spurious bouncing on the LS gate signal is caused by the voltage drop across package parasitic inductances (especially, source inductance), related to negative dI/dt (the current is falling to zero). Obviously, the bigger the parasitic inductance (package, wire bonding and layout) the higher the bouncing amplitude. At the same time, the low-side V_{DS} is fixed by the parasitic inductance and $dI_{D,LS}/dt$.

During device turn-off, the gate current is negative, because of the Power MOSFET intrinsic capacitances discharge process. The current is sunk by the driver, with a speed linked to the gate voltage level and overall gate resistance ($R_{G,TOT} = R_{G,INT} + R_{DR,SINK}$).

It is important to underline that, at LS turn-off, the driver, external and intrinsic FET gate resistance should be as low as possible in order to minimize the device shoot-through risks, caused by high dv/dt across drain-source, coupled to the gate signals through Miller capacitance in *Figure 3*.

Figure 3.   Shoot-through event caused by dv/dt
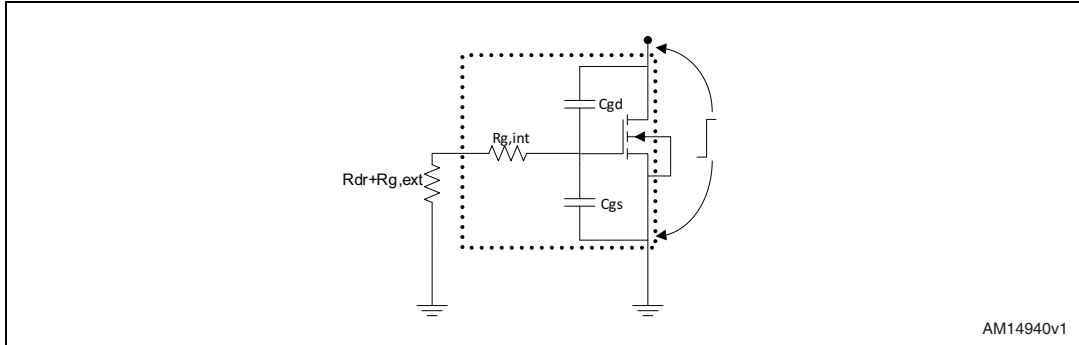
For reference, in *Figure 4* the relevant waveforms for the LS turn-on process are reported.

Figure 4.   HS/LS waveforms during LS turn-on
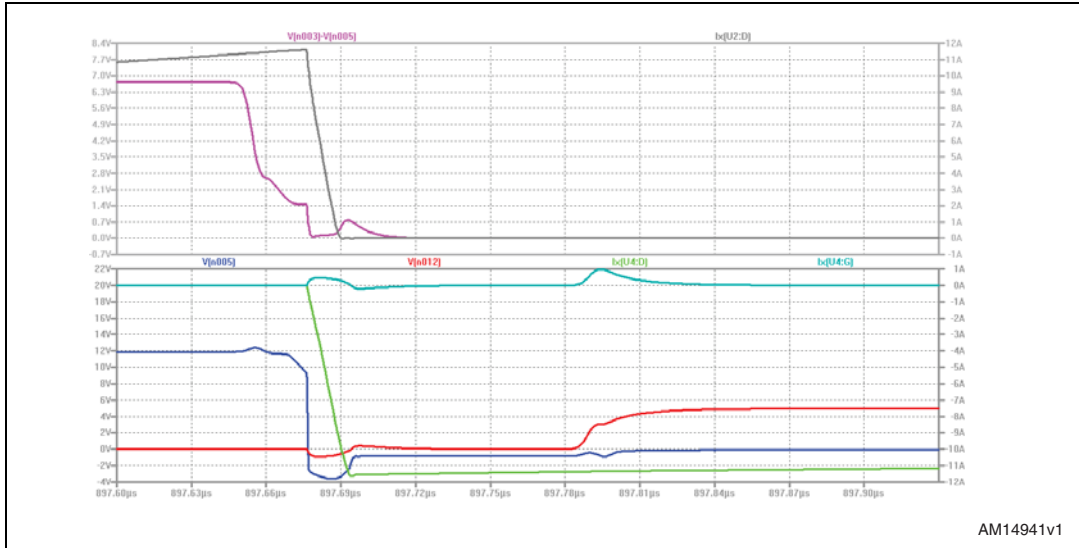
2 Synchronous buck converter testing demonstration board

The test vehicle is a synchronous buck converter, which lowers the input voltage (12 V) in 1.25 V as output; the converter switching frequency is 300 kHz, fixed by an internal oscillator, while the maximum output current is 20 A.

Figure 5.   Testing demonstration board schematic
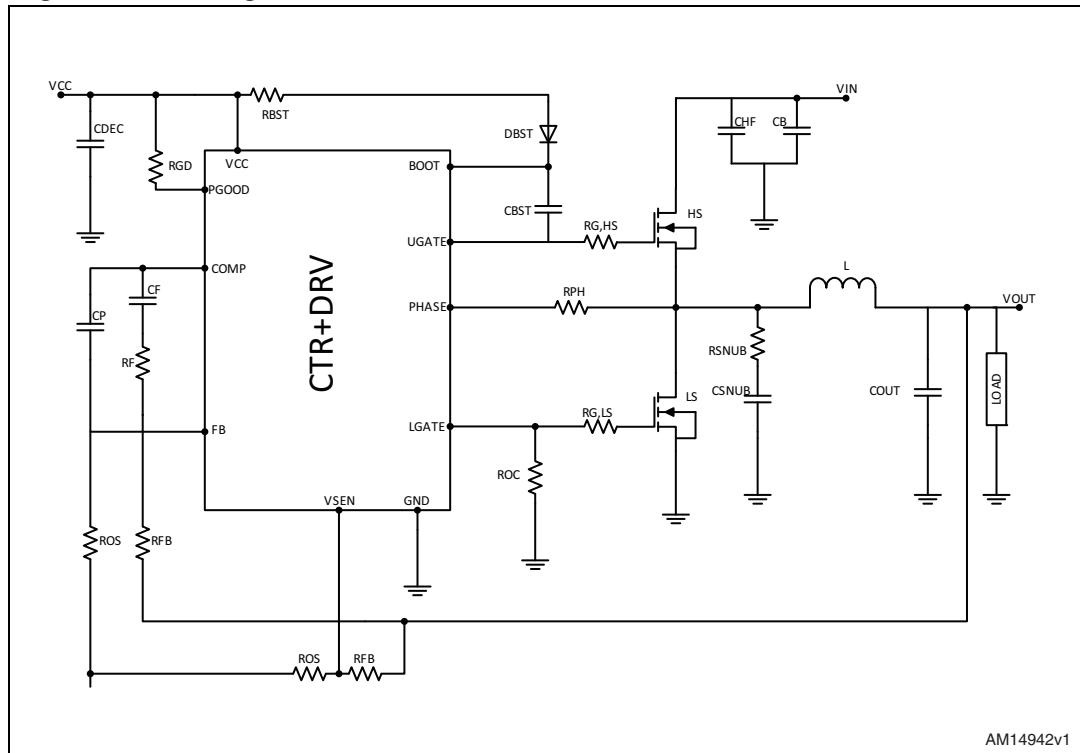
The converter has a single device both for high-side and low-side positions. The Power MOSFET gate drive voltage is 12 V for both devices; HS and LS external gate resistances are 2.2 Ω .

The Power MOSFETs are driven by a single-phase PWM controller with integrated driver ($I_{HS,SRC}$ = 2 A, $R_{HS,SINK}$ = 2 Ω, $I_{LS,SRC}$ = 3 A, $R_{LS,SINK}$ = 1 Ω). The controller shows very low LS sink resistance value in order to prevent any spurious gate-source bouncing and cross-conduction phenomenon during device turn-off.

The main advantage of this analysis is the availability of both the physical board and the full Cadence OrCAD Capture model of the converter (including driver and Power MOSFETs). Based on the same schematic, with identical passive and semiconductor devices, it is possible to use the converter Cadence OrCAD Capture model for testing various operating conditions, validating and explaining the experimental results. Moreover, the simulation data are very helpful to evaluate the Power MOSFET currents (especially drain current), as in the real board they cannot be measured easily by standard current probes, due to SMD packages and high switching frequency.

To overcome these difficulties, in the real board, the Power MOSFET gate current measurement is made by using a "Rogowski coil" current probe (CWT ultra mini), properly connected to the Power MOSFET gate pin. The features of this device are interesting, because it is flexible and open-ended and can be wrapped around a conductor without disturbing it. Moreover, it is able to respond correctly to fast-changing currents and it is highly linear even at very high current levels.

In *Figure 6*, the Rogowski coil probe end placing on a Power MOSFET DPAK gate pin is shown.

Figure 6. Rogowski coil package for I$_{gate}$ measurement

AM14943v1
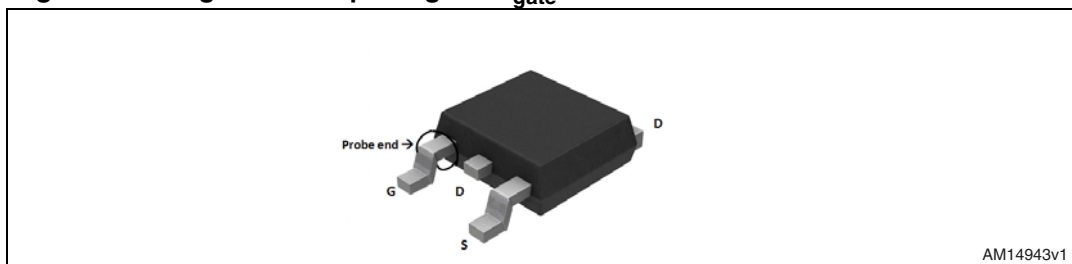
2.1 Power MOSFET selection for comparative tests

The aim of this document is to evaluate and explain the MOSFET technology gate current relationship; the analysis starts by choosing two different low-side devices, with the same die size, to be tested on the board:

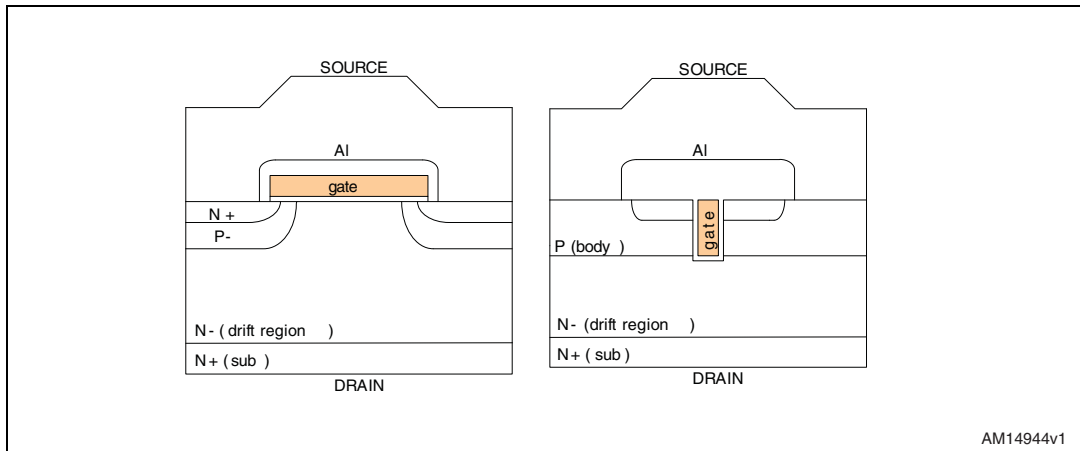   a) Device A - "planar" technology
    b) Device B - "trench" technology

All the devices are 30 V logic level FETs (1 V < V$_{th}$ < 2.5 V). In the following table, the main Power MOSFET dynamic parameters (intrinsic capacitances and resistances) are reported:

Table 1. Power MOSFET electrical parameters

Device	Q$_G$ @ 4.5 V (nC)	Q$_{GS}$ (nC)	Q$_{GD}$ (nC)	Ciss @ 25 V	Crss @ 25 V	Coss @ 25 V	R$_G$ (Ω)
A	14	6.8	4.7	1850	58	380	1.2
B	20	8.2	7.5	2200	280	400	1.1

Figure 7 gives the cross sections of the two above mentioned devices.

**Figure 7.   Device A (left) and device B (right) cross sections**

In a Power MOSFET with planar technology, the gate structure is on the device surface, realized by a planar poly-silicon electrode, a gate oxide layer and the silicon; these three layers form the "MOS" capacitor. The gate oxide isolates the metal contact and its thickness is in the range of a few or several hundreds of angstroms. The drain current flows from the source (n+region), through the conductive channel, in the vertical direction to the drain.

Considering now the trench technology, some relevant differences are immediately visible. The gate structure is realized by a deeply dug poly-silicon electrode (highly doped), isolated by a gate oxide layer. The trench depth is one of the most important process parameters, affecting device static ($R_{DS(on)}$) and dynamic (Q_{GD}) performance (it can vary in the range 1-2 µm). The drain current flows vertically along the trench sidewall towards the drain contact.

Figure 8 shows the same device structures highlighting the geometrical aspects that affect the Power MOSFET switching performance.

Figure 8.   Device A (left) and device B (right) cross sections with geometrical details
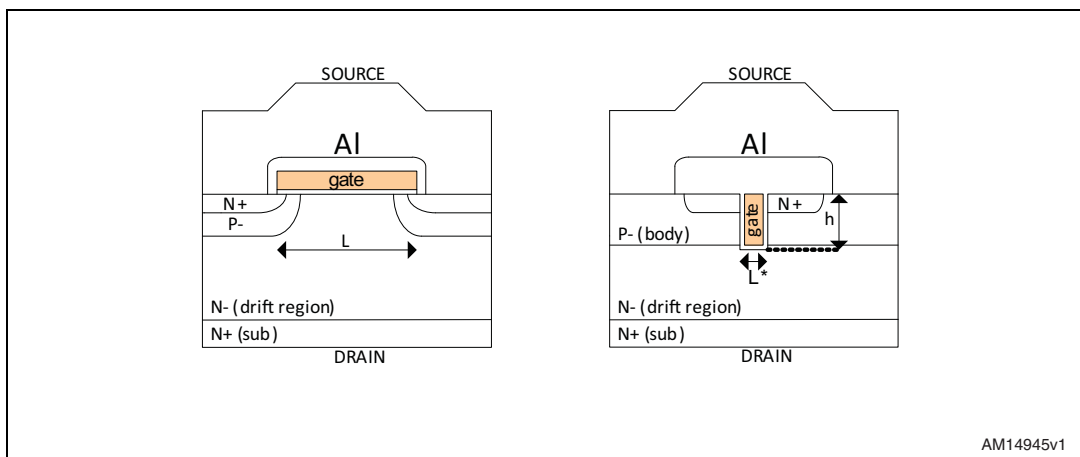
For a planar structure, L is the gate electrode width while the pitch is the cell-to-cell distance. In a trench device, L* is the trench width and h is the trench depth. Q_g/A (gate charge per area) links the Power MOSFET dynamic performance to the device geometry, providing a good tool for a technology comparison:

Equation 3

$$\frac{Q_g}{A} \propto \frac{L}{(pitch)_A}$$

Equation 4

$$\frac{Q_g}{A} \propto \frac{L^* + 2h}{(pitch)_A}$$

Equation 3 is valid for a planar device, while *4* is valid for trench. For modern silicon technology, the following considerations are valid:

Equation 5

$$L^* << 2h$$

Equation 6

$$L < 2h$$

So, merging Equation *3*, *4*, *5* and *6* and considering that $(pitch)A > (pitch)B$:

Equation 7

$$\left(\frac{Q_g}{A}\right)_{planar} < \left(\frac{Q_g}{A}\right)_{trench}$$

Equation 8

$$\left(\frac{C_{xx}}{A}\right)_{planar} < \left(\frac{C_{xx}}{A}\right)_{trench}$$

In other words, the intrinsic capacitive contribution of planar technology is lower than that of trench. This is of basic importance when the system/application requires switching performance improvement.

The specific capacitance difference between devices A and B shown in *Figure 8* is reflected into dissimilar gate charge curves: all the components of the gate charge are much larger for dev.B (red curve).

Figure 9.   Gate charge comparison
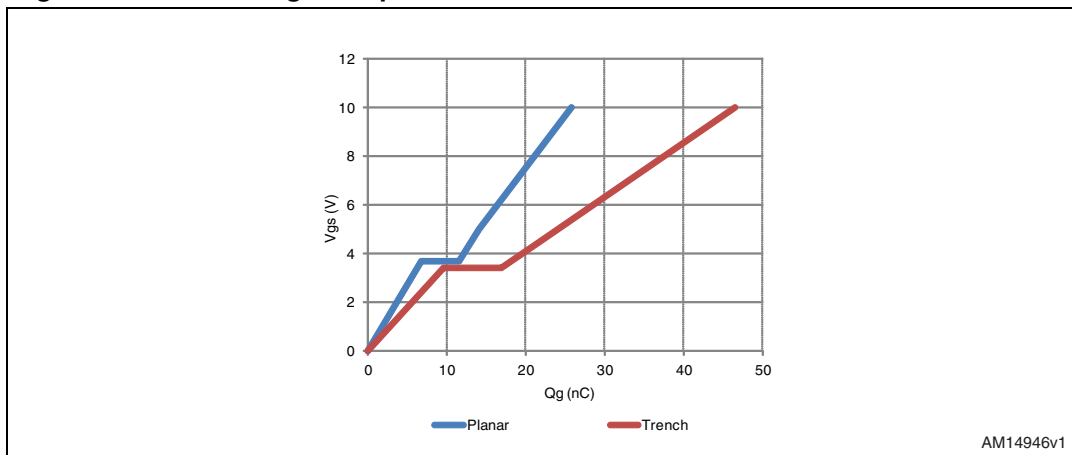
3   Bench tests and simulation results overview

By an external DC electronic load, the converter output current is fixed at I_{OUT} = 15 A. Low-side turn-on and turn-off transients are captured. For a complete comparison in terms of gate current performance, the following parameters are measured for both devices:

– $I_{gate,max}$: maximum peak during turn-on;
– $I_{gate,min}$: minimum value during turn-off;
– $\Delta t(I>0)$: time interval duration with Igate > 0;
– $\Delta t(I<0)$: time interval duration with Igate < 0;
– $I_{gate,avg(ON)}$: average gate current during turn-on;
– $I_{gate,avg(OFF)}$: average gate current during turn-off;
– I_{maint}: gate current value when the device is fully ON;
– t_f: low-side V_{GS} fall time, measured from 90% to 10% of V_{GS};
– t_r: low-side V_{GS} rise time, measured from 10% to 90% of V_{GS}.

In *Figure 10* and *Figure 11* the low-side waveforms for device A and device B, respectively, are reported; the green trace is the LS gate current (1 A/div) whereas the yellow trace is $V_{GS,LS}$ (5 V/div).
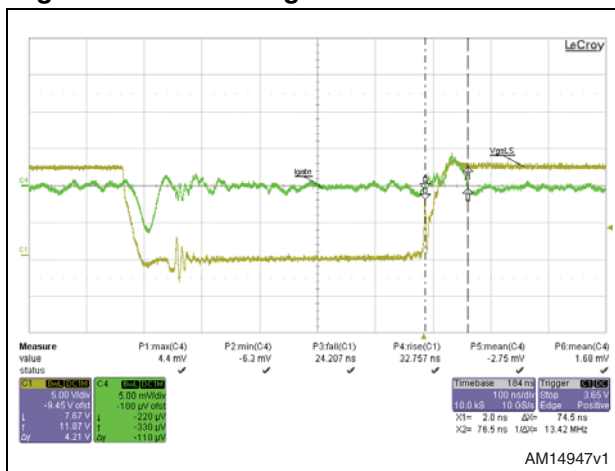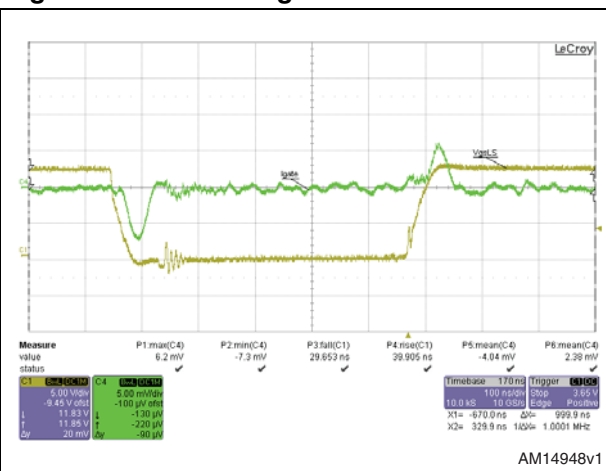
Figure 10. Device A gate waveforms	Figure 11. Device B gate waveforms

In the above images the turn-on and turn-off transients are clearly visible, with the relative gate current. During low-side turn-off, the gate current is negative, sunk by the driver to discharge Power MOSFET intrinsic capacitance. On the other hand, a positive gate current is needed to provide the right Q_G (total gate charge) to fully turn on the FET.

The following chart summarizes the parameter measurements performed on device A and device B:

Figure 12. Device A vs. device B (experimental results)
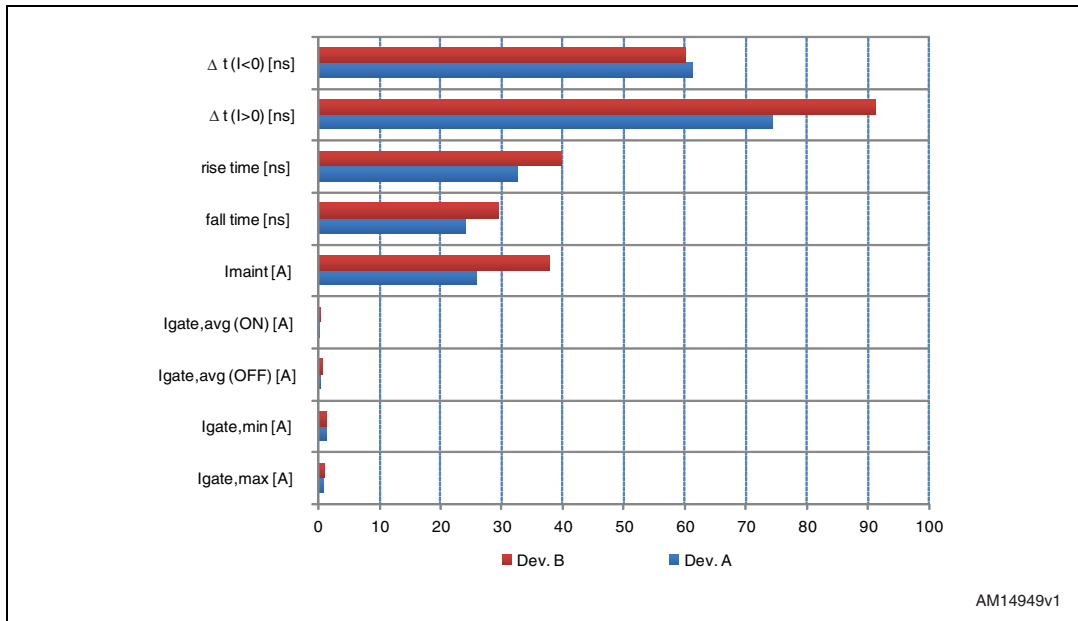
In *Table 2* the percentage variations (device B vs. device A) of the measured parameters are reported and defined as:

$$\Delta(\text{parameter})_{B-A} = \frac{(\text{parameter})_B - (\text{parameter})_A}{(\text{parameter})_B}$$

Table 2. Percentage variation (experimental results)

|	**Device B vs. device A**
$\Delta I_{\text{gate, max}}$ (A)	29.03%
$\Delta I_{\text{gate, min}}$ (A)	13.70%
$\Delta I_{\text{gate, avg(OFF)}}$ (A)	31.93%
$\Delta I_{\text{gate, avg(ON)}}$ (A)	29.41%
ΔI_{maint} (A)	31.58%
Δt_f (ns)	18.24%
Δt_r (ns)	18.05%
$\Delta t_{(I>0)}$ (ns)	18.49%
$\Delta t_{(I<0)}$ (ns)	-2.16%

As shown in *Figure 12* and *Table 2*, device B shows higher values for almost all measured parameters; in particular, the gap becomes wide for maximum peak, average values at turn-on and off and maintenance current.

Consider now the Cadence OrCAD Capture simulator, performing a transient analysis to capture LS waveforms, at a fixed output current level (I_{OUT} = 15 A). In *Figure 13* and *Figure 14* device A low-side gate signals are shown:

Figure 13. Device A gate waveforms @ LS turn-off (simulated)
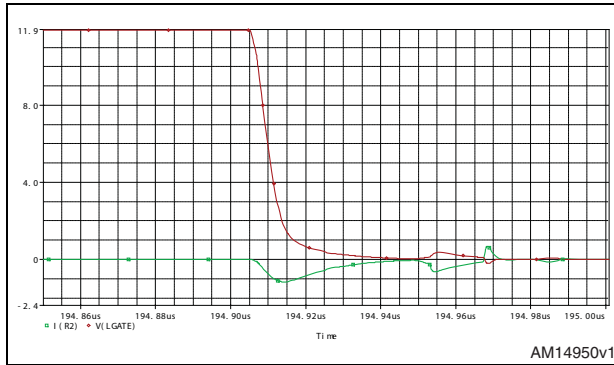
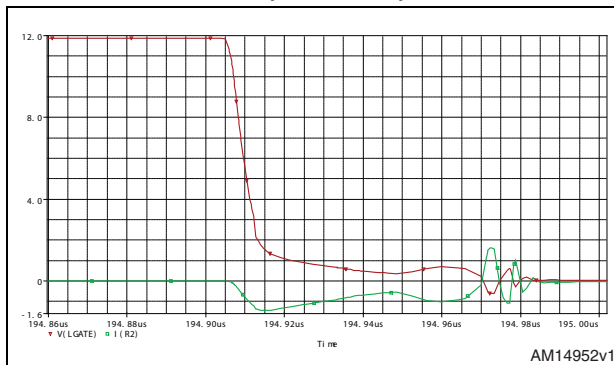**Figure 14. Device A gate waveforms @ LS turn-on (simulated)**
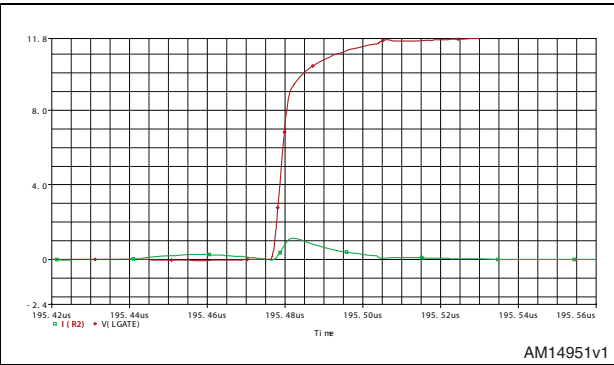
The red trace is the LS gate-source signal, while the green trace is the Power MOSFET gate current.

Comparing *Figure 10*, *Figure 13* and *Figure 14*, it is noticeable that the good accuracy of simulation results matches well with experimental ones in terms of waveform behavior.

In *Figure 15* and *Figure 16* the LS turn-off and on waveforms of device B are reported:

**Figure 15. Device B gate waveforms @ LS turn-off (simulated)**

Figure 16. Device B gate waveforms @ LS turn-on (simulated)
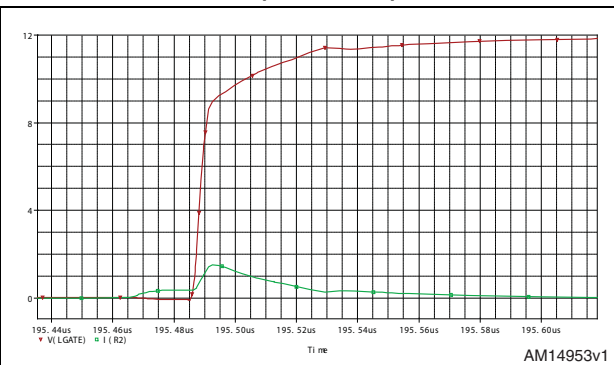
Finally, in *Figure 17* the measurements given by Cadence OrCAD Capture simulations are shown. Experimental and simulation results are strictly aligned; in fact, comparing *Figure 13* - *Figure 14* and *Figure 15* - *Figure 16*, some important observations can be made:

a)　Device B shows higher maximum and minimum gate current peaks, as reported in *Table 3*;

b)　Device B LS gate waveforms have slower rising and falling edges, with consequently longer rise and fall times;

c)　Device B gate current, at device turn-on, shows much higher peak and stays above the zero level for a longer time than device A.

Figure 17. Device A vs. device B (simulation results)
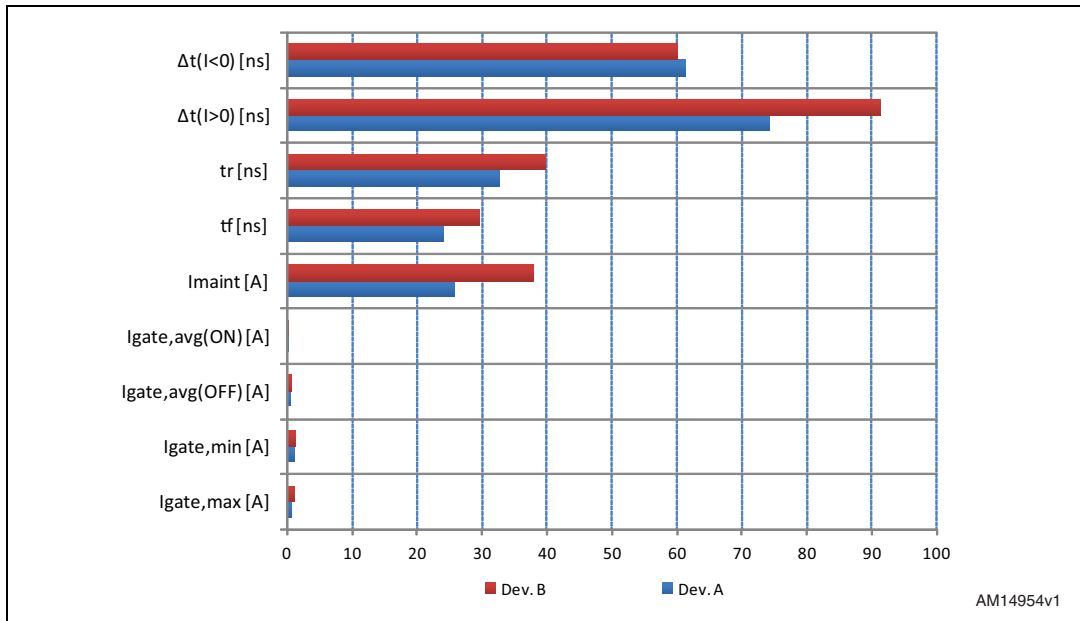
Starting from the simulation results, *Table 3* reports the switching parameters' percentage variations:

Table 3.   Percentage variation (simulation results)

	Device B vs. device A
$\Delta I_{gate,\ max}$ (A)	30.43%
$\Delta I_{gate,\ min}$ (A)	18.75%
Δt_f (ns)	15.38%
Δt_r (ns)	28.57%
$\Delta t_{(I>0)}$ (ns)	57.82%
$\Delta t_{(I<0)}$ (ns)	7.10%

Table 2 and *Table 3* give very good matching between experimental and simulation results, particularly for $I_{gate,max}$ and $I_{gate,min}$ (maximum and minimum gate current) and for V_{GS} fall time. Furthermore, the trend is confirmed also for the other switching values.

4 Conclusion

Starting from a single-phase synchronous buck converter topology, the impact of silicon technology on low-side Power MOSFET gate current has been thoroughly analyzed, by bench tests and Cadence OrCAD Capture simulations. Trench technologies, which are preferable in high efficiency DC-DC converters due to their very competitive figure of merit (FOM = $R_{DS(on)} * Q_G$) values, have higher specific capacitance values (Cxx/A) compared to planar ones; this affects the overall device switching performance. This also means different gate current behavior, with bigger maximum and minimum gate current peaks and longer rise/fall times.

These different device characteristics should be monitored particularly when application features (switching frequency, number of paralleled devices, etc.…) are more critical for switching behavior, making driver-MOSFET matching optimization mandatory.

Two examples can be given to enforce the previous statements. When more FETs are paralleled, to minimize the overall $R_{DS(on)}$ and the conduction losses, the driver must charge and discharge a bigger equivalent capacitance to switch on and off the devices. So, to minimize the gate drive losses, the driver must have special features, in terms of sink/source current and resistance, particularly when driving trench Power MOSFETs.

Similarly, in hard-switching applications, where larger losses occur during switching transients, proper driver choice is needed when higher (Cxx/A) Power MOSFETs must be turned on and off, improving gate current source and sink and reducing the switching losses.

5 References

- Power Electronics Handbook, M. H. Rashid, 2001
- Fundamentals of Power Electronics, R. W. Erickson, 2000

6   Revision history

Table 4.   Document revision history

Date	Revision	Changes
12-Oct-2012	1	Initial release.

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