AN4192
Application note

Power MOSFETs: best choice guide for VRM applications

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Introduction

In the latest generation of CPUs for modern desktop and notebook platforms, the VRMs (voltage regulator modules) must have some specific features in order to reach high performance in terms of power management. This target can be reached by analyzing all the design parameters and their optimization, with a particular focus on the MOSFET electrical characteristics and configuration.

The power stage must deliver very low core voltage (typically 1.2 V - 1.3 V) to the CPU at high current levels (up to 160 A), with ever-increasing switching frequencies (up to 500 - 700 kHz). In order to match these requirements, the basic topology used in the VRMs is the “multiphase synchronous buck converter”, which typically steps down to 12 V input voltage, providing the desired core voltage.

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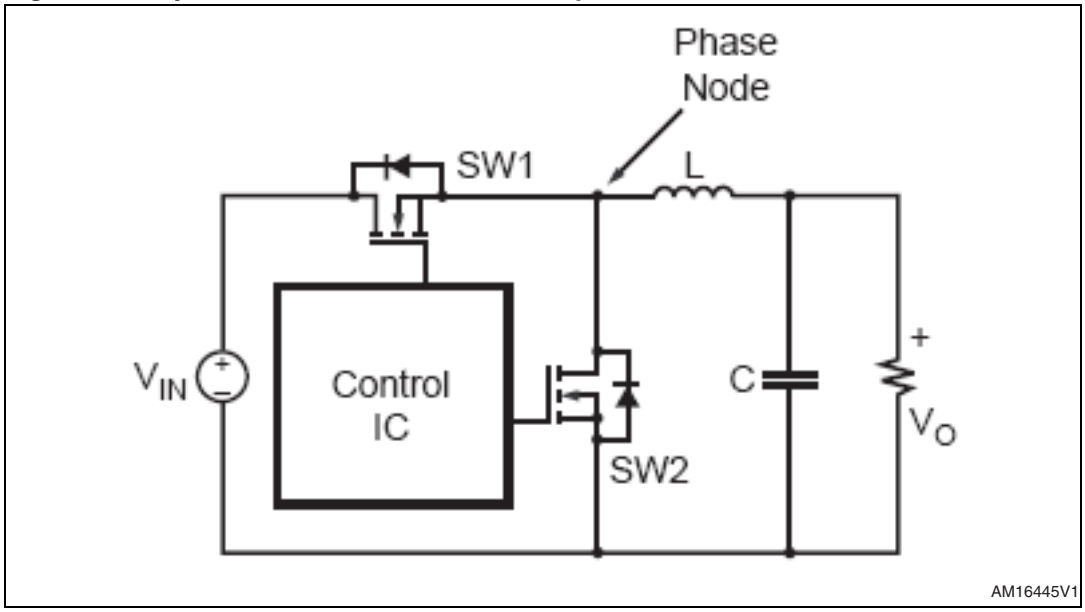
1 Synchronous buck converter: a brief introduction

The basic topology of a single-phase synchronous buck converter (SBC) is shown in *Figure 1*; SW1 is the main (or high-side) FET, SW2 is the synchronous (or low-side) FET, L and C are the output filters.

Figure 1. Synchronous buck converter simplified schematic



Comparing this topology to the standard buck converter, the main difference is the synchronous rectifier (SW2) instead of the free-wheeling diode; as $V_{DS(on)} < V_{F,DIODE}$, a strong reduction of the ON-state losses is guaranteed.

SW1 and SW2 are driven in a “synchronous” way: in other words, the control IC generates the gate driving signals, avoiding the simultaneous conduction of the two FETs (cross-conduction or shoot-through). So, when SW1 is in the ON-state, SW2 is turned off and vice versa. Obviously, to prevent HS and LS gate-source voltages overlapping and any cross-conduction issue, there are some time intervals (fixed by the control IC) where HS and LS FETs are in the OFF-state (deadtime).

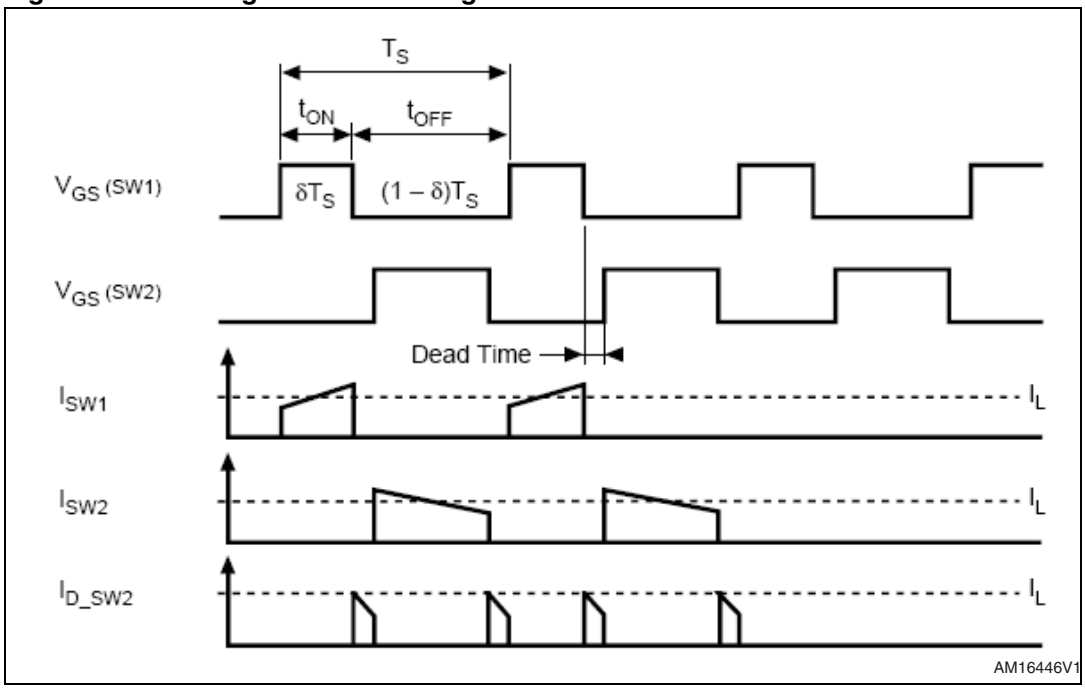
In *Figure 2*, the typical waveforms of a single-phase synchronous buck converter are represented. When the HS FET (SW1) is turned on, its drain current rises with a positive slope:

$$\frac{dI_L}{dt} = \frac{V_{in} - V_{core}}{L}$$

during HS t_{on}. When HS switches off, the LS FET remains in the HOLD state: the energy stored in L can't become zero immediately, so it freewheels through the LS body-drain diode (from source to drain, $V_{DS,LS}$ = -0.7 V). When the LS turns on, the load current diverts from the body diode to the LS channel, with a negative slope:

$$\frac{dI_L}{dt} = -\frac{V_{core}}{L}$$

Figure 2. HS/LS gate-source voltages



The load current doesn't become zero (the output coil doesn't discharge completely): the converter works in continuous current mode (CCM). After the LS turns off, the load current re-flows through the LS body diode (deadtime) and then another switching cycle begins.

As the input voltage is typically 12 V and the core voltage is 1.2 - 1.3 V, the converter duty cycle is small (0.1- 0.2%): then, the HS FET is on for a shorter time, while the LS FET has longer t_{on}.

Modern VRM topologies should have some additional features:

- High switching frequencies working capability
- Ever-increasing output current to be delivered to the load
- Input and output current ripple minimized.

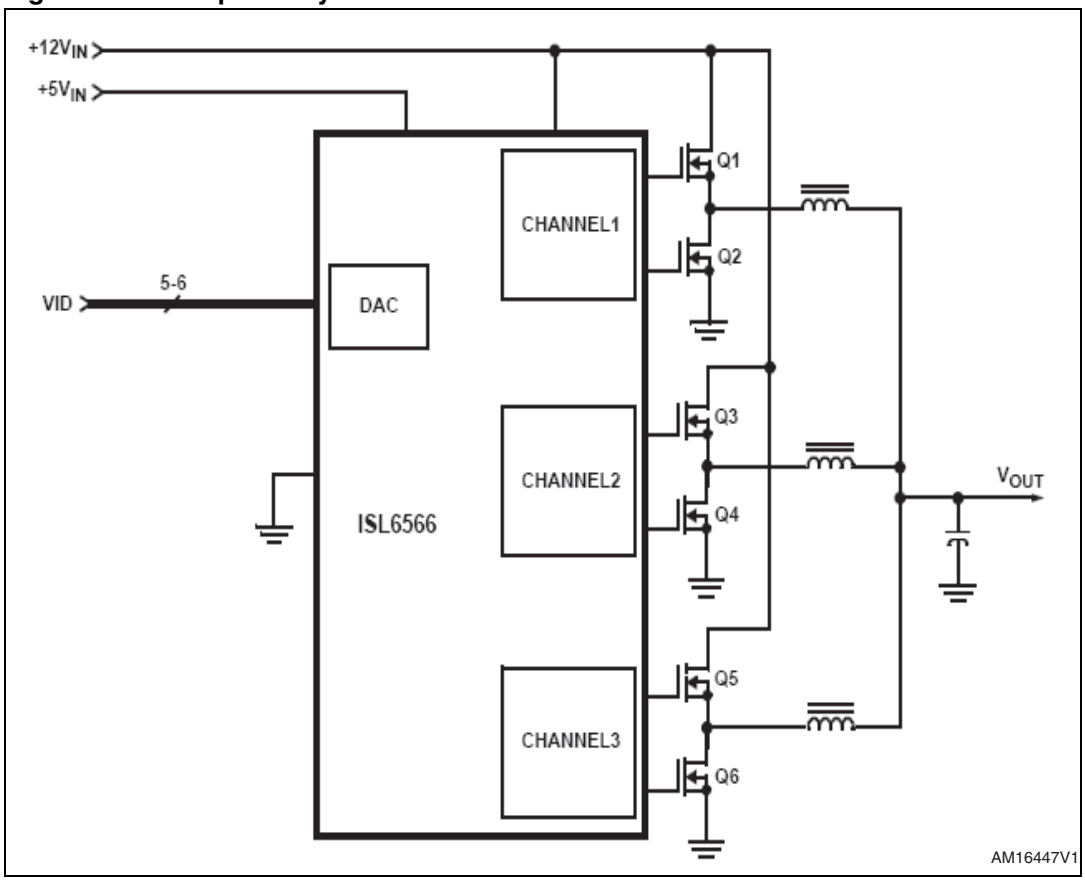
To match these requirements, the “multiphase” approach (*Figure 3*) is universally used, developed by interleaving more single-phase SBCs, connected together in the output capacitor pins. In this way, we obtain some advantages:

a) Each phase can manage up to 25 - 30 A (according to the layout and cooling down characteristics): so, it is possible to handle high currents, with improved efficiency. Moreover, the device reliability increases.

b) The total load current is given by adding all the phase currents: this causes a strong reduction of the output current ripple.

c) Input and output filter component size and dimension can be minimized; the converter working capability at high switching frequencies increases.

Figure 3. Multiphase synchronous buck converter schematic



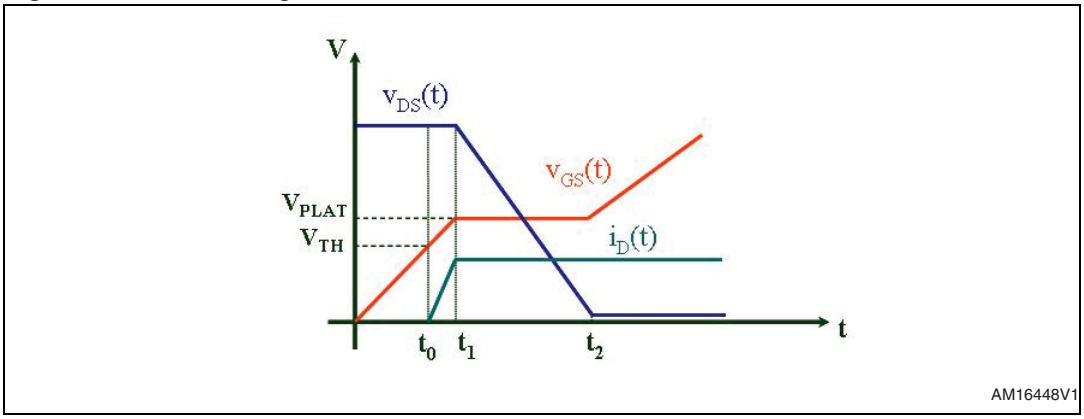
The maximum output current establishes the number of the phases that must be interleaved in the VRM (see point (*a*) above). The MOSFET selection must be equal in each phase, for the converter symmetry and right current balance; however, it is possible to use one or more HS or LS FETs in order to minimize some converter power losses.

2 High-side MOSFET selection

For the right choice of high-side FET, the following MOSFET electrical parameters must be considered:

1. **Q_g** (total gate charge): it impacts the HS switching speed (at turn-on and turn-off) and then the switching losses. Moreover, slightly bigger intrinsic capacitances, slowing down the HS turn-on, may smooth the phase node ringing (overshoot and high frequency oscillations on the phase node at HS turn-on).
2. **$R_{DS(on)}$** (ON-state drain-source resistance): when the converter duty cycle is low, the HS stays on for a short time, so the minimization of $R_{DS(on)}$ doesn't impact greatly on the efficiency. However, the higher the VRM output voltage (i.e. there are 3.3 V or 5 V sections in the notebook platforms), the bigger the $R_{DS(on)}$ impact.
3. **$R_{G,HS}$** (external gate resistance) and gate drive network settings: the right $R_{G,HS}$ value should be a trade-off between high switching speed and efficiency (low $R_{G,HS}$) and the phase node ringing improvement (high $R_{G,HS}$). Some gate drive network configurations, such as “asymmetric gate drive”, are able to enhance the converter switching behavior with limited consequences on the efficiency.

Figure 4. Gate charge waveform



In *Figure 4*, the simplified gate charge waveform for N-MOS (neglecting the parasitic effects) is illustrated, which represents the V_{GS} behavior as a function of time. The switching transient is the interval $[t_0,t_2]$, when $v_{DS}(t)$ and $i_D(t)$ are simultaneously bigger than zero. At $t = t_0$, the gate-source capacitance (C_{gs}) is charged and the drain current starts to increase. During $[t_0,t_1]$, the drain current increases linearly until it reaches its final value (I_{OUT}). At $t = t_1$, the gate-source capacitance (C_{gs}) is totally charged, the drain-source voltage begins to fall (we assume that the falling edge is linear) and the gate current flows through the Miller (or transfer) capacitance. For $t > t_2$, the switching losses are negligible because the MOSFET is in the ohmic zone, with a constant $R_{DS(on)}$.

The charge amount $Q_{G,SW} = Q_{GD} + Q_{GS2}$ is needed to turn on the FET: it is also called “switching charge”. The high-side FET switching losses (for a single-phase synchronous buck converter) can be expressed as:

Equation 1

$$P_{SW} = \frac{1}{2} \cdot V_{IN} \cdot I_{OUT} \cdot f_{SW} \cdot \frac{Q_{G,\,SW}}{I_{GATE}}$$

where f_{SW} is the converter switching frequency, and I_{GATE} is the total gate current, provided by the driver to the HS FET during turn-on and turn-off transients. Looking at (*1*), two main parameters impact the HS switching losses, playing a crucial role in converter performance optimization:

1. The higher the f_{SW}, the more relevant the switching losses.
2. The bigger the $Q_{G,SW}$ (and the slower the HS switching speed), the higher the P_{SW}.

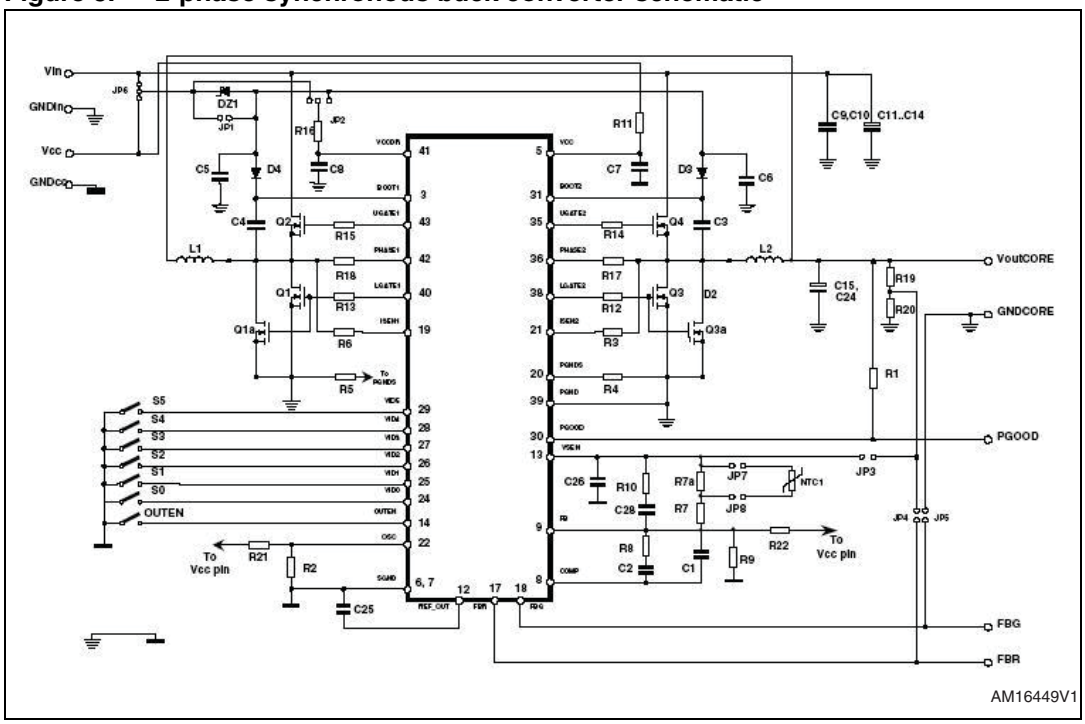
In the following examples, we can see the impact of the above mentioned parameters on the converter performance.

2.0.1 $Q_{G,SW}$ and f_{SW} impact on the efficiency

Four different 30 V HS FETs are compared in a 2-phase synchronous buck converter (V_{IN} = 12 V, V_{OUT} = 1.5 V, I_{OUT} = 44 A, 1 x HS, 2 x LS, f_{SW} = 440 kHz). External HS and LS gate resistances are present in the layout ($R_{G,HS}$ = 2.2 Ω, $R_{G,LS}$ = 2.2 Ω), whereas no RC snubber network is used. The low-side FET is the same for all configurations (called “Low Side”).

Here below (*Figure 5*), the converter schematic is shown, while in *Table 1* the main electrical parameters of the HS FETs (R_{DSon}, BV_{DSS}, etc.) are reported.

Figure 5. 2-phase synchronous buck converter schematic

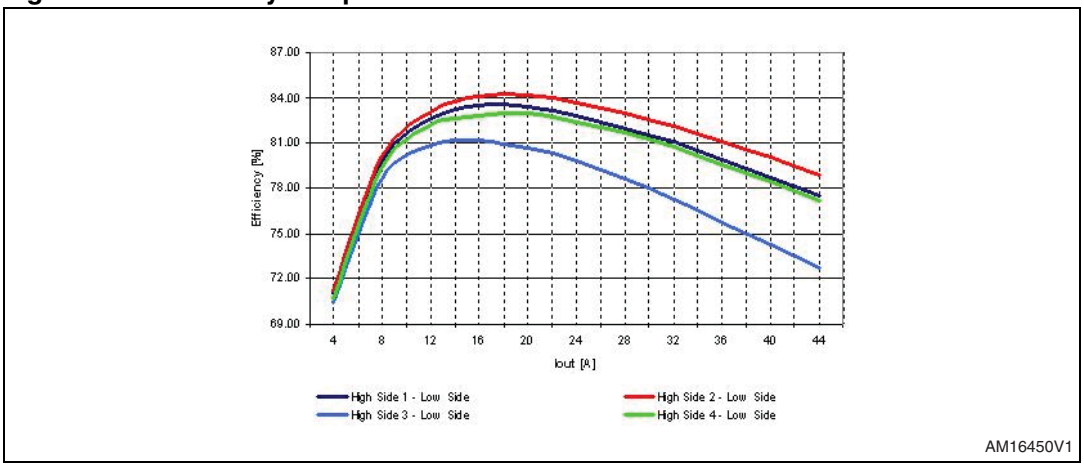


As shown in the following table, the “High-side 2” has the lowest “switching charge” (-49% compared to “High-side 3"). In *Figure 6*, the efficiency curves at f_{SW} = 440 kHz are compared.

Table 1. HS FETs electrical parameters comparison

	BV [V]	$R_{DS(on)}$ [mΩ]	$Q_{g,SW}$ [nC]
High-side 1	30	9.2 / 10.5	6.85
High-side 2		7.3 / 8.3	4.65
High-side 3		7.6 / 9.5	9.25
High-side 4		7.0 / 9.0	7

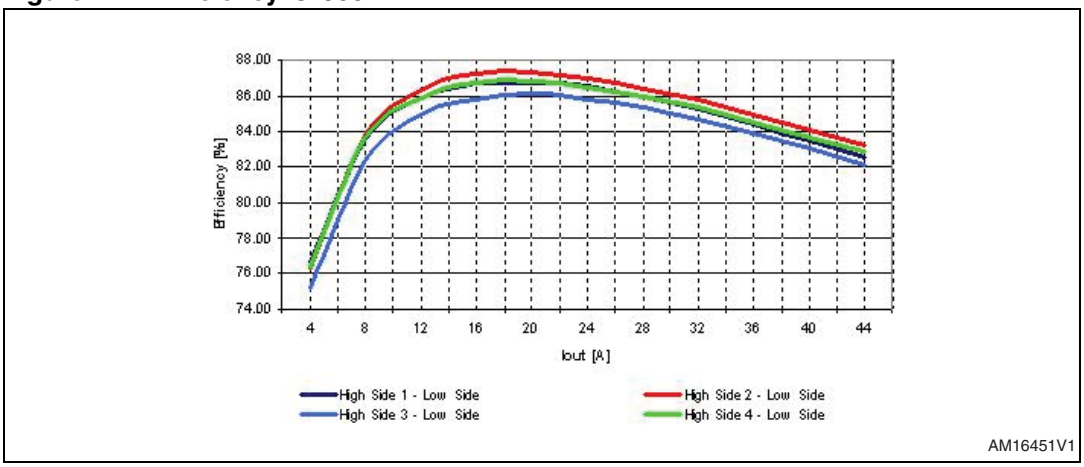
Figure 6. Efficiency comparison @ 440 kHz



As can be clearly seen, the high-side 2 has the best efficiency in the whole current range, because of the switching loss minimization (see (*1*)).

Now, let's consider the converter performance, with the same MOSFET configurations, at two different switching frequencies: 300 kHz and 440 kHz. Increasing f_{SW}, the converter efficiency decreases, as some power losses increase with the frequency (switching losses, HS/LS gate drive and LS reverse recovery losses, etc.…). Furthermore, the importance of a high switching speed rises when the switching frequency increases. In *Figure 6* and *Figure 7*, the efficiency curves at 300 kHz and 440 kHz are illustrated.

Figure 7. Efficiency @ 300 kHz



At f_{SW} = 300 kHz, the different “switching charge” values don't strongly affect the efficiency curves (1.2% efficiency improvement of “high-side 2” vs. “high-side 4”). But, if we step up the switching frequency to 440 kHz, the HS FET with the lowest $Q_{G,SW}$ (“high-side 2”) has the best efficiency in the overall current range, due to the switching losses reduction.

Then, high-side FETs with very low $Q_{G,SW}$ make the design more efficient and are the best solution in high frequency VRM applications.

2.0.2 $Q_{G,SW}$ impact on the HS switching behavior

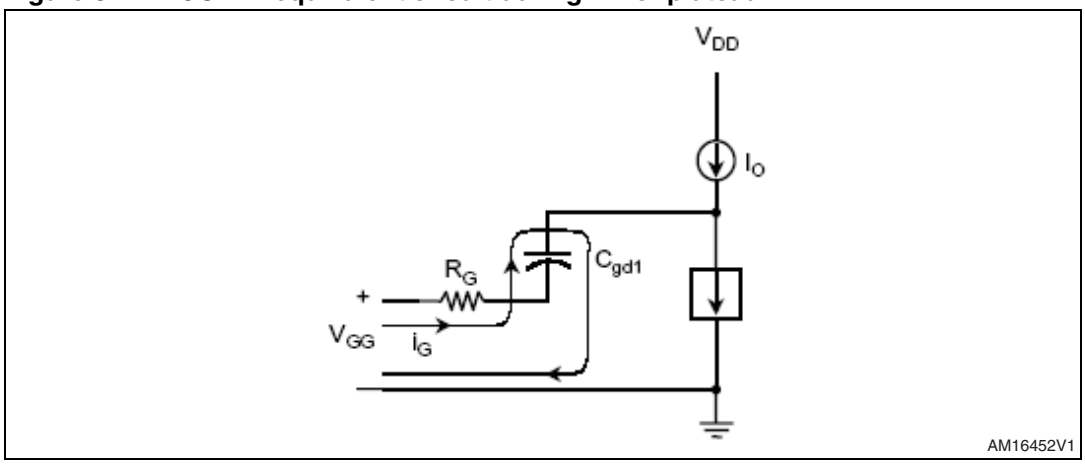
$Q_{G,SW}$, particularly Q_{GD}, also affects the high-side switching behavior during turn-on and turn-off. Referring to the gate charge image (*Figure 4*), during the “Miller plateau” (from t_1 to t_2) the MOSFET works in the active region ($V_{DS} > V_{DS,SAT}$), so the gate-source voltage is constant while the drain current is the full load current. In this time interval, the MOSFET drain-source voltage drops from high level to zero (at turn-on) or rises from zero to high level (at turn-off) (see *Figure 8*). Since C_{GS} is fully charged, the gate current flows only through C_{GD}, so there is a strong relationship between V_{DS} falling edge slope and Q_{GD}:

Equation 2

$$\frac{dV_{DS}}{dt} = \frac{I_G}{V_{GD}}$$

I_G is the total gate charging current. The bigger the Miller capacitance, the lower the V_{DS} slope, and vice versa.

Figure 8. MOSFET equivalent circuit during Miller plateau



In order to show the C_{GD} impact on the HS switching performance, two 30 V FETs (MOS1, C_{GD} = 76 pF @ 25 V and MOS2, C_{GD} = 150 pF @ 25 V) are compared as high-side FETs in a two-phase synchronous buck converter (V_{IN} = 12 V, V_{OUT} = 1.5 V, I_{OUT} = 44 A, 1 x HS, 2 x LS, f_{SW} = 440 kHz). External HS and LS gate resistances are present in the layout ($R_{G,HS}$ = 2.2 Ω, $R_{G,LS}$ = 2.2 Ω), whereas no RC snubber network is used.

Figure 9. MOS1 (C_{GD} = 76 pF) - HS turn-off waveforms

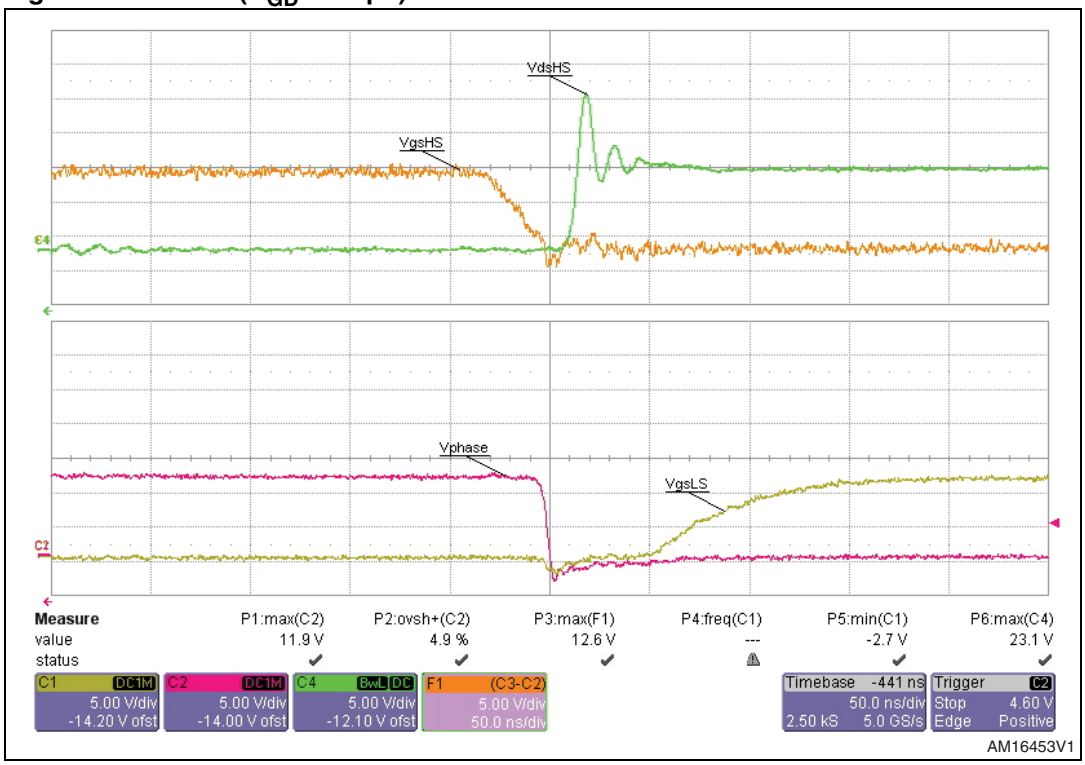
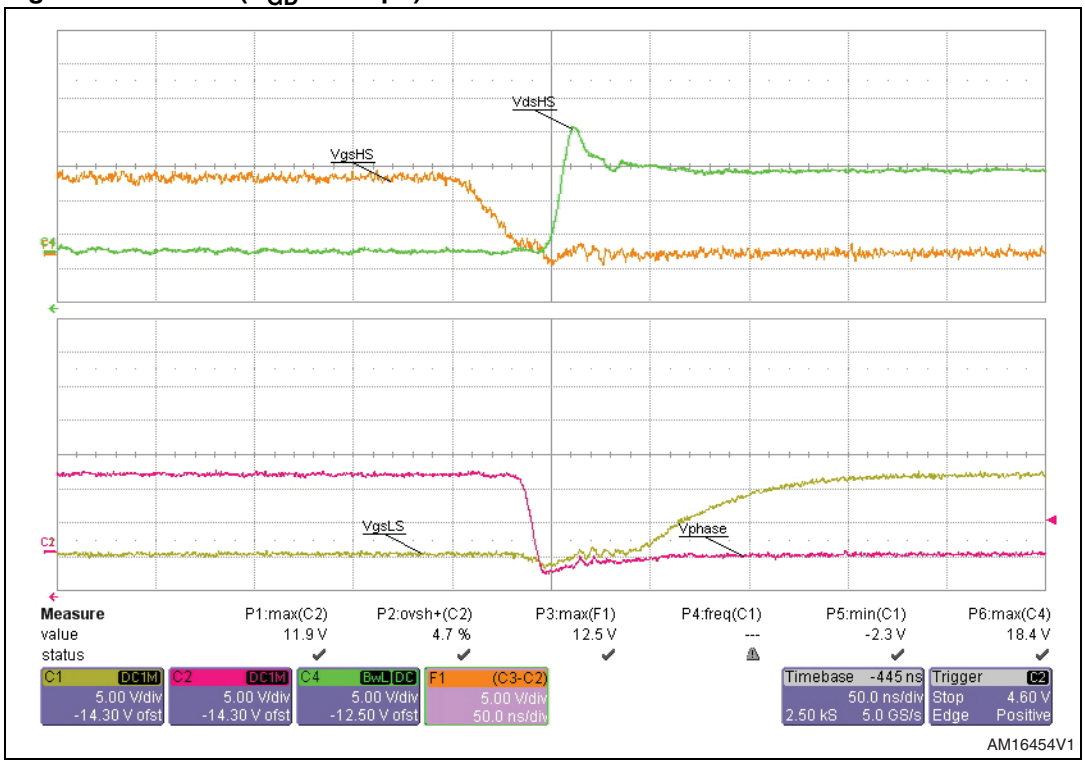


Figure 10. MOS1 (C_{GD} = 150 pF) - HS turn-off waveforms



In *Figure 9* and *10*, the HS turn-off waveforms of the two FETs are shown. Higher C_{GD} values reduce the HS V_{DS} maximum spike (18.4 V vs. 23.1 V) and

$$\frac{dV_{DS,HS}}{dt}$$

(2.1 V/ns vs. 3.9 V/ns); furthermore, the V_{GS} falling edge slope is slower (the Miller plateau is more visible and V_{GS} fall time is higher). Obviously, the main design rule is that $V_{DS,HS}$ must be lower than the HS breakdown voltage (typically, $V_{DS,HS(max)} \leq 0.8 * BV_{DS,HS}$ to increase MOSFET reliability).

The Miller capacitance value should be the correct trade-off between efficiency improvement at high f_{SW} (low $Q_{G,Sw}$ and Q_{GD}) and HS maximum voltage stress reduction (high Q_{GD}).

2.1 $R_{DS(on)}$ and conduction losses minimization

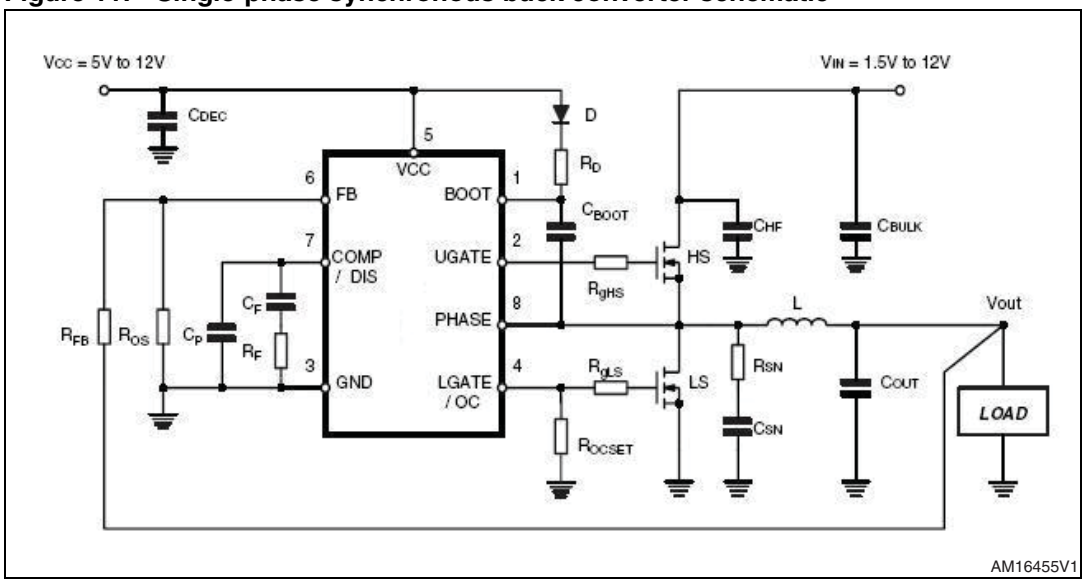
Considering a single-phase synchronous buck converter with a single HS device, the HS conduction losses are shown in the following formula:

Equation 3

$$P_{HS,COND} = D \cdot R_{DS(on)}|T| \cdot I^2_{D,HS}$$

where D is the converter duty cycle, $R_{DS(on)}$ is the ON-state drain-source resistance, evaluated at the operating temperature (T °C), and $I_{D,HS}$ is the HS drain current. As D is low (0.1% - 0.2%), this term is not the most important in converter performance enhancement. However, a slight efficiency enhancement can be noted at high output currents, when a lower RDSon high-side FET is used.

Figure 11. Single-phase synchronous buck converter schematic



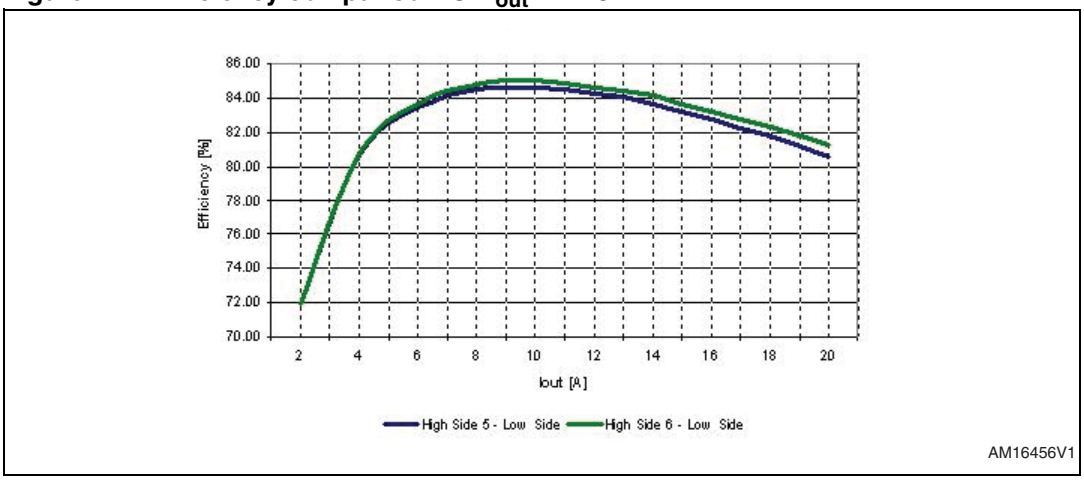
In *Figure 11*, a single-phase synchronous buck converter schematic (V_{IN} = 12 V, V_{OUT} = 1.25 V, $I_{OUT,MAX}$ = 20 A, f_{SW} = 270 kHz, 1 x HS, 1 x LS) is shown, where two different high-side FETs (“high-side 5” and “high-side 6”) are compared with a fixed LS device. External gate resistances are connected to HS (2.2 Ω) and LS (1.8 Ω) FETs. An RC snubber network

(R_{SNUB} = 1 Ω C_{SNUB} = 6.8 nF) is used to smooth the phase node ringing. The main MOSFET electrical parameters are reported in *Table 2*.

Table 2. MOSFET electrical parameters

	BV [V]	$R_{DS(on)}$ [mΩ]	$Q_{g,SW}$ [nC]
High-side 5	30	11.0 / 13.0	8
High-side 6		8 / 10.5	7.9

Figure 12. Efficiency comparison @ V_{out} = 1.25 V



As shown in *Figure 12*, at medium and high load currents, “high-side 6” assures the best efficiency results, due to its lower $R_{DS(on)}$ (+0.8% at full load).

In some applications (i.e. notebooks), there are some functional blocks that generate 3.3 V/5 V as output voltages. In these cases, the HS t_{ON} becomes longer, because of the duty cycle enlargement, making the HS conduction losses more important. In this case, the HS and LS device features tend to be quite similar in order to reach the right trade-off between conduction and switching losses.

2.2 Gate drive network optimization

Typically, the HS and LS gate drive networks are developed by a single external resistor ($R_{G,EXT}$), connected between the driver and the MOSFET gate pin, which acts both as turn-on and turn-off resistor. The HS external gate resistor choice should be the correct trade-off between switching speed increase and efficiency improvement at high f_{SW} (low $R_{G,EXT}$) and HS switching behavior optimization and phase node ringing reduction (high $R_{G,EXT}$).

An optimization of the gate drive circuits can help to improve the phase node switching behavior without negative consequences on the converter efficiency. When the HS turns on, due to the energy previously stored in the stray inductances, there is an overvoltage stress between LS drain-source (*Figure 13* and *14*). Furthermore, after the first overshoot in the phase node, there are high frequency oscillations (50-100 MHz) due to the LC circuit formed by the LS COSS and the stray inductances. The phase node ringing (*Figure 15*) is mainly related to the LS intrinsic capacitances, the LS RC snubber network (see *Section 3.5: RC snubber network settings*): however, it depends also on the HS turn-on speed.

Figure 13. HS turn-off

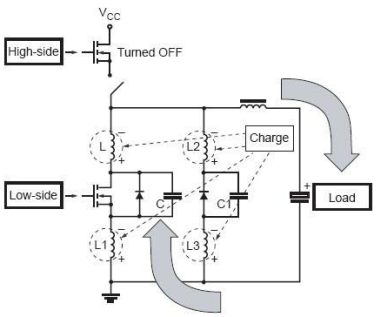


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Figure 14. HS turn-on (phase node spike)

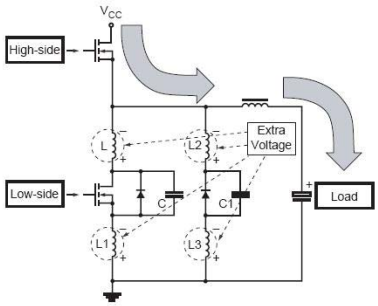

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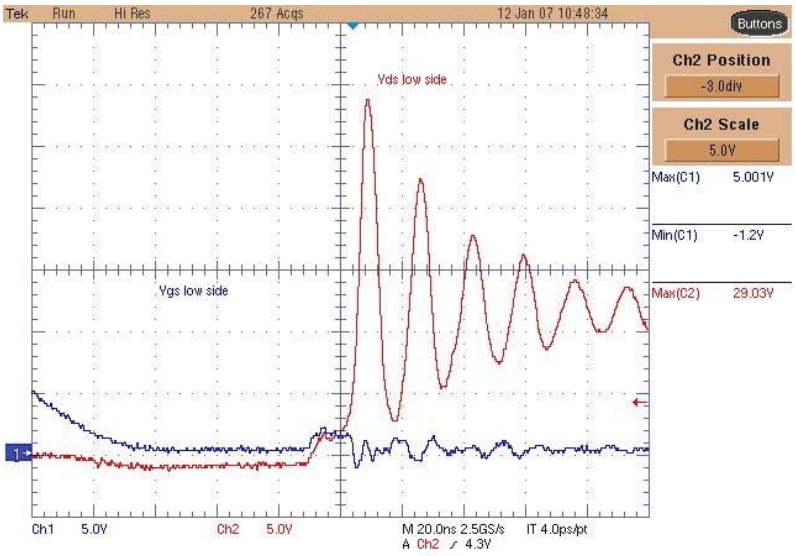
Figure 15. Typical phase node waveform (without RC snubber network)



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Slowing down the HS turn-on is useful in order to reduce the phase node ringing, so a higher $R_{G,EXT}$ should be used. But, the higher the $R_{G,EXT}$, the bigger the switching losses (particularly at turn-off) become: a low $R_{G,EXT}$ is helpful because it reduces the HS switching losses at turn-off. The “asymmetric gate drive circuit” tries to make a trade-off between these two different requirements (*Figure 16*). RG1 is the turn-on gate resistor, D is a diode and RG2 is the turn-off gate resistor:

- When the HS turns on, D is reverse biased so the gate voltage is applied to the gate through R_{G1}. So, its value may be selected high enough, in order to lower the HS switching speed and therefore the phase node spike.
- At HS turn-off, D is forward biased offering a low-resistance path to the HS discharging current. R_{G2} is the turn-off resistor because R_{G1} is shorted. If R_{G2} is 0 Ω, the HS switching speed at turn-off is the highest and the impact on the switching losses is minimized.

Figure 16. Asymmetric HS gate drive circuit

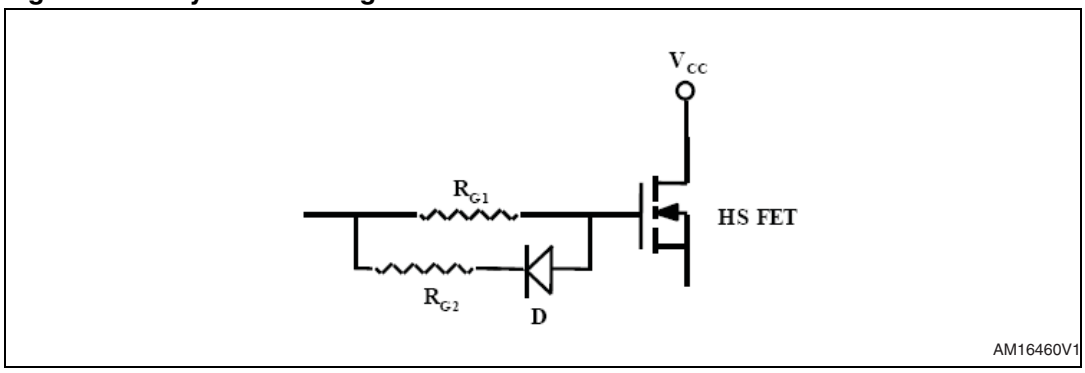
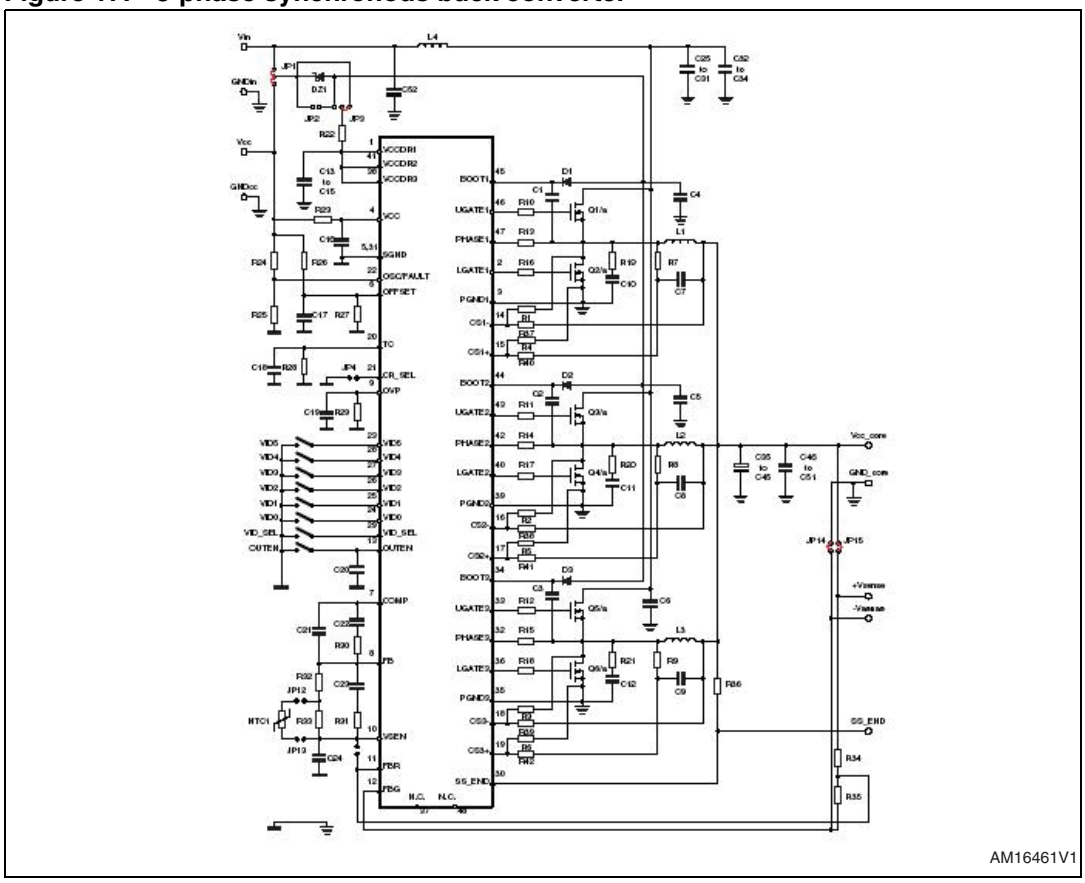


Figure 17. 3-phase synchronous buck converter



Let's now consider a 3-phase synchronous buck converter (*Figure 17*) (V_{IN} = 12 V, V_{OUT} = 1.25 V, f_{SW} = 270 kHz, 2 x HS, 2 x LS, I_{OUT} = 75 A). External gate resistances are connected to HS (2.2 Ω) and LS (2.2 Ω) FETs. An RC snubber network (R_{SNUB} = 2.2 Ω, C_{SNUB} = 4.7 nF) is used to smooth the phase node. Two different HS driving configurations (standard with $R_{G,EXT}$ = 2.2 Ω, "asymmetric gate drive" with R_{G1} = 3.9 Ω, R_{G1} = 1.8 Ω) are compared in terms of phase node ringing and efficiency comparison. In *Figure 18* and *19* the phase node waveforms of the two configurations are shown.

Figure 18. Phase node waveform - standard configuration

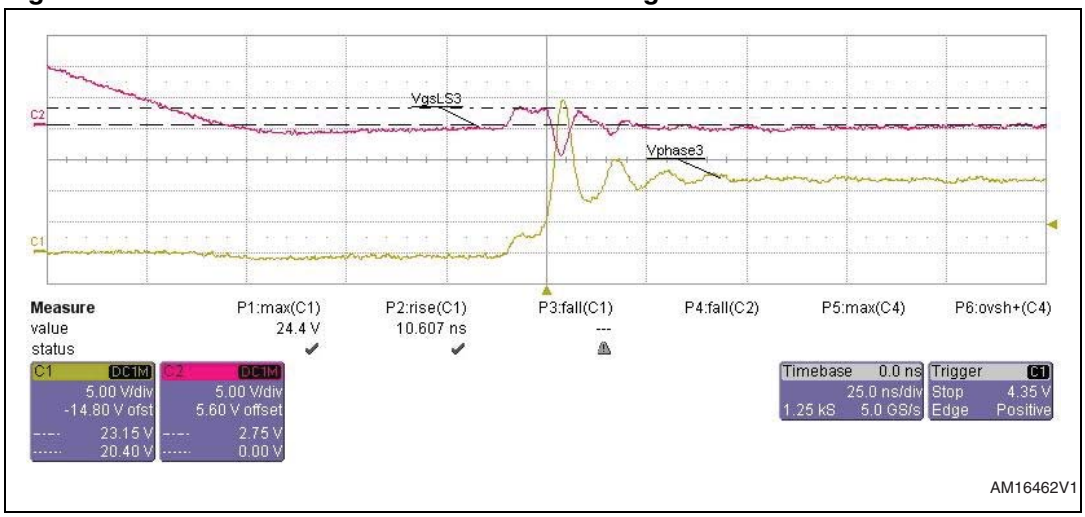
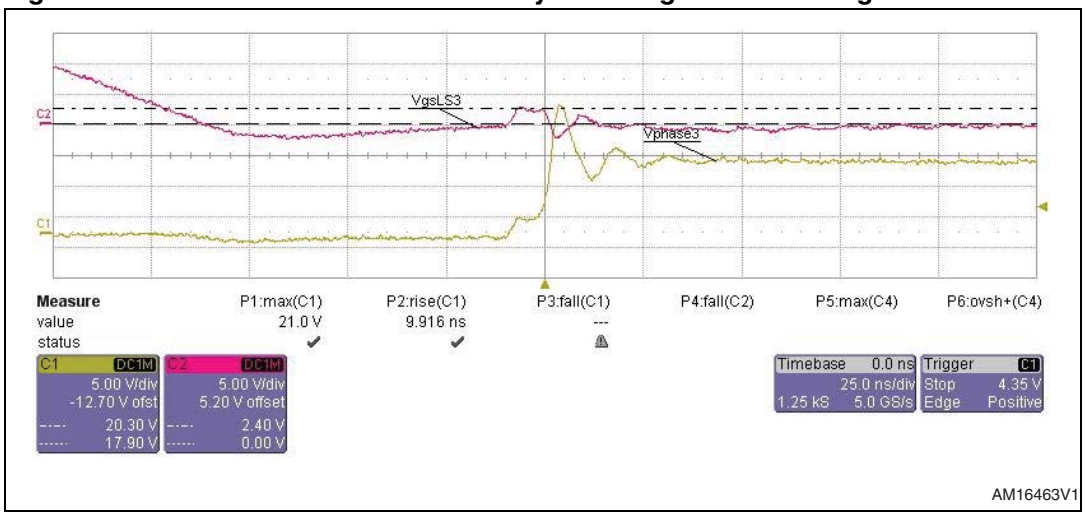


Figure 19. Phase node waveform - HS asymmetric gate drive configuration

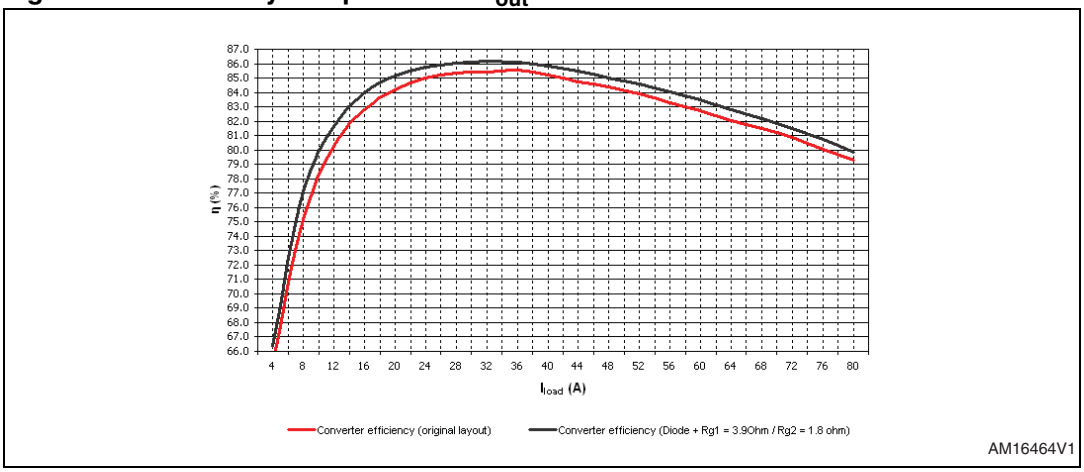


Looking at the previous waveforms, due to the reduced HS turn-on speed, there is a clear reduction of the phase node spike (21 V vs. 24.4 V), when the HS asymmetric gate drive is used. Moreover, the LS gate-source bouncing, induced at HS turn-on, is smoothed.

Comparing the efficiency curves (*Figure 20*), the asymmetric gate drive has slightly better efficiency (+0.7% at full load). This can be explained considering that:

1. The HS turn-off resistor is smaller (1.8 Ω vs. 2.2 Ω) and consequently the switching losses at turn-off are lower.
2. Even if the HS turn-on resistor is bigger, the switching losses at turn-on are negligible.

Figure 20. Efficiency comparison @ V_{out} = 1.26 V



The “asymmetric gate driving” approach can be used to reduce voltage stresses on the phase node without detrimental effects on the converter efficiency. The drawbacks are the number of devices (one resistor + one Schottky diode) and the cost increase.

3 Low-side FET selection

The low-side FET performance can be enhanced by properly choosing the following MOSFET electrical parameters:

1. **$R_{DS(on)}$** (ON-state drain-source resistance): as the LS FET is in the ON-state for a longer time, the conduction losses, strictly related to the $R_{DS(on)}$ value, are the most important power dissipation contribution. Based on the converter layout and the output current requirements, one or more paralleled LS FETs can be used.
2. **C_{GD}** (Miller capacitance): it affects the LS switching behavior, in terms of phase node spike and dVphase/dt. On the other hand, too high C_{GD} values increase the LS "switching charge" ($Q_{G,SW}$): in high frequency applications or when more LS FETs are paralleled to reduce the RDSon, this may increase the switching and gate drive losses, even if the LS switches at nearly ZVS (due to its body diode conduction).
3. **Q_{RR}** (LS body-drain diode reverse recovery charge): during the deadtime (when the HS and LS are in the HOLD state), the load current flows through the body-drain diode (forward biased). When the HS turns on, the excess charge stored in the LS body diode (Q_{RR}) must be removed before the phase node turns high.
4. **R_G** (external and intrinsic gate resistance): when no additional smoothing effects are present (i.e. snubber network), the higher the R_G, the lower the $V_{phase,max}$. The drawback is the LS G-S spurious ringing that may induce the LS spurious turn-on again.

Furthermore, the LS FET performance is also influenced by the RC snubber network setting, connected between LS drain and source, which helps to smooth the phase node noise. Another important aspect is the spurious LS gate-source bouncing, induced by the fast rising edge of the phase node through the Miller capacitance; it is analyzed with a particular focus on the different solutions to reduce these parasitic oscillations. Finally, the converter output voltage (and the converter duty cycle) affects the phase node noise behavior: the higher the V_{OUT}, the lower the phase node overshoot, during the HS turn-on.

3.1 $R_{DS(on)}$ and conduction losses minimization

The LS conduction losses are given by:

Equation 4

$$P_{COND,LS} = R_{DS(on)}|T| \cdot I_D^2 \cdot (1 - D)$$

As the converter duty cycle (for typical VRM applications) is very low (0.1 - 0.2%), the LS FET is in the ON-state for a longer time: the conduction losses are the most important power dissipation term. The $R_{DS(on)}$ minimization is crucial for the optimization of the LS performance. Bigger die sizes are preferred, even though the device cost is a constraint. If the output current to be delivered to the load is high, more LS can be used in parallel.

To better understand the impact of the $R_{DS(on)}$ on the converter efficiency, two LS FETs are compared in a 3-phase buck converter (V_{IN} = 12 V, V_{OUT} = 1.25 V, f_{SW} = 300 kHz, 2 x HS, 2 x LS, I_{OUT} = 75 A; see *Figure 21*). External gate resistances are connected to HS (2.2 Ω) and LS (2.2 Ω) FETs. An RC snubber network (R_{SNUB} = 2.2 Ω, C_{SNUB} = 4.7 nF) is used to smooth the phase node.

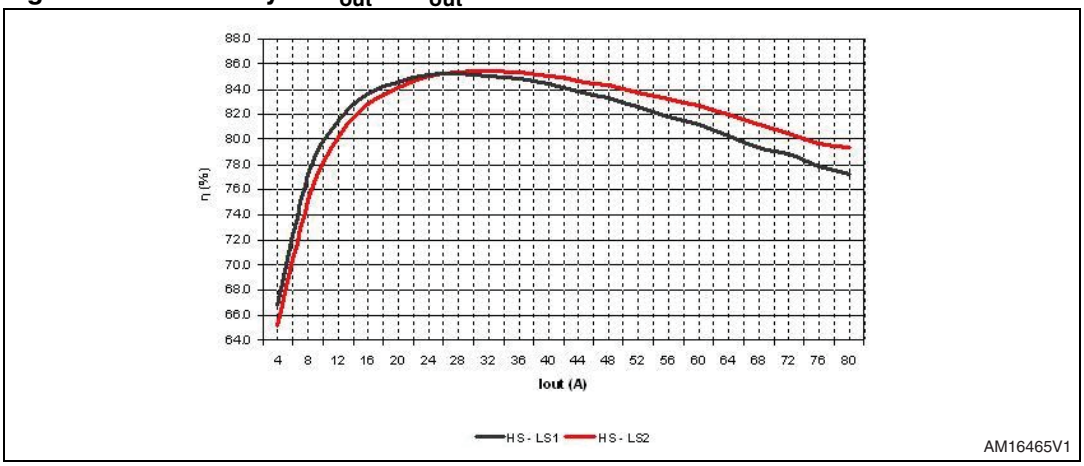
In the following table the main electrical parameters of the two tested LS FETs are reported. The high-side FET used is called “HS”.

Table 3. Main electrical parameters

	BV [V]	$R_{DS(on)}$ [mΩ]	$Q_{g,SW}$ [nC]
HS	25	13	8.5
LS1	30	6	15
LS2	25	5.2	18

As shown in the previous table, the “LS1” has higher $R_{DS(on)}$, but slightly lower total gate charge. In *Figure 21* the relevant efficiency curves are depicted; at low output currents, the LS1, due to its slightly lower Q_g and then switching/gate drive losses, has higher efficiency. But, at medium and heavy load conditions, the $R_{DS(on)}$ improvement makes “LS2” the best in terms of efficiency.

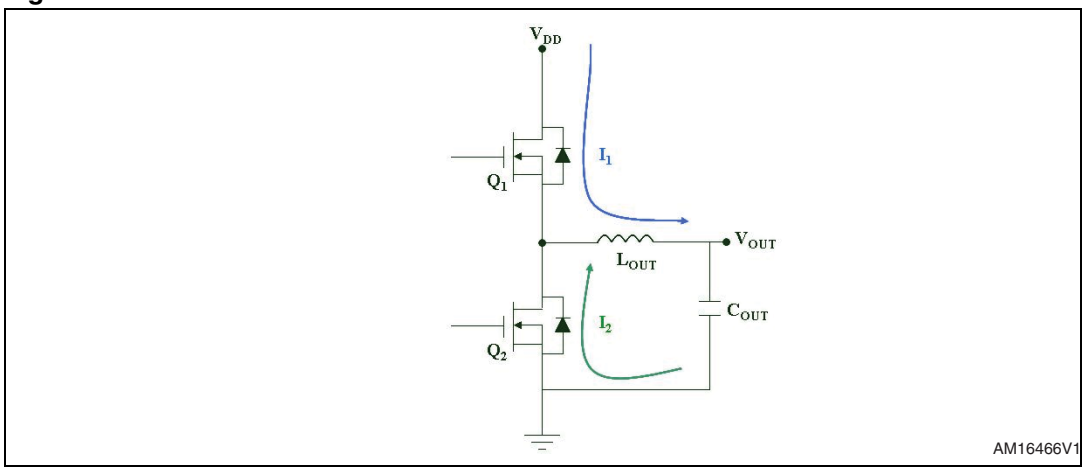
Figure 21. Efficiency vs. I_{out} @ V_{out} = 1.25 V



3.2 C_{GD} (Miller capacitance)

The Miller capacitance (C_{gd}) plays a crucial role in the LS switching behavior improvement. As already known, before the HS turns on, the load current flows through the LS body-drain diode (deadtime) (*Figure 22*, green trace, I2).

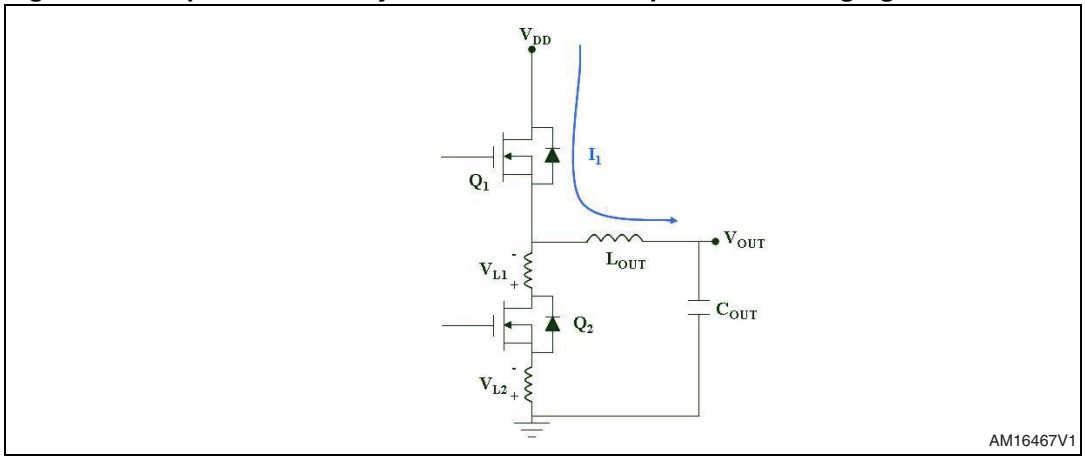
Figure 22. Buck converter schematic



When the HS turns on (the load current is I1), the phase node goes from low to high level in a few nanoseconds: depending on several factors, an overvoltage (plus high frequency oscillations) event may appear on the LS drain-source voltage (phase node ringing): if the maximum spike is higher than the breakdown voltage (BV_{DSS}), the MOSFET safety and reliability can worsen. This issue is related to three main factors:

1. When the HS turns on, $V_{DS,LS}$ rises from -0.7 V (body-drain diode conduction) to supply voltage. If the HS switches sharply (very low $Q_{G,SW}$), high $dV_{DS,LS}/dt$ and phase node spike is measured on the LS FET.
2. During the deadtime, when the load current flows through the LS body-drain diode, parasitic voltage drops (V_{L1} and V_{L2}) appear across the PCB stray inductances (connected to LS drain and source, *Figure 23*). So, the parasitic voltage drops, and V_{L1} and V_{L2} increase the $V_{DS,LS}$ maximum value, creating potential issues for MOSFET safety and reliability, if the maximum spike is higher than the BV_{DSS} guaranteed in the datasheet.
3. During the deadtime, the LS body-drain diode is forward biased ($V_{DS,LS}$ = -0.7 V). This excess stored charge must be removed before the LS can sustain the supply voltage; in order to reverse bias the body diode, a “reverse recovery current” flows (from drain to source) immediately after the HS turn-on. The larger this current is, the higher the phase node spike is. In the next section, there is a more thorough analysis of the benefits given by a “soft” LS body-drain diode.

Figure 23. Impact of the stray inductances on the phase node ringing



In *Figure 24* and *25*, two phase node waveforms of high-C_{RSS} (C_{RSS} = 315 pF) and low-C_{RSS} (C_{RSS} = 190 pF) devices are compared. These FETs are mounted on a 3-phase VRM (f_{SW} = 500 kHz, V_{OUT} = 1.4 V, $R_{G,HS}$ = $R_{G,LS}$ = 2.2 Ω, C_{SNUB} = 4.7 nF, R_{SNUB} = 2.2 Ω) and the load current is 80 A.

Figure 24. Low-C_{RSS} LS FET phase node waveform @ 80 A

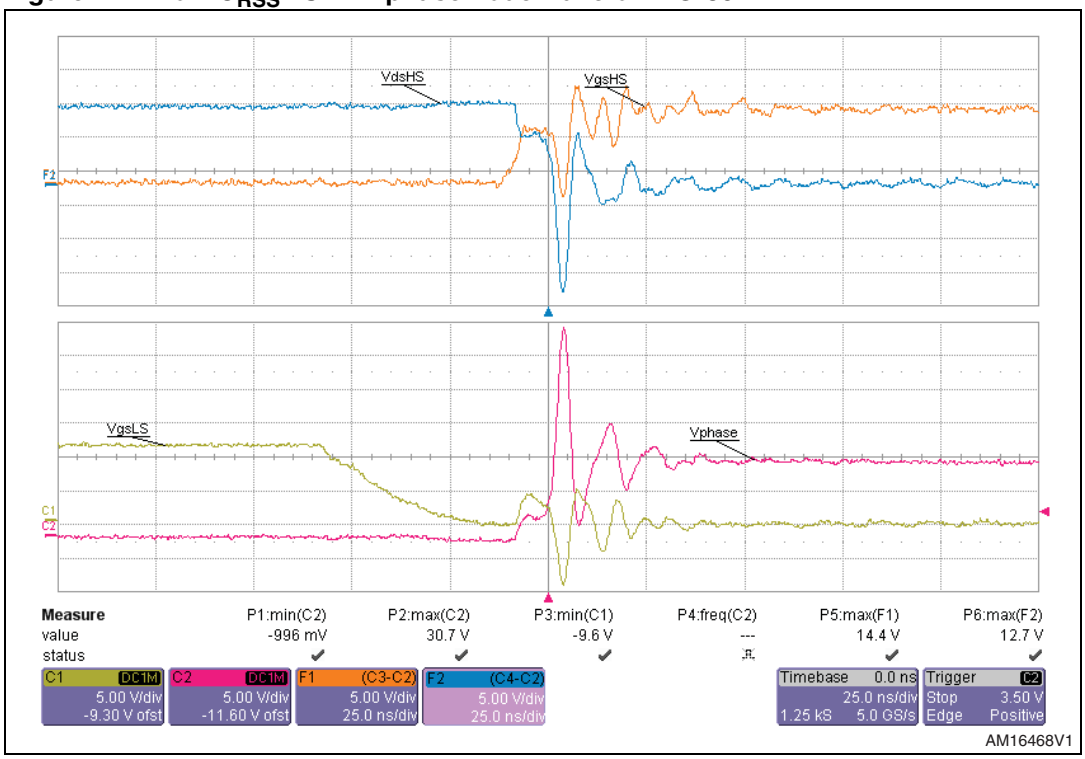
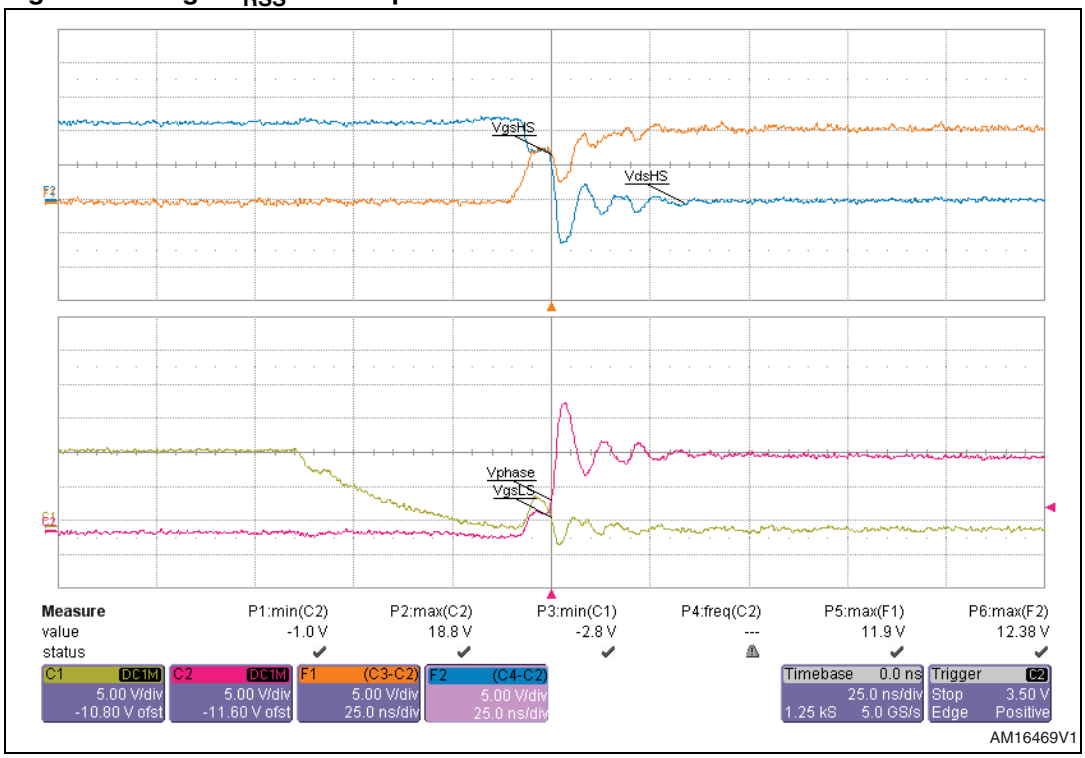


Figure 25. High-C_{RSS} LS FET phase node waveform @ 80 A



As shown in previous images, the “high-C_{RSS}” device has lower phase node spike (18.8 V vs. 30.7 V of the low-C_{RSS} FET).

The right value of the Miller capacitance allows a good improvement on the LS switching behavior, reducing the maximum phase node spike, without detrimental effects on other device features (shoot-through issue, LS gate-source bouncing). Increasing the C_{RSS} value, we obtain some important effects on LS performance:

a) Low-side FET intrinsic slow-down.

b) “Intrinsic and V_{DS} linked” R-C snubber (R_{gate} - C_{RSS}) effect (R_{gate} is the total gate resistance): at HS turn-on, the Miller capacitance is in series with the total gate resistance, creating an “intrinsic” snubber. The capacitive effect is linked to the applied V_{DS} across the LS FET.

c) Higher C_{RSS} value causes a “sub-threshold” conduction, which helps to divert the load current from the body diode (during the deadtime) to the channel, reducing the reverse recovery process stresses.

3.3 LS body-drain diode Q_{rr} (reverse recovery charge)

During the deadtime, when both HS and LS FETs are in the OFF-state, the load current cannot immediately drop to zero so it flows through the LS body-drain diode, that is forward biased ($V_{DS,LS}$ = -0.7 V). In *Figure 26*, the red arrow represents the load current flowing through the body diode. The charge stored in the body diode depends mainly on the load current amplitude and the deadtime length. This charge must be removed before the LS can sustain voltage (OFF-state). In *Figure 27*, from T_0 to T_1, the body diode current becomes negative, depleting the excess charge stored. In this period, the LS body diode acts as the energy source, delivering energy to other components. When the stored charge is totally

removed, the voltage drop across the LS diode becomes equal to the steady-state reverse biased value and, after its turn-on, the HS FET provides all the load current.

Figure 26. Single-phase synchronous buck converter

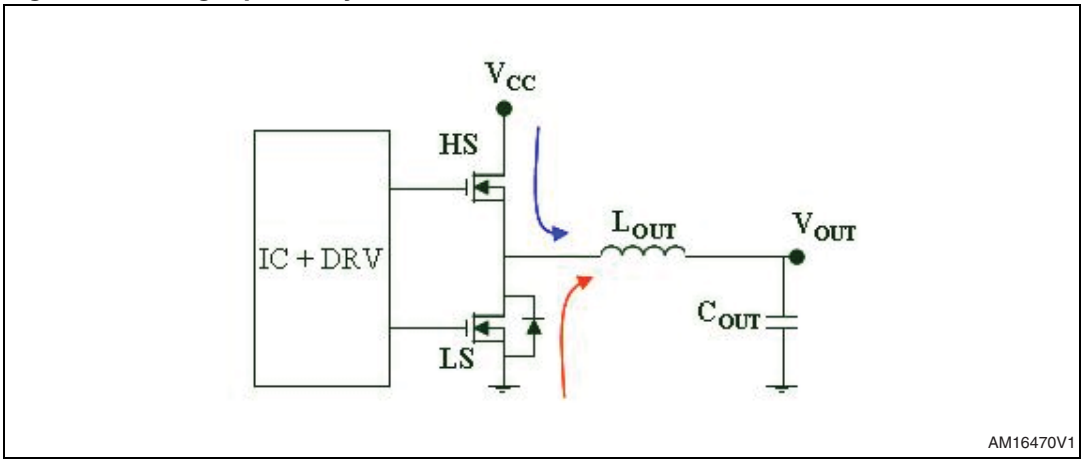
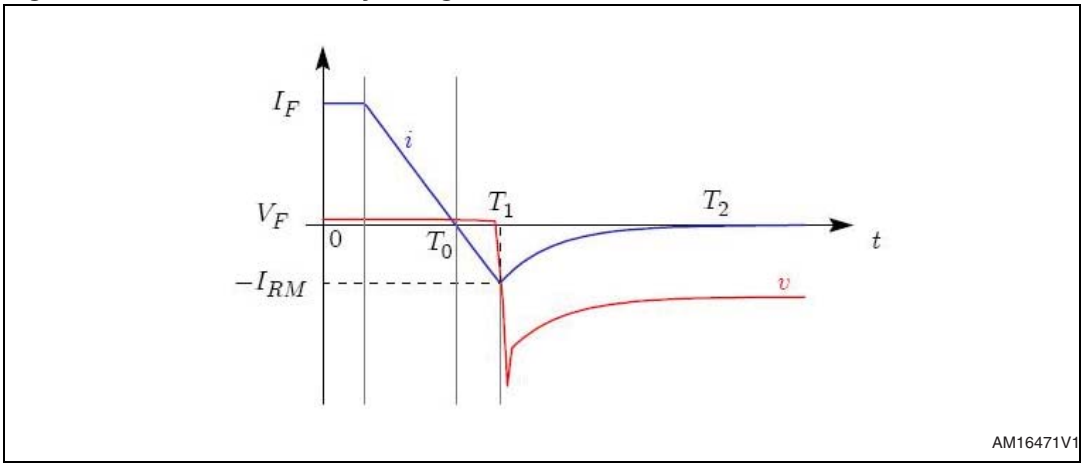


Figure 27. Reverse recovery charge waveforms



The “reverse recovery” charge process causes power dissipation, which depends on the charge amount to be recovered (Q_{rr}), the switching frequency and the converter input voltage:

Equation 5

$$P_{rr} = Q_{rr} \cdot V_{in} \cdot f_{SW}$$

In standard technical literature, the “reverse recovery losses” are added to the HS losses: in fact, as previously explained, during the reverse recovery process, the LS body diode transfers energy to the HS FET, which, in other words, must provide not only the load current but also the diode reverse recovery current.

The body-drain diode optimization plays a crucial role not only for the efficiency improvement but also for the LS switching performance. In fact, reducing Q_{rr} (the excess charge stored during deadtime), the LS body diode transfers less energy (smaller reverse

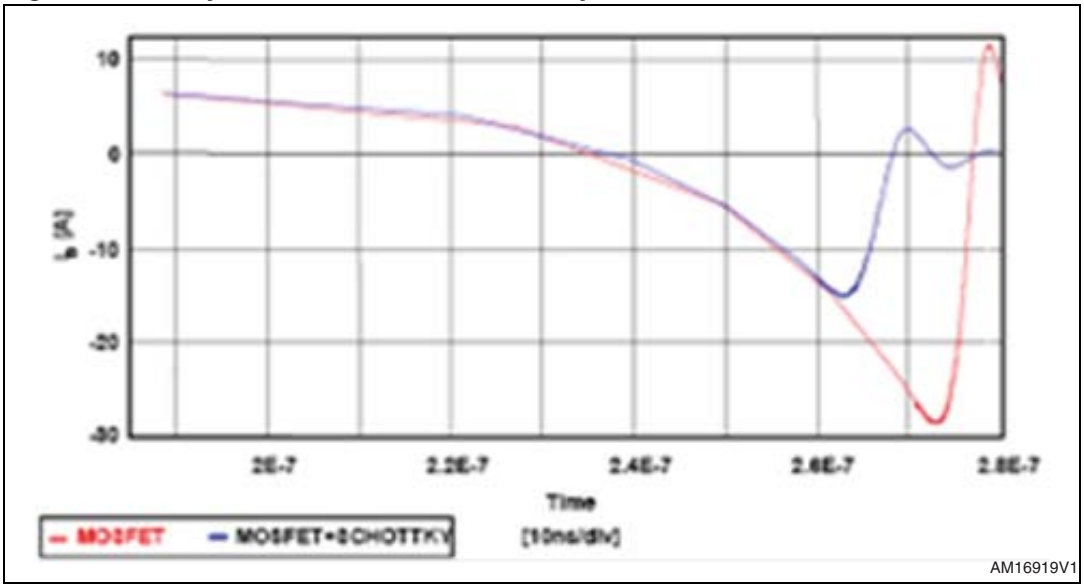
recovery current and losses) to the HS FET and consequently the phase node overshoot is lower.

Typically, to reach this target, a monolithic Schottky diode is integrated inside the same MOSFET structure. This solution eliminates the parasitic effects induced by the stray inductances, which impact negatively on the MOSFET + external Schottky (discrete) configuration. The only drawback is the MOSFET $R_{DS(on)}$ increase due to the Schottky integration and reduction of the active area. The MOSFET with the monolithic Schottky integrated has lower Q_{rr} and V_{FEC} (forward-biased voltage drop), reducing, at the same time, the LS diode conduction losses.

Table 4. Device electrical parameters

	BV [V]	Q_{rr} [nC] I_d = 12.5 A	V_{FEC} [V] I_d = 12.5 A
LS	30	56	0.85
LD + Sch		516	0.68

Figure 28. Body-drain diode reverse recovery current



In a single-phase buck converter demonstration board (V_{IN} = 12 V, V_{OUT} = 1.25 V, f_{SW} = 270 kHz, 1 x HS, 1 x LS, I_{OUT} = 20 A, *Figure 29*), LS and LS+Sch. are compared (*Table 4* and *Figure 28*): the two devices have the same die size but one LS has a monolithic Schottky diode integrated. External gate resistances are connected to HS (2.2 Ω) and LS (1.8 Ω) FETs. An RC snubber network (C_{SNUB} = 6.8 nF, R_{SNUB} = 1.8 Ω) is used to improve the switching behavior.

As shown in the converter waveforms at full load (20 A) (*Figure 30* and *31*), the monolithic Schottky diode integrated helps to smooth the phase node ringing: in fact, for the LS+SCH. device, there is about 10% of V_{phase} decrease (24.2 V vs. 21.7 V).

Figure 29. Single-phase synchronous buck converter schematic

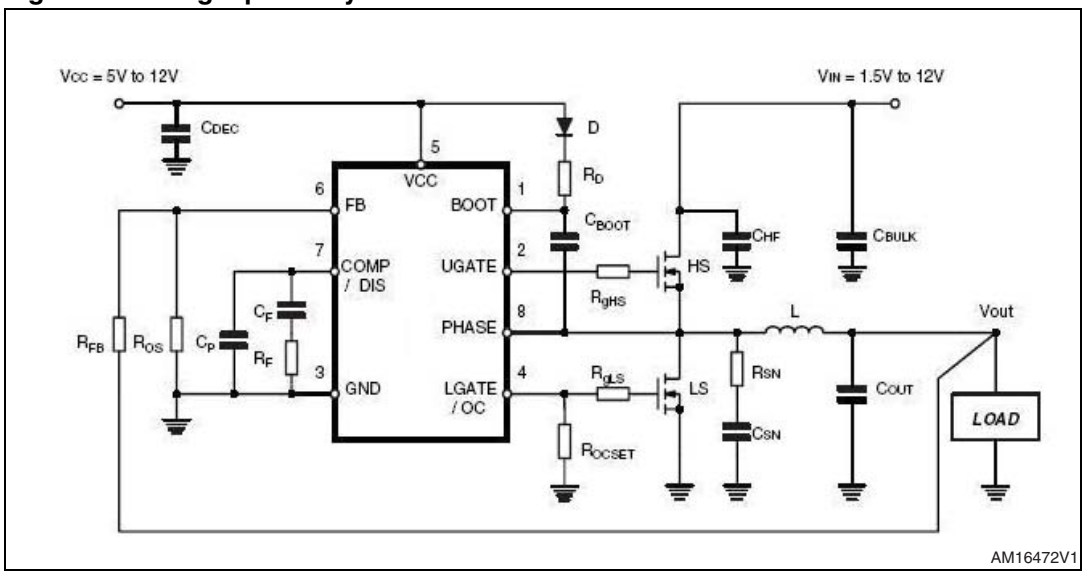


Figure 30. Standard LS waveforms @ 20 A

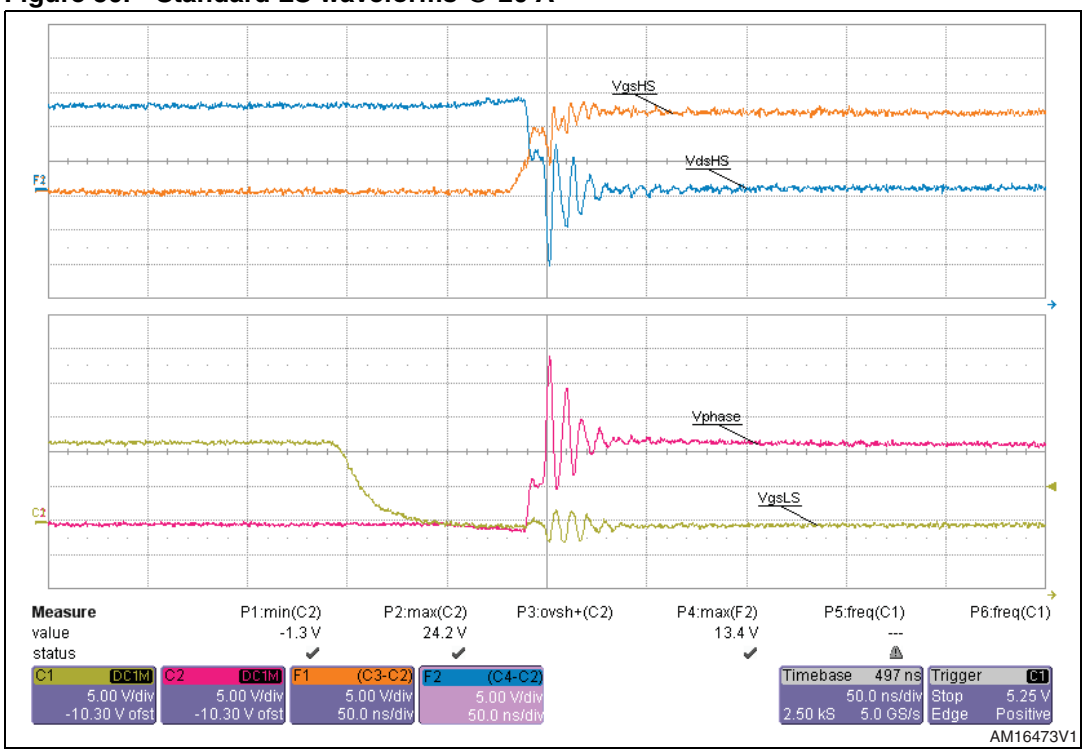
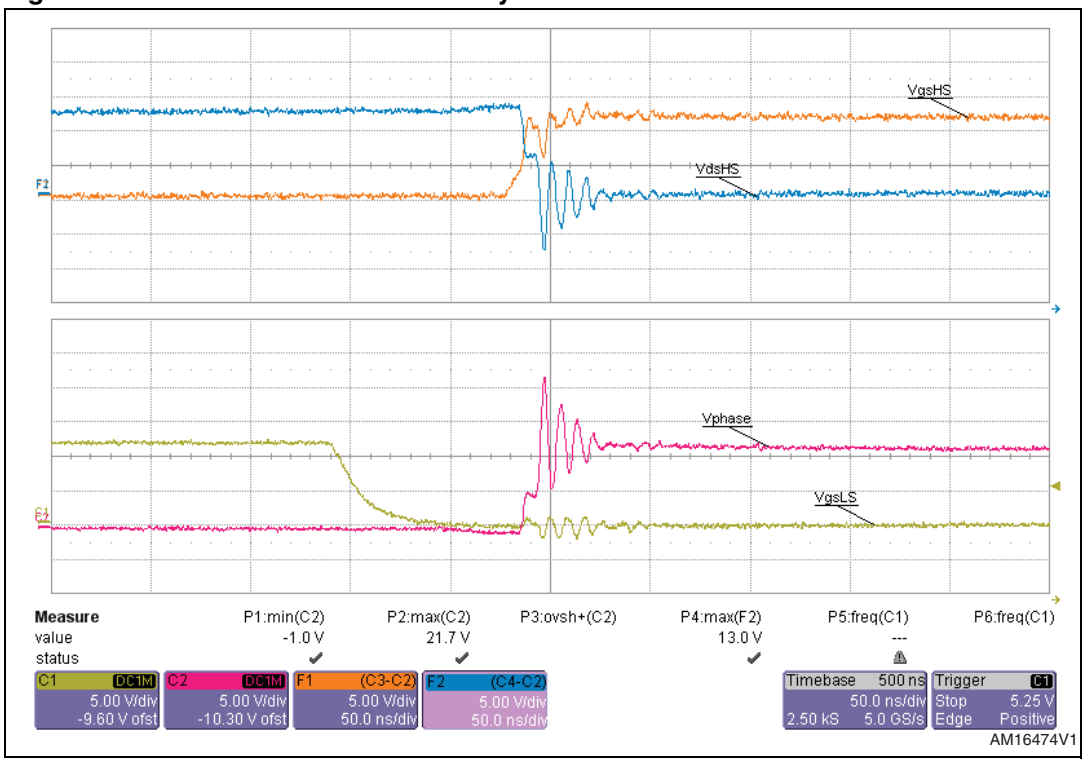


Figure 31. LS with monolithic Schottky diode waveforms @ 20 A



The efficiency improvement caused by an optimized LS body diode can be appreciated only if the converter switching frequency increases: in fact, the higher the f_{SW}, the larger the reverse recovery losses (see (*5*)). We compare the above mentioned LS FETs (LS and LS+Sch.) in a 2-phase synchronous buck converter (V_{IN} = 12 V, V_{OUT} = 1.5 V, f_{SW} = 610 kHz, 2 x HS, 2 x LS, I_{OUT} = 60 A - *Figure 32*). External gate resistances are connected to HS (2.2 Ω) and LS (2.2 Ω) FETs. No snubber network is mounted on the board.

As can be seen in *Figure 33*, at high output currents, due to lower diode conduction and reverse recovery losses, the solution with LS+Sch. has higher efficiency (+1.5% at full load).

Figure 32. 2-phase synchronous buck converter schematic

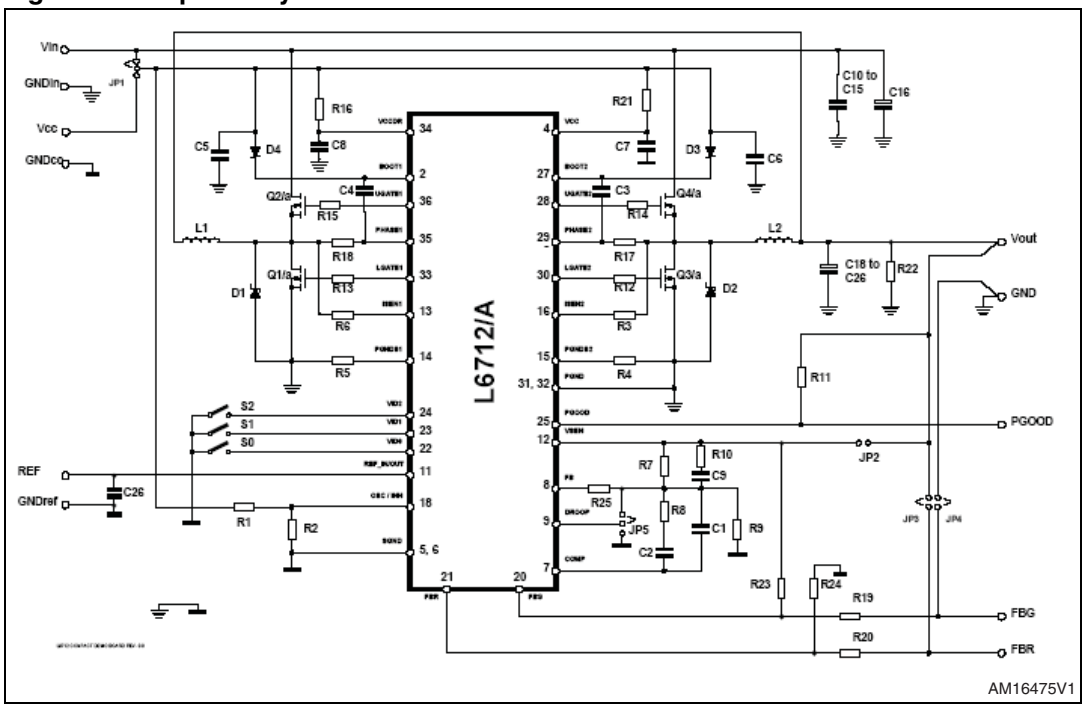
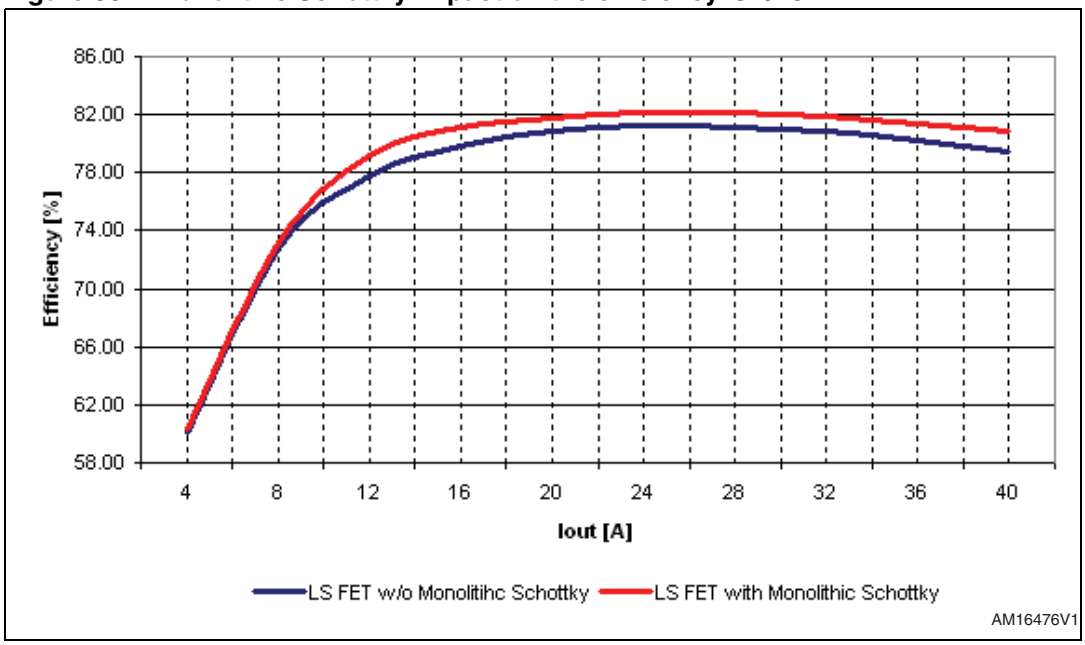


Figure 33. Monolithic Schottky impact on the efficiency @ 610 kHz



Therefore, the choice of an LS FET with monolithic Schottky integrated in the same die is best in high frequency VRM applications, both in terms of efficiency enhancement and device switching behavior improvement.

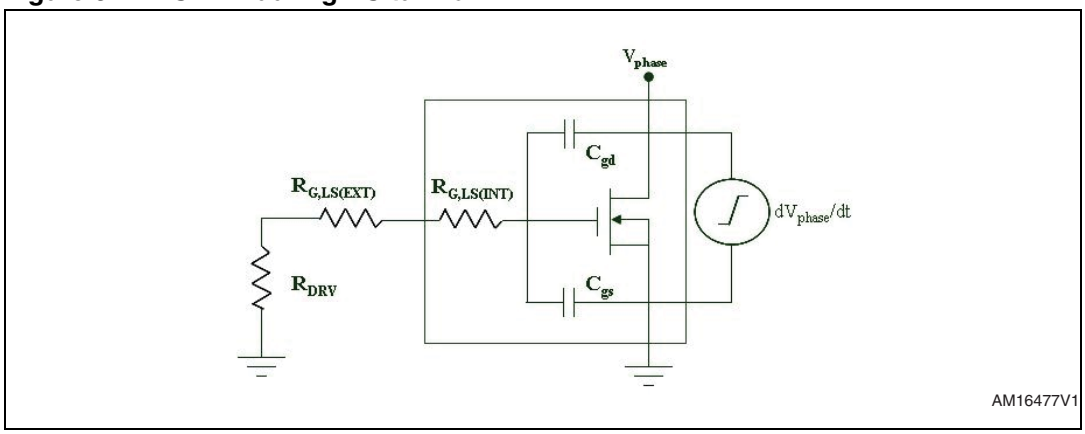
3.4 R_G and LS gate-source bouncing

Now, the impact of the intrinsic and external gate resistances on the overall converter behavior is analyzed.

The intrinsic gate resistance of a MOSFET mainly affects its switching speed and consequently the switching losses. So, for a HS FET, it is mandatory to have a total gate resistance ($R_{G,HS(EXT)} + R_{G,HS(INT)}$) not too big in order to diminish the HS switching losses (major losses contribution), particularly at high f_{SW}.

On the other hand, the LS FET turns on and off with nearly zero voltage drop across it (because, before its turn-on and after turn-off, the current flows through the LS body-drain diode, so $V_{DS,LS}$ = -0.7 V); therefore, the switching losses are not comparable to the conduction ones. The right R_G value should be chosen considering the trade-off between phase node spike smoothing (high R_G) and CdV/dt spurious turn-on immunity (low R_G). In fact, when the HS turns on, a high dV_{phase}/dt appears across the LS device (its value depends also on the HS switching speed).

Figure 34. LS FET during HS turn-on



A capacitive current flows through the Miller capacitance (C_{gd}):

Equation 6

$$I_{gd} = C_{gd} \cdot \frac{dV_{phase}}{dt}$$

During the OFF-state, the LS gate is pulled down to GND through the driver sink resistance (R_{DRV}). So, if $R_{DRV} + R_{G,LS(EXT)} + R_{G,LS(INT)} << Z_{gs}$, most of the capacitive current flows in the resistive path towards GND. As a consequence, a “spurious” voltage drop appears between LS gate and source:

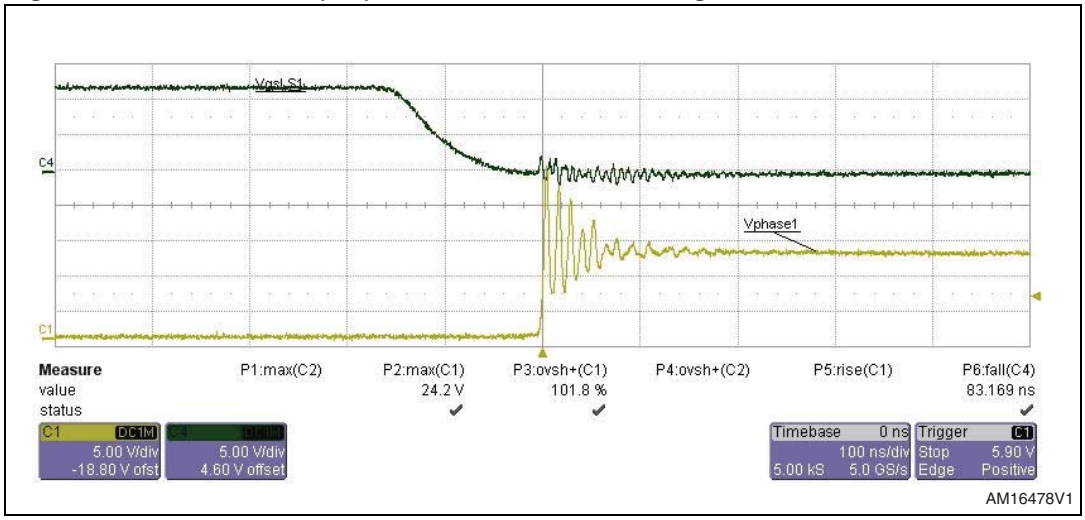
Equation 7

$$V_{gs,LS} = (R_{DRV} + R_{G,LS(EXT)} + R_{G,LS(INT)}) \cdot C_{gd} \cdot \frac{dV_{phase}}{dt}$$

If $V_{gs,LS}$ is higher than the LS threshold voltage, the FET may turn on, creating a low-impedance path, between phase node and GND. There is a potential risk of a “cross-conduction” (or shoot-through) event, because the HS is turned on and a low impedance path between V_{DD} and GND exists.

Due to the above mentioned issue, in most VRM applications, one common design guideline is to reduce the total gate resistance.

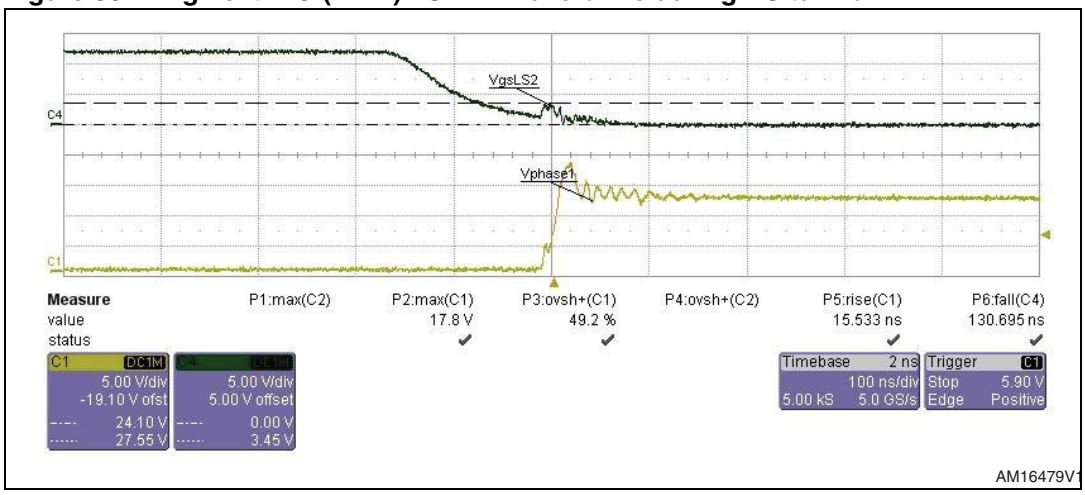
Figure 35. Low ext. RG (2 Ω) LS FET waveforms during HS turn-on



Increasing $R_{G,LS(EXT)}$, there are three main effects on the LS switching behavior:

- A higher induced voltage appears between gate and source (*7*) (see *Figure 36*).
- Longer VGS, LS fall time (130 ns vs. 83 ns), due to the input time constant enlargement (the LS VGS bounces before reaching zero level).
- Phase node overshoot reduction, because of the intrinsic LS slow-down.

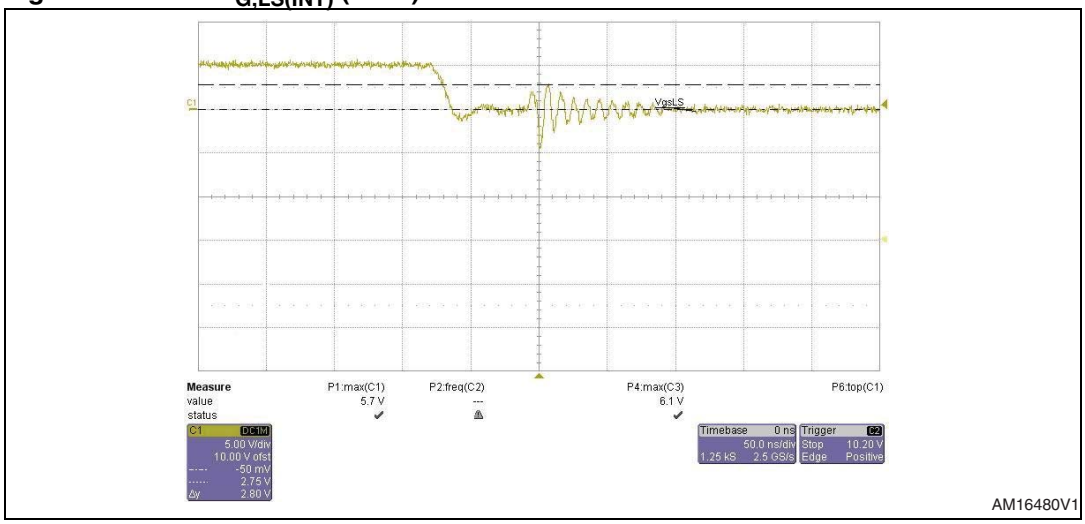
Figure 36. High ext. RG (4.7 Ω) LS FET waveforms during HS turn-on



Generally, the higher the $R_{G,LS(EXT)}$, the lower the efficiency, due to bigger gate drive losses. In particular, the efficiency loss is much higher when more LS FETs are paralleled or bigger die size devices are used (more capacitances to be switched on/off). For the above mentioned issues, typically, the more common $R_{G,LS(EXT)}$ values are 0 - 2.2 Ω

In the same way, by increasing the LS intrinsic gate resistance ($R_{G,LS(EXT)}$), the spurious gate-source voltage tends to grow (see *Figure 37* and *38*).

Figure 37. Low $R_{G,LS(INT)}$ (1.5 Ω) LS FET waveforms @ full load



In these images the LS gate-source waveforms for two 30 V LS devices are depicted: the first has $R_{G,LS(INT)}$ = 1.5 Ω, the second has 3 Ω The spurious LS G-S voltage drop rises (5.5 V vs. 2.7 V), if only for a very short time (2-3 ns).

Figure 38. High $R_{G,LS(INT)}$ (3 Ω) LS FET waveforms @ full load

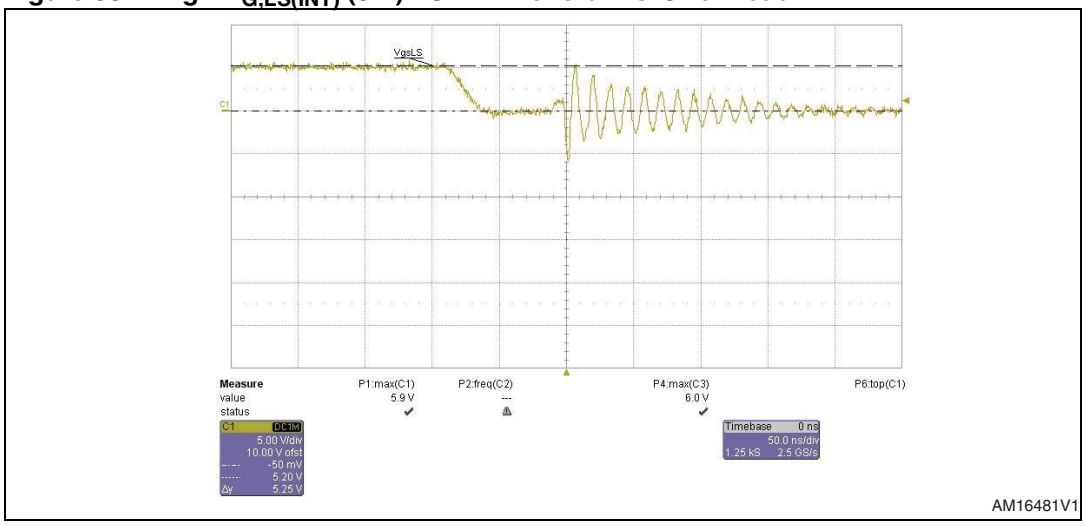
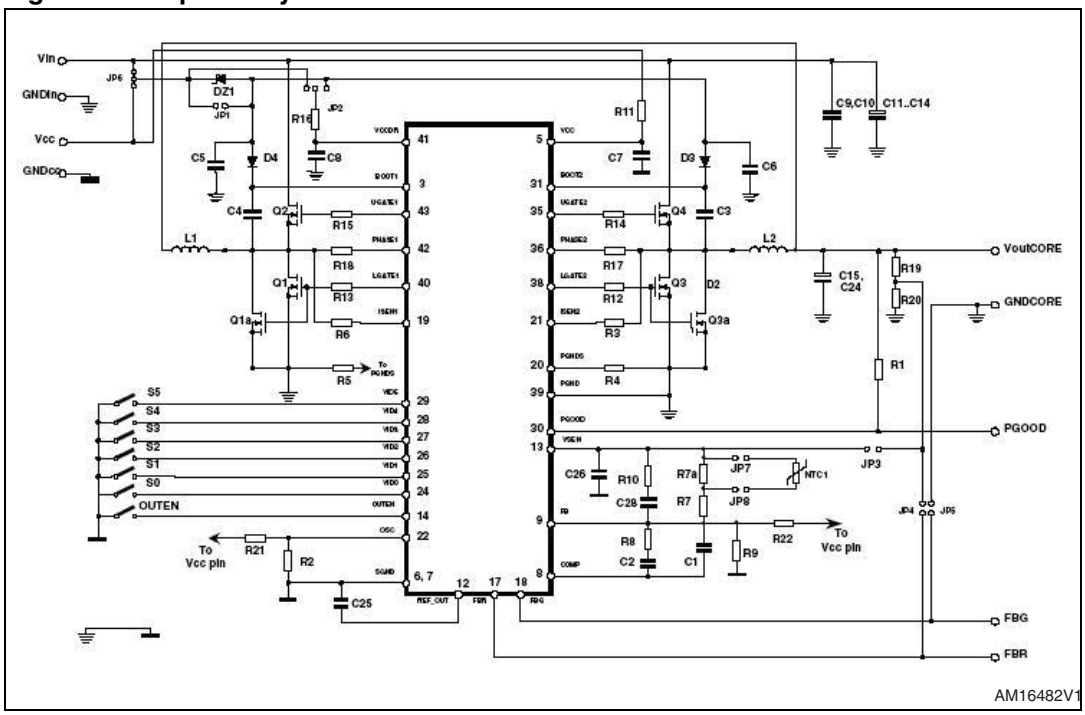


Figure 39. 2-phase synchronous buck converter



In a 2-phase synchronous buck converter (*Figure 39*) (V_{IN} = 12 V, V_{OUT} = 1.5 V, I_{OUT} = 44 A, 1 x HS, 2 x LS, f_{SW} = 440 kHz), two LS FETs with different $R_{G,INT}$ values (R_{G1} = 1.3 Ω, R_{G2} = 2.8 Ω) are compared. External HS and LS gate resistances are present in the layout ($R_{G,HS}$ = 2.2 Ω, $R_{G,LS}$ = 2.2 Ω).

Higher intrinsic gate resistance is helpful to smooth the phase node overshoot, when no RC snubber network is connected in parallel to the LS FET. In *Figure 40* and *41* the phase node waveforms of the two LS FETs tested at full load conditions (I_{OUT} = 44 A) are compared.

Figure 40. Low $R_{G,LS(INT)}$ (1.3 Ω) waveforms @ full load

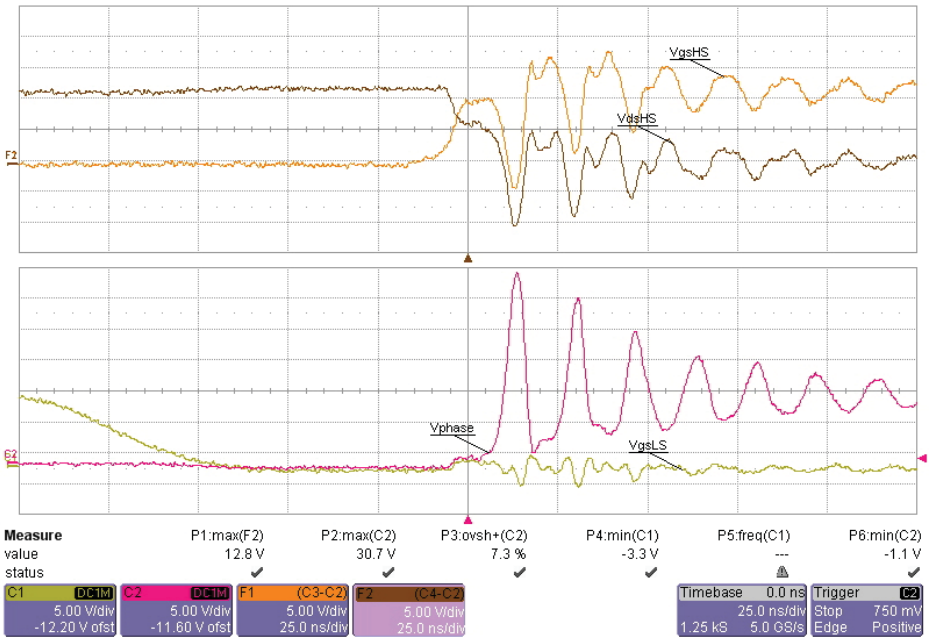
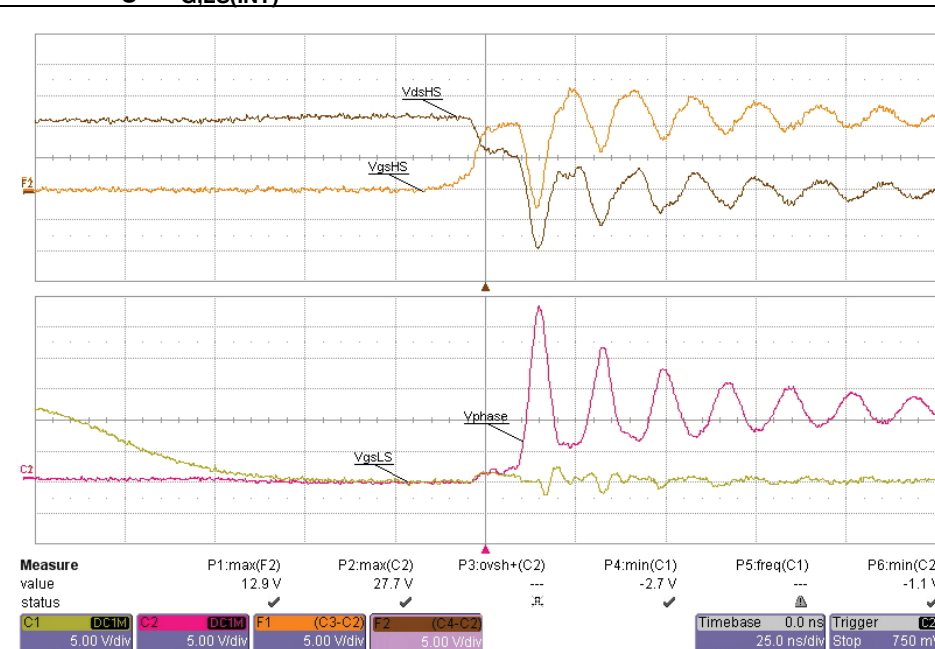


Figure 41. High $R_{G,LS(INT)}$ waveforms @ full load

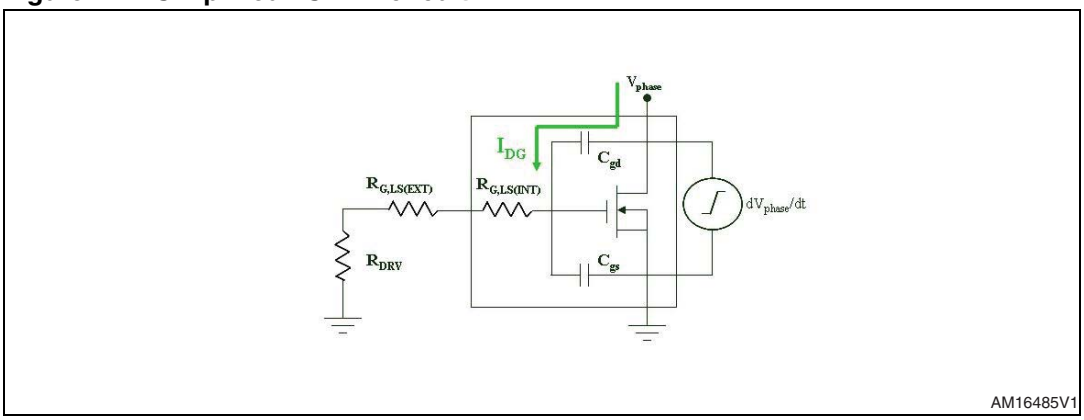


As shown in the previous images, there is a 10% reduction on the phase node spike, due to the intrinsic LS slow-down.

It is important to underline that the same benefit in terms of phase node spike reduction is not evident with an RC snubber network mounted on the board, which provides the

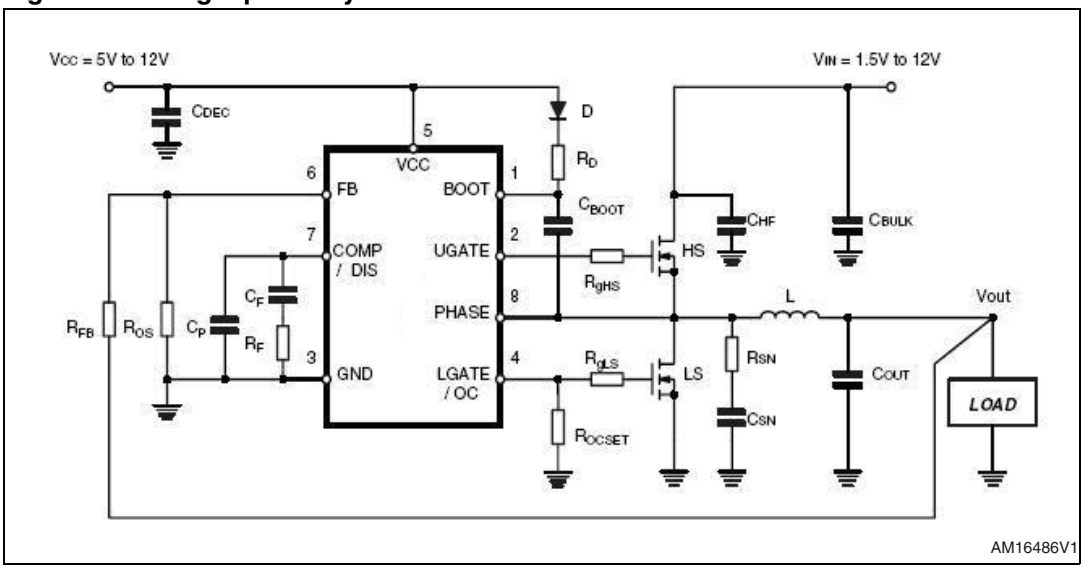
strongest smoothing effect. Another important phenomenon that affects the LS switching performance is the LS gate-source spurious oscillations. When the HS turns on, spurious ringing appears between LS gate and source, caused by high dV_{phase}/dt and the parasitic effects due to the PCB stray inductances (at all the MOSFET pins).

Figure 42. Simplified LS FET circuit



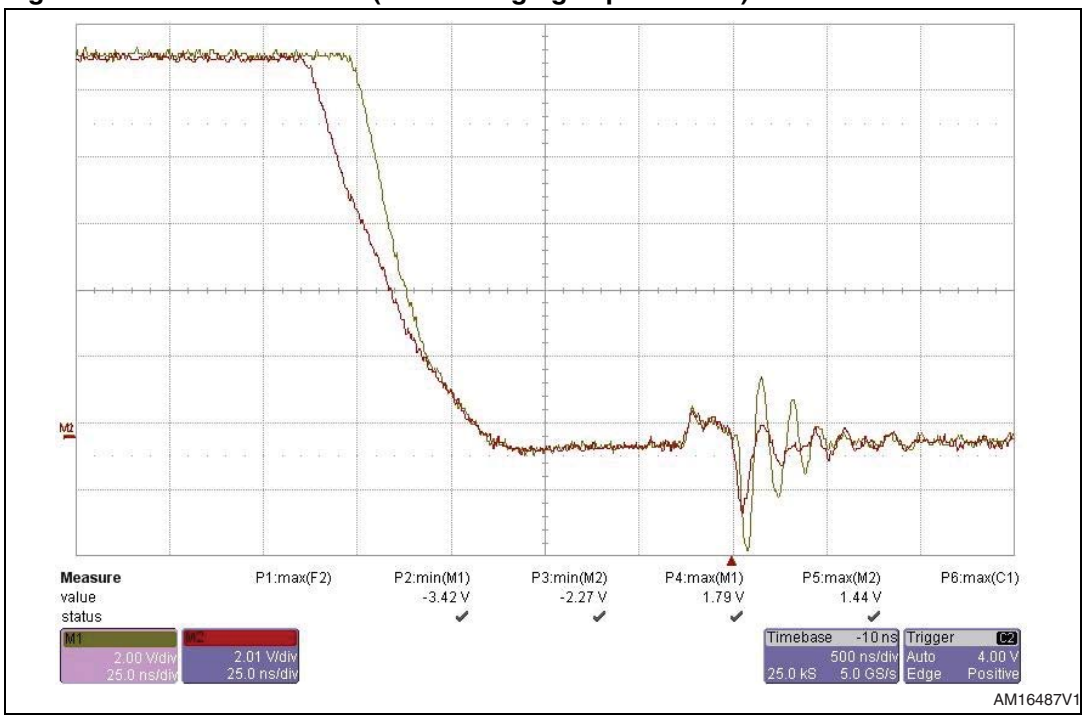
To reduce the phase node spike and therefore LS gate-source parasitic fluctuations, the "filter effect" provided by the MOSFET intrinsic output capacitance ($C_{OSS} = C_{GD} + C_{DS}$) is important. In fact, C_{OSS} works as an "intrinsic" capacitive snubber between drain and source.

Figure 43. Single-phase synchronous buck converter schematic



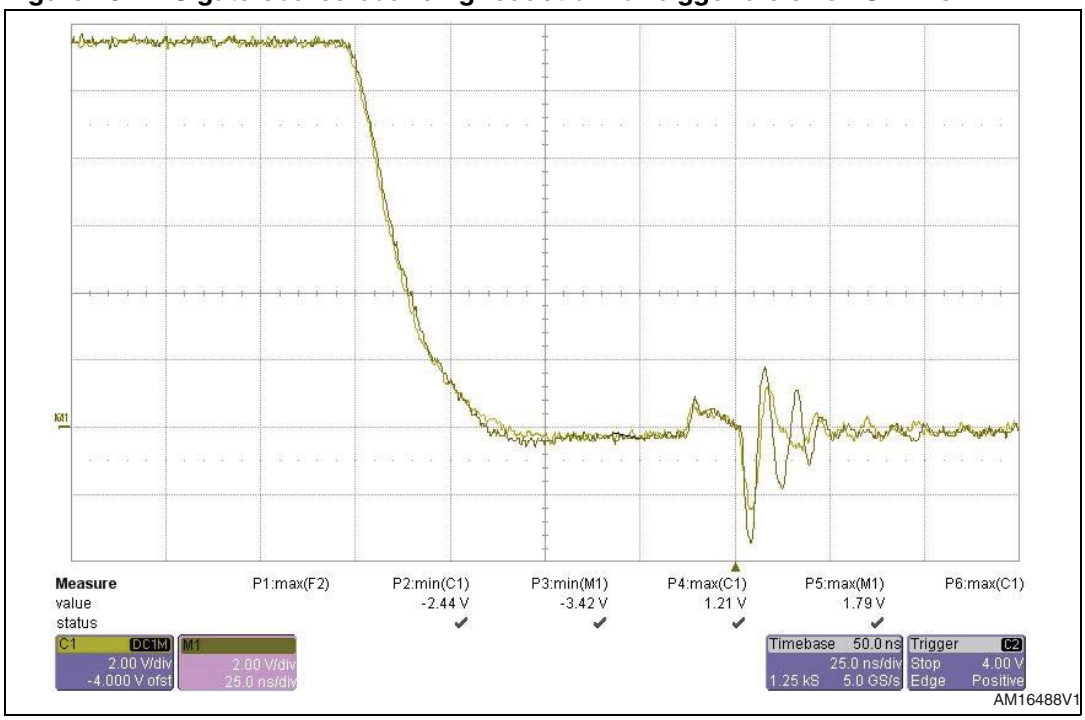
In a single-phase buck converter demonstration board (V_{IN} = 12 V, V_{OUT} = 1.25 V, f_{SW} = 270 kHz, 1 x HS, 1 x LS, I_{OUT} = 20 A, *Figure 43*), the benefits given by two paralleled 30 V FETs (doubled C_{gs}) in terms of LS G-S induced ringing are evaluated. External gate resistances are connected to HS (2.2 Ω) and LS (2.2 Ω) FETs. An RC snubber network (C_{SNUB} = 6.8 nF, R_{SNUB} = 1.8 Ω) is used to improve the switching behavior. As shown in *Figure 44* (purple trace: 2 x LS - yellow trace: 1 x LS), the two paralleled LS FETs have smoothed high frequency LS oscillations, both in the highest and in the lowest spike.

Figure 44. 1 x LS vs. 2 x LS (LS G-S ringing improvement)



The conspicuous reduction of the LS gate-source bouncing (especially for the high frequency oscillation after the first spike) provided by the increased C_{OSS} is obtained also using a bigger die size LS device, as shown in *Figure 45* (light green trace: LS1, dark green trace: LS2).

Figure 45. LS gate-source bouncing reduction for bigger die size LS FETs

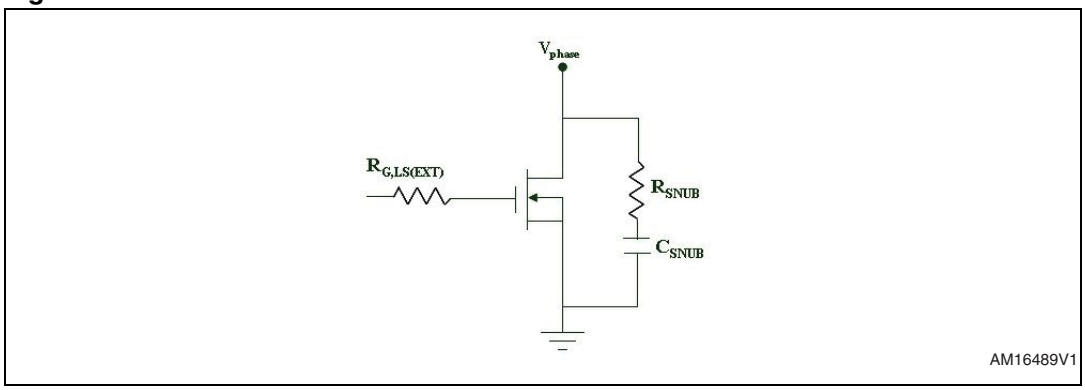


3.5 RC snubber network settings

In high frequency converters, designers must choose the right electric topology and device in order to minimize the switching noise. In particular, when the HS turns on, the LS body diode that was delivering the whole load current must be in the HOLD state. Due to the body diode reverse recovery process and stray inductances, an overshoot may appear on the phase node voltage, affecting the MOSFET reliability. Furthermore, the positive and negative spikes on the phase node waveforms are also dangerous for other electronic components surrounding the LS FET.

The simplest way to reduce these switching oscillations is by connecting an RC snubber network across the LS FET. Theoretically, a simple capacitive snubber would be useful to smooth the switching noise; but, a series resistance is added to decrease the current amplitude during the capacitor discharging and to dissipate the energy at turn-off (when an overvoltage event occurs).

Figure 46. LS FET with RC snubber network



The right R_{SNUB} and C_{SNUB} selection depends on several factors: overshoot reduction, damping effect and energy losses in the snubber circuit:

$$E = \frac{1}{2} \cdot V_{SNUB} \cdot {}_{DD}^{2}$$

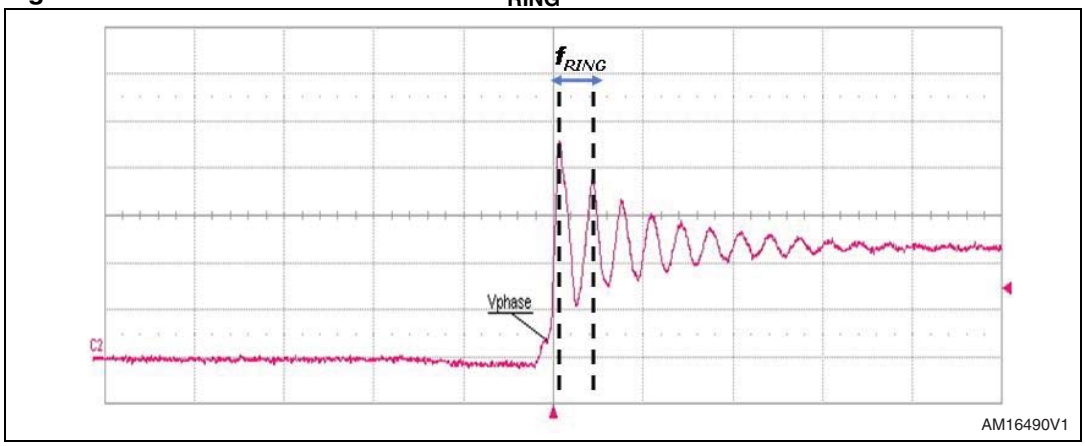
Typically, the snubber resistor is equal to the characteristic impedance of the freely oscillating circuit L-C:

Equation 8

$$R_{SNUB} = \sqrt{\frac{L_{stray}}{C_{oss}}}$$

where L_{stray} includes the PCB and package inductances. Its value can be extrapolated by the phase node waveform, measuring the ringing oscillation f_{RING} (*Figure 47*) and using (*9*):

Figure 47. Phase node waveform and f_{RING} evaluation



Equation 9

$$L_{stray} = \frac{1}{f^2_{RING} \cdot 4\pi^2 \cdot C_{OSS}}$$

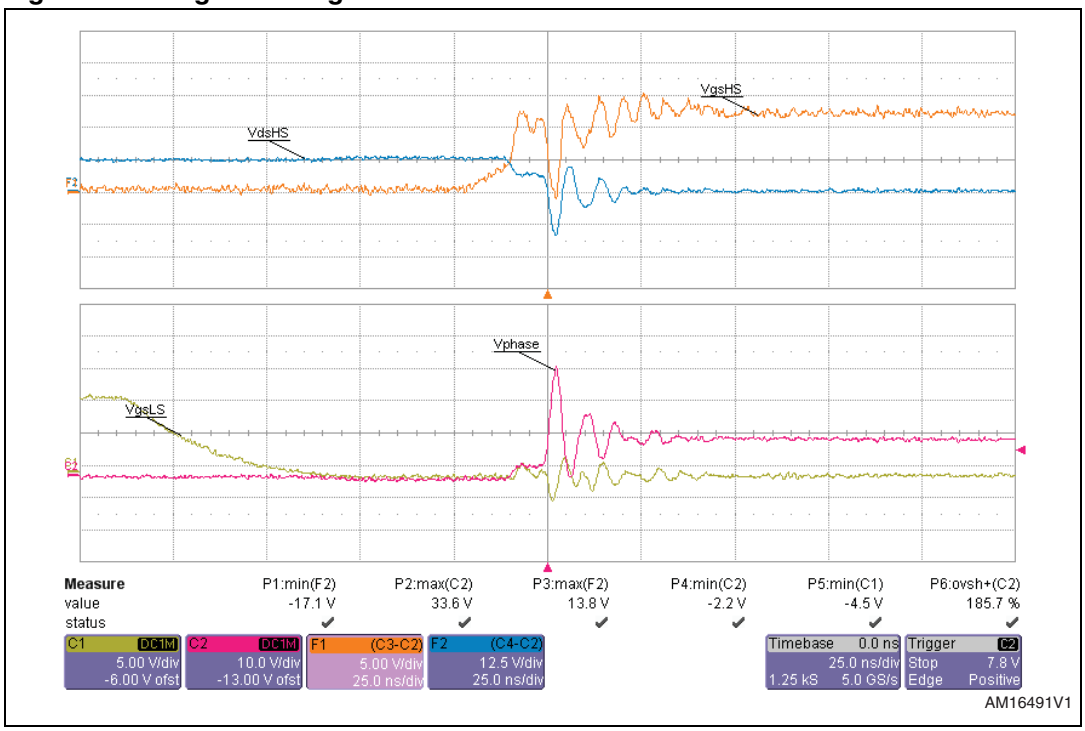
The snubber capacitor value is a trade-off between the over-damping effect (reduction of the number of oscillations) (high C_{SNUB}) and limited energy losses (low C_{SNUB}). Typically, the snubber network constant time (τ_{SNUB}) is chosen as:

Equation 10

$$\tau_{SNUB} = R_{SNUB} \cdot C_{SNUB} = \frac{3}{f_{RING}}$$

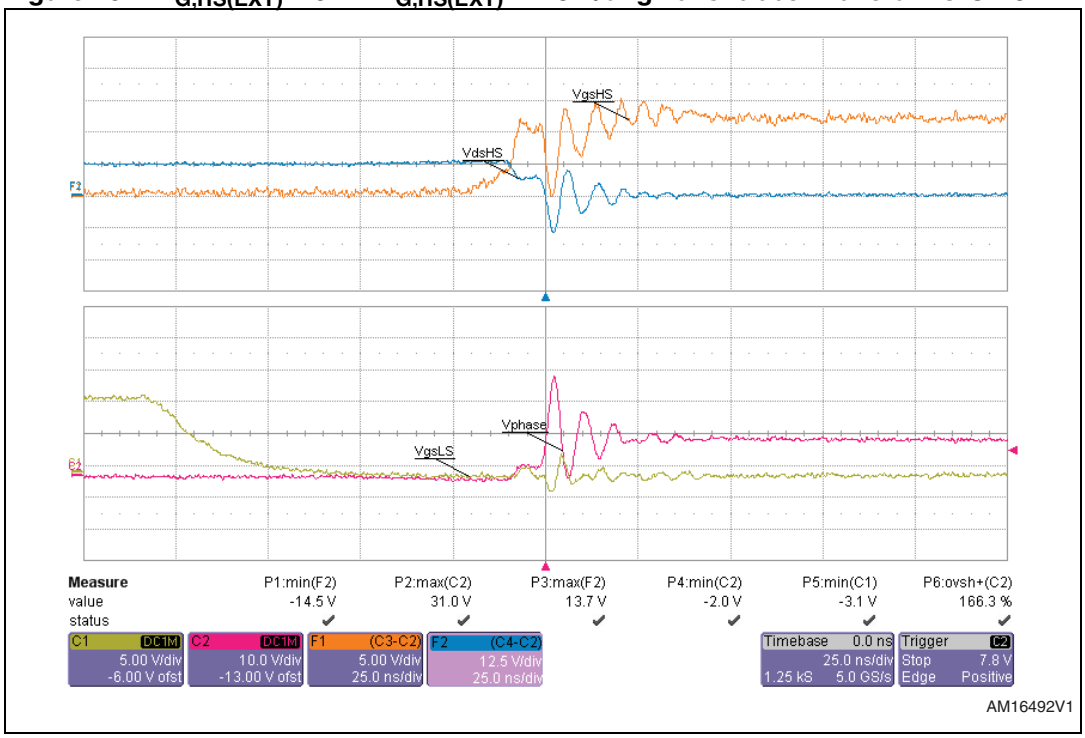
The correct fine tuning of the snubber components, together with a suitable selection of the external gate resistors, allows a sensible reduction of the phase node overshoot. For example, let's consider a single-phase synchronous buck converter (V_{IN} = 12 V, V_{OUT} = 1.25 V, f_{SW} = 270 kHz, 1 x HS, 1 x LS, I_{OUT} = 20 A, with the following original configuration: C_{SNUB} = 6.8 nF, R_{SNUB} = 1.8 Ω, $R_{G,HS(EXT)}$ = 0 Ω, $R_{G,LS(EXT)}$ = 0 Ω). Moreover, a very low $Q_{G,SW}$ HS FET is used to maximize the switching speed and emphasize the phase node ringing issue. In *Figure 48*, the waveforms for the original configuration are shown: the maximum phase node spike is 33.6 V.

Figure 48. Original configuration waveforms @ 20 A



As a first step, the LS external gate resistance is increased to 1.8 Ω ("Configuration 1"); in *Figure 49* the relevant waveforms are depicted. The phase node overshoot is 31 V.

Figure 49. $R_{G,HS(EXT)}$ = 0 Ω - $R_{G,HS(EXT)}$ = 1.8 Ω/original snubber waveforms @ 20 A



Subsequently, the external HS gate resistor becomes 2.2 Ω, while the other components remain unchanged (“Configuration 2”). A further reduction of the phase node spike is achieved (30.1 V). In *Figure 50*, the waveforms at full load conditions are reported.

Finally, the snubber resistor value is decreased from 1.8 Ω to 1 Ω, to emphasize the C_{SNUB} effect (“Configuration 3”). The gate resistors are unmodified (*Figure 51*).

Figure 50. $R_{G,HS(EXT)}$ = 2.2 Ω - $R_{G,HS(EXT)}$ = 1.8 Ω/ original snubber waveforms @ 20 A

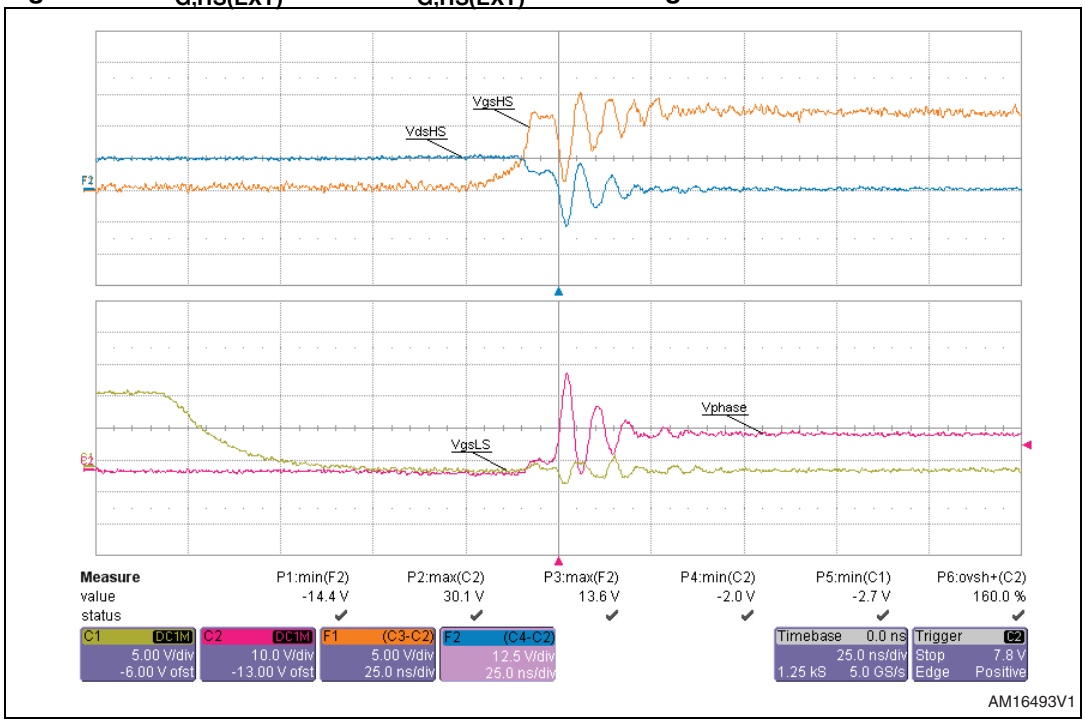
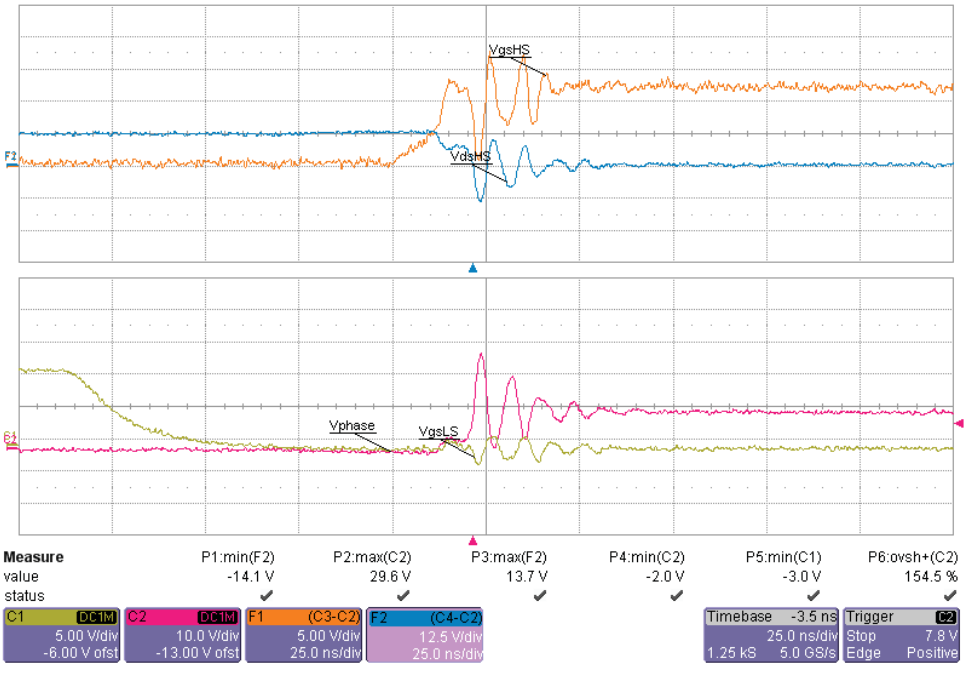


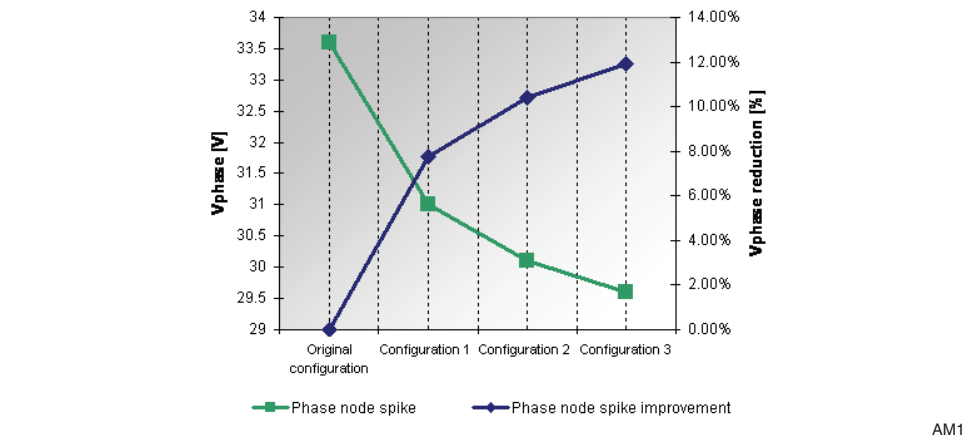
Figure 51. $R_{G,HS(EXT)}$ = 2.2 Ω - $R_{G,HS(EXT)}$ = 1.8 Ω/ R_{SNUB} = 1 Ω waveforms @ 20 A



Therefore, the last configuration is the best in terms of phase node ringing smoothing (12%, from 33.6 V to 29. 6 V, see *Figure 52*).

The increased LS gate resistor value (1.8 Ω) doesn't negatively effect the LS gate-source bouncing and the potential shoot-through risks: this spurious voltage is higher than $V_{TH,min}$ (1 V) for only 1.7 ns; it is not enough to charge the MOSFET input capacitance and turn-on of the device itself.

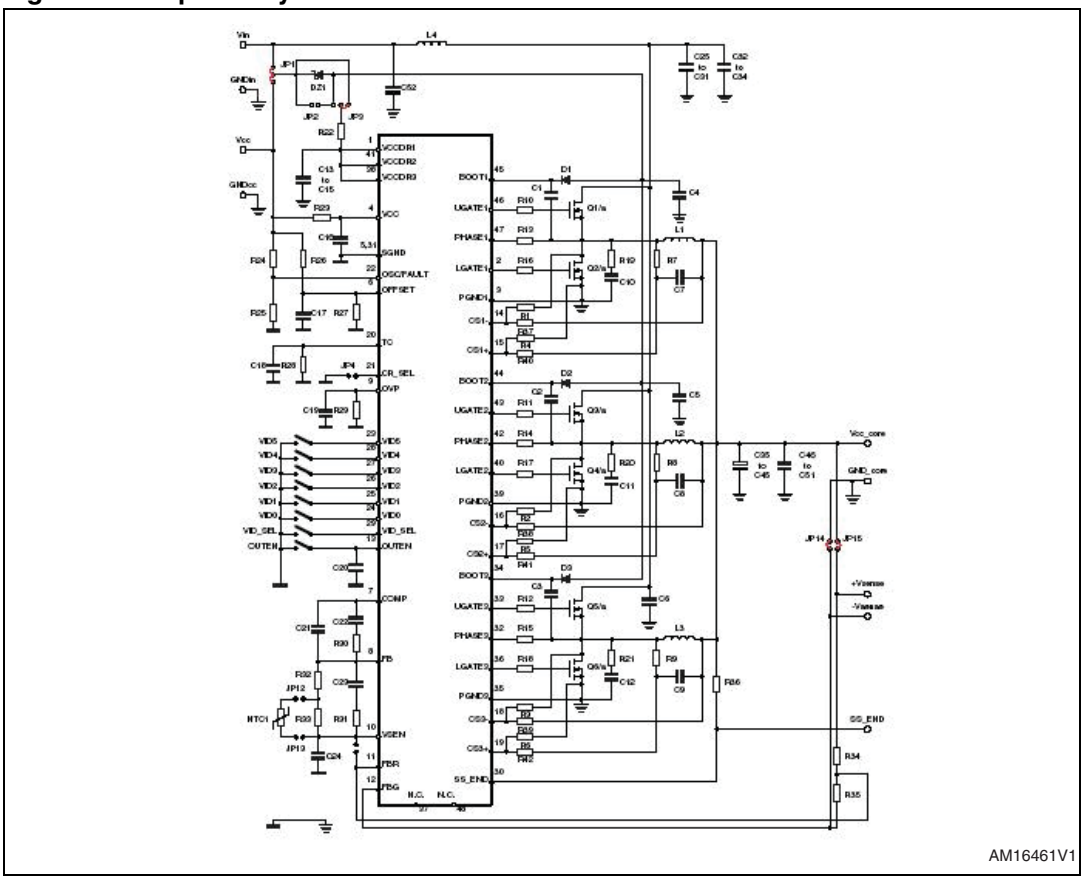
Figure 52. Phase node improvement



3.6 Phase node spike - V_{CORE} relationship

Let's consider the impact of a different output voltage on the phase node ringing. In *Figure 53* the schematic of a 3-phase synchronous buck converter (V_{IN} = 12 V, V_{OUT} = 1.25 V, f_{SW} = 270 kHz, 2 x HS, 2 x LS, I_{OUT} = 75 A) is depicted. External gate resistances are connected to HS (2.2 Ω) and LS (2.2 Ω) FETs. An RC snubber network (R_{SNUB} = 2.2 Ω, C_{SNUB} = 4.7 nF) is used to smooth the phase node.

Figure 53. 3-phase synchronous buck converter



Adjusting a 6-pin DIP switch configuration, it is possible to change the converter output voltage, from 2.5 V to 3.3 V. In *Figure 54* and *55*, the relevant waveforms are reported.

Figure 54. Phase node waveform @ 2.5 V

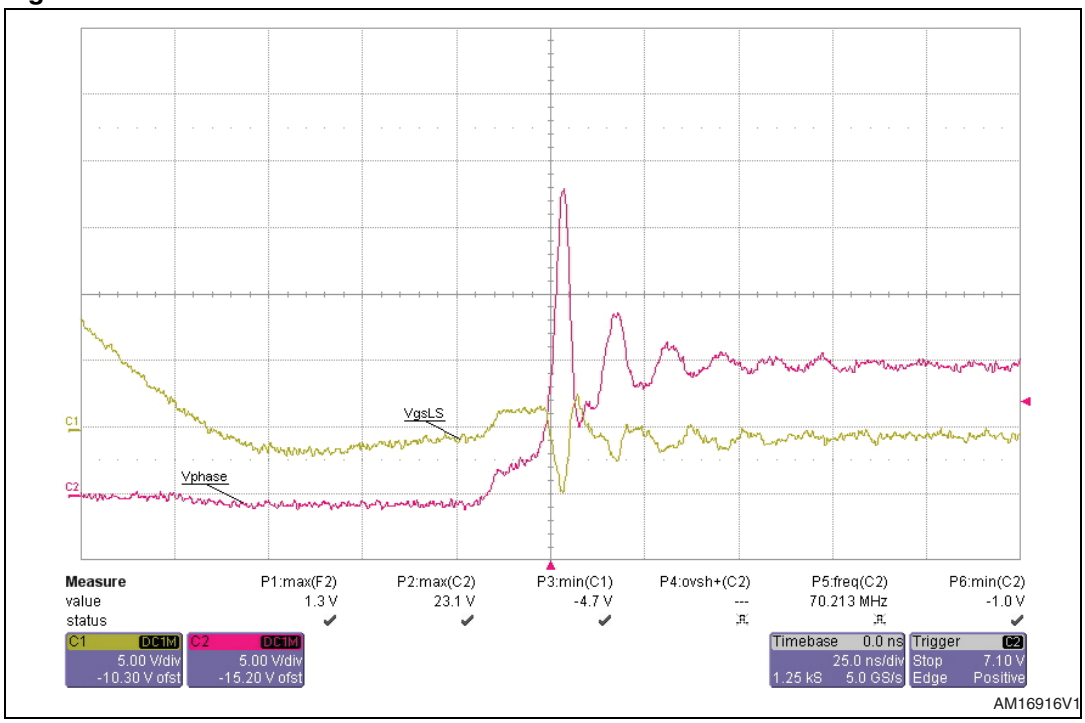
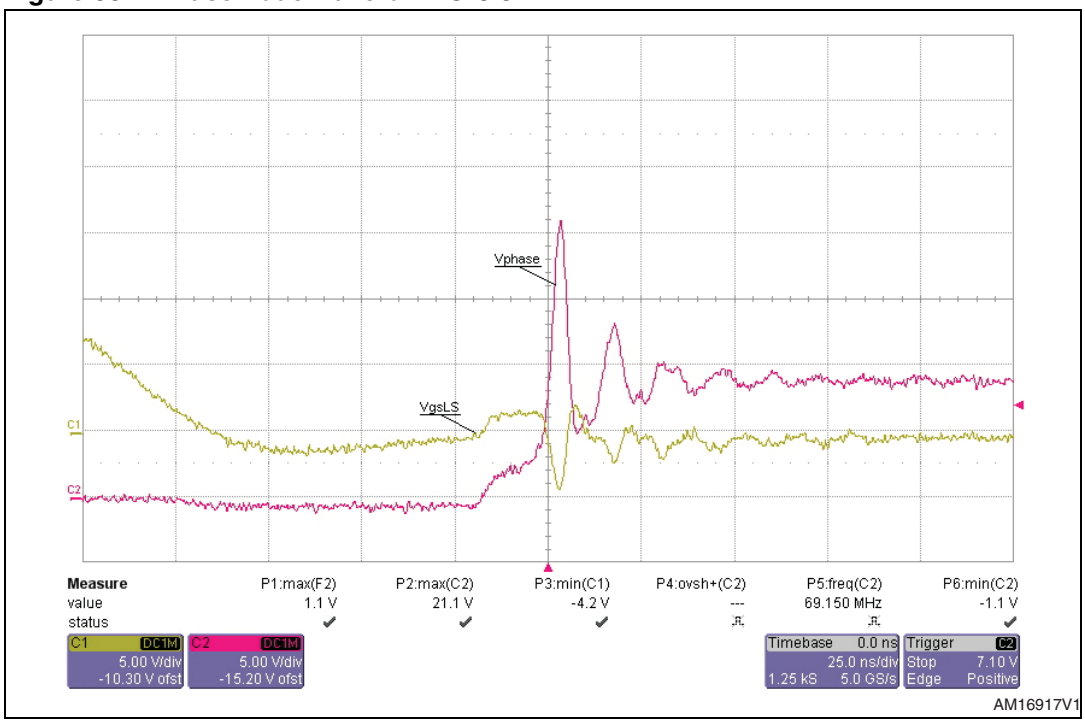
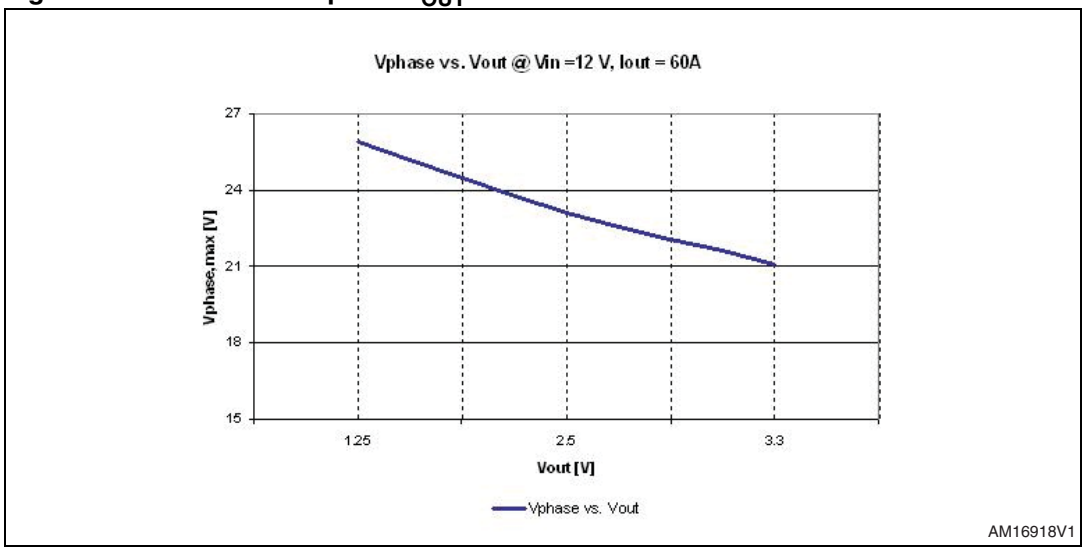


Figure 55. Phase node waveform @ 3.3 V



As shown in the previous images, by increasing the output voltage the phase node spike decreases (*Figure 56*). This is due to the higher HS ON-state interval and to its lower switching speed.

Figure 56. Phase node spike - V_{OUT} chart



4 Conclusion

The main electrical parameters for correct MOSFET selection in VRM applications are QG and intrinsic capacitances for high-side FETs, while $R_{DS(on)}$, Q_{RR} and C_{GD} are crucial for LS FETs.

5 Bibliography

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   c) Fairchild Semiconductor AN6005, Synchronous buck converter power losses calculation.
   d) T.Wu, Cdv/dt induced turn-on in synchronous buck regulators.
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   g) Q.Zhao,G.Stojcic, Characterization of CdV/dt induced power losses in synchronous buck DC-DC converters.
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6 Revision history

Table 5. Document revision history

Date	Revision	Changes
13-Nov-2012	1	Initial release.