AN4199
Application note

Two-layer demonstration board based on the STA333IS

Introduction

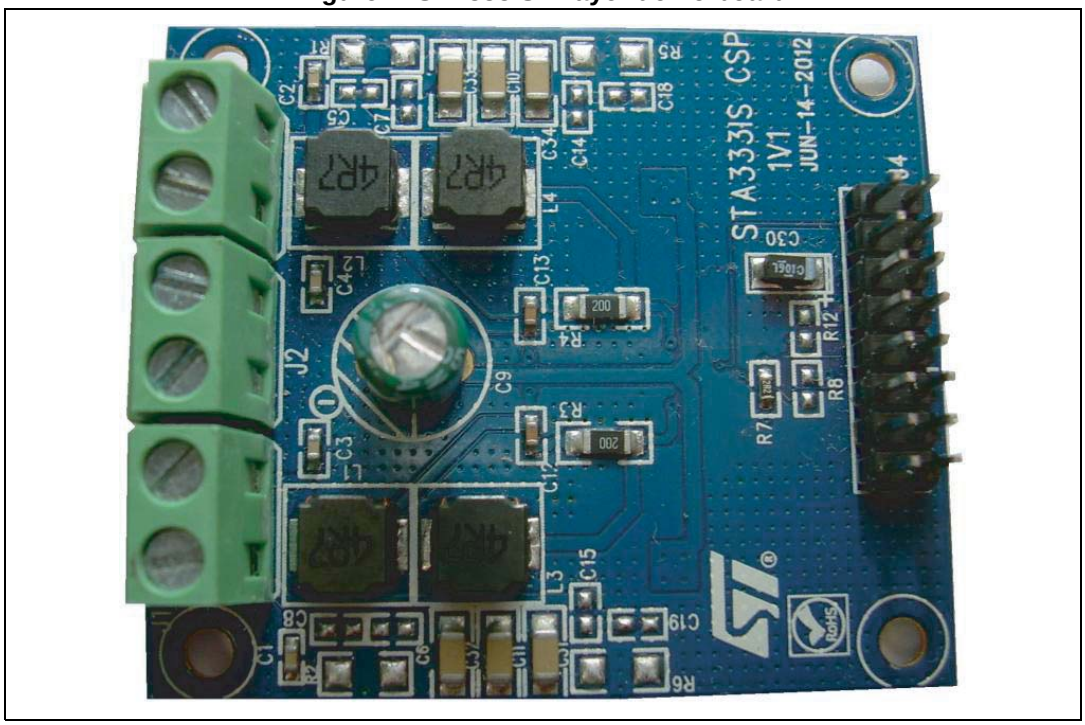
The board shown in *Figure 1* is a two-layer demonstration board designed for the evaluation of the STA333IS two-channel, high-efficiency Sound Terminal® device.

The purpose of this application note is to show:

- how to connect the STA333IS demonstration board
- the performance of the STA333IS device
- how to avoid critical board and layout issues

All the results and characterization data included in this application note have been measured using Audio Precision equipment. Reference documents consist of the STA333IS datasheet, schematic diagrams and PCB layout.

Figure 1. STA333IS 2 layer demo board



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1 Test conditions and connections of demonstration board

1.1 Power supply signal and interface connection

1. Connect the power supply to the $+V_{CC}$ and GND terminal blocks (J2)
2. Connect the STEVAL-CCA035V1 interface board to the J4 connector
3. Connect the S/PDIF signal cable to the RCA jack on the STEVAL-CCA035V1 board. The signal source should be the Audio Precision equipment or a DVD player.
4. Adjust the voltage level of the power supply. The voltage range of the DC power supply is 4.5 V to 18 V.
5. Connect the load to the connectors J1 and J3

1.2 Output configuration

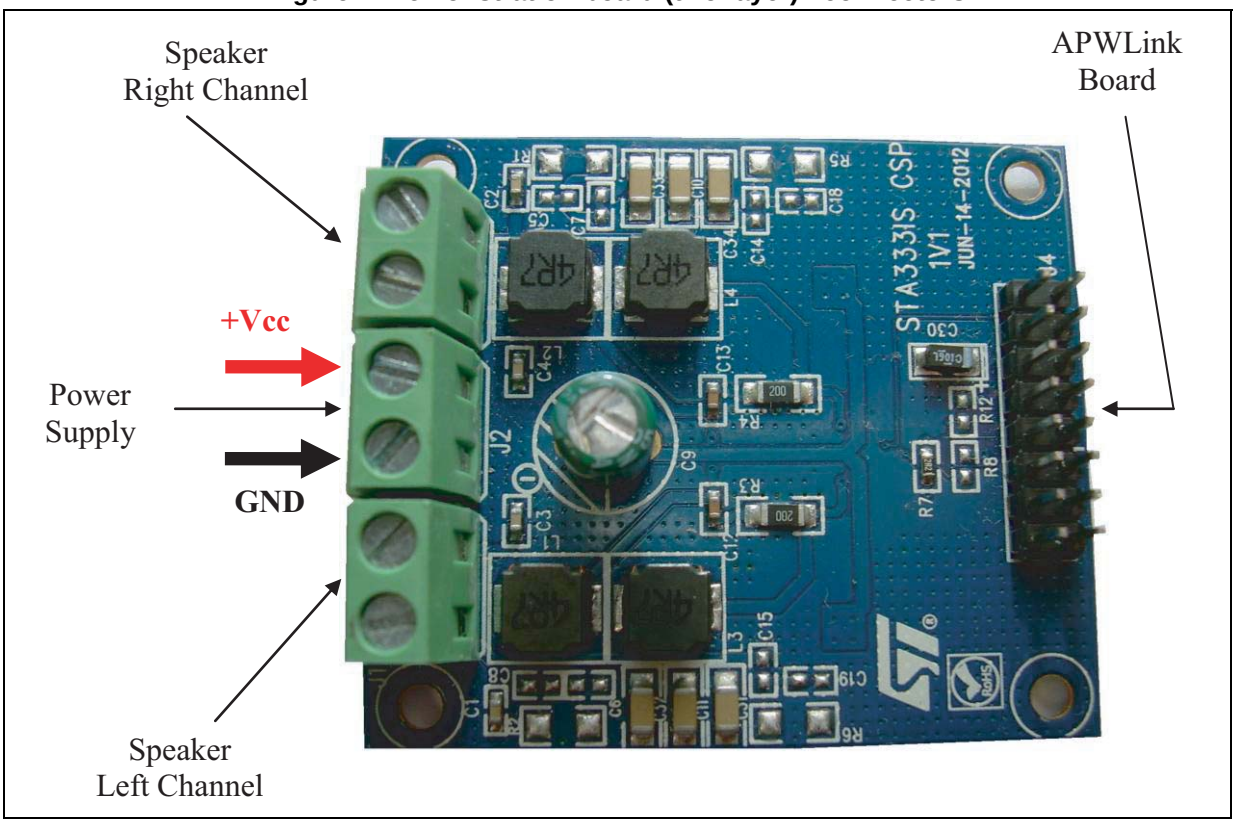
The STA333IS demonstration board can be only configured for 2.0 channels and BTL outputs.

1.3 Required equipment

- Audio Precision (System 2700)
  - Audio Analyzer: Mod. SYS2722 -192K
  - Class-D filter: AUX-0025 filter
  - Multifunction module: DCX-127
- DC power supply (4.5 V to 18 V)
  - Lambda Genesys Gen 80-19
  - HP 6038A
- Digital oscilloscope: Tektronix TDS5054B
- Digital multimeter: AGILENT Mod. 34410A
- PC with APWorkbench control software installed

1.4 Board connections

Figure 2. Demonstration board (two-layer) - connectors



2 Schematic diagram and PCB layout

2.1 Schematic

Figure 3. Schematic diagram - part 1

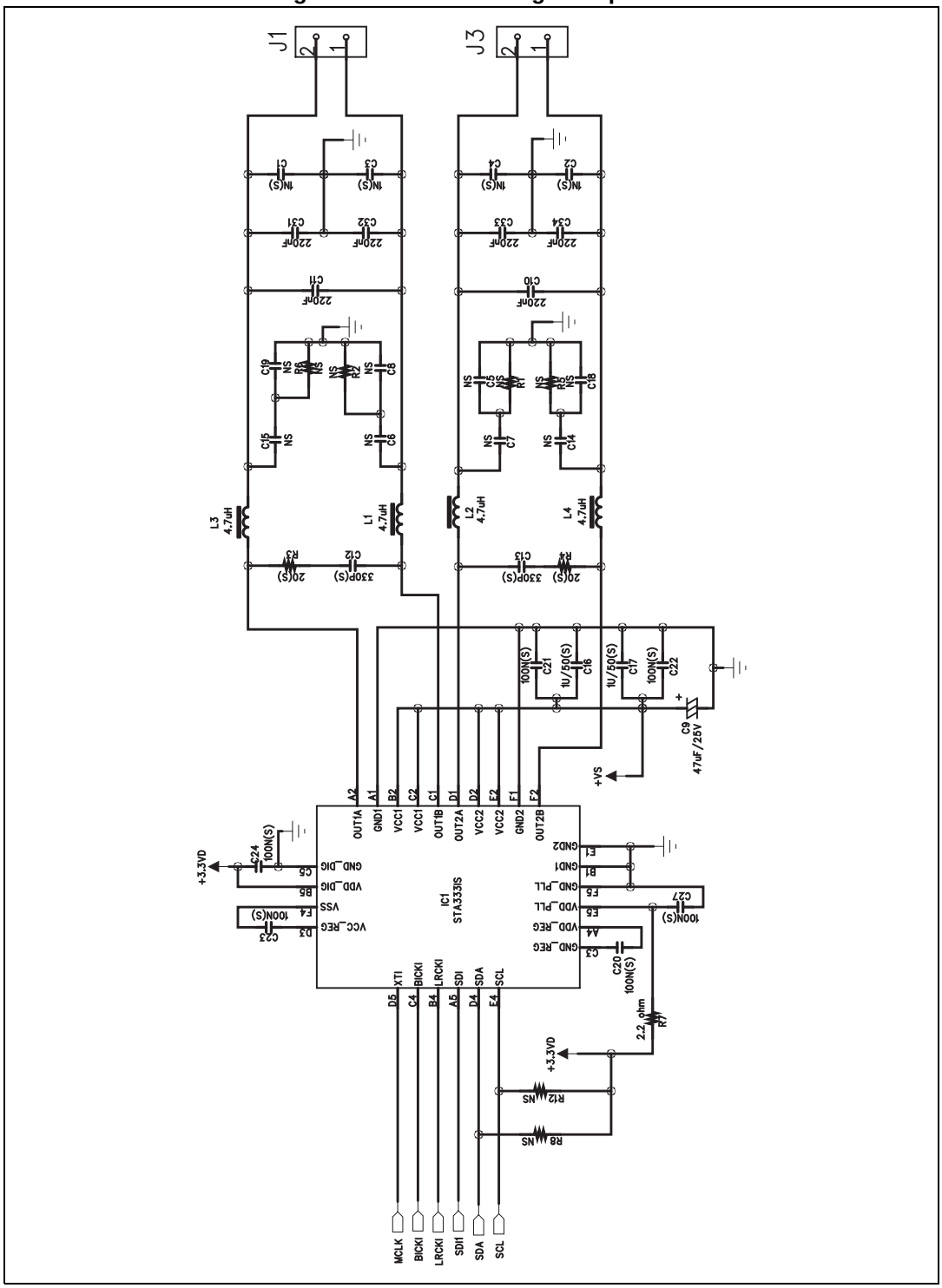
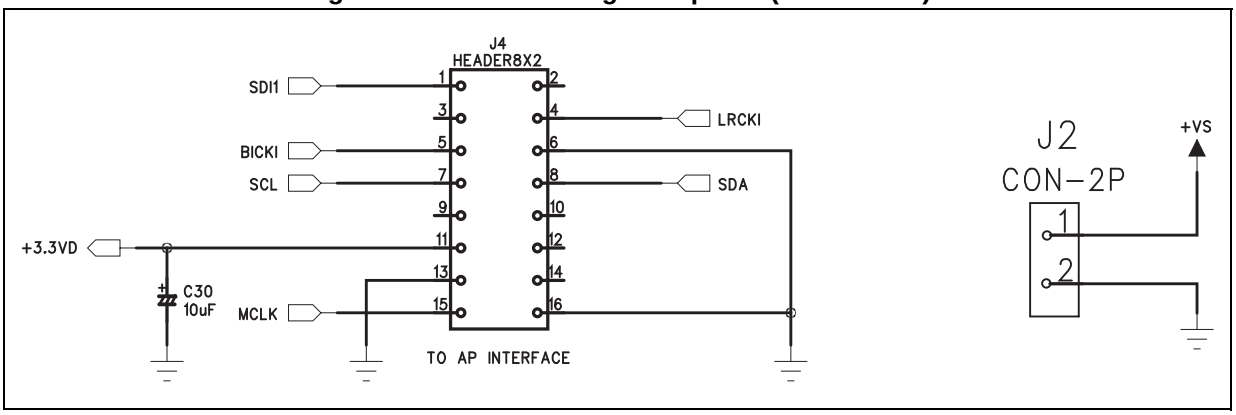


Figure 4. Schematic diagram - part 2 (connectors)



2.2 PCB layout

Figure 5. STA333IS demonstration board - two-layer PCB (top view)

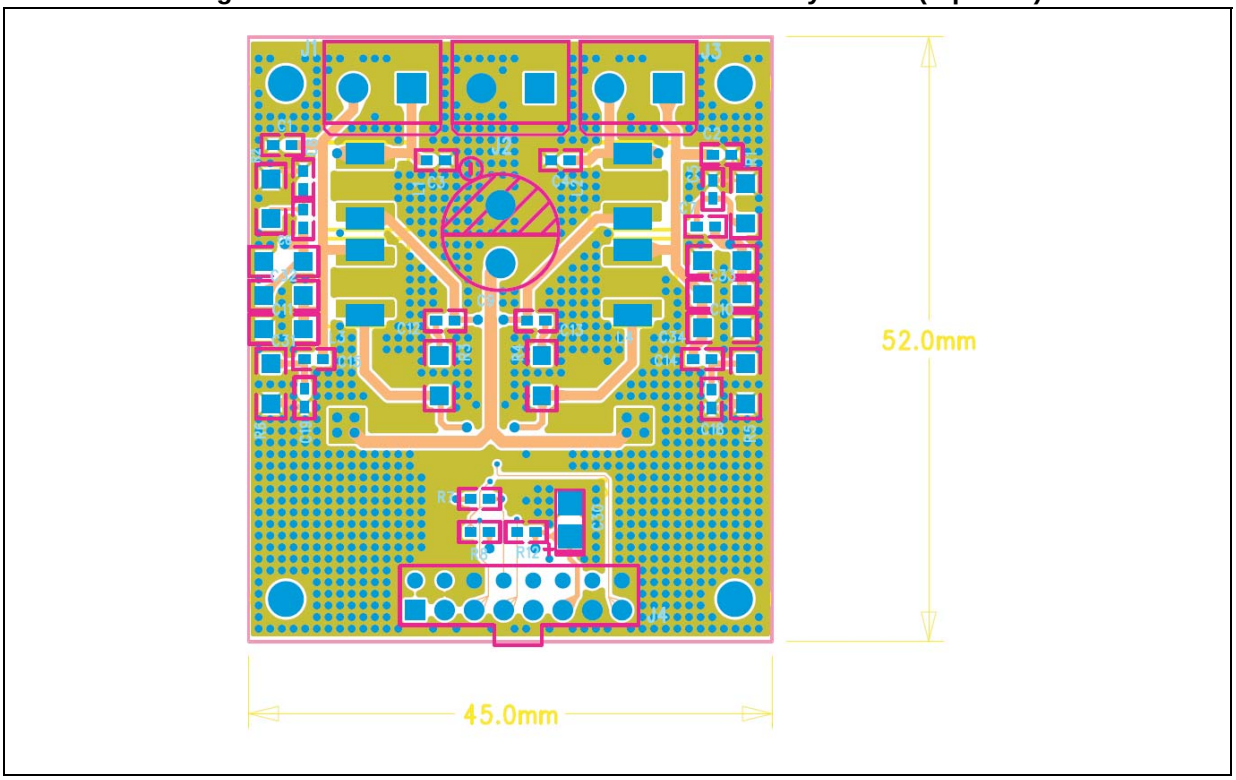
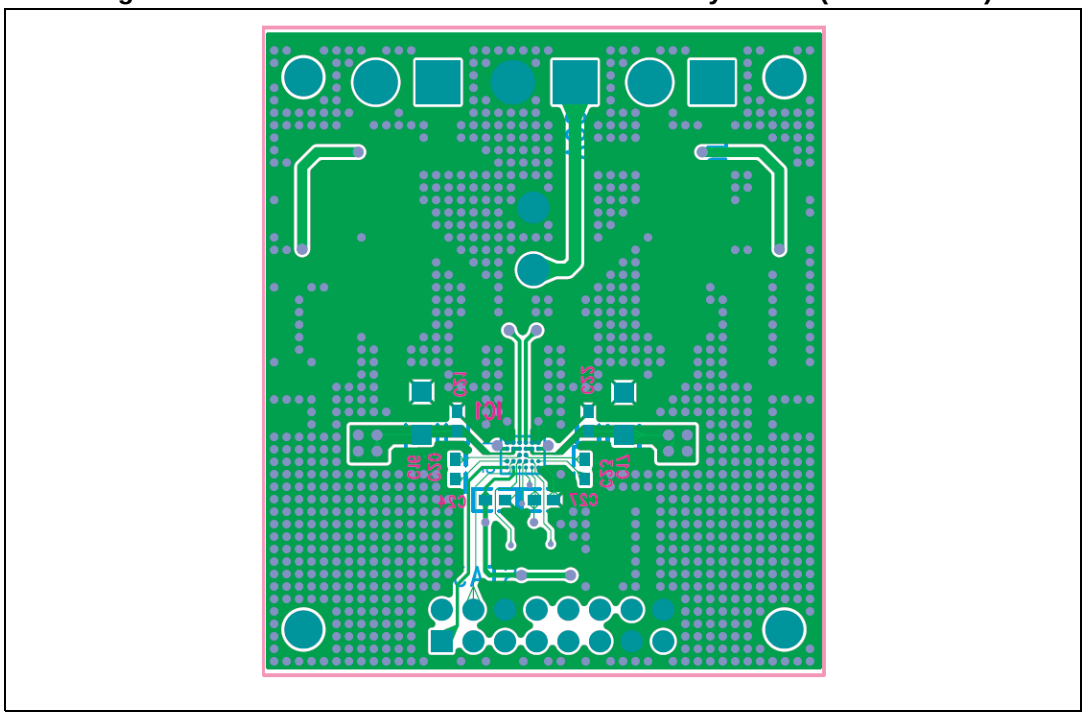


Figure 6. STA333IS demonstration board - two-layer PCB (bottom view)



2.3 Bill of material

Table 1. Bill of material

N°	Type	Footprint	Description	Q.ty	Reference	Manufacturer
1	Connector	Through-hole	2P pitch: 5 mm connector terminal	3	J1, J2, J3	
2	Header	Through-hole	16P (8x2 row) 2.5 mm header	1	J4	
3	CCAP	CAP0603	50 Volt NPO 330 pF ±10%	2	C12, C13	Murata
4	CCAP	CAP0603	50 Volt 1 nF ±10%	4	C1, C2, C3, C4	Murata
5	CCAP	CAP0603	50 Volt 100 nF ±10%	6	C20, C21, C22, C23, C24, C27	Murata
6	CCAP	CAP0603	NS	8	C5, C6, C7, C8, C14, C15, C18, C19	Murata
7	CCAP	CAP1206	50 Volt 220 nF ±10%	6	C10, C11, C31, C32, C33, C34	Murata
8	CCAP	CAP1206	50 Volt 1U ±10%	2	C16, C17	Murata
9	ECAP	CAP1206	10 µF / 16 V	1	C30	Samsung
10	ECAP	Through-hole	47 µF / 25 V, pitch = 5 mm,ϕ10 mm	1	C9	Panasonic
11	RES	R1206	NS	4	R1, R2, R5, R6	Murata
12	RES	R1206	20 ±5% 1/8W	2	R3, R4	Murata
13	RES	R0603	2R2 ±5% 1/16W	1	R7	Murata
14	RES	R0603	NS	2	R8, R12	
15	Plastic rod		Hexagonal rod 15 mm length, male type	4	Four corners	
16	Plastic rod		Hexagonal rod 8 mm length, female type	4	Four corners	
17	IC	BGA30	STA333IS	1	IC1	STMicroelectronics
18	Coil	SMD	SWPA6045S4R7MT, 4.7 µH	4	L1, L2, L3, L4	Sunlord
19	PCB		STA333IS CSP 2-layer 1V1	1		Fastprint

3 APWorkbench settings

Figure 7. APWorkbench - device selection

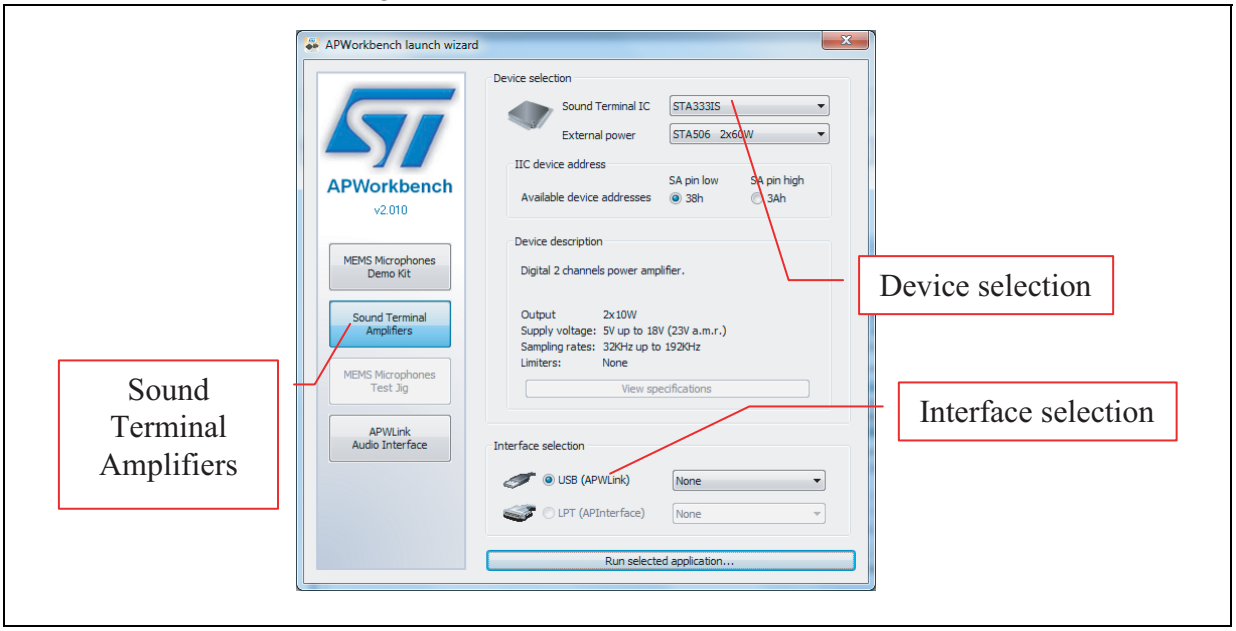
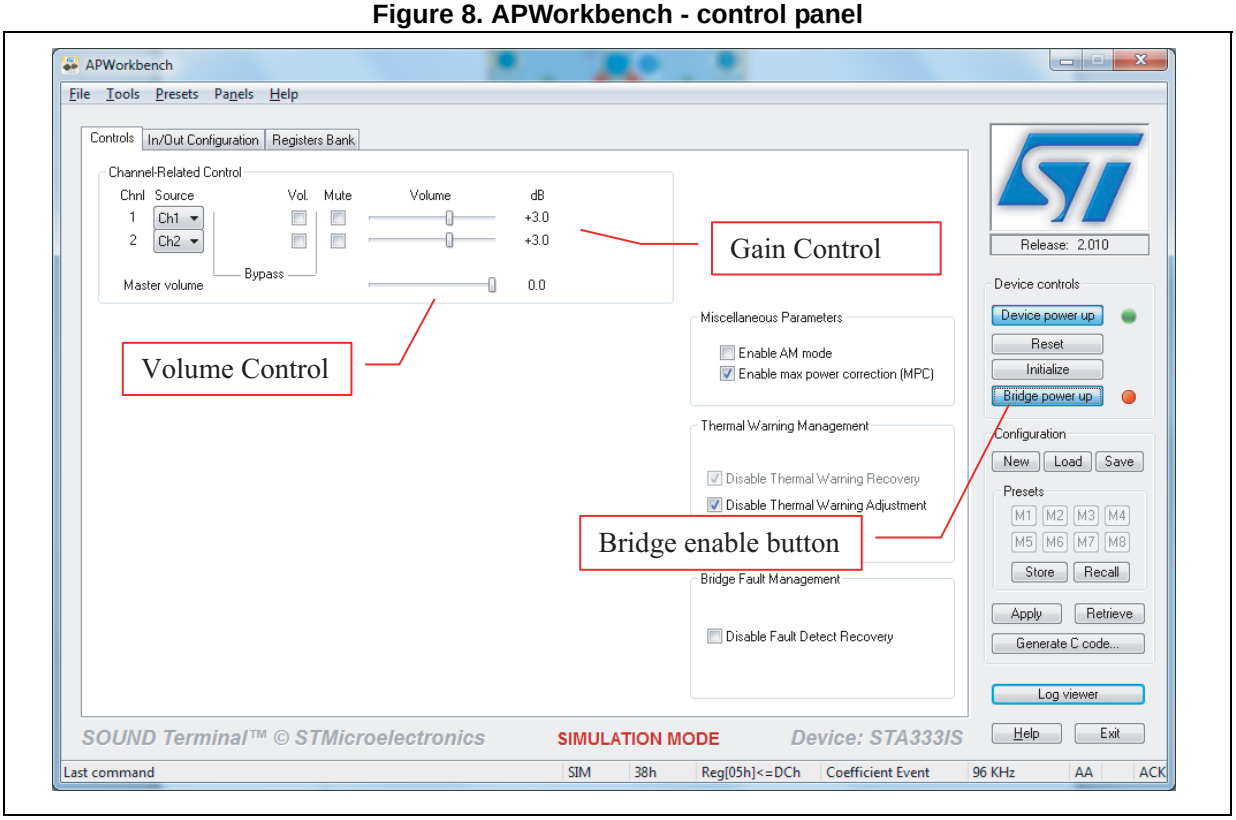


Figure 8. APWorkbench - control panel



4 Test results

Figure 9. THD+N vs. power - V_{CC} = 12 V, load = 8 Ω, 1 kHz

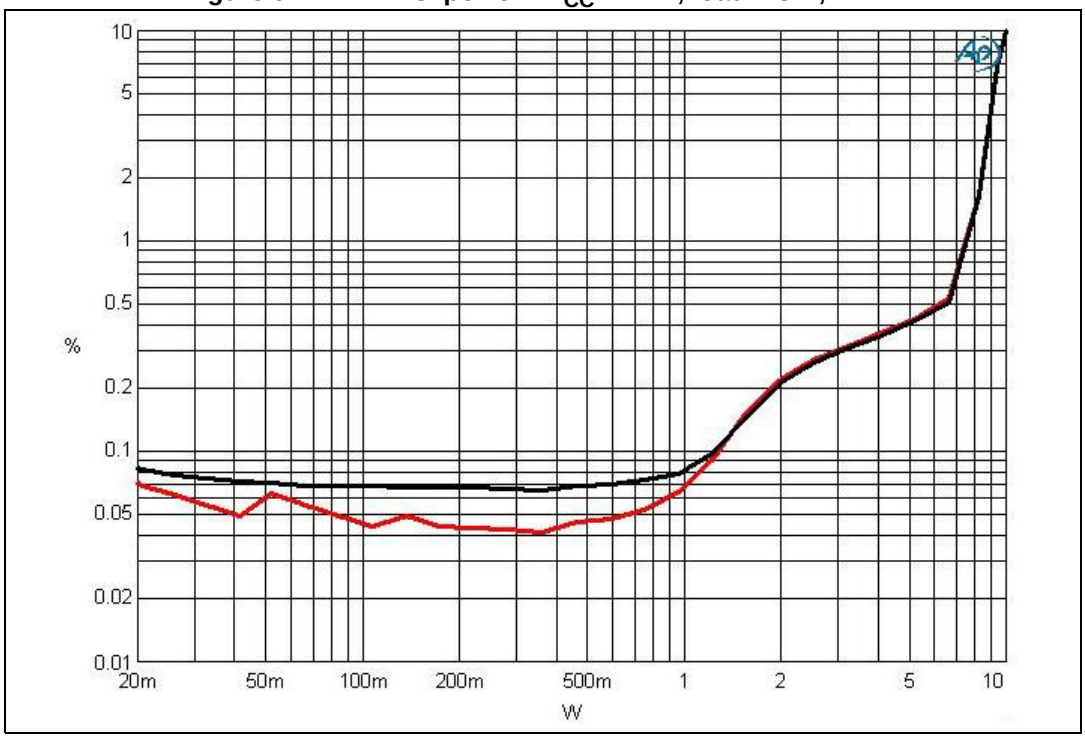


Figure 10. THD+N vs. frequency - V_{CC} = 12 V, load = 8 Ω, Pout = 1 W at 1 kHz

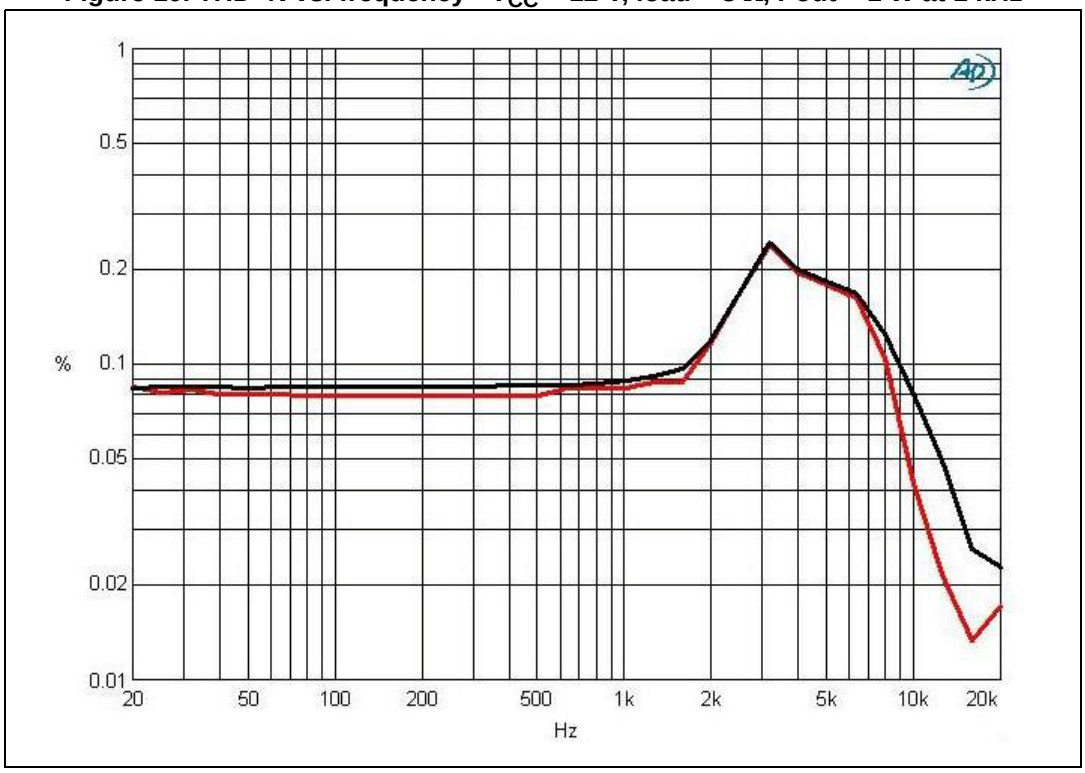


Figure 11. Frequency response - V_{CC} = 12 V, load = 8 Ω, Pout = 1 W at 1 kHz

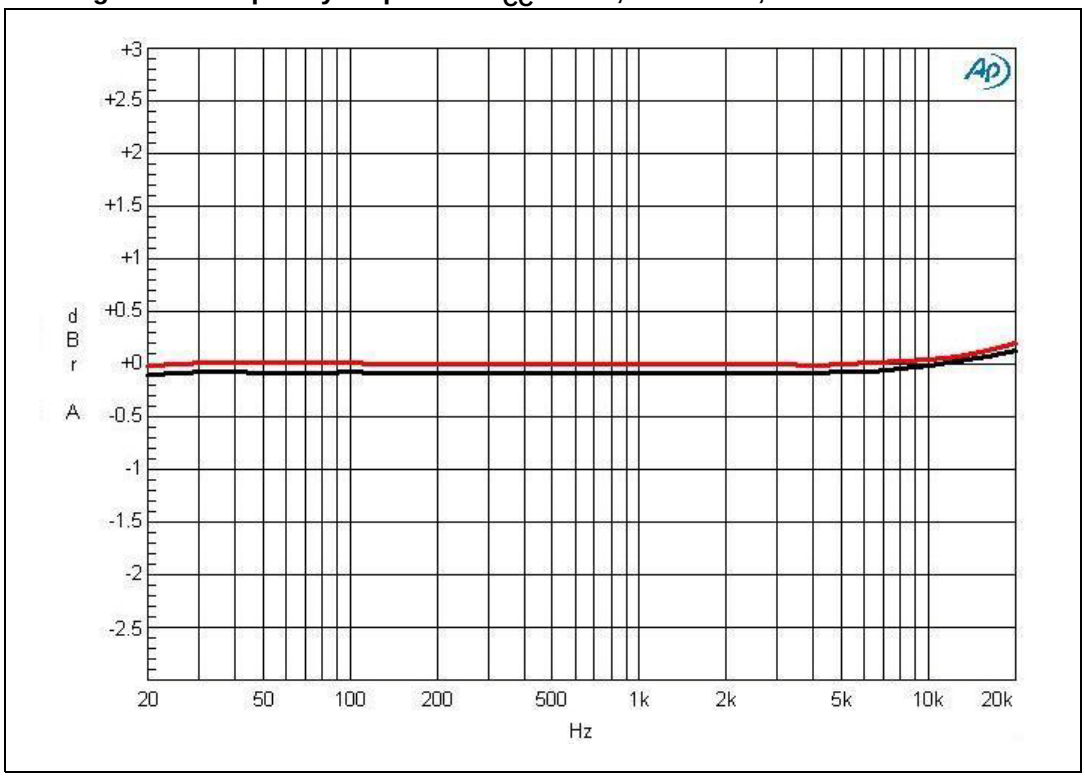


Figure 12. Crosstalk - V_{CC} = 12 V, load = 8 Ω, Pout = 1 W at 1 kHz

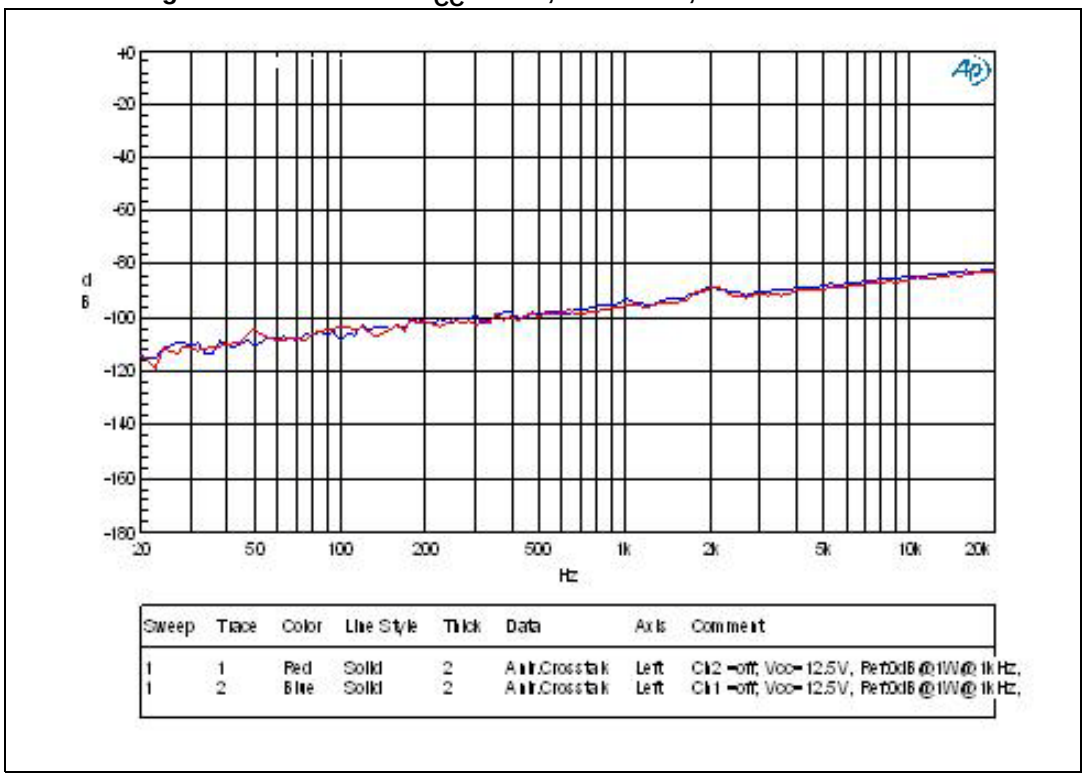


Figure 13. FFT - V_{CC} = 12 V, load = 8 Ω, Pout = 1 W at 1 kHz

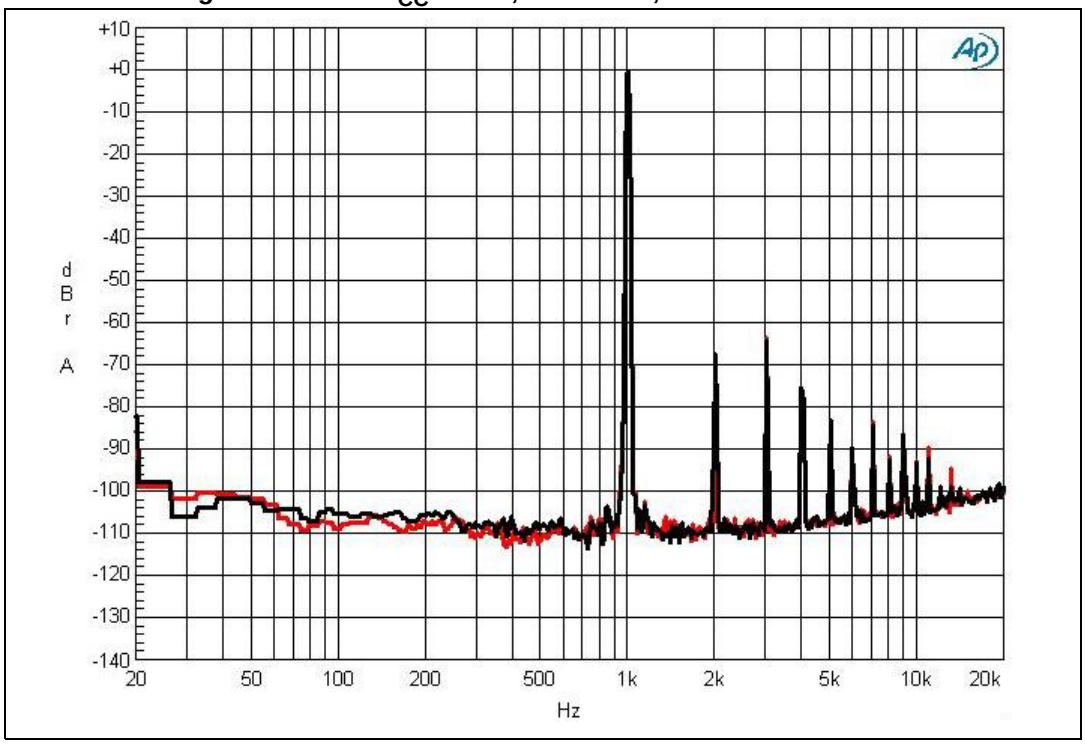


Figure 14. Output power vs. supply voltage - load = 8 Ω, 1 kHz

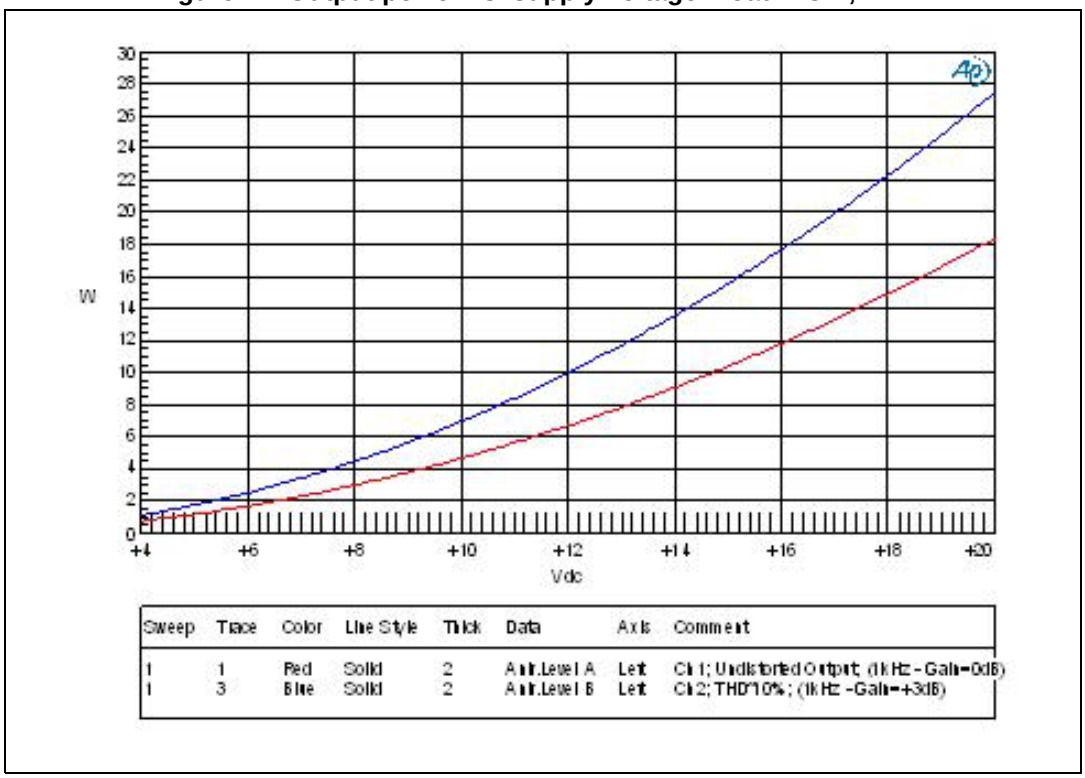
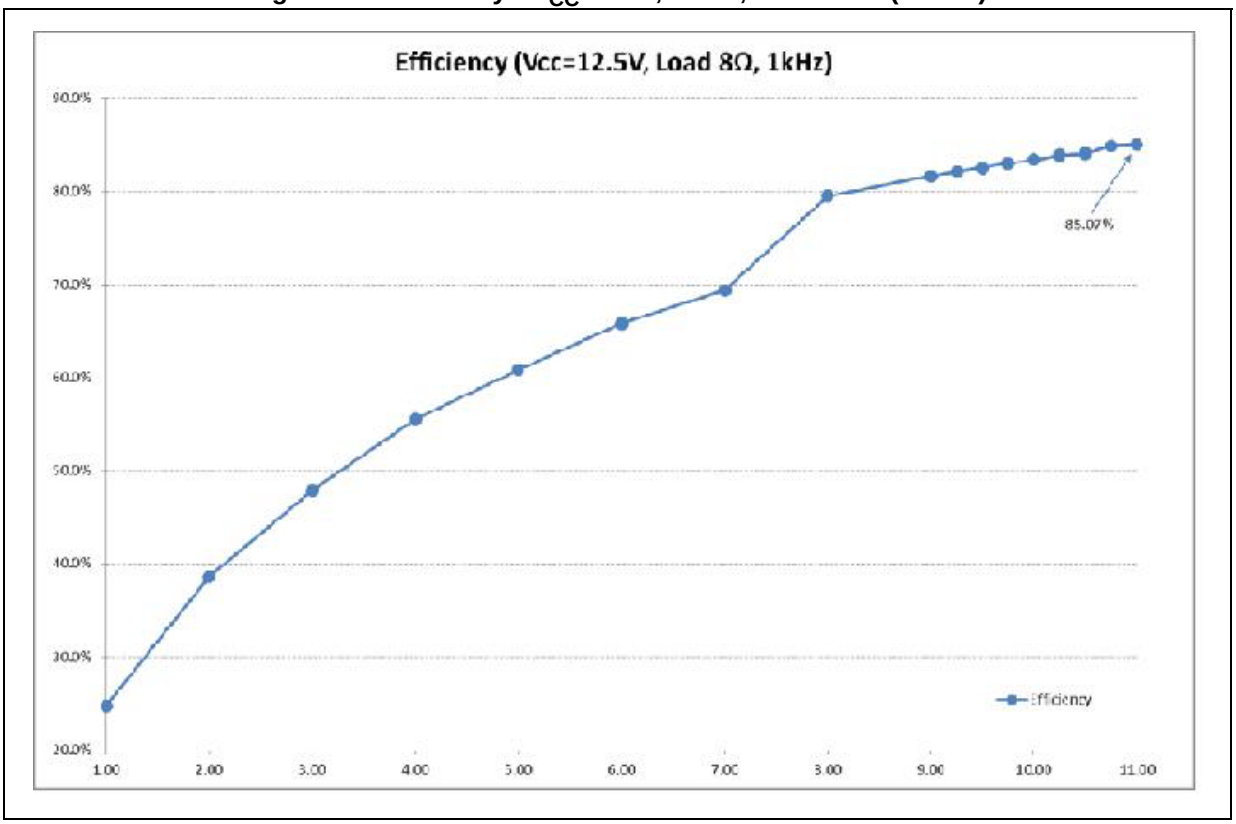


Figure 15. Efficiency - V_{CC} =12 V, 1 kHz, load = 8 Ω (stereo)

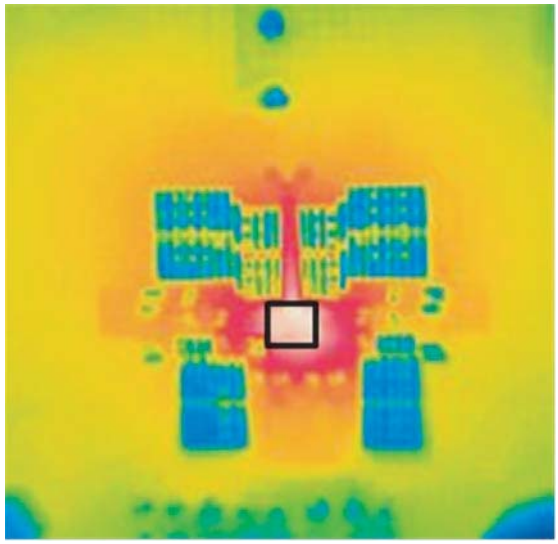


5 Thermal performance

Test conditions:

- V_{CC} = 12 V
- 1 kHz sine wave
- Load = 2 x 8 Ω
- Output power: 2 x 10 W

Figure 16. Thermal performance



	Tamb = 25 °C	Tamb = 40 °C
IC temp	78°C	93°C

6 Design guidelines for schematic and PCB layout

6.1 General

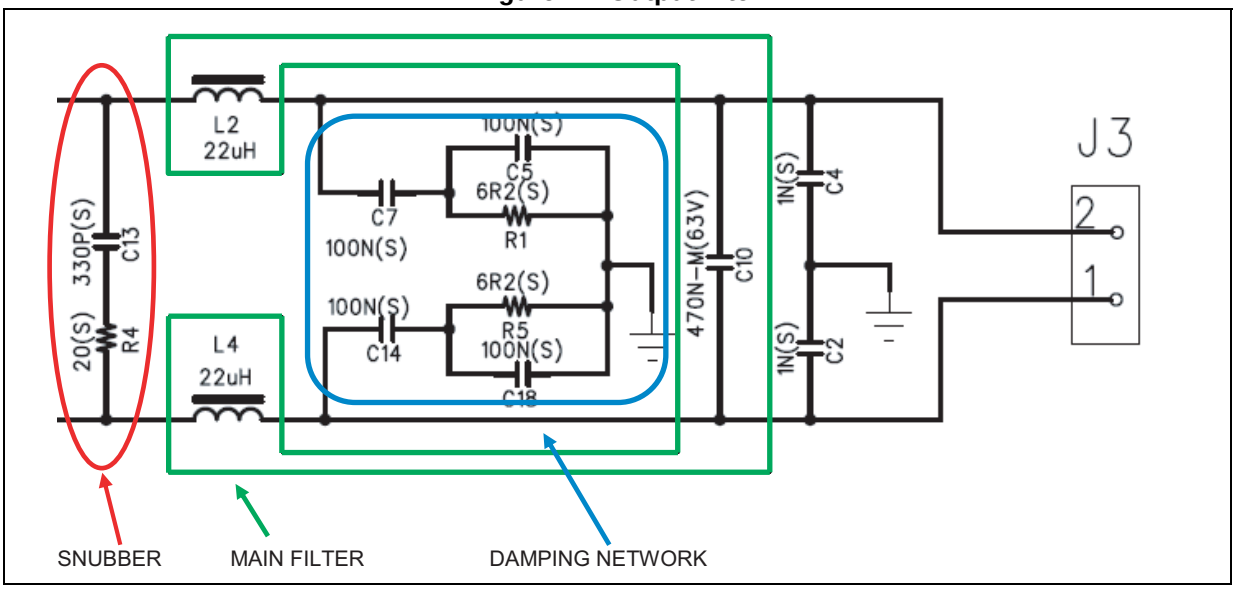
- Absolute maximum rating: 20 V
- Bypass capacitor 100 nF in parallel to 1 µF and 10 µF for each power V_{CC} branch. Preferable dielectric is X7R.
- Vdd and ground for the digital section should be separated from the other power supply.
- Coil saturation current compatible with the peak current of the application

6.2 Decoupling capacitors

The decoupling capacitors can be shared for each V_{CC} branch. The decoupling capacitors must be placed as close as possible to the IC pins.

6.3 Output filter

Figure 17. Output filter



6.3.1 Snubber network

The snubber circuit must be optimized for the specific application. Starting values are 330 pF in series to 22 Ω.

The power dissipation in this network can be defined by the following formula which considers the power supply, frequency and capacitor value:

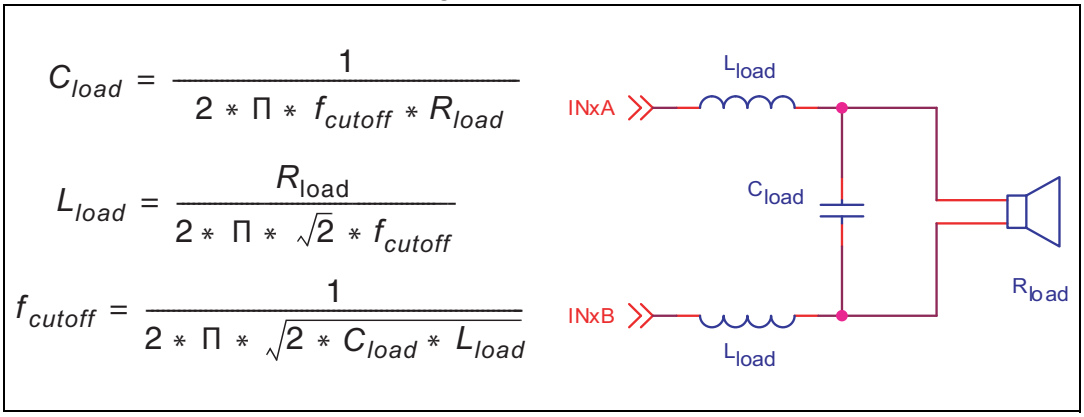
$P = C \cdot Freq_{PWM} \cdot (2 \cdot Vout)^2$

This power is dissipated on the series resistance.

6.3.2 Main filter

The main filter is an L and C based Butterworth filter. The cut-off frequency must be chosen between the upper limit of the audio band (~20 kHz) and the carrier frequency (384 kHz).

Figure 18. Main filter



6.3.3 Damping network

The C-R-C is a damping network. It is mainly intended for high inductive loads where the speaker load could be disconnected.

Figure 19. Damping network

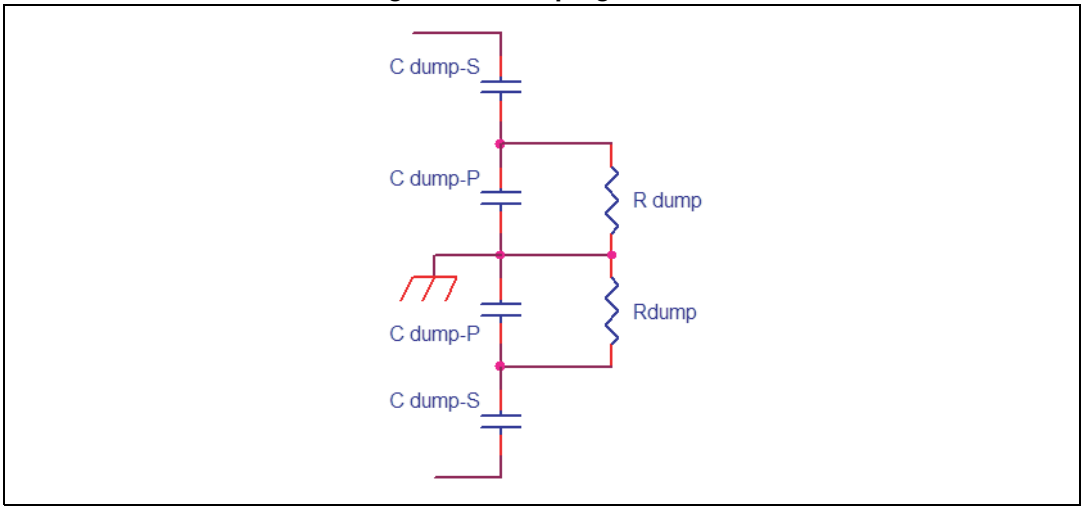


Table 2. Recommended values for main filter and damping network

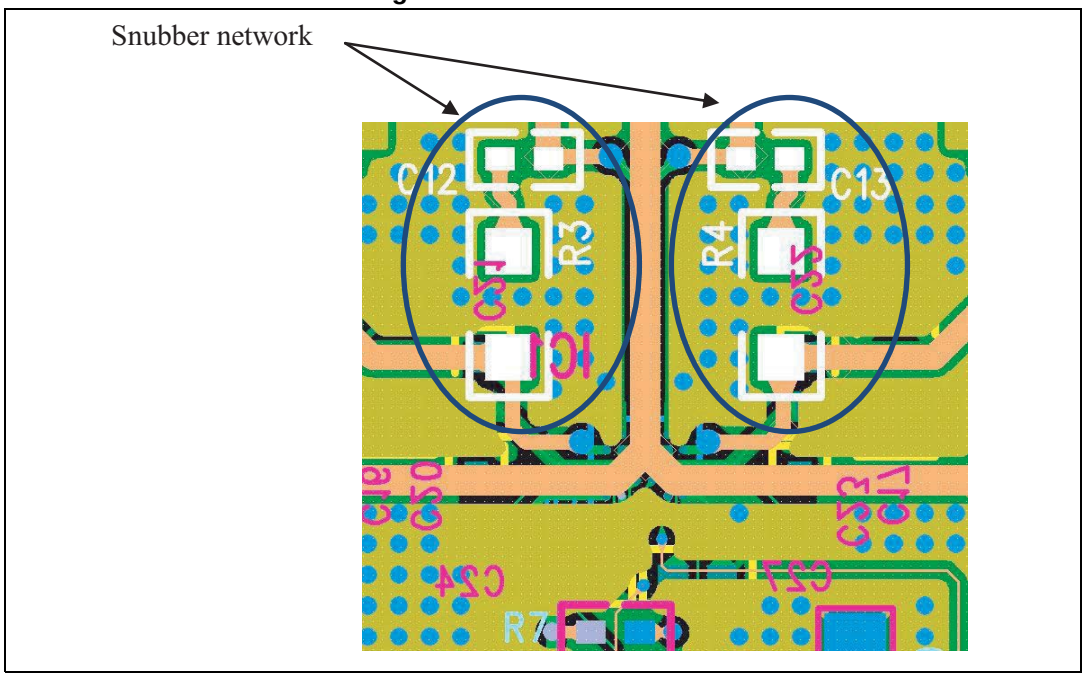
	Rload	16 Ω	12 Ω	8 Ω	6 Ω	4 Ω
Main filter	Lload	47 µH	33 µH	22 µH	15 µH	10 µH
	Cload	220 nF	330 nF	470 nF	680 nF	1 µF
Damping network	C damp-S	100 nF	100 nF	100 nF	100 nF	220 nF
	C damp-P	100 nF	100 nF	100 nF	100 nF	220 nF
	R damp	10 Ω	8.2 Ω	6.2 Ω	4.7 Ω	2.7 Ω

6.4 PCB layout

6.4.1 Snubber network

Solder the snubber network as close as possible to the related IC pin.

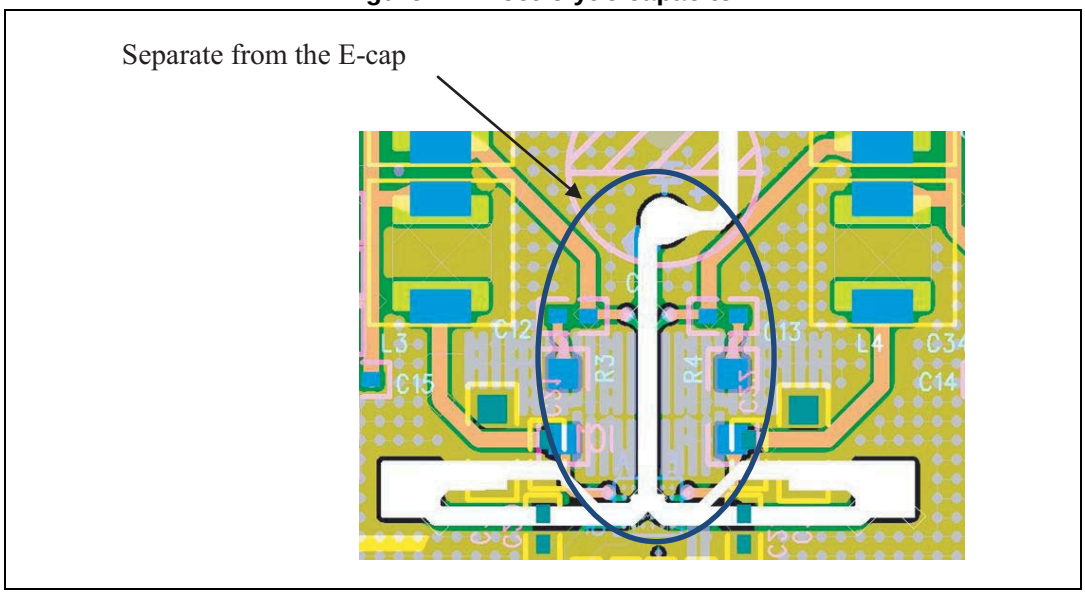
Figure 20. Snubber network



6.4.2 Electrolytic capacitor

Place the electrolytic capacitor first to separate the Vcc branches.

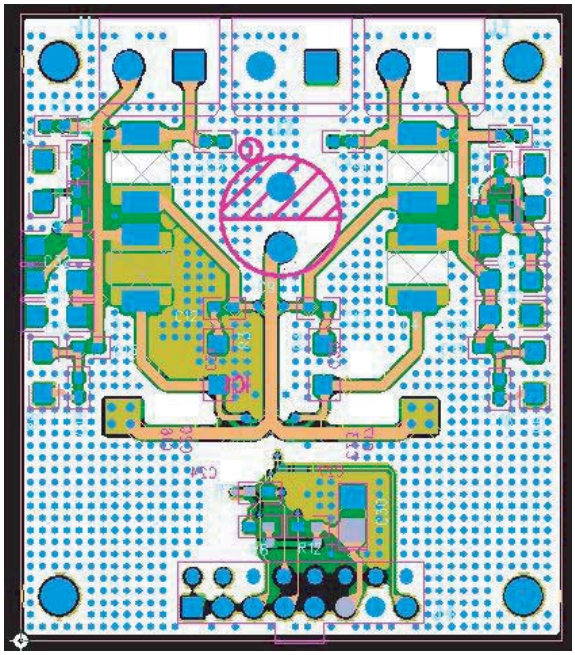
Figure 21. Electrolytic capacitor



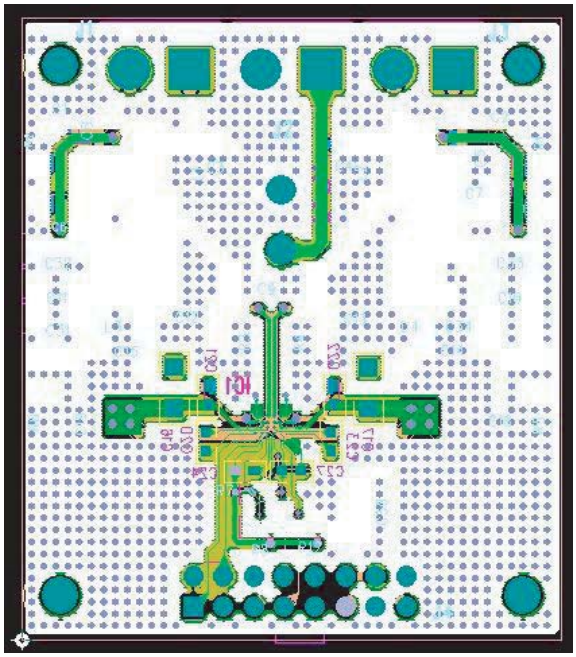
6.4.3 Ground plane and heatsink

In order to dissipate the heat, a large ground plane is used. It is mandatory to have a large ground plane on the top and bottom layers and solder the slug on the PCB.

Figure 22. Ground plane



Large ground plane on the top side

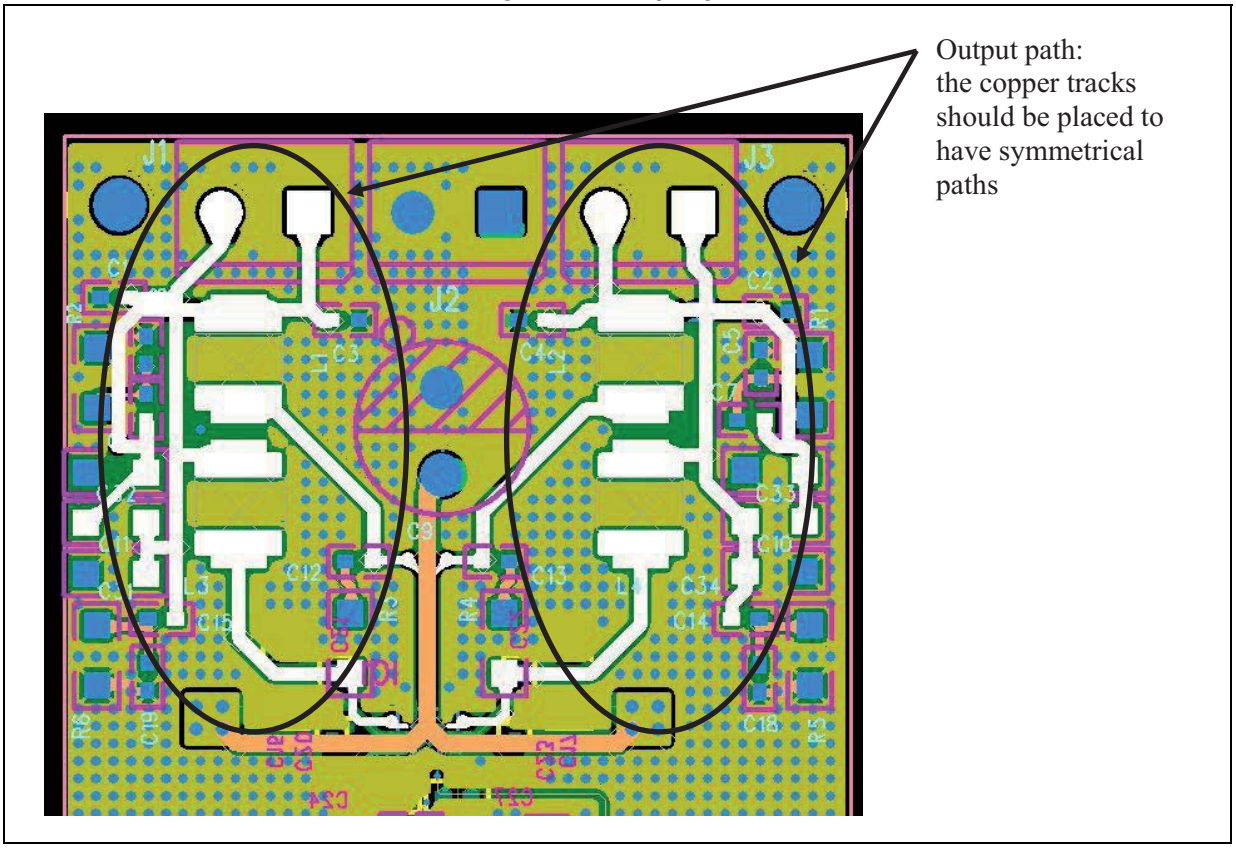


Large ground plane on the bottom side

6.4.4 PCB symmetrical paths

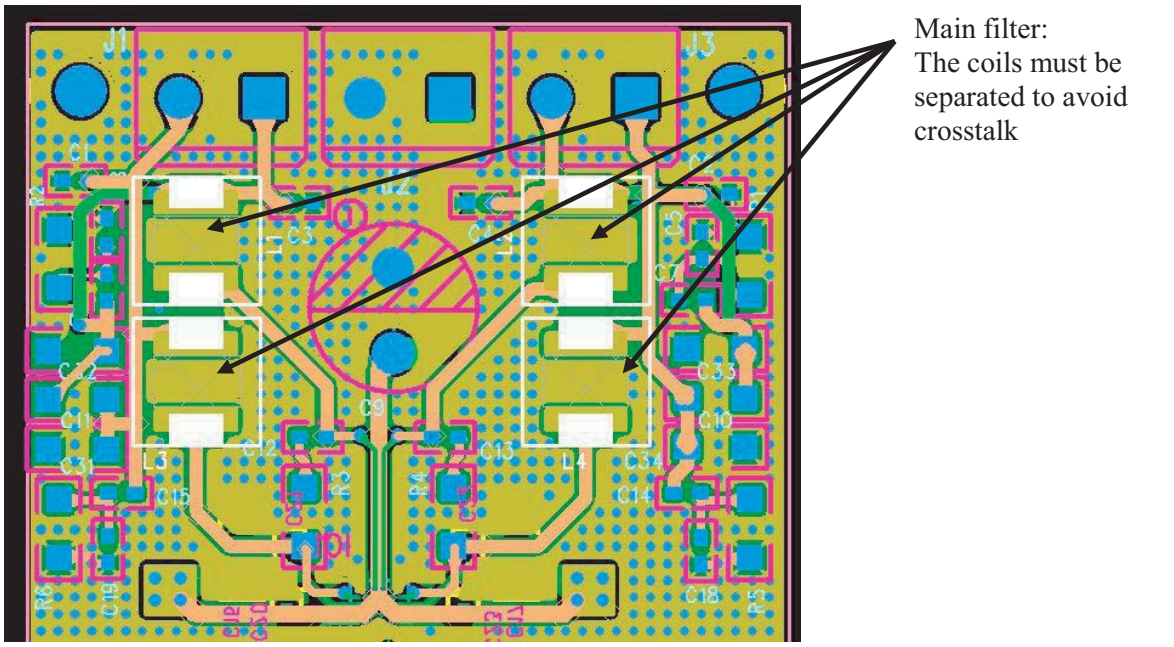
For differential applications, creating symmetrical paths for the output stage is recommended.

Figure 23. Output path



The coils must be separated to avoid crosstalk. Shielded parts must be used.

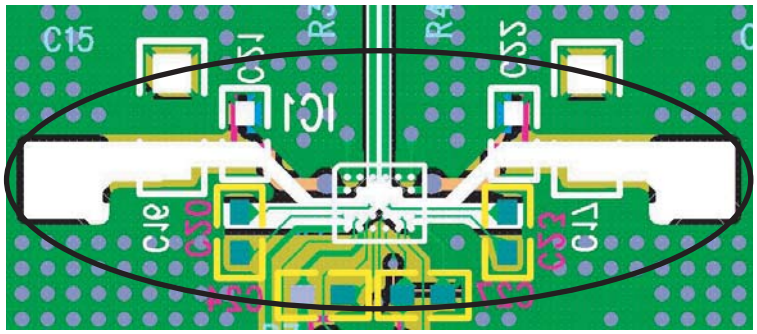
Figure 24. Coils



6.4.5 V_{CC} filter for high frequency

The V_{CC} filter capacitors must be placed as close as possible to the supply pins as well as the ceramic capacitors.

Figure 25. V_{CC} filter capacitors



The PWM frequency is 384 kHz. In order to compensate the inductive effect of the copper track, the ceramic capacitors must be placed as close as possible to the supply pins. The recommended distance between the capacitors and the supply pins is less than 5 mm.

7 Revision history

Table 3. Document revision history

Date	Revision	Changes
01-Jul-2013	1	Initial release.

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