AN4345
Application note

STEVAL-ISA119V1: 1.5 W double output buck product evaluation board based on the VIPER16LD

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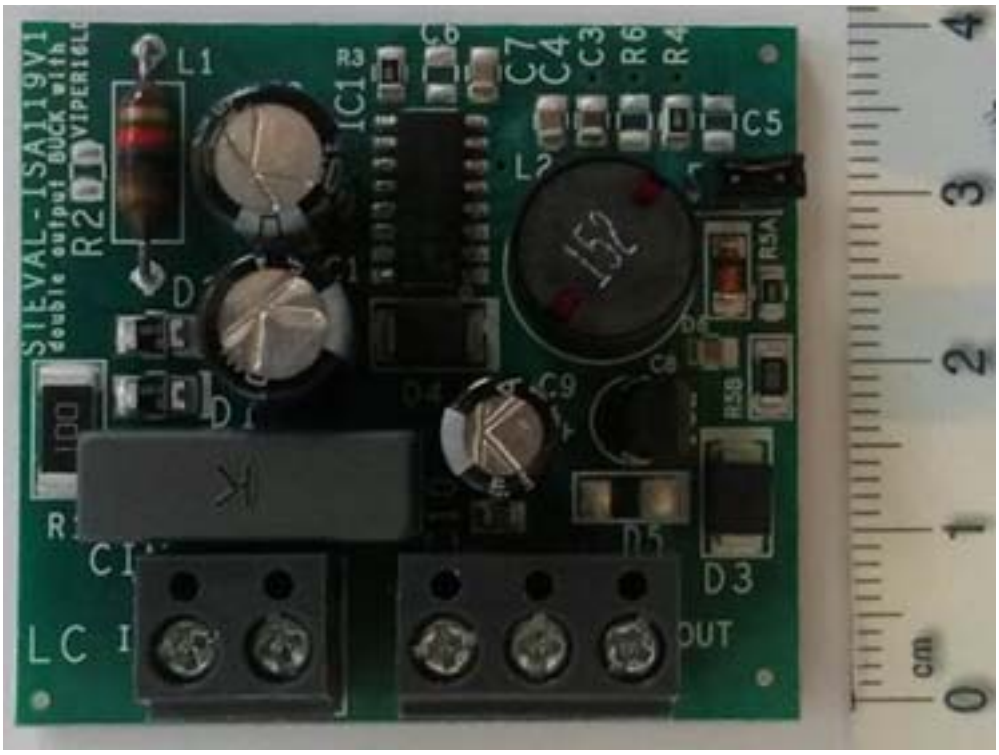
Introduction

This document describes a two output buck with the VIPer16LD, a new offline high voltage converter by ST, specifically developed for non-isolated SMPS. In fact the output regulation is easily obtained by a voltage divider connected to the feedback FB pin. Moreover, the VIPer16LD can be externally biased or self-biased. The former reaches very low standby-consumption (< 60 mW at 230 V_{AC}), the latter saves costs and complication of the IC supplying network. The other device's features are:

- 800 V avalanche rugged power section,
- PWM operation at 60 kHz with frequency jittering for lower EMI
- Limiting current with adjustable set point
- On-board soft-start
- Safe auto-restart after a fault condition

The available protection includes: thermal shutdown with hysteresis, delayed overload protection and open loop failure protection. Protection is in auto-restart mode.

Figure 1. Product evaluation board picture



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Electrical specifications of the product evaluation board are listed in *Table 1*.

Table 1. Electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	[90 V_{AC}; 265 V_{AC}]
Output voltage 1	V_{OUT1}	12 V
Max. output current 1	I_{OUT1}	0.1 A
Output voltage 2	V_{OUT2}	5 V (through LDO)
Max. output current 2	I_{OUT2}	0.05 A
Precision of output regulation	ΔV_{OUT_LF}	±5%
High frequency output voltage ripple	ΔV_{OUT_HF}	50 mV
Max. ambient operating temperature	T_{AMB}	60 ºC

2 Circuit description

The converter schematic is given in *Figure 4*. The input section includes a resistor R1 for inrush current limiting, diodes D1 and D2 and a Pi filter (C1, L1, C2) for rectification and EMC suppression.

The FB pin is the inverting input of the internal transconductance error amplifier and its reference voltage is V_{FB_REF} = 3.3 V. The output voltage V_{OUT1} is regulated by the voltage divider, which is composed of R4 and R5, according to the following formula:

Equation 1

$$V_{OUT1} = \left(1 + \frac{R5}{R4}\right) \cdot V_{FB\_REF}$$

where R5 is split into R5A and R5B to allow a better tuning of the output voltage.

V_{OUT2} comes from V_{OUT1} through a linear voltage regulator, the compensation is performed by the R-C-C network connected between COMP and GND pins.

At power-up, the DRAIN pin supplies the internal HV start-up current generator, which charges the C3 capacitor up to V_{DDON} (13 V). At this point, the power MOSFET starts switching, the generator is turned off and the IC is powered by the energy stored in C3.

If the jumper J1 is not selected, the VIPer16LD is self-biased: the C3 capacitor voltage, due to the system consumption, falls down and when it reaches V_{DDCS_ON} (10.5 V typ.), the internal HV current generator is turned on, recharging C3 up to V_{DDON}, after that the HV generator is switched off again. The VIPer16LD is internally supplied without any external network, which minimizes the number of external components. Moreover this function allows the designer to generate output voltages below the voltage lockout (5 V for example) with a simple inductor.

If the jumper J1 is selected, the HV start-up generator is activated at power on only: when V_{OUT1} has reached its steady-state value, IC is biased from the output through the diode D6, allowing the system to reach very low standby-consumption values. This is referred to “external biasing” and can be obtained only if V_{OUT1} is high enough to keep the C3 voltage always above the V_{DDCS_ON} threshold.

The shape of the V_{DD} voltage is depicted in *Figure 5* and *6* for self-biasing and external biasing respectively.

The R6 resistor, if connected, reduces the default current limitation of the device I_{DLIM} by a certain percentage depending on the resistor value, as reported in the curve I_{LIM} vs. R_{LIM} of the datasheet. This optimizes the design of the magnetic and power elements.

3 Bill of material, layout and schematic

Table 2. Bill of material

Reference	Part	Description	Manufacturer
Cin	100 nF, X2	Series B32922	Epcos
C1, C2	3.3 µF, 450 V	Electrolytic capacitor	Series M Panasonic
C3	1 µF, 35 V	Electrolytic capacitor	Series NHG Panasonic
C4	100 nF, 50 V	Ceramic capacitor	
C5	Not mounted	Ceramic capacitor	
C6	Not mounted	Ceramic capacitor	
C7	1.5 nF, 50 V	Ceramic capacitor	
C8	100 nF, 50 V	Ceramic capacitor	
C9	330 µF, 16 V	Electrolytic capacitor ultra-low ESR	Rubycon
C10	100 nF, 50 V	Ceramic capacitor	Epcos
R1	10 Ω	1/2 W resistor	
R2	Not mounted	1/4 W resistor	
R3	1 kΩ	1/4 W resistor	
R4	12 kΩ	1/4 W resistor	
R5A	33 kΩ	1/4 W resistor	
R5B	0	1/4 W resistor	
R6	Not mounted		
D1, D2	GL1M	1000 V/ 1 A diode	Semikron
D3, D4	STTH1L06	Ultra-fast 600 V diode	ST
D5	Not mounted	Zener diode	
D6	LL4148	Diode	Vishay
L1	1 mH	Axial inductor	Epcos
L2	1.5 mH	Power inductor	Coilcraft
IC1	VIPer16LD	Controlled switch	ST
IC2	L78L05	Voltage regulator	ST

Figure 2. Layout

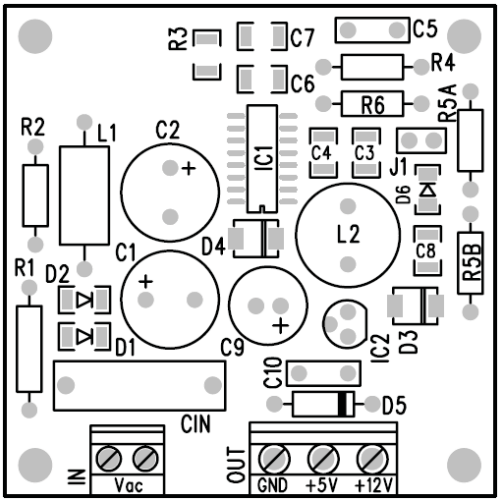

Figure 3. Routing

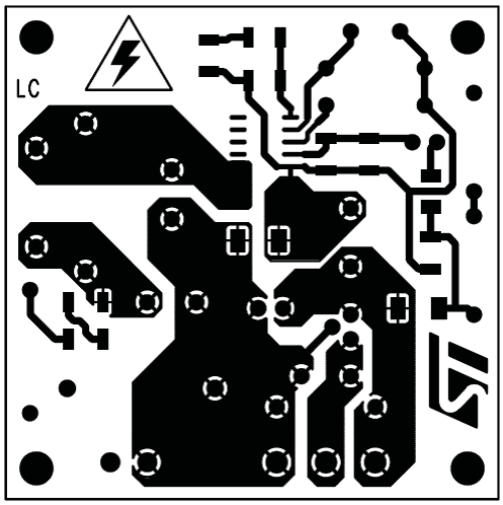

Figure 4. Schematic

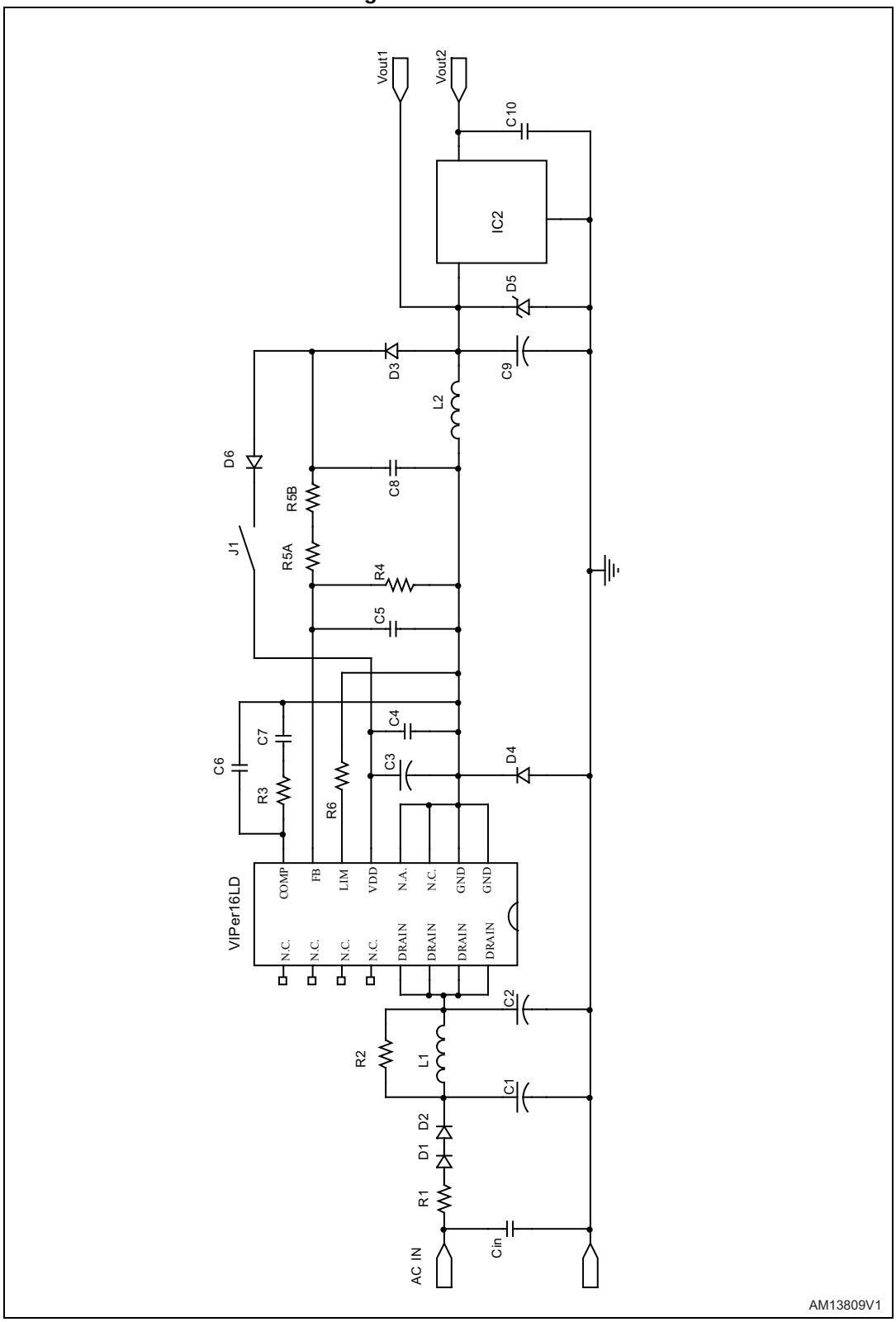

Figure 5. V_{DD} waveform, self-biasing (J1 not selected)

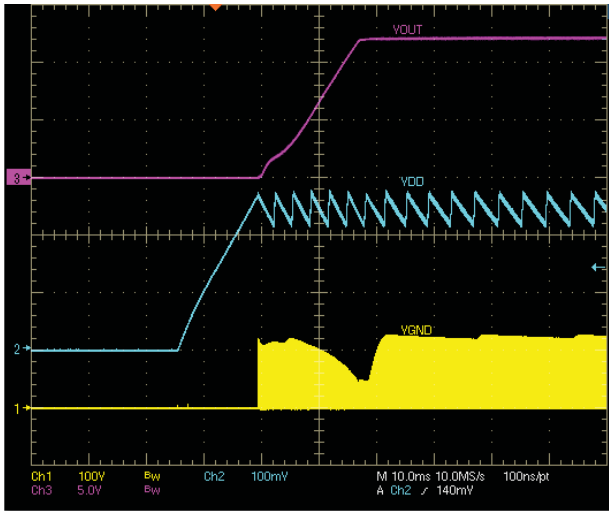

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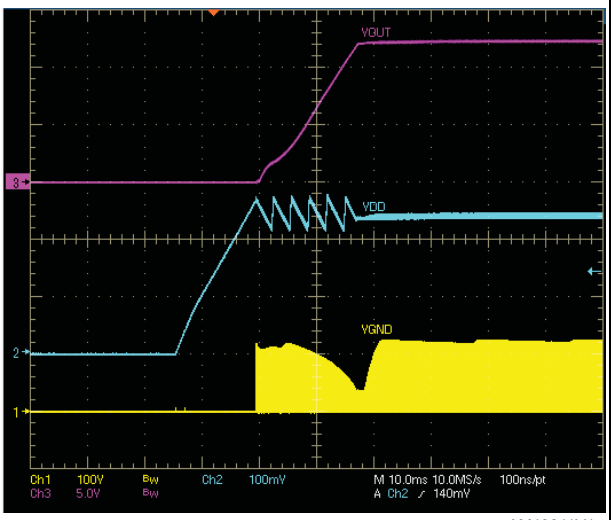
Figure 6. V_{DD} waveform, external biasing (J1 selected)



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4 Board testing

4.1 Typical waveforms

Source voltage and current waveforms in full load conditions are reported for two nominal input voltages in *Figure 7* and *8*, and for minimum and maximum input voltage in *Figure 9* and *10* respectively.

Figure 7. Source current and voltage at max. load 115 V_{AC}

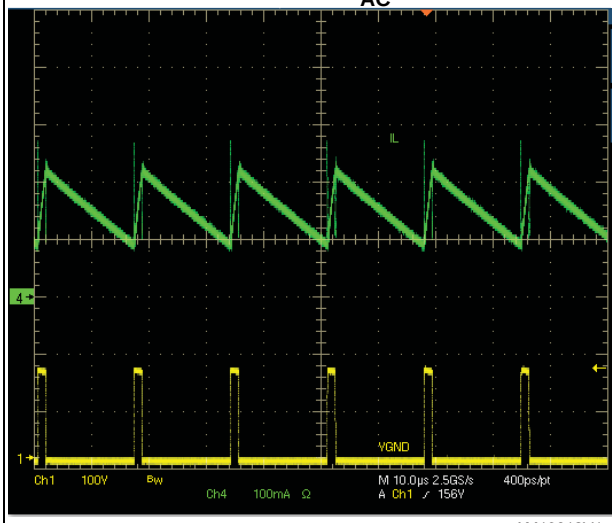

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Figure 8. Source current and voltage at max. load 230 V_{AC}

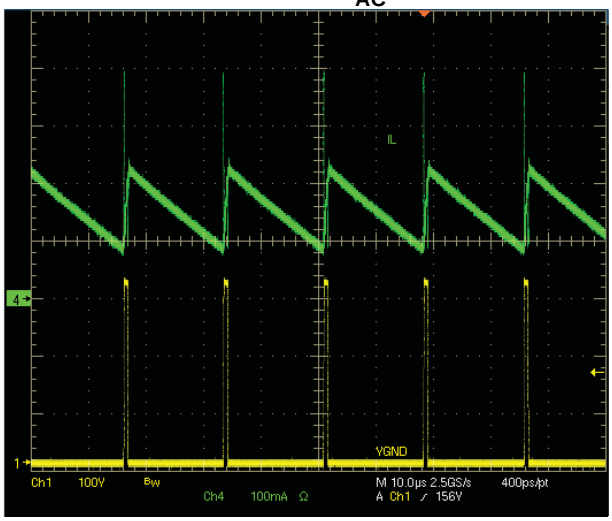

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Figure 9. Source current and voltage at max. load 90 V_{AC}

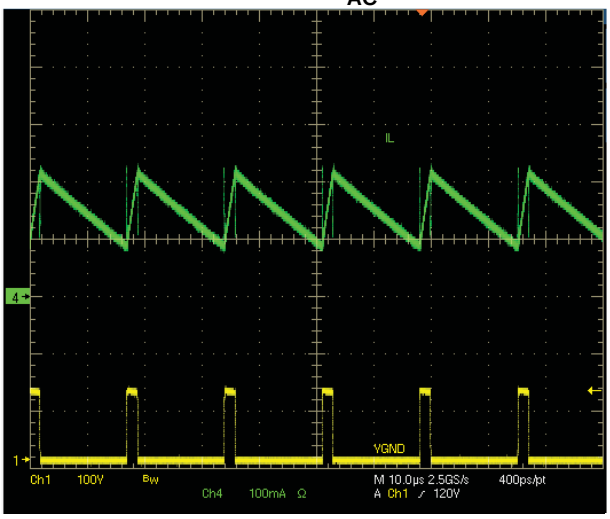

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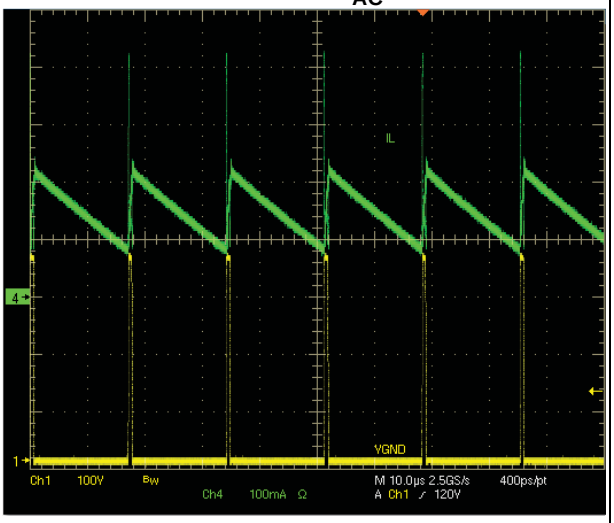
Figure 10. Source current and voltage at max. load 265 V_{AC}



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4.2 Precision of the regulation and output voltage ripple

The output voltage V_{OUT1} of the board has been measured according to different lines and load conditions, both when 5 V output (obtained through linear regulator) is open loaded and full loaded. Results are reported on *Table 3*. The output voltage is not affected by the line condition and by the IC biasing (external or self-biasing).

Table 3. Output voltage line-load regulation - V_{OUT1} (I_{OUT2} = 0 mA)

V_{IN} (V_{AC})	V_{OUT1} (I_{OUT2} = 0 mA)									
	No load		25% load		50% load		75% load		100% load	
	External biasing	Self-biasing	External biasing	Self-biasing	External biasing	Self-biasing	External biasing	Self-biasing	External biasing	Self-biasing
90	12.74	12.61	12.14	12.04	12.09	12.02	12.07	11.99	12.05	11.98
115	12.73	12.61	12.14	12.04	12.08	12.01	12.06	11.99	12.04	11.97
150	12.76	12.65	12.14	12.04	12.08	12.01	12.06	11.98	12.04	11.97
180	12.79	12.68	12.15	12.05	12.08	12.00	12.06	11.98	12.04	11.97
230	12.86	12.76	12.16	12.06	12.08	12.00	12.05	11.98	12.04	11.97
265	12.87	12.78	12.17	12.08	12.08	12.00	12.05	11.98	12.04	11.97

Table 4. Output voltage line-load regulation - V_{OUT1} (I_{OUT2} = 50 mA)

V_{IN} (V_{AC})	V_{OUT1} (I_{OUT2} = 50 mA)									
	No load		25% load		50% load		75% load		100% load	
	External biasing	Self-biasing	External biasing	Self-biasing	External biasing	Self-biasing	External biasing	Self-biasing	External biasing	Self-biasing
90	12.01	12.11	12.06	11.98	11.97	12.06	11.97	12.03	11.96	12.01
115	12.00	12.09	12.05	11.98	11.97	12.04	11.96	12.02	11.94	12.00
150	12.00	12.08	12.04	11.97	11.97	12.03	11.95	12.02	11.93	12.00
180	12.00	12.08	12.04	11.97	11.96	12.03	11.95	12.01	11.93	12.00
230	12.00	12.08	12.04	11.98	11.96	12.03	11.95	12.01	11.93	12.00
265	12.00	12.08	12.04	11.98	11.96	12.03	11.95	12.01	11.93	12.00

Figure 11. Line regulation (external biasing, I_{out2} = 0 mA)

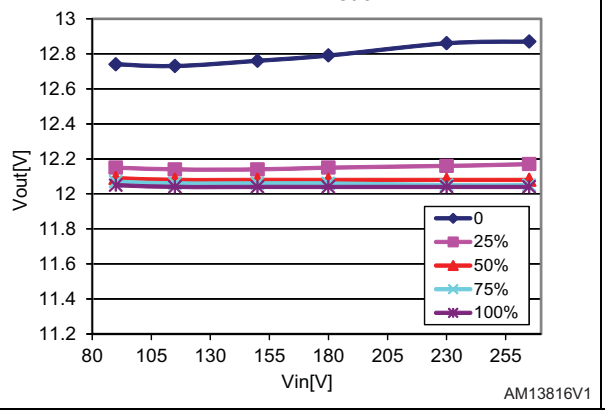


Figure 12. Line regulation (external biasing, I_{out2} = 50 mA)

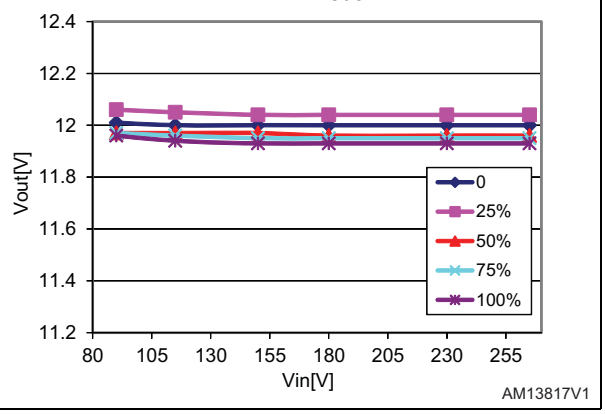


Figure 13. Load regulation (external biasing, I_{out2} = 0 mA)

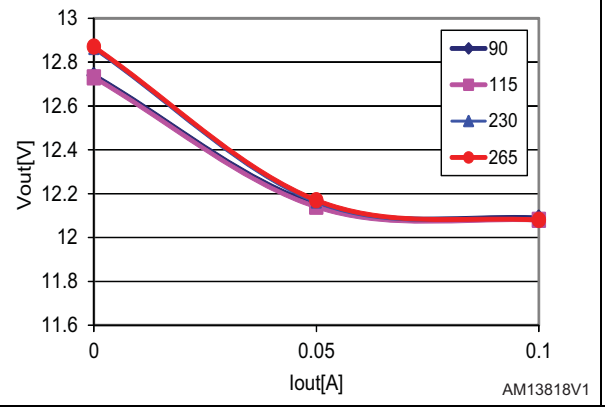
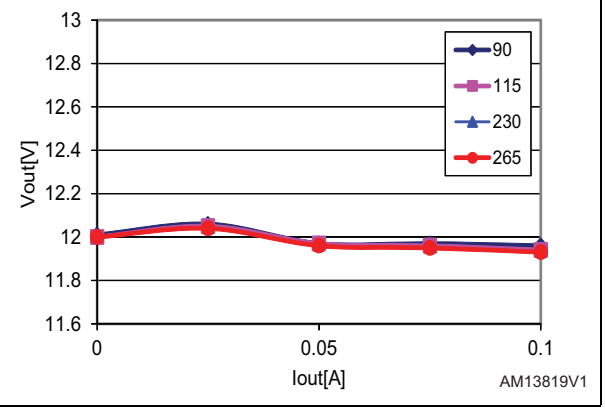


Figure 14. Load regulation (external biasing, I_{out2} = 50 mA)



The ripple at the switching frequency, superimposed to the output voltage V_{OUT1}, has also been measured and it is shown in figures below at maximum load and nominal input voltages.

Figure 15. Output voltage ripple at max. load 90 V_{AC}

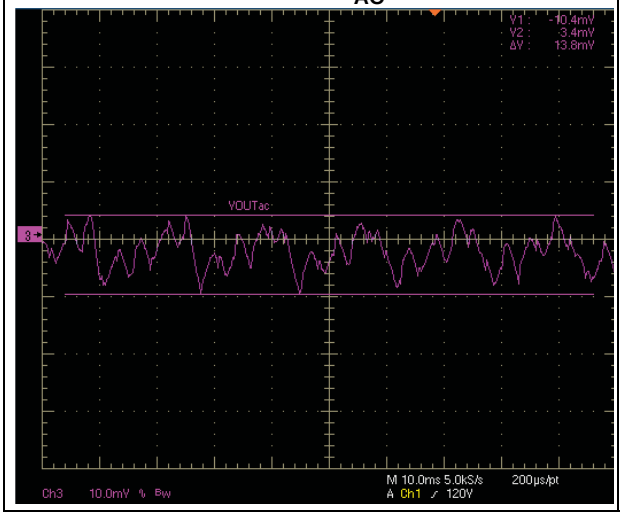
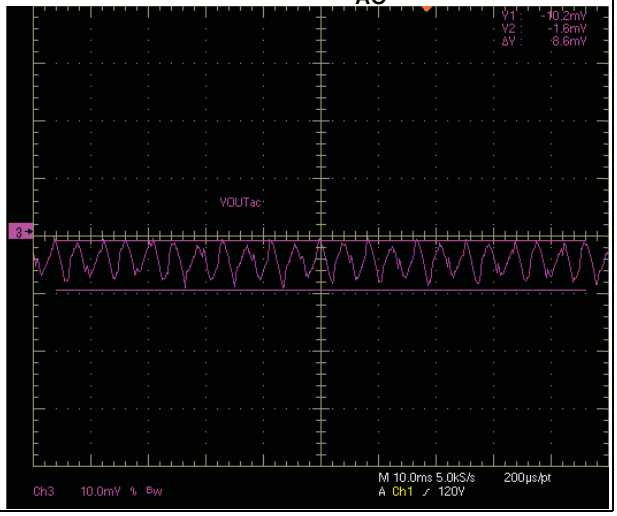


Figure 16. Output voltage ripple at max. load 265 V_{AC}



4.3 Standby performance

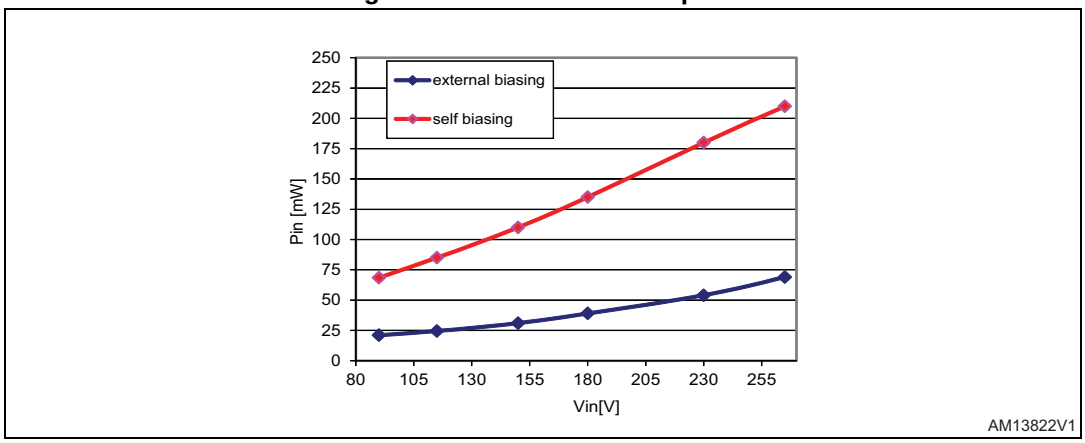
As explained in *Section 2*, two different settings of the IC biasing are possible in the present product evaluation board.

If low standby power loss is a priority, J1 should be selected; it connects diode D6 and disables the HV current generator during steady-state operation. If standby loss is not the main focus, the IC can be self-biased (by deselecting J1), saving the cost of the D6 diode.

The standby performance is shown in the figure below for both cases, with linear regulator disconnected and a 15 V Zener diode across the 12 V output to avoid overvoltage in no load conditions.

The highest line represents the consumption of the converter in those cases where diode D6 is not assembled (IC self-biased), the lower line is the consumption of the converter with diode D6 (IC externally biased).

Figure 17. No load consumption



4.4 Efficiency

The active mode efficiency is defined as the average of efficiency measured at 25%, 50%, 75% and 100% of maximum load, at nominal input voltages (V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC}).

External power supplies (those contained in a separate housing from the end-use devices they are powering) need to comply with the Code of Conduct, version 5 active mode efficiency criterion, which, for a power throughput of 1.5 W, states the active mode efficiency is higher than 67.4% (CoC5 Tier 1, entered into force in january 2014); this limit should increase to 70% starting from january 2016 (CoC5 Tier 2).

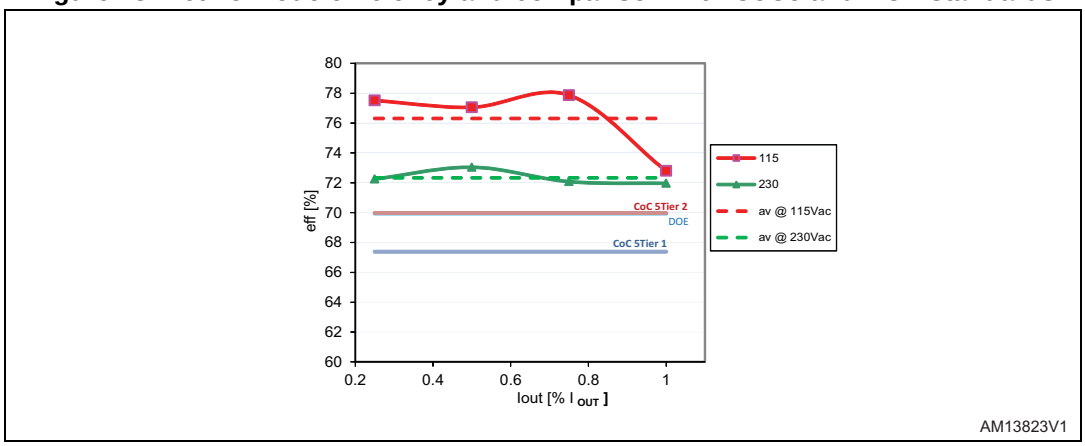
DOE (department of energy) recommendation is another standard, whose active mode efficiency requirement for the same power throughput is 69.9%.

The above requirements refer to single output converters and they do not apply to the presented evaluation board, which has two outputs. However, due to the following setting, this board can be evaluated as a single output converter:

- OUT1 loaded with a nominal load: $I_{OUT}1$ = 130 mA (corresponding to the nominal power throughput of the board when loaded on both outputs)
- The L7805 connected but no loaded ($I_{OUT}2$ = 0)

In this manner, the board is compliant with the above mentioned standards, see *Figure 18*, where the average efficiency measurements at 115 V_{AC} (76.3%) and at 230 V_{AC} (72.3%) are plotted with dotted lines. In the same figure the efficiency at 25%, 50%, 75% and 100% of load for both input voltages is also shown.

Figure 18. Active mode efficiency and comparison with CoC5 and DOE standards



CoC5 standard has also some requirements on the active mode efficiency when the output load is 10% of the nominal output power. The comparison between the requirement for an external power supply with a power throughput of 1.5 W and the performance of the evaluation board is shown in *Table 5*, where the STEVAL-ISA119V1 is Tier 1 and Tier 2 compliant.

Table 5. CoC5 requirement and performance at 10% output load

CoC5 minimum efficiency requirement in active mode at 10% of full load (P_{OUT} = 1.5 W)		Board performance
Tier 1	Tier 2	
57.4%	60%	62.7%

4.5 Light load performance

In the version 5 of the Code of Conduct, the power consumption of the power supply is considered even if it is not loaded. Concerning standards, *Table 6* gives some indications:

Table 6. Energy consumption criteria for no load

Nameplate output power (Pno)	Maximum power in no load for AC-DC EPS	
	Tier 1	Tier 2
0.3 W < Pno ≤ 49 W	0.15 W	0.075 W
50 W < Pno < 250 W	0.25 W	0.15 W

In no load condition and with different input voltages, the input power of the converter has been measured and results are reported in *Table 7*.

The board is compliant with both Tier 1 and Tier 2 requirements. In the same table the consumption of the board in some other light load cases (P_{OUT} = 25 mW, P_{OUT} = 50 mW and P_{OUT} = 250 mW) is also shown.

The load profile is: load applied on OUT1 only; the L7805 connected but I_{OUT2} = 0 (see *Section 4.4*)

Table 7. Light load consumption

V_{IN} [V_{AC}]	P_{IN} [mW]			
	@ P_{OUT} = 0	@ P_{OUT} = 25 mW	@ P_{OUT} = 50 mW	@ P_{OUT} = 250 mW
115	56	85	115	365
230	67	98	128	390

According to the equipment supplied, there are several criteria to measure the performance of a converter. For instance, the ErP lot 6 criterion for light load performance, states that the input power in the standby condition should be less than 500 mW. A typical market requirement would be to achieve the same with a 250 mW load. The evaluation board can meet this requirement, as shown in *Table 7*.

Another criterion for light load evaluation is the measurement of the output power (or the efficiency) when the input power is equal to one watt. This and some other measurements under light load conditions are shown in *Table 7* and *Table 8*:

Table 8. Light load efficiency

V_{IN} [V_{AC}]	Efficiency [%]		
	@ P_{IN} = 250 mW	@ P_{IN} = 500 mW	@ P_{IN} = 1 W
115	64.2	72.6	76.3
230	58.3	68.2	70.5

5 Functional check

5.1 Startup

The start-up phase at maximum load is shown in *Figure 19*, *20*, *21* and *22* at both nominal input voltages (115 V_{AC} and 230 V_{AC}).

Figure 19. Startup at V_{IN} = 115 V_{AC} full load

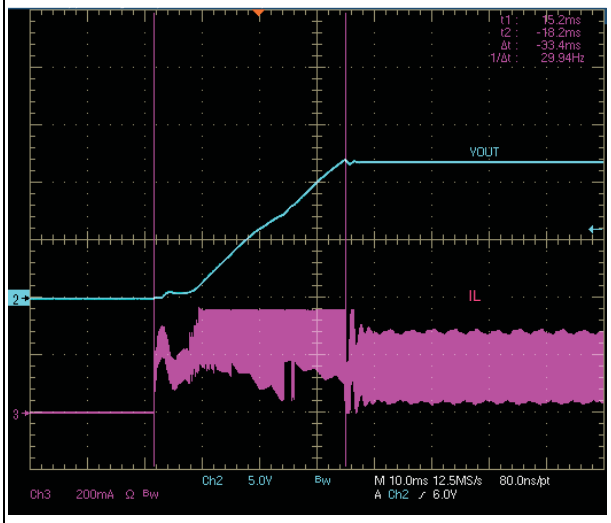


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Figure 20. Startup at V_{IN} = 115 V_{AC} full load (zoom)

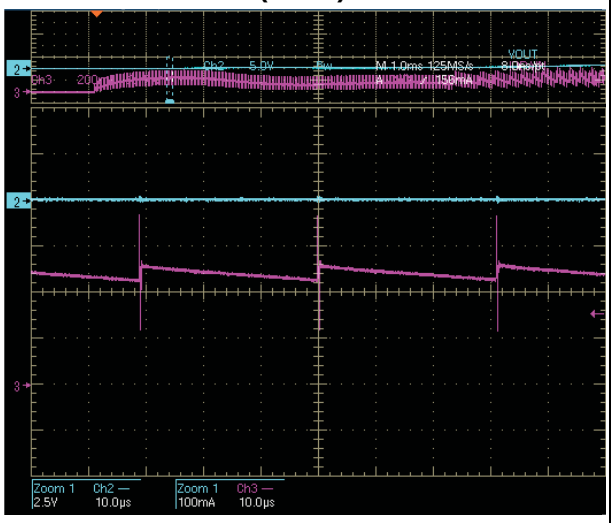

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Figure 21. Startup at V_{IN} = 230 V_{AC} full load

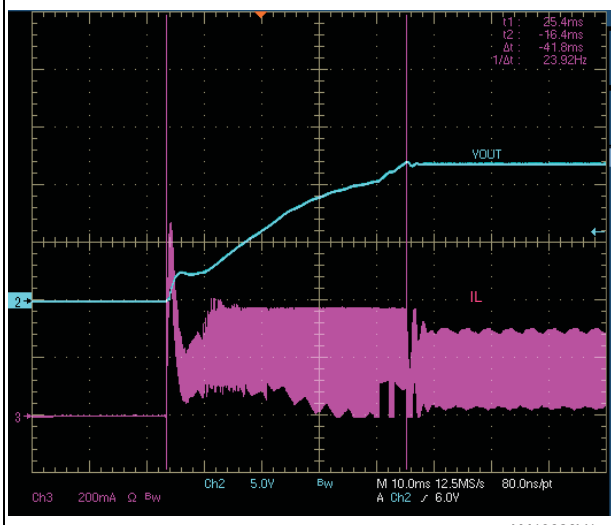

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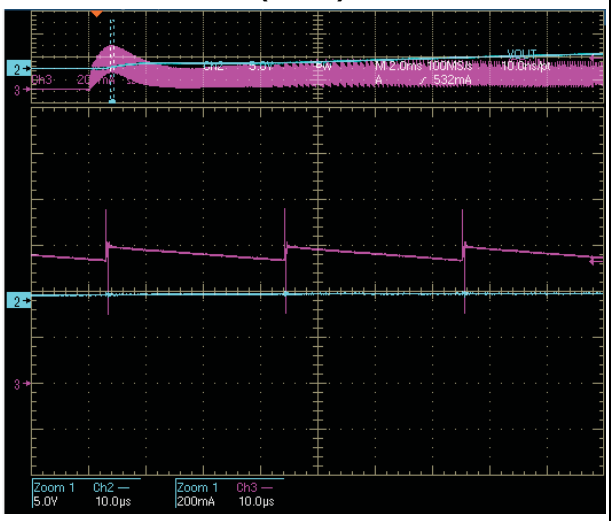
Figure 22. Startup at V_{IN} = 230 V_{AC} full load (zoom)



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5.2 Overload protection

In case of overload or short-circuit (see *Figure 23*), the current across the inductor L2 reaches the I_{DLIM} value. In every cycle where this condition is met, a counter is incremented; if it is maintained continuously for t_{OVL} time (50 msec typical, internally set) the overload protection is tripped, the power section is turned off and the converter is disabled for a $t_{RESTART}$ time (1 sec typical). When this time has elapsed, the IC resumes switching and, if the short is still present, the protection occurs indefinitely in the same way (see *Figure 24*). This ensures restart attempts of the converter with low repetition rate, so that it can work safely with extremely low power throughput and avoid the IC overheating in case of repeated overload events.

After the short removal, the IC resumes working normally. If the short is removed during t_{SS} or t_{OVL}, i.e. before the protection tripping, the counter is decremented on a cycle-by-cycle basis down to zero and the protection is not tripped.

If the short-circuit is removed during $t_{RESTART}$, the IC must wait for the $t_{RESTART}$ period to elapse before switching is resumed (see *Figure 26*).

Figure 23. Output short-circuit applied: OLP tripping

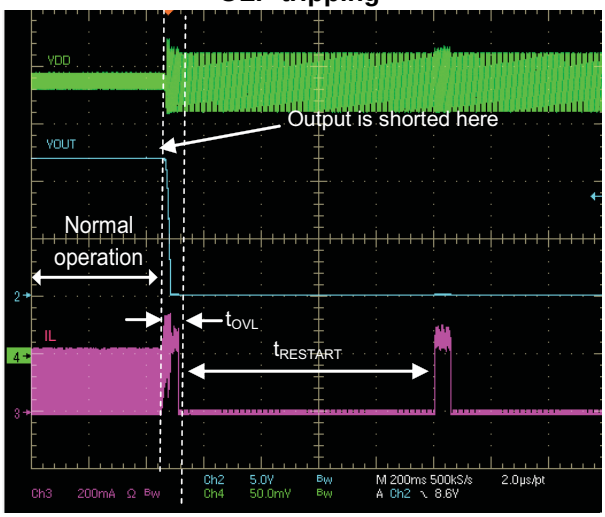


Figure 24. Output short-circuit maintained: OLP steady-state

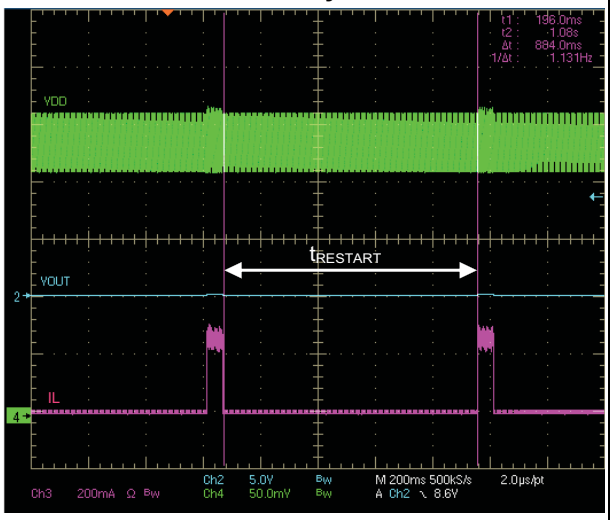


Figure 25. Output short-circuit maintained: OLP steady-state (zoom)

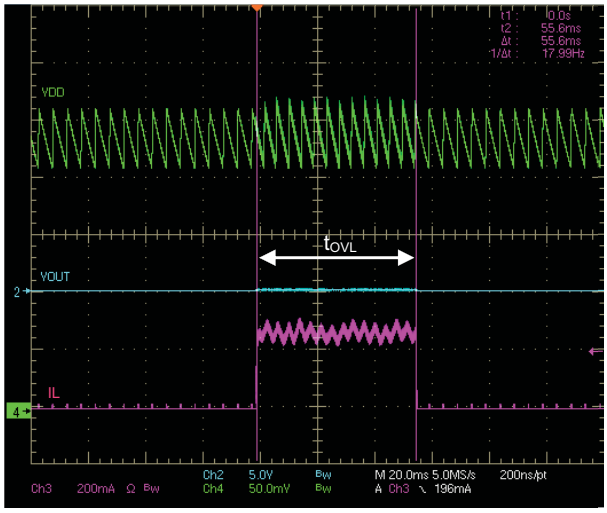
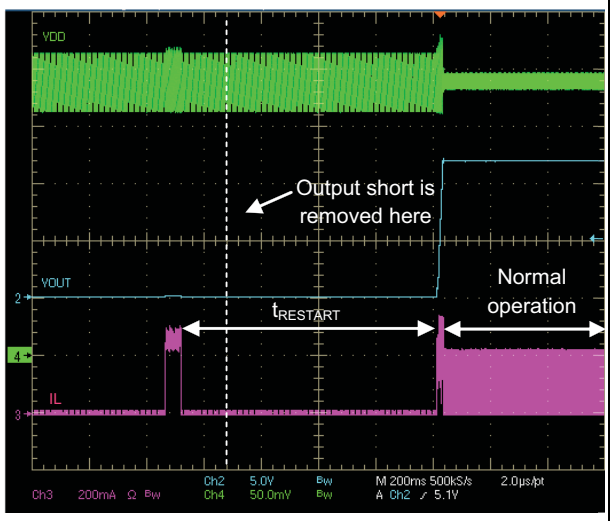


Figure 26. Output short-circuit removal and converter restart



5.3 Feedback loop failure protection

This protection is available any time IC is externally biased. As the loop is broken (R4 shorted or R5 open), V_{OUT1} increases and the VIPER16LD runs to its maximum current limitation. If J1 is selected, V_{DD} pin voltage increases as well, because it is linked to V_{OUT1} through diode D6.

If V_{DD} voltage reaches $V_{DDclamp}$ threshold (23.5 V min.) in less than 50 msec, IC is shut down by open loop failure protection (see *Figure 27* and *28*), otherwise by OLP, as described in the previous section. The breaking of the loop has been simulated by shorting the low-side resistor of the output voltage divider, R4. The same behavior can be induced opening the high-side resistor, R5 = R5A + R5B.

The protection acts in auto restart mode with $t_{RESTART}$ = 1 sec (see *Figure 28*). As the fault is removed, normal operation is restored after last $t_{RESTART}$ interval has been completed (see *Figure 30*).

Figure 27. Feedback loop failure protection: tripping

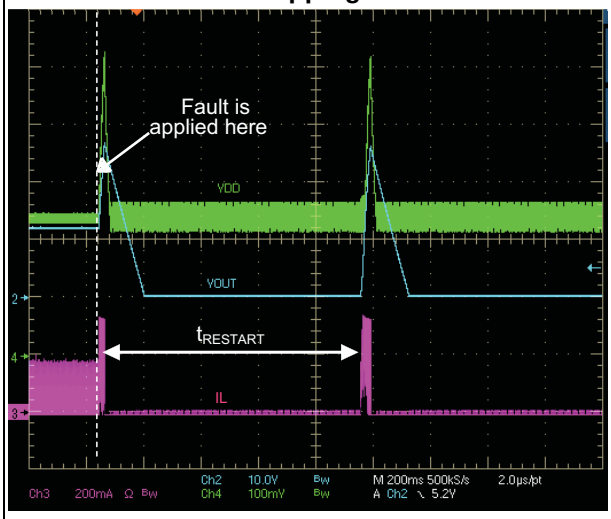


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Figure 28. Feedback loop failure protection: steady-state

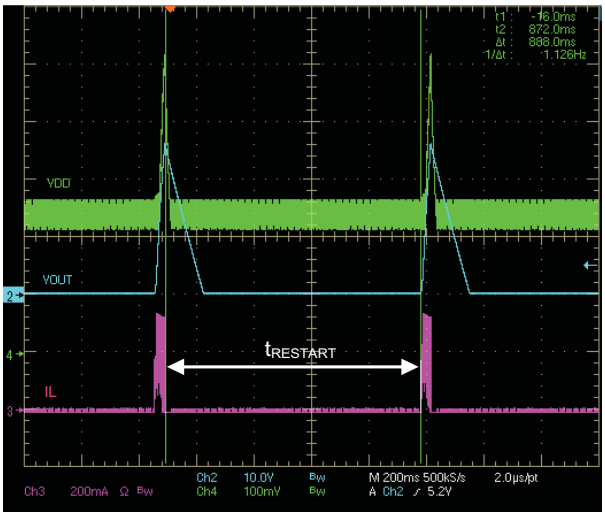

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Figure 29. Feedback loop failure protection: steady-state (zoom)

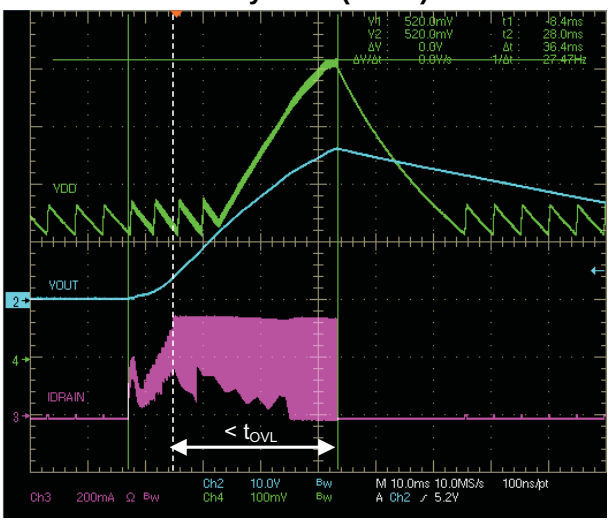

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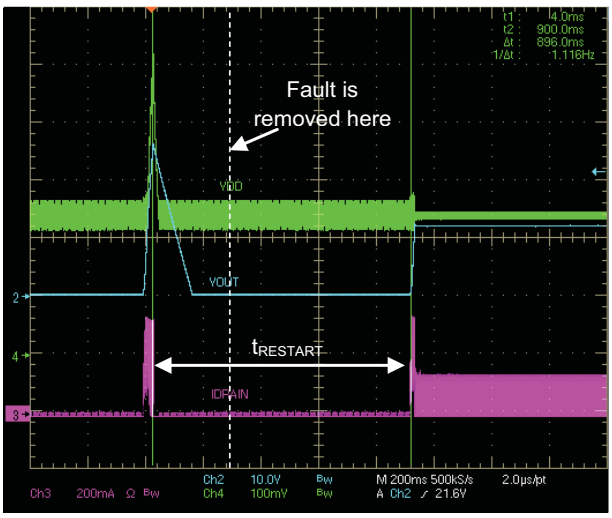
Figure 30. Feedback loop failure protection: converter restart



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6 Thermal measurements

A thermal analysis of the product evaluation board in full load conditions at T_{AMB} = 25 °C has been performed using an IR camera. Results are shown in the following figures, where the check points A, B, C and D indicate respectively: IC2, VIPer16LD, D4 and room temperature.

Figure 31. Thermal measurement at V_{IN} = 90 V_{AC}, full load (I_{OUT1} = 100 mA, I_{OUT2} = 50 mA)

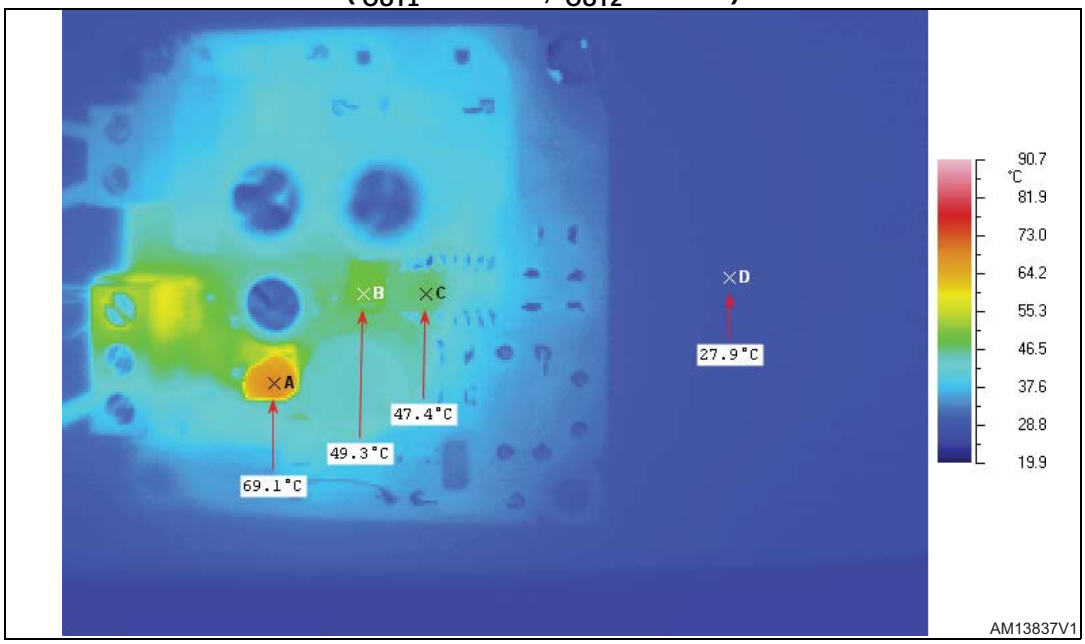


Figure 32. Thermal measurement at V_{IN} = 115 V_{AC}, full load (I_{OUT1} = 100 mA, I_{OUT2} = 50 mA)

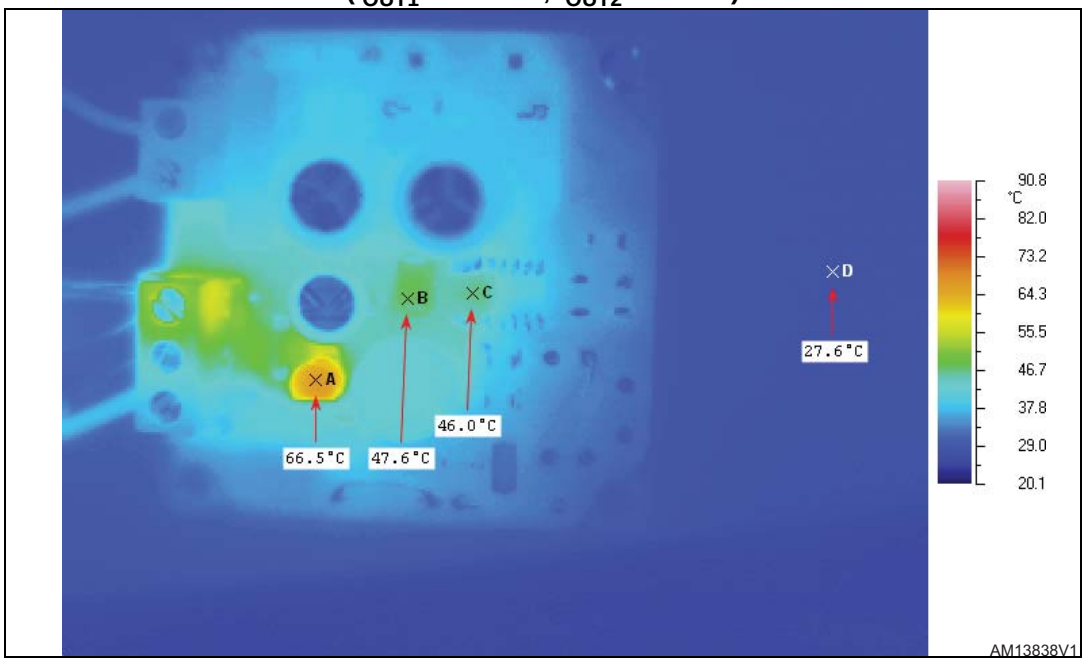


Figure 33. Thermal measurement at V_{IN} = 230 V_{AC}, full load (I_{OUT1} = 100 mA, I_{OUT2} = 50 mA)

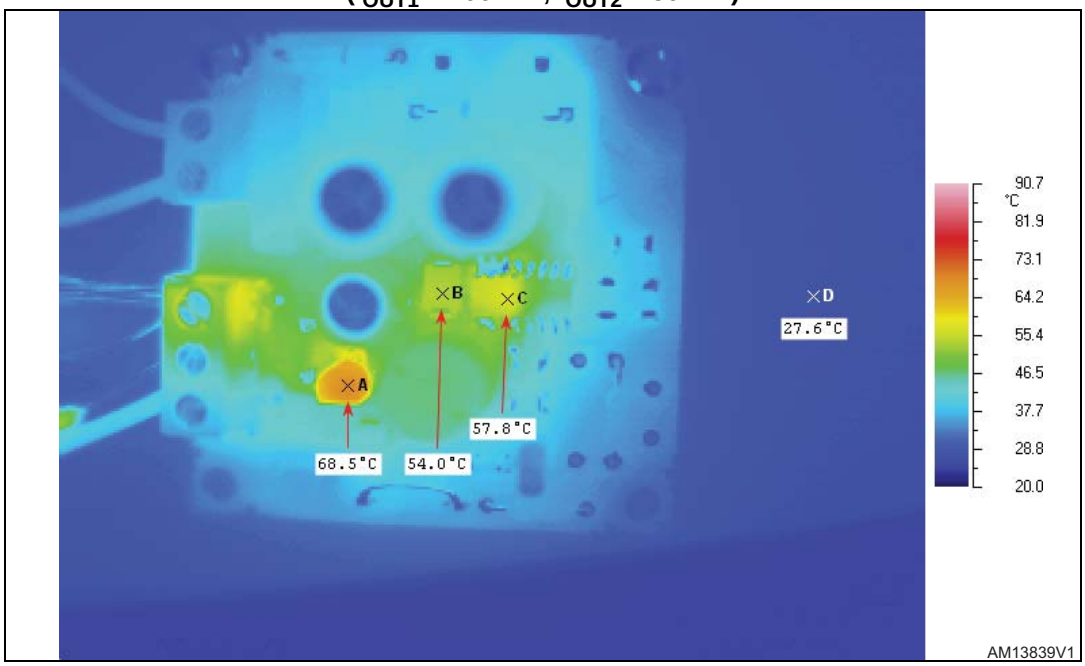
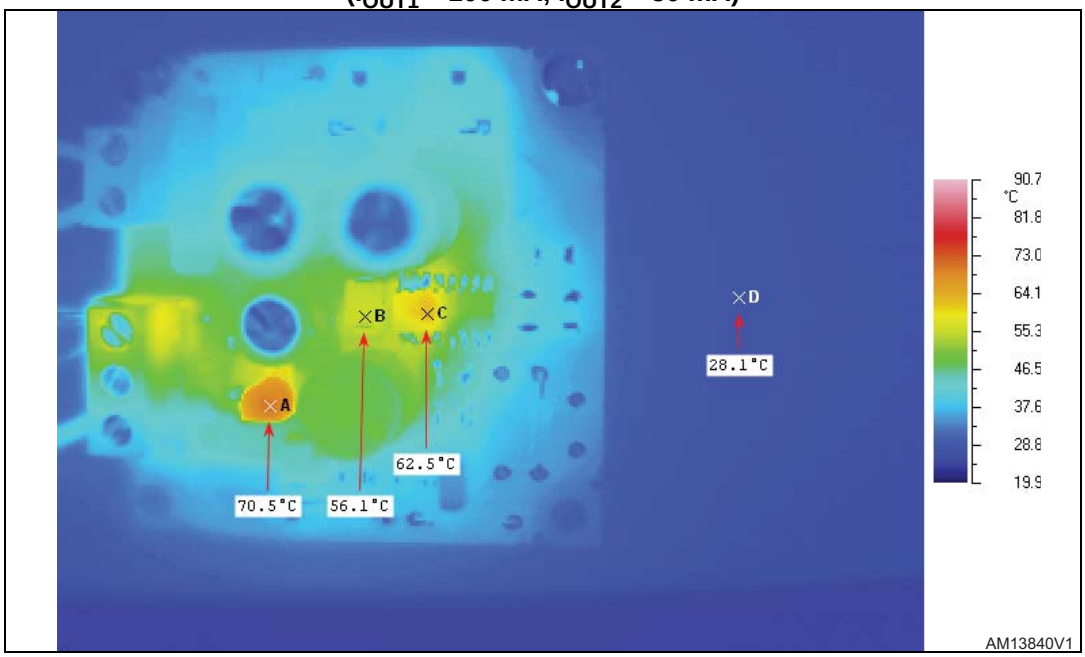


Figure 34. Thermal measurement at V_{IN} = 265 V_{AC}, full load (I_{OUT1} = 100 mA, I_{OUT2} = 50 mA)



7 EMI measurements

A pre-compliance test to EN55022 (Class B) european normative has been performed using an EMC analyzer and an LISN. The average EMC measurements at 115 V_{AC}/full load and 230 V_{AC}/full load have been performed and the results are shown in *Figure 35* and *36*.

Figure 35. Average measurement at V_{IN} = 115 V_{AC}, full load (I_{OUT1} = 100 mA, I_{OUT2} = 50 mA)

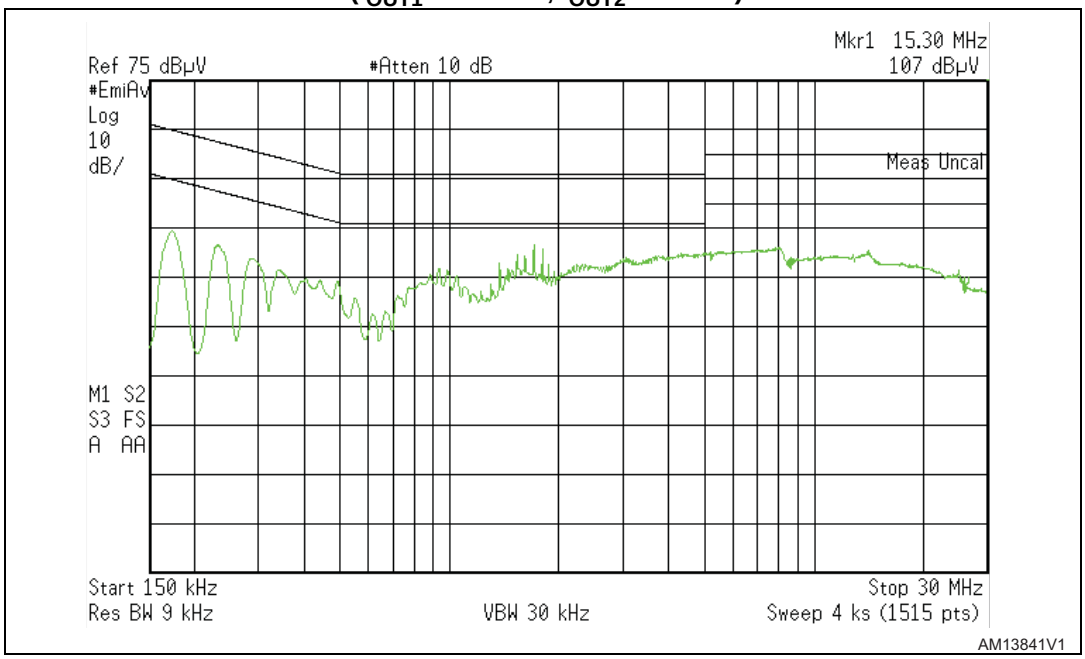
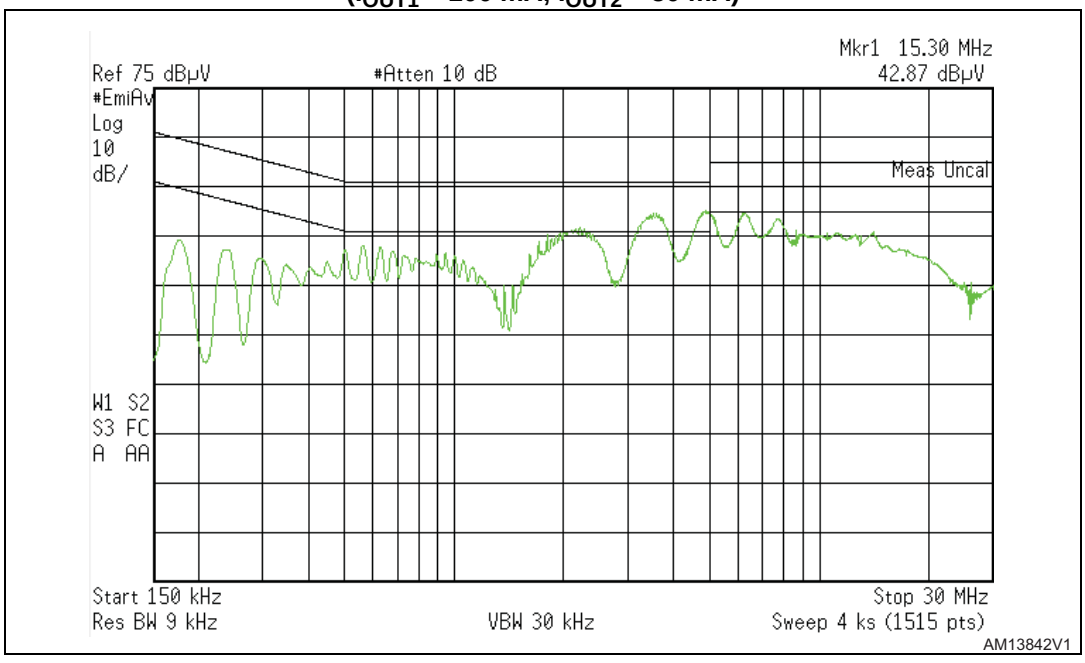


Figure 36. Average measurement at V_{IN} = 230 V_{AC}, full load (I_{OUT1} = 100 mA, I_{OUT2} = 50 mA)

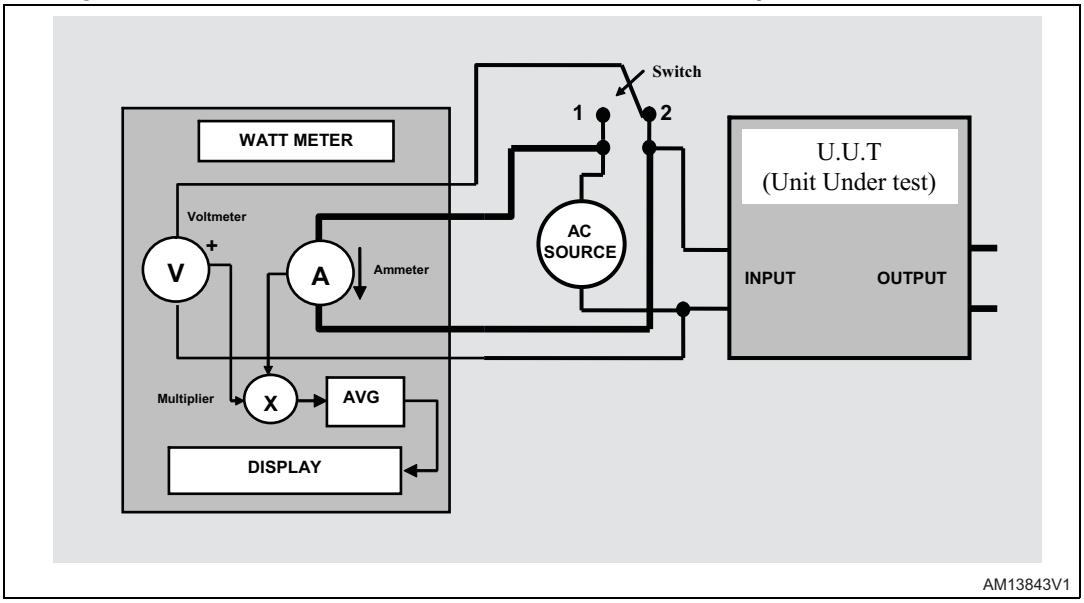


Appendix A Test equipment and measurement of efficiency and light load performance

The converter input power has been measured using a wattmeter. The wattmeter measures simultaneously the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The wattmeter is a digital instrument so it samples the current and voltage and converts them to digital forms. Digital samples are then multiplied giving the instantaneous measured power. The sampling frequency is in the range of 20 kHz (or higher depending on the instrument used). The display provides the average measured power, averaging the instantaneous measured power in a short period of time (1 sec typ.).

Figure 37 shows how the wattmeter is connected to the UUT (unit under test) and to the AC source and the wattmeter internal block diagram.

Figure 37. Connections of the UUT to the wattmeter for power measurements



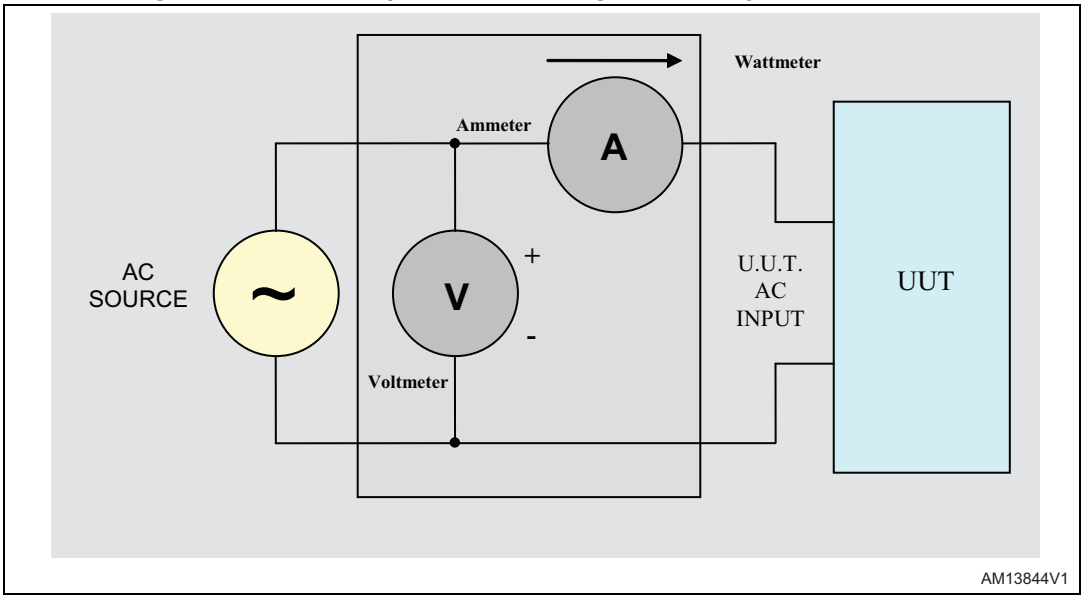
An electronic load has been connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage has been measured by a voltmeter. The output power is the product between load current and output voltage. The ratio between the output power, calculated as previously stated, and the input power, measured by the wattmeter, is the converter's efficiency, which has been measured in different input/output conditions.

A.1 Measuring input power

With reference to *Figure 37*, the UUT input current causes a voltage drop across the ammeter's internal shunt resistance (the ammeter is not ideal so it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

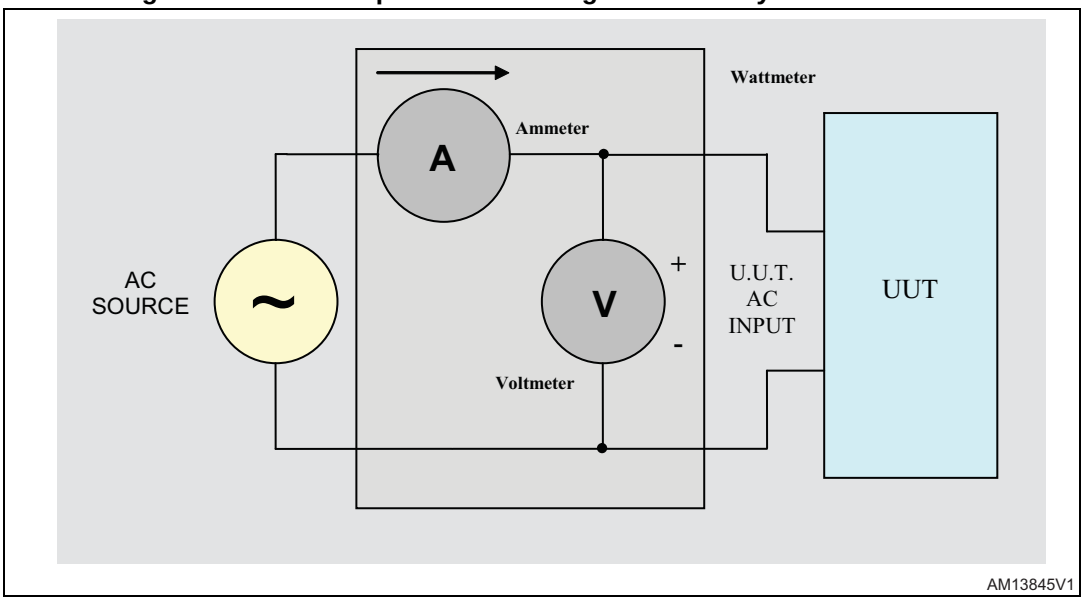
If the switch of *Figure 37* is in position 1 (see also the simplified scheme of *Figure 38*), this voltage drop causes an input measured voltage higher than the input voltage at the UUT input that, of course, affects the measured power. The voltage drop is generally negligible if the UUT input current is low (for example when we are measuring the input power of UUT in light load conditions).

Figure 38. Switch in position 1-setting for standby measurements



In case of high UUT input current (i.e. for measurements in heavy load conditions), the voltage drop can be relevant compared to the UUT real input voltage. If this is the case, the switch in *Figure 37* can be changed to position 2 (see simplified scheme of *Figure 39*) where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 39. Switch in position 2-setting for efficiency measurements



On the other hand, the position of *Figure 39* may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (which is not an ideal instrument and doesn't have infinite input resistance) is not negligible. This is the reason why it is better to use the setting of *Figure 38* for light load measurements and *Figure 39* for heavy load measurements.

If it is not clear which measurement scheme has the lesser effect on the result, both of them should be tested and then, the lower input power value should be registered.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT is operated at 100% of nameplate output current for at least 30 minutes (warm-up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power is monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and measurements can be recorded at the end of the 5-minute's period. If AC input power is not stable over a 5-minute's period, the average power or accumulated energy is measured overtime for both AC input and DC output.

Some wattmeter models allow integration of the measured input power in a time range and then measure the energy absorbed by the UUT during the integration time. The average input power is calculated dividing by the integration time itself.

8 References

[1] Code of Conduct on energy efficiency of external power supplies, version 4

[2] VIPER16 datasheet

9 Revision history

Table 9. Document revision history

Date	Revision	Changes
09-Dec-2014	1	Initial release.