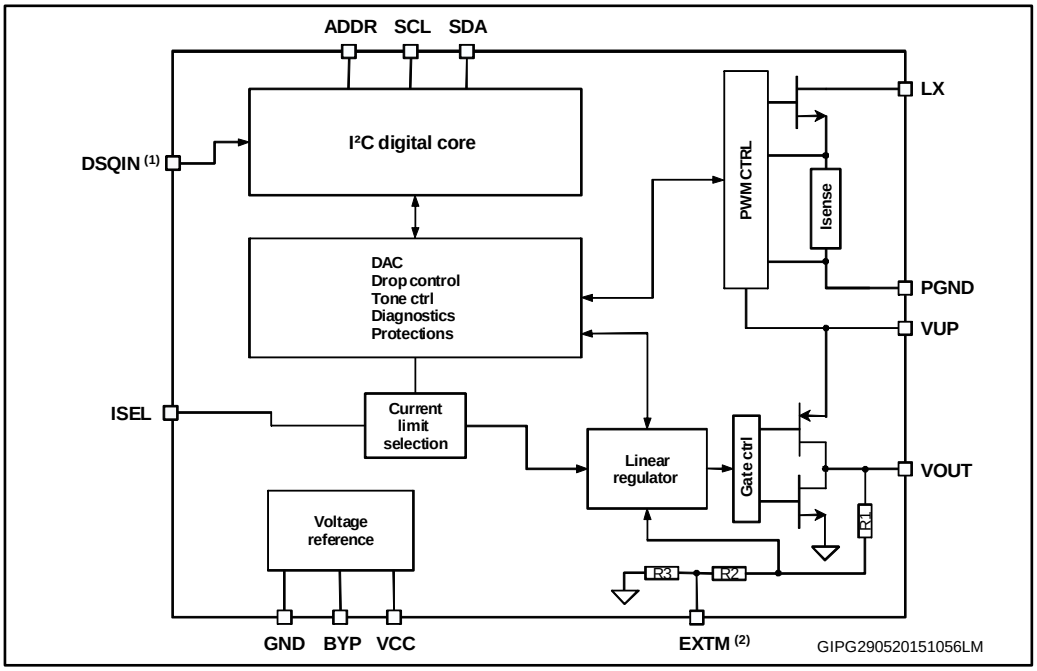
AN4693
Application note

LNBH29 supply and control IC with step-up and I²C interface

Introduction

This application note provides additional information and suggestions about the correct use of the LNBH29 device. All waveforms shown are based on the evaluation board STEVAL-CBL015V1 for the LNBH29 version and the STEVAL-CBL016V1 for the LNBH29E version, described in *Section 5: "Layout guidelines"* . The LNBH29 is a low-cost integrated solution for supplying/interfacing satellite LNB modules. Its performance is very good with the minimum quantity of external components. It includes all functions needed for the LNB supply and interface, in accordance with international standards. Moreover, it includes an I^{2}C bus interface and, thanks to a fully integrated step-up DC-DC converter, it works with a single input voltage supply range from 8 V to 17.5 V.

Figure 1: Internal block diagram



- DSQIN pin is available on the LNBH29 version only.
- EXTM pin is available on the LNBH29E version only.

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1 Internal blocks

1.1 Voltage reference block

This block includes the undervoltage lockout circuit, which disables the whole circuit when the supplied VCC pin drops below a fixed threshold (4.7 V typ.) and a power-on reset sets all the I^2C registers to zero when the VCC turns on and rises from zero above the threshold (4.8 V typ.). If the input voltage is lower than LPD (low power diagnostic) minimum thresholds (6.7 V typ.), the PNG I²C bit is set to “1” by the voltage reference block.

1.2 I^2C interface digital core and diagnostic

The device main functions are controlled by I^2C bus, the data communication protocol from the main microprocessor to the LNBH29 and viceversa, which takes place through SDA and SCL pins. By writing to control register, all the LNBH29 functions can be managed. Moreover, the status register can be read back and provide 5 diagnostic functions received by the IC. The LNBH29 I^2C interface address can be selected between two different addresses by setting the voltage level of the dedicated ADDR pin.

Five bits report the diagnostic status of eight internal monitoring functions:

-OLF: overload fault. If the output current required exceeds the current limit threshold or a short-circuit occurs, OLF I^2C bit is set to "1".

- OTF: overtemperature fault. If an overheating occurs, (junction temperature exceeds 150 °C typ.) the OTF I^2C bit is set to "1".

- PNG: power not good. If the input voltage (VCC pin) is lower than LPD minimum threshold (6.7 V typ.) the PNG I^2C bit is set to "1".

-VMON: voltage monitoring. If the output voltage (VOUT pin) is lower than VMON specification thresholds, the VOM I^2C bit is set to "1".

-PDO: pull-down overcurrent. If the device output rises to a voltage level higher than the output nominal voltage selected, PDO I^2C bit is set to "1". This may happen due to an external voltage source present on the LNB output (VOUT pin).

1.3 Linear post-regulator and current limit

The output voltage selection and the current selection commands join this block, which manages all the LNB output functions. This block gives feedback to the I^2C interface overcurrent protection and output settings. The linear post-regulator current limit threshold can be set by an external resistor connected to the ISEL pin.

2 DiSEqC data encoding

The LNBH29 series includes two versions with different DiSEqC control pin solutions: the LNBH29 version with DSQIN pin and the LNBH29E version with EXTM pin, which is connected to an external 22 kHz DiSEqC tone source. The tone output waveform depends on the characteristics of an external signal injected due to the EXTM pin. The LNBH29 version is provided with the DSQIN logic input pin (TTL compatible) to be controlled by an external DiSEqC data envelope source, which activates the internal 22 kHz tone generator factory trimmed. This guarantees the tone output waveform in accordance with the DiSEqC standards.

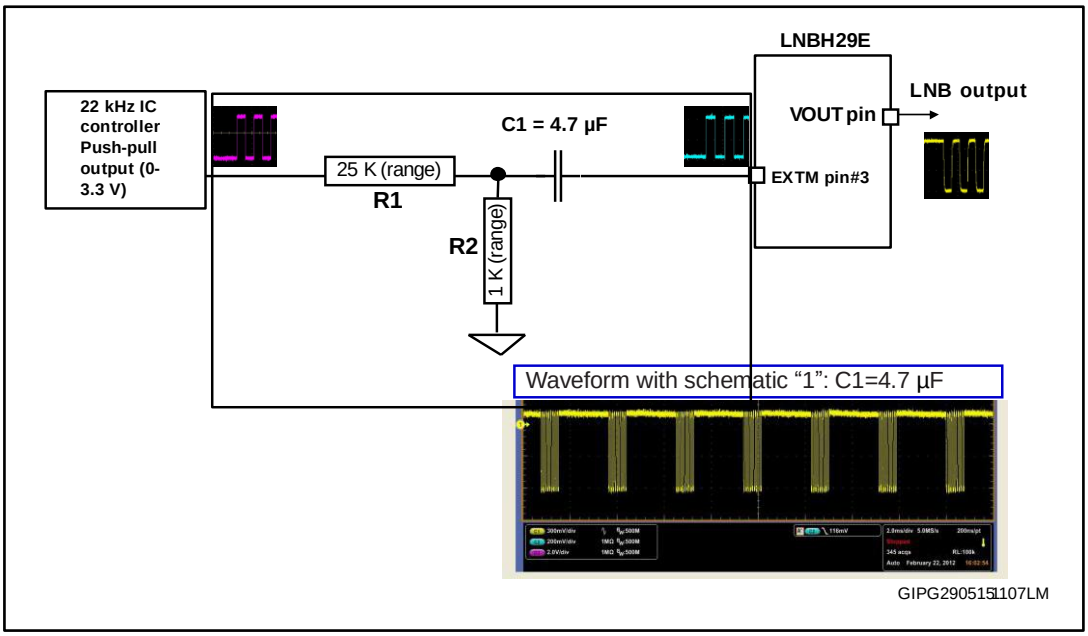
2.1 LNBH29E version: 22 kHz external source (EXTM function)

In order to improve the design flexibility, an analogic modulation input pin is available (EXTM) to generate 22 kHz tone superimposed to the VOUT DC output voltage. An appropriate DC blocking capacitor must be used to couple the 22 kHz modulating signal source to the EXTM pin. The EXTM pin tunes the VOUT voltage through the series decoupling capacitor, in this manner:

VOUT(AC) = VEXTM(AC) x GEXTM

where VOUT(AC) and VEXTM(AC) are, respectively, the peak-to-peak AC voltage on the VOUT pin and on the EXTM pin, while GEXTM is the voltage gain between the EXTM voltage and VOUT signal.

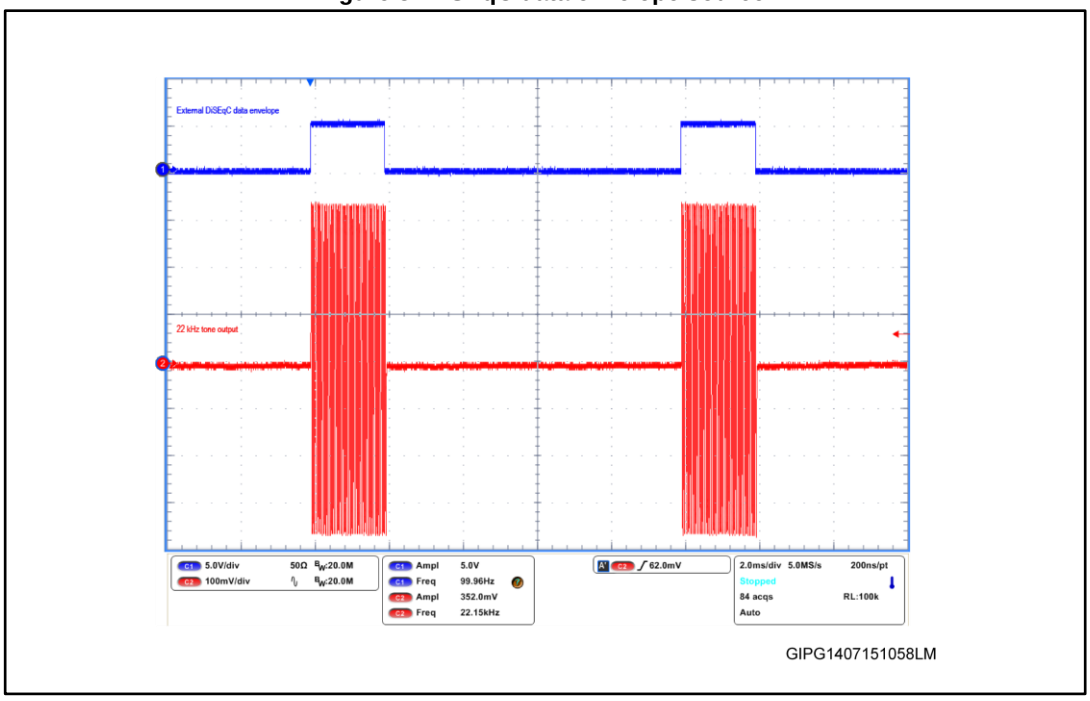
Figure 2: 22 kHz external source



2.2 LNBH29 version: DiSEqC data envelope source

If an external DiSEqC code envelope source is available, it is possible to use the internal 22 kHz generator activated during the tone transmission by connecting the DiSEqC envelope source to the DSQIN pin. During the period in which the DSQIN is kept high, the internal control circuit activates the 22 kHz tone output.

Figure 3: DiSEqC data envelope source



22 kHz tone on the VOUT pin is active with about 6 µs delay from the DSQIN TTL signal rising edge, and it stops with a delay time in the range from 15 µs to 60 µs after the 22 kHz TTL signal on DSQIN has expired (refer to *Figure 2*).

Figure 4: DiSEqC data envelope source activation delay

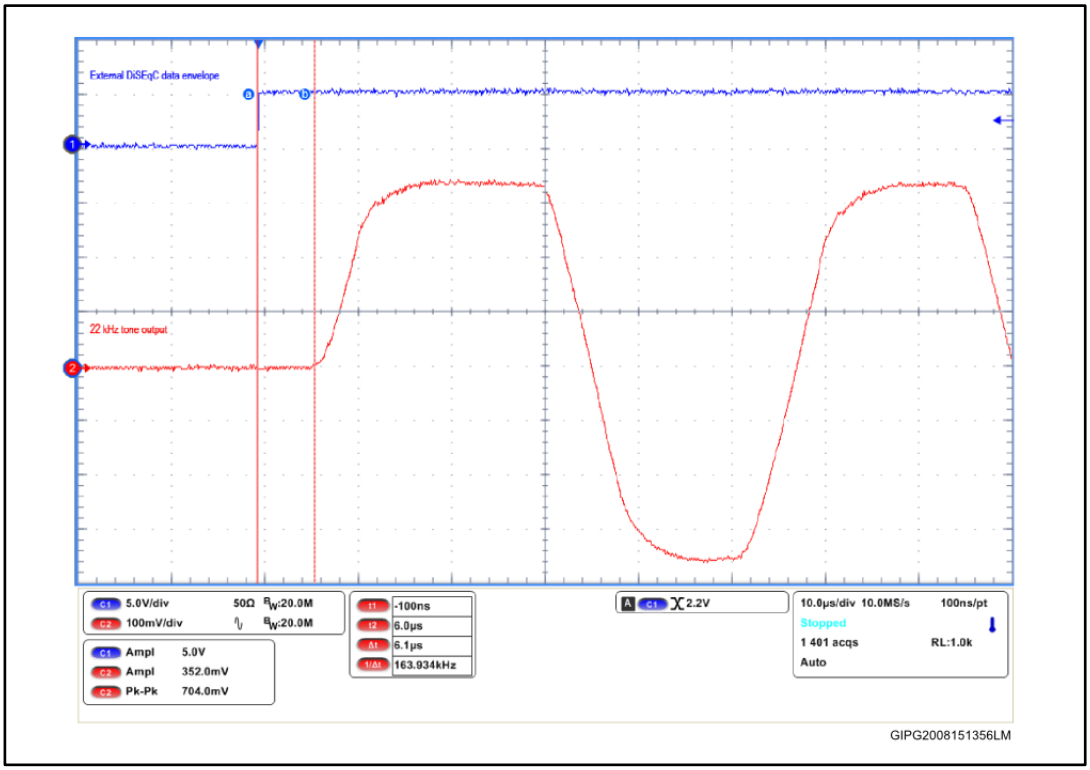
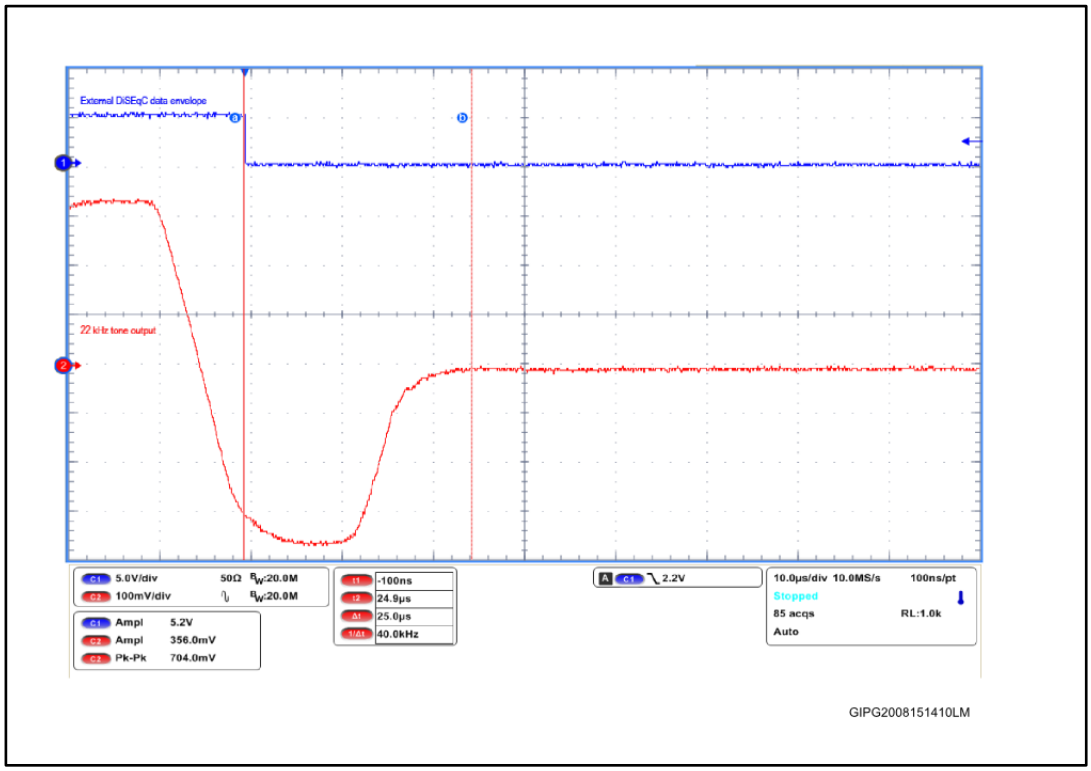
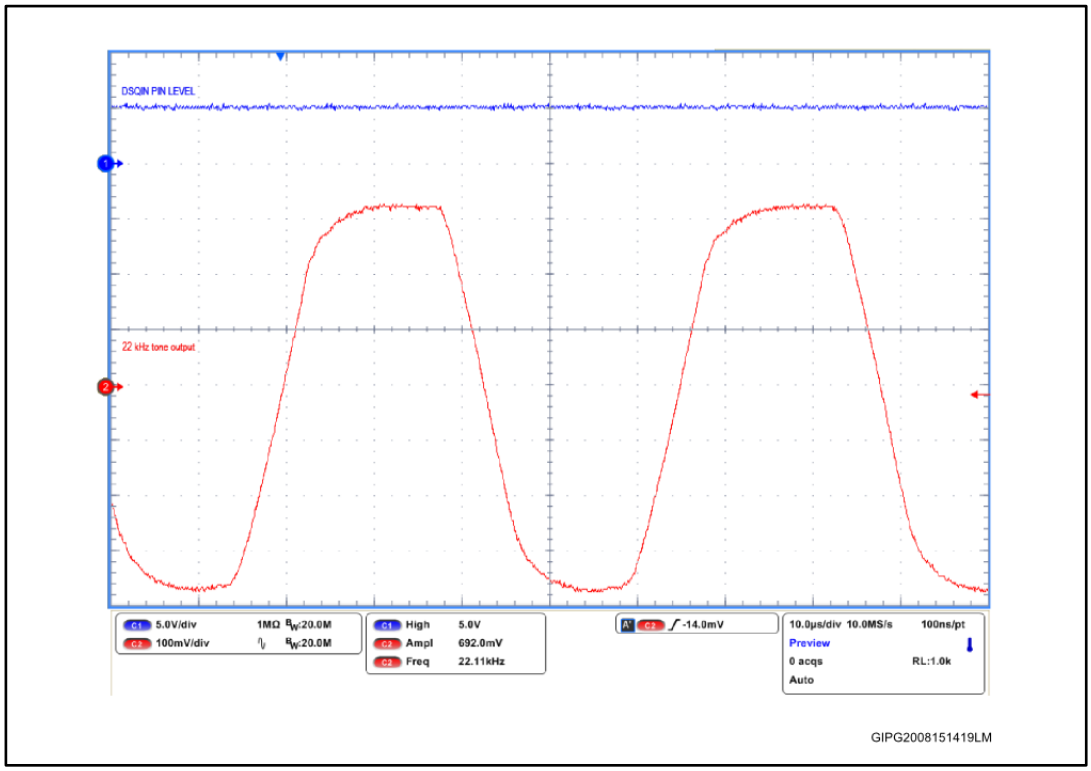


Figure 5: DiSEqC data envelope source deactivation delay



If a 22 kHz tone presence is requested in continuous mode, the DSQIN TTL pin must be pulled high.

Figure 6: 22 kHz tone in continuous mode



3 Pin description

The LNBH29 is available in QFN16L 3x3 and 4x4 with exposed pad package for surface mount assembly. The below figure shows the device pinout while *Table 1* briefly summarizes the pin functions.

Figure 7: Pin configuration (marking view)

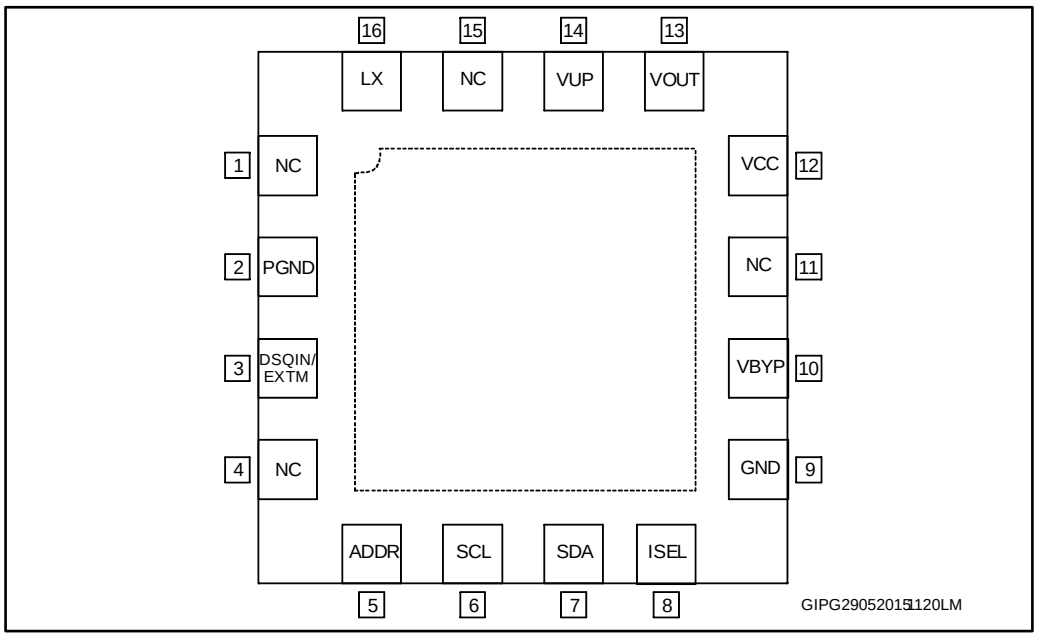


Table 1: Pin description

Pin	Symbol	Name	Function
16	LX	NMOS drain	Integrated N-channel power MOSFET drain
2	PGND	Power ground	DC-DC converter power ground
5	ADDR	Address setting	Two I^2C bus addresses available by setting the address pin level voltage
6	SCL	Serial clock	Clock from/to I^2C bus
7	SDA	Serial data	Bi-directional data from/to I^2C bus
8	ISEL	Current selection	Defines the linear regulator current limit threshold
9	GND	Analog ground	Analog circuit ground
10	BYP	Bypass capacitor	Needed for internal pre-regulator filtering
12	VCC	Supply input	8 to 16 V IC DC-DC power supply
13	VOUT	LNB output port	Output of the integrated very low drop linear regulator
14	VUP	Step-up voltage	Input of the linear post-regulator
3	EXTM/ DSQIN	External 22 kHz TTL input	External 22 kHz (LNBH29E version) DiSEqC envelope input (TTL compatible) from the main DiSEqC microcontroller (LNBH29 version)

Pin	Symbol	Name	Function
Epad	Epad	Exposed pad	To be connected with power ground and to the ground layer through vias to dissipate heat
1,11,15	NC	Not internally connected	Not internally connected pins. These pins can be connected to GND to improve thermal performance

4 Component selection guide

The LNBH29 application schematic in *Figure 8* and *Figure 9*, shows the typical configurations for a single LNB power supply for DiSEqC 1.x communication.

Figure 8: STEVAL-CBL015V1, LNBH29, evaluation board schematic

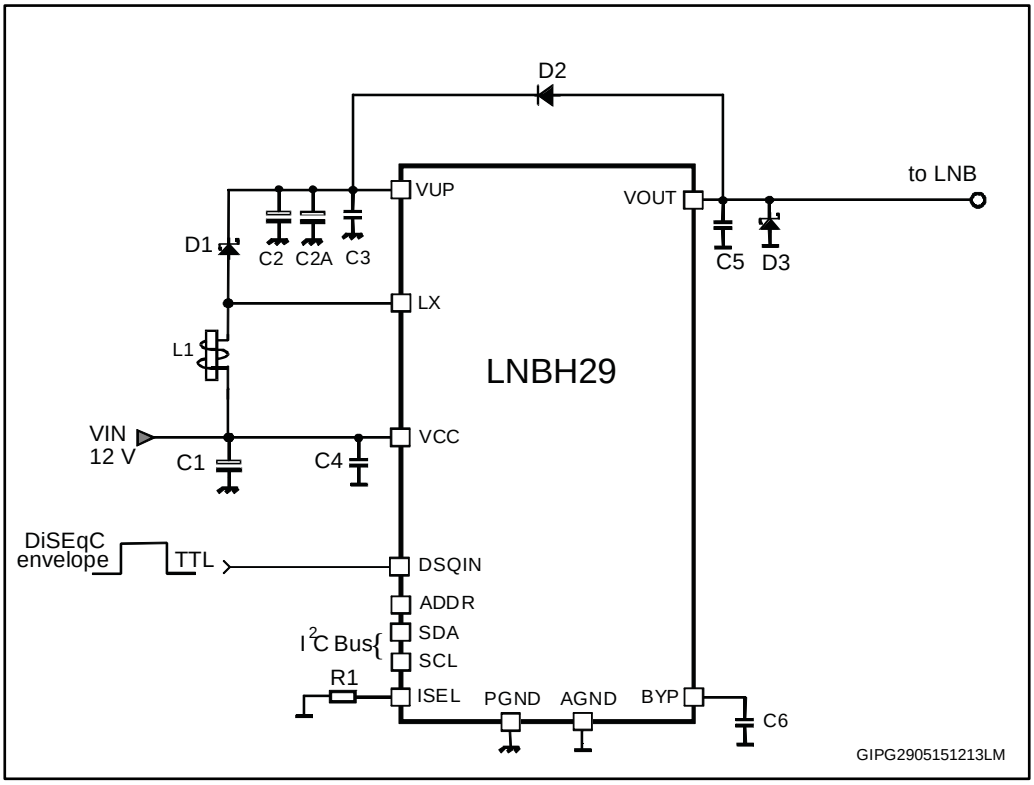


Figure 9: STEVAL-CBL016V1, LNBH29E version, evaluation board schematic

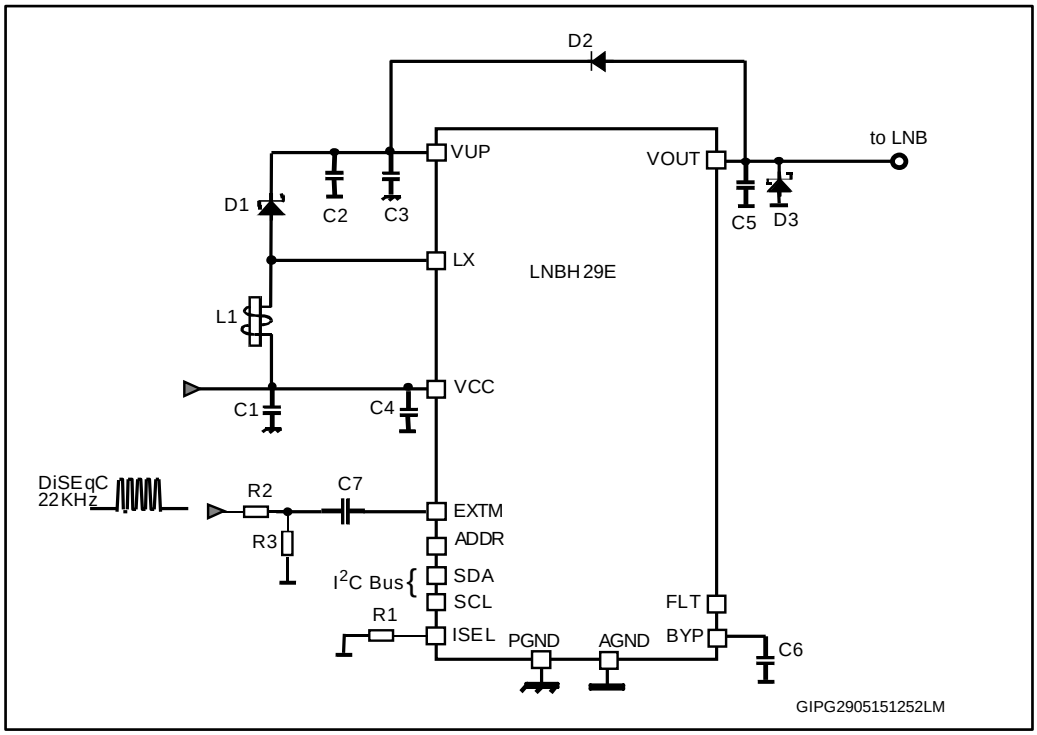


Table 2: LNBH29 evaluation board BOM list

Component	Notes
IC1	LNBH29 (QFN16L) exposed pad
C1	> 25 V electrolytic capacitor, 100 µF or higher is suitable or > 25 V ceramic capacitor, 10 µF or higher is suitable
C2	With COMP = 0, > 25 V electrolytic capacitor, 100 µF or higher is suitable or with COMP = 1, > 35 V ceramic capacitor, 22 µF (or 2 x 10 µF) or higher is suitable
C3	From 470 nF to 2.2 µF ceramic capacitor placed as close as possible to VUP pin. Higher values allow lower DC-DC noise
C4, C5, C6	0.22 µF 50 V ceramic capacitors
D1	STPS130A or any similar Schottky diode
D2	S1A general purpose diode
D3	BAT43 (or any Schottky diode with $I_{F(AV)}$>0.2 A, V_{RRM}>25 V) or BAT30, BAT54, TMM BAT43, 1N5818
TVS	LNBTVS22-XX TVS protection diode is suggested. Any other solution can be used depending on the requested surge protection level
L1	With COMP = 0, use 10 µH inductor with I_{sat} > I_{peak} where I_{peak} is the boost converter peak current or with COMP = 1 and C2 = 22 µF, use 6.8 µH inductor with I_{sat} > I_{peak} where I_{peak} is the boost converter peak current
RSEL	16.2 kΩ 1/16 W resistor

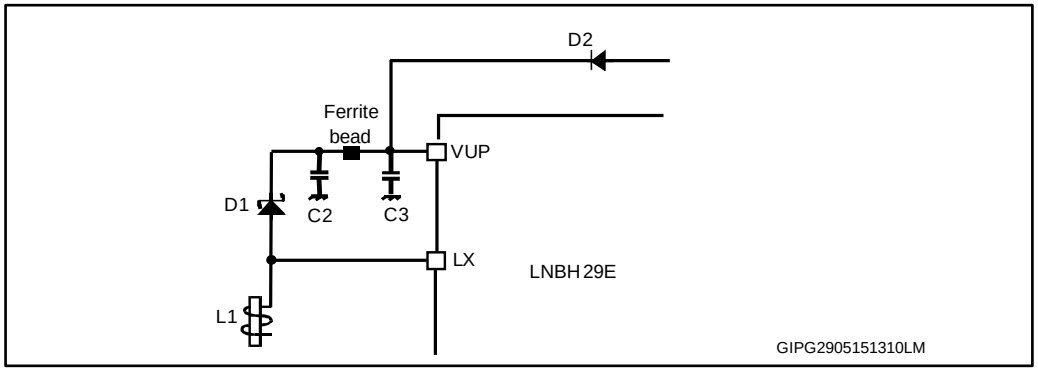
4.1 Input capacitors

A ceramic bypass capacitor (C1 in figure 8 and figure 9) between 10 µF and 47 µF placed near the LNBH29 is needed for a stable operation. In any case, a ceramic capacitor in the range from 100 nF to 470 nF is recommended to reduce the switching noise on the input voltage pin (C4 in figure 8 and figure 9).

4.2 DC-DC converter output capacitors

Electrolytic or ceramic capacitors are needed on the DC-DC converter output stage (C2 in *Figure 8* and *Figure 9*). With COMP I^2C bit is set 0, > 25 V electrolytic capacitor, 100 µF or higher is suitable. With COMP I^2C bit set to 1, > 25 V ceramic capacitor, 22 µF (or 2 x 10 µF) or higher is suitable. Moreover, a ceramic capacitor between 1 µF and 4.7 µF is recommended to reduce high frequency switching noise. The switching noise is due to the voltage spikes of the fast switching action of the output switch, and to the parasitic inductance of the output capacitors. To further reduce the switching noise, a ferrite bead is recommended between the capacitors (refer to *figure 10*).

Figure 10: DC-DC output stage with ferrite bead



The capacitor voltage rating must be at least 25 V, but if the highest voltage selection condition is used (V_{SEL1}= V_{SEL2}= V_{SEL3} = 1), 35 V or higher voltage capacitors are suggested.

4.3 COMP I^2C bit: boost compensation setting

The DC-DC converter compensation loop can be optimized to properly work with both ceramic and electrolytic capacitors (VUP pin). For this purpose, one I^2C bit in the DATA register (COMP) can be set to “1” or “0” as follows:

- COMP = 0 for electrolytic capacitors
- COMP = 1 for ceramic capacitors

For recommended DC-DC capacitor and inductor values refer to *Section 4.1: "Input capacitors"*, and to the BOM in *Table 2: "LNBH29 evaluation board BOM list"*.

4.4 DC-DC converter Schotty diode

In typical application conditions, 1 A Schottky diode is suitable for the LNBH29 DC-DC converter (D1 in *figure 8* and *figure 9*). Taking into consideration that the DC-DC converter Schottky diode must be selected depending on the application conditions,(VRRM > 25 V) one N-channel Schottky diode, such as the STPS130A is recommended. The average current flowing through the Schottky diode is lower than I_{peak} and can be calculated using

the equation 2. In worst-case conditions, such as low input voltage and higher output current, a Schottky diode capable of supporting the I_{peak} should be selected. See below formula:

Equation 1:

I_d = IOUT x VOUT/VIN

Table 3: Recommended Schottky diode

Vendor	Order code	I_F(AV)	V_F(max.)
STMicrolectronics	1N5818	1 A	0.50 V
	1N5819	1 A	0.55 V
	STPS130A	1 A	0.46 V
	STPS1L30A	1 A	0.30 V
	STPS2L30A	2 A	0.45 V
	1N5822	3 A	0.52 V
	STPS340	3 A	0.63 V
	STPS3L40A	3 A	0.5 V

4.5 DC-DC converter inductor

The LNBH29 operates with a 10 µH or 6.8 µH inductor for the entire range of supply voltage and load current (L1 in *Figure 8* and *Figure 9*). The inductor saturation current rating (where inductance is approximately 70% of zero current inductance) must be greater than the switch peak current (I_{peak}) calculated at:

- maximum load (IOUTmax.)
- minimum input voltage (VINmin.)
- maximum DC-DC output voltage (VUPmax. = VOUTmax. + 1 V)

In this condition the switch peak current is calculated using the formula:

Equation 2:

$$Ipeak = \frac{VUPmax. \cdot IOUTmax.}{Eff \cdot VINmin.} + \frac{VINmin.}{2LF}\left(1 - \frac{VIN\,min.}{VUPmax.}\right)$$

where:

Eff: is the efficiency of the DC-DC converter (93% typ. at the highest load)

L: is the inductance (10 µH or 6.8 µH typ.)

F: is the PWM frequency (440 kHz typ.)

Here below an example by using 10 µH coil.

The application condition as follows:

VOUTmax. = 18.817 V (supposing V_{SEL1} = V_{SEL2} = V_{SEL3} = 1) VINmin. = 11 V VUPmax. = VOUTmax. +V_{DROP} = 18.817 V+1 V = 19.817 V IOUTmax. = 500 mA Eff = 90%

By using equation 2 , I_{peak} is:

Equation 3:

$$Ipeak = \frac{19.817 \cdot 0.5}{9 \cdot 110} + \frac{11}{2 \cdot 10 \cdot 10^{-6} \cdot 440 \cdot 10^{3}} \left(1 - \frac{11}{19817}\right) = 1.55\,A$$

Table 4: Recommended inductors

Supplier	Order code	I_{SAT}(A)	DRC(mΩ)	Mounting type
Coilcraft	LPS6235-103MLB	2.3	100	SMT
TDK	SLF6045T-100M1R6	1.6	39	
Coilcraft	LPS6235-682MLB	2.6	75	
TDK	SLF6045T-6R8N2R0	2	33	

Several inductors suitable for the LNBH29 are listed in the above table, although there are many other manufacturers and devices that can be used. Consult each manufacturer for more detailed information since many different shapes and sizes are available. Ferrite core inductors should be used to obtain the best efficiency. Choose an inductor that can handle at least the I_{peak} current without saturating, and ensure that the inductor has a low DCR (copper wire resistance) to minimize power losses and, consequently, to maximize total efficiency.

4.6 Output current limit selection

The linear regulator current limit threshold can be set through an external resistor (RSEL) connected to ISEL pin. The resistor value defines the output current limit using the below equation:.

Equation 4 :

$$I_{max.}\ typ.\ (A) = \frac{13915}{RSEL(k\Omega)^{1.111}}$$

Where RSEL is the resistor connected between the ISEL pin and GND. The highest selectable current limit threshold is 0.750 A (typ.) with RSEL = 16.2 kΩ.

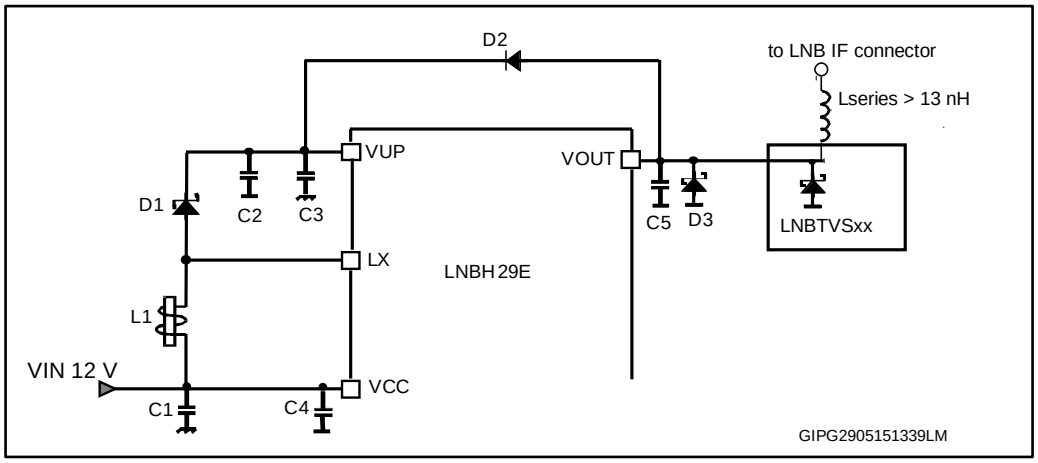
4.7 Undervoltage diode protection

During a short-circuit removal on the LNB output, negative voltage spikes may occur on the VOUT pin. To prevent reliability problems, a low-cost Schottky diode is used between this pin and GND.

4.8 TVS diode

The LNBH29 device is directly connected to the antenna cable in a set-top box. Atmospheric phenomenon can cause high voltage discharges on the antenna cable causing damage to the attached devices. Surge pulses occur due to direct or indirect lightning strikes to an external (outdoor) circuit. This leads to currents or electromagnetic fields causing high voltage or current transients. The LNBH29 device doesn't withstand such high energy discharges, so transient voltage suppressor (TVS) devices are used to protect the LNBH29 and other devices electrically connected to the antenna cable.

Figure 11: Recommended TVS diode connection



The LNBTVS, developed by STMicroelectronics, is a dedicated lightning and electrical overstress surge protection for LNB voltage regulators. This protection complies with the stringent IEC61000-4-5 standard with surges up to 500 A with a whole range of products for a cost/performance optimization.

The correct choice of the TVS diode must be taken into account according to the maximum peak power dissipation that the diode supports.

Table 5: Recommended LNBTVS

Supplier	Order code	$VBR_{typ.}$ (V)	Ppp (W) 10/100 µs
STMicroelectronics	LNBTVS4-220	23.1	1800
	LNBTVS4-221	23.1	2000
	LNBTVS4-222S	23.1	2000
	LNBTVS6-221S	21.3	3000

Select the TVS diode, which is able to support the Ppp(W) whose value is indicated in *Table 5*.

5 Layout guidelines

Due to high current levels and fast switching waveforms, which radiate noise, a proper PC board layout and a star ground configuration to protect sensitive analog ground are very important. Besides, lead lengths should be minimized to reduce stray capacitances, trace resistance, and radiated noise. Ground noise could be minimized by connecting GND, the input bypass capacitor ground lead, and the output filter capacitor ground lead to a single point (star ground configuration). Input bypass capacitors (C1 and C4) should be placed as close as possible to VCC and GND and the DC-DC output capacitors (C2 and C3) as close as possible to VUP. Excessive noise on the VCC input may falsely trigger the undervoltage circuitry, resetting the I^2C internal registers. If this occurs, the registers are set to zero and the LNBH29 is in shutdown mode.

5.1 PCB layout

Any switch mode power supply requires a good design of the PCB (printed circuit board) layout in order to achieve the top of performance in terms of system functionality. Component placing, GND trace routing and their widths are usually the major issues. Basic rules, commonly used for DC-DC converters for a good PCB layout, should be followed. All traces, carrying current, should be drawn on the PCB as short and thick as possible. This should minimize resistive and inductive parasitic effects, gaining system efficiency.

Figure 12: STEVAL-CBL015V1 top layer

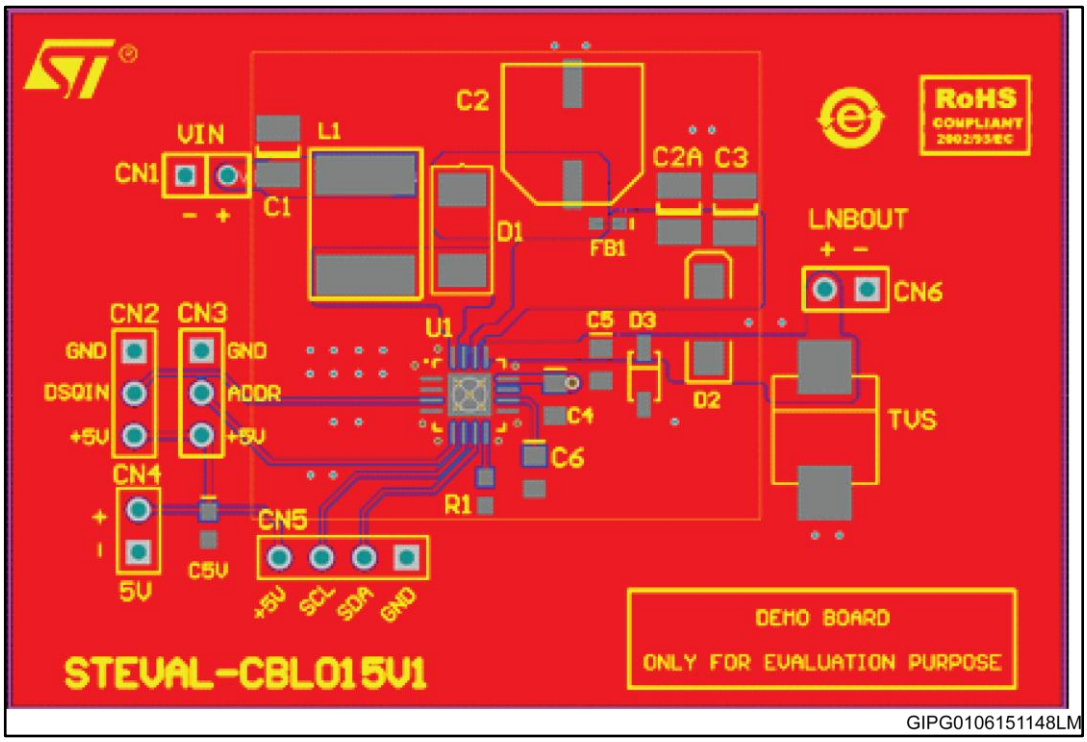


Figure 13: STEVAL-CBL016V1 top layer

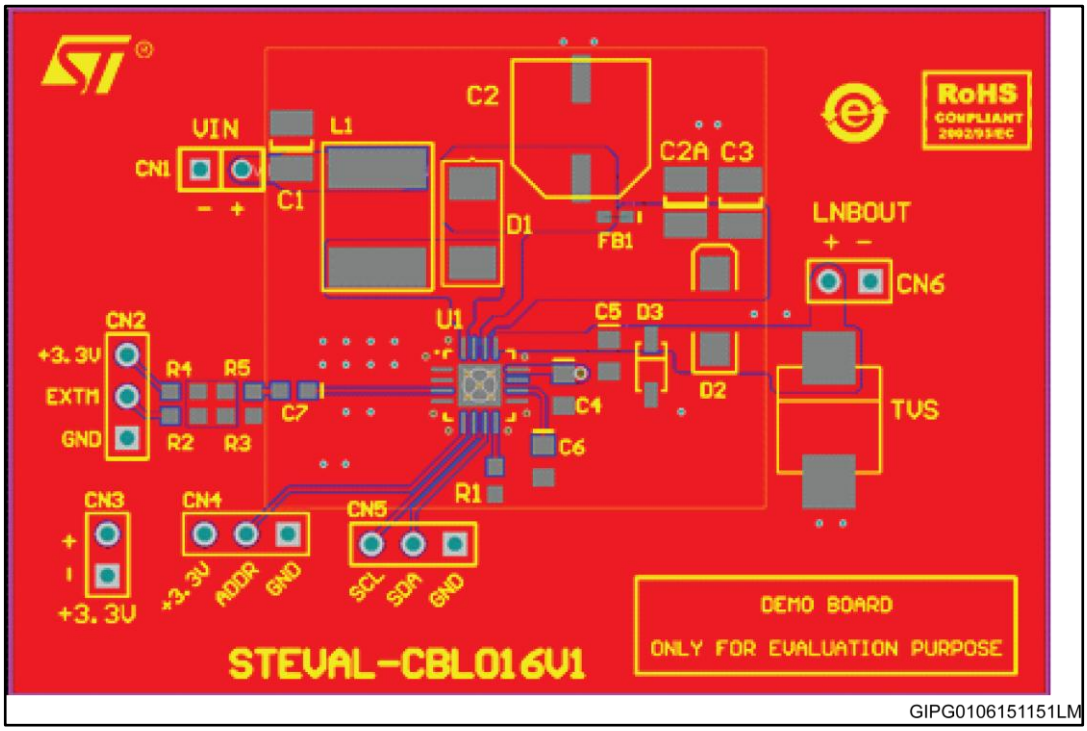


Figure 14: STEVAL-CBL015V1 bottom layer

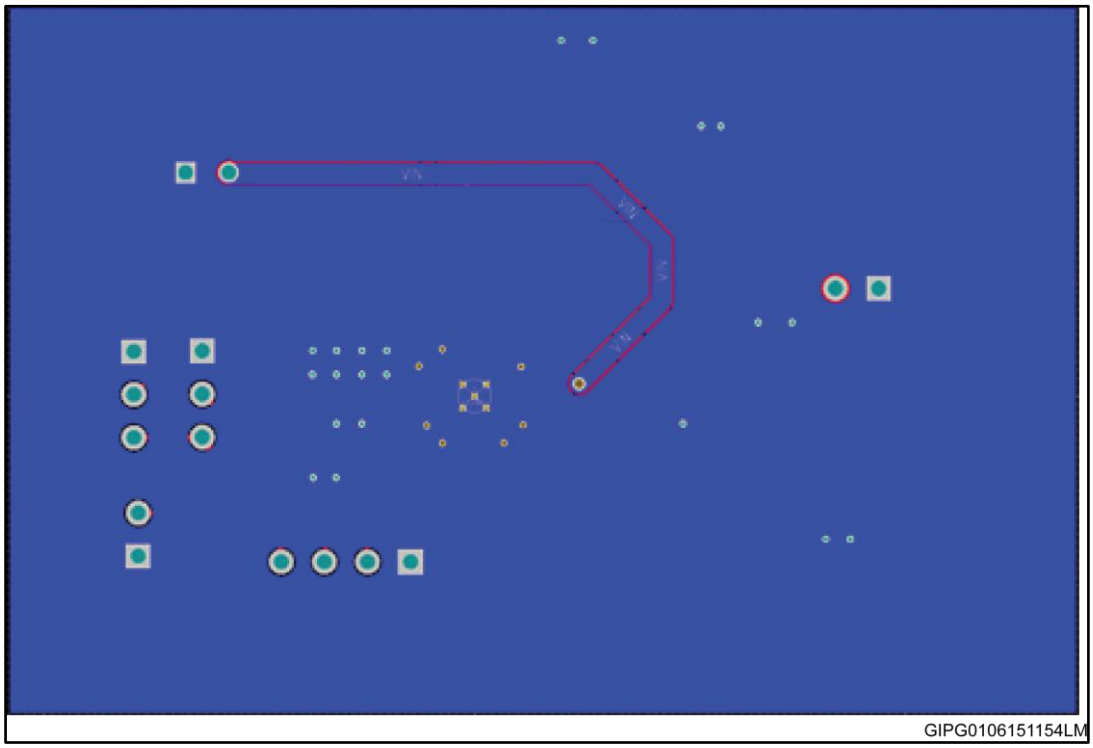


Figure 15: STEVAL-CBL016V1 bottom layer

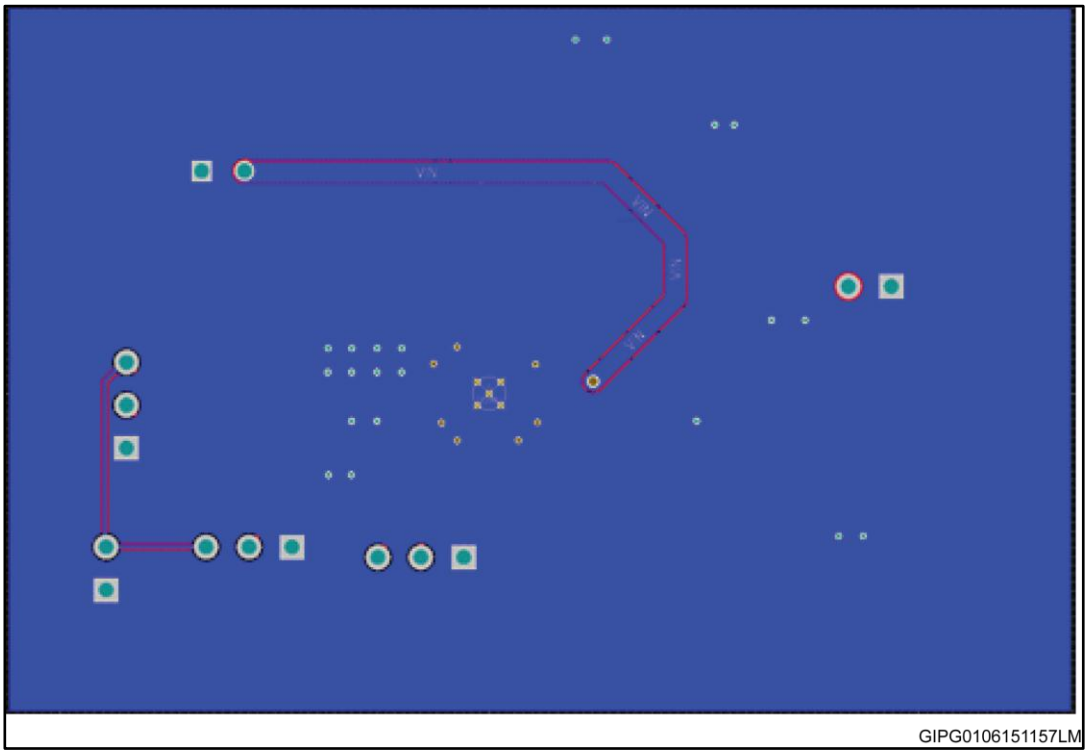


Figure 16: STEVAL-CBL015V1 component layout

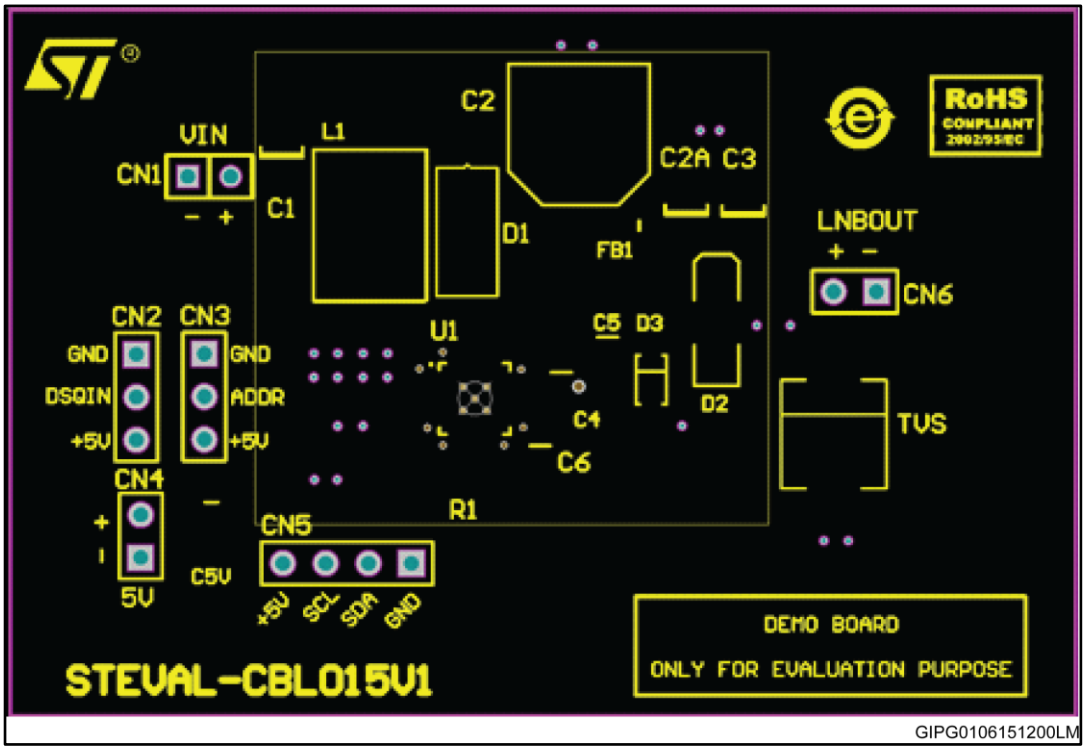
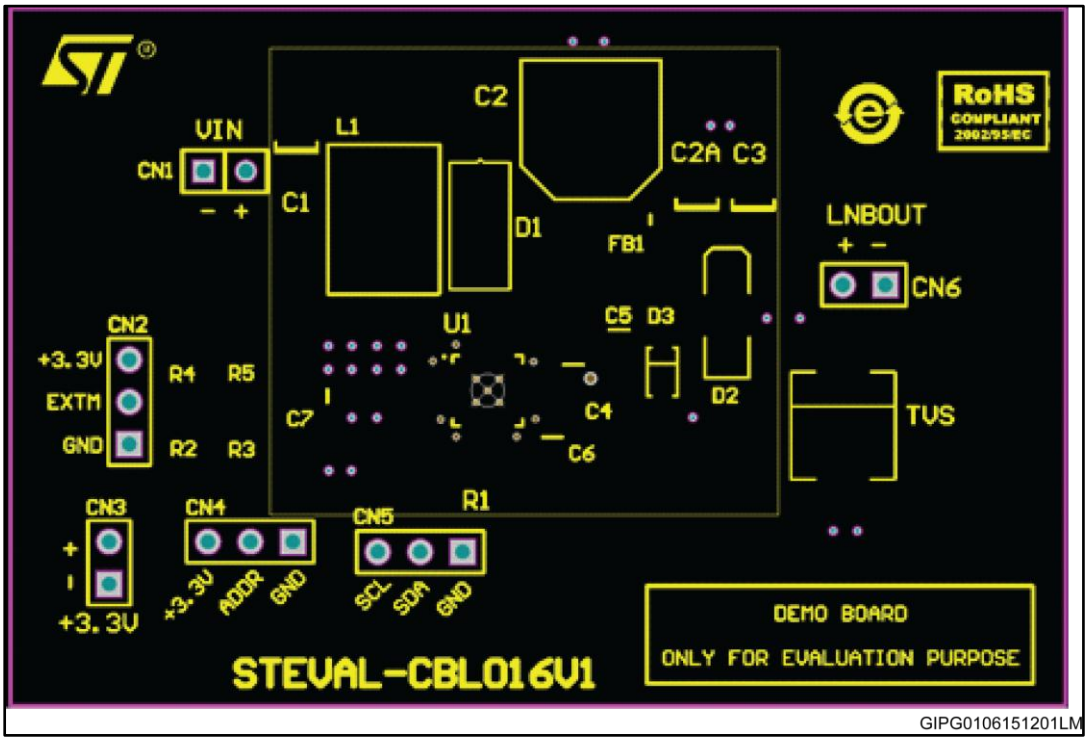


Figure 17: STEVAL-CBL016V1 component layout



5.2 Start-up procedure

To test the board, you need:

- PC with USB port
- USB I^2C BUS interface
- LNBH29 testing software
- Dual output power supply
- Pulse generator
- Voltmeter
- Oscilloscope

Step 1: the LNBH29 testing software

Step 2: plug the I^2C connector in CN5

Step 3: supply the evaluation board with CN1

Step 4: test the evaluation board (see *Section 5.1: "PCB layout"*)

Figure 18: PCB connector

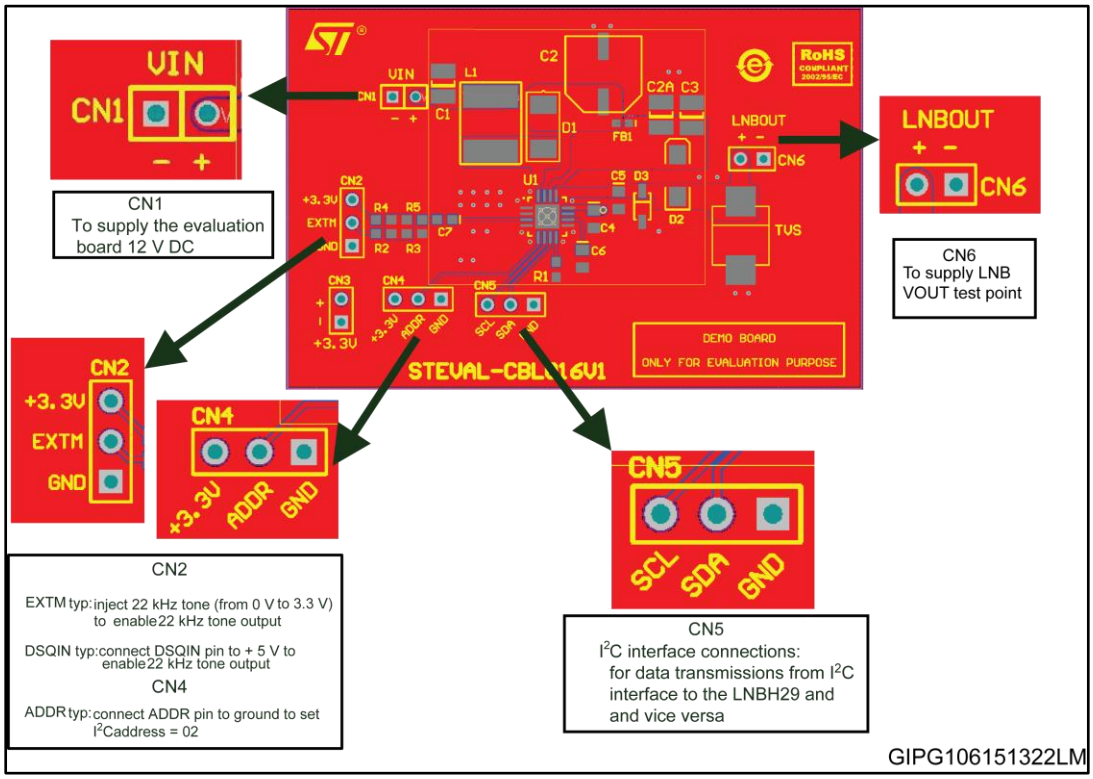
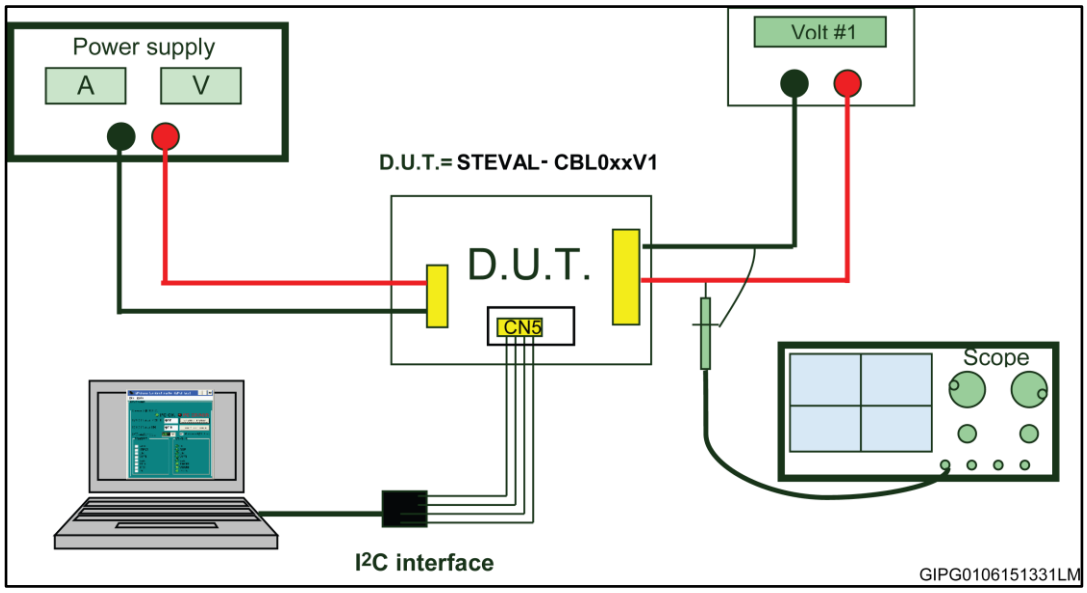


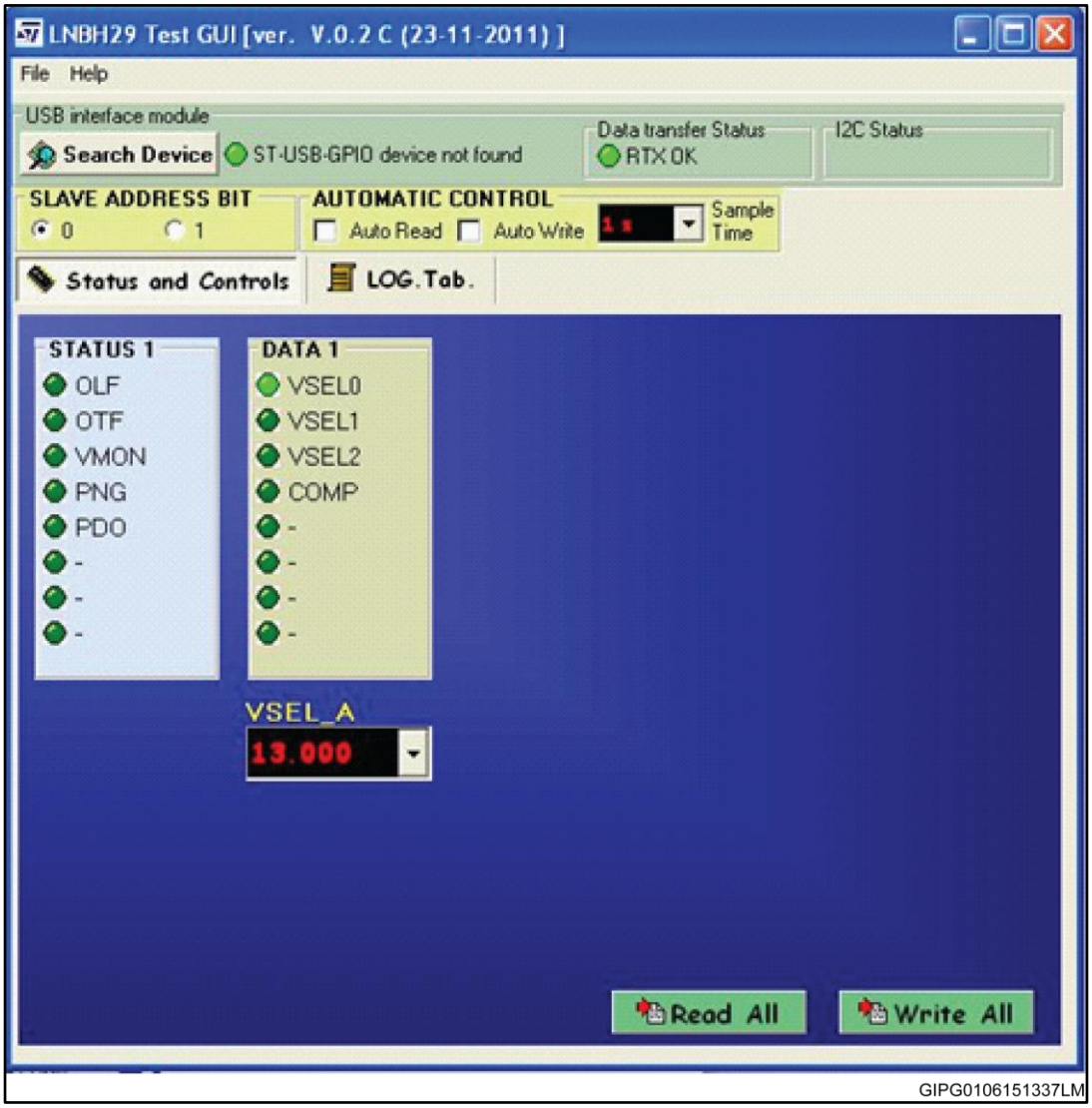
Figure 19: STEVAL-CBL0xxV1 bench test



5.3 Testing software

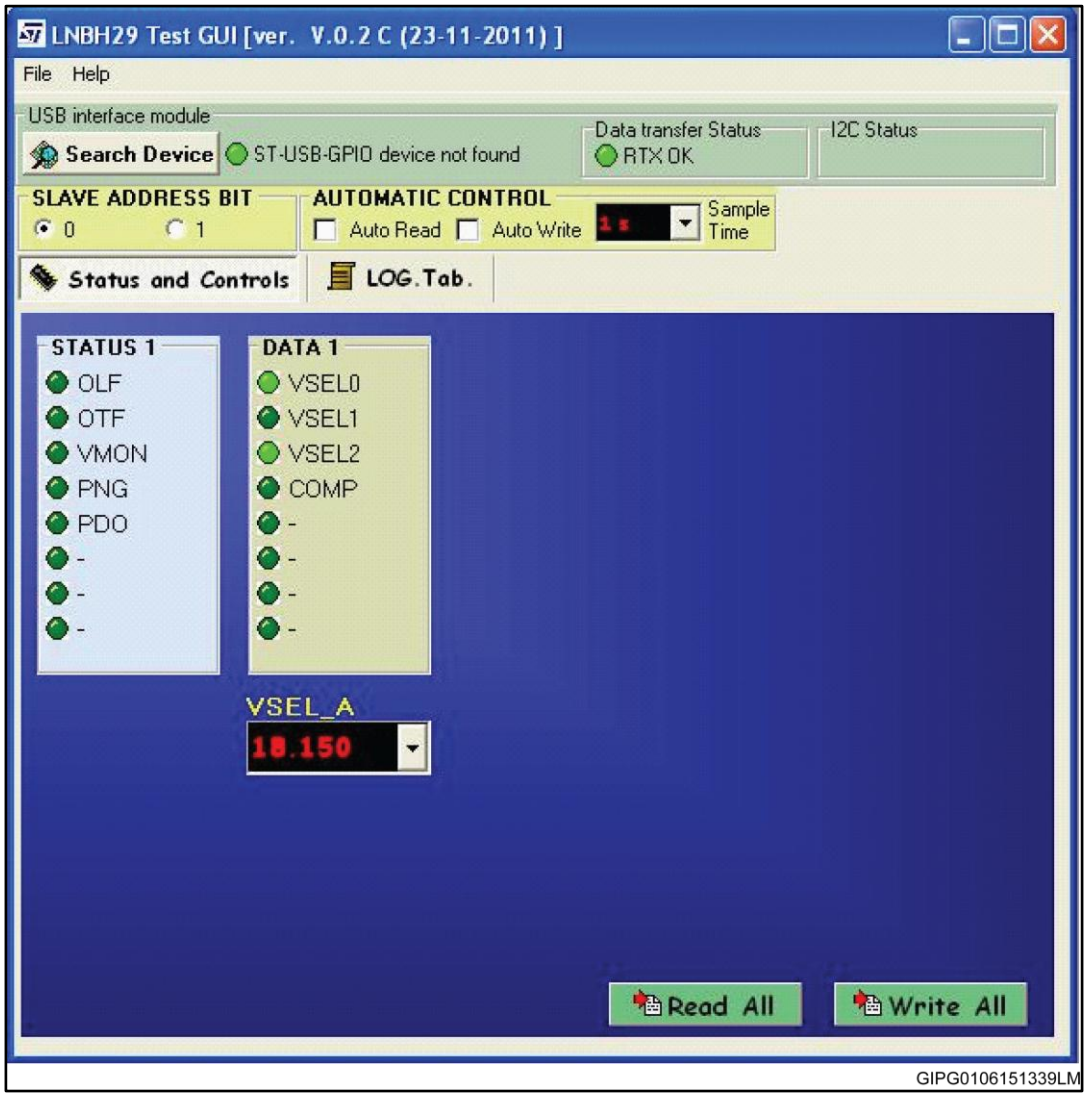
To power on the IC, select the voltage output and click “Write All”, if the device accepts the command string, “ACK Fail” can be read in I^2C status box, in the following screen shot:

Figure 20: VSEL0 = 1 (CN6 output voltage 13 V)



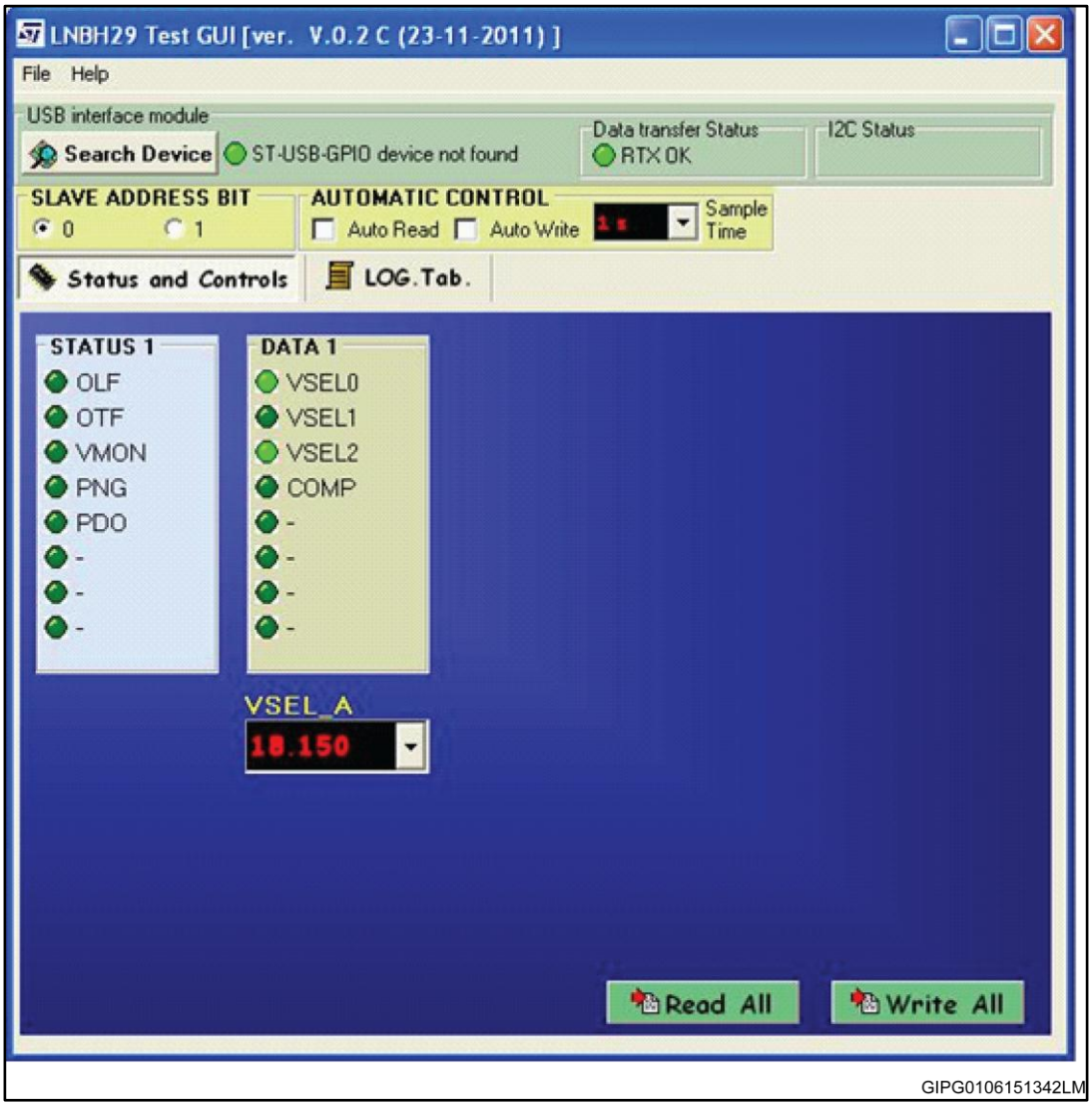
- Ignore VMON green light
- On the CN5 testing point: output voltage measured by voltmeter
- Output voltage = 12.54 V to 13.45 V (typ.13 V)

Figure 21: VSEL0 = VSEL2 = 1 (CN6 output voltage 18.15 V)



- On CN6 testing point: output voltage measured by voltmeter
- Output voltage = 17.51 V to 18.78 V (typ.18.15 V)

Figure 22: SEL0 = VSEL2 = 1 (22 kHz signal)



For the LNBH29E version: the input signal from 0 V to 3.3 V is injected into EXTM pin (CN2 connector).

For the LNBH29, DSQIN pin (CN2 connector) must be set high (+5 V).

CN6 output voltage is 18.15 V + 22 kHz tone.

- On CN6 test point: tone amplitude measured by the oscilloscope
- Tone amplitude = 0.55 V to 0.8 V (typ. 0.675 V)

6 Revision history

Table 6: Document revision history

Date	Revision	Changes
21-Jul-2015	1	Initial release.
07-Sep-2015	2	Updated the STEVAL-CBL016V1, LNBH29E version, evaluation board schematic.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

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