SLLIMM™ 2nd series small low-loss intelligent molded module

Introduction

The SLLIMM™ (small low-loss intelligent molded module) 2nd series is ST's new family of compact, high efficiency, dual-in-line intelligent power modules, with optional extra features. This family is designed with a new internal configuration with only two drivers: one high-side driver and one low-side driver.

This new approach allows a more compact package and, thanks to the new features provided by low-side driver, advanced protection functions. In addition, this new product offers the best compromise between conduction and switching energy with outstanding robustness and EMI behavior, rendering it ideal for improving efficiency for compressors, pumps, fans and low power motors working up to 20 kHz in hard-switching circuitries.

Two IPM package versions are available: the full molded and the DBC (Direct Bonded Copper); both compatible with each other.

This new series both complements and surpasses the original SLLIMM series in terms of features, package types and flexibility.

The SLLIMM™ 2nd series features:

- two different package technologies: DBC for improved thermal behavior, and fully molded for a cost effective solution (both compatible with each other)
- improved thermal performance (up to 20% thermal resistance reduction for DBC version)
- trench field stop (TFS) IGBT technology for efficiency improvement
- higher max. junction temperature of power chips (175 °C)
- newly developed high-side and low-side driver pin-out arrangement for easier PCB routing
- expanded line-up to 35 A
- two different temperature monitoring options: NTC thermistor and thermal sensor
- two fault events with signal output: overcurrent and undervoltage lockout

The SLLIMM 2nd series product family combines optimized silicon chips, integrated into three main inverter blocks:

- power stage
  - six short-circuit rugged IGBTs in TFS technology and six freewheeling diodes
- driving network
  - two differents low and high voltage gate drivers
  - three bootstrap diodes
- protection and optional features
  - comparators for fault protection against overcurrent and short-circuit
  - two temperature monitoring options: output thermal sensor (TSO) embedded on the low-side gate driver and NTC thermistor (optional)
  - two fault event types with fault signal output: overcurrent and undervoltage
  - smart shutdown function and undervoltage lockout on V_{CC} and V_{boot} voltages

The aim of this application note is to provide a detailed description of the new products family, providing the guidelines to the motor drive designers for an efficient, reliable, and fast design when using the 2nd series of ST SLLIMM family.

1 Comparison of SLLIMM 1st and 2nd series

The principal differences between the SLLIMM 2nd series and the previous generation (SLLIMM 1st and 1.i series) are listed below.

Table 1. SLLIMM 1st and 2nd series differences

Feature	SLLIMM 1st series: STGIPSxxK60yy STGIPLxxK60yy	SLLIMM 1.i series: STGIPSxxC60yy STGIPLxxC60yy	SLLIMM 2nd series: STGIFxxCH60yy STGIBxxCH60yy STGIBxxM60yy
IGBT technology	Planar	Trench field stop	Trench field stop
Current capability IC (@25°C)	10 to 20 A	10 to 30 A	8 to 35 A
Max T_j power chips	150°C	150°C	175°C
Package	SDIP-25L (DBC) SDIP-38L (DBC)	SDIP-25L (DBC) SDIP-38L (DBC)	SDIP2F-26L (full molded) SDIP2B-26L (DBC)
Number of leads	25/38	25/38	26
Control ICs	3 x half bridge IC	3 x half bridge IC	1 x triple high-side IC 1 x triple low-side IC
Fault event monitoring	Overcurrent	Overcurrent	Overcurrent. Undervoltage (with differing fault signal output timing)
Temperature monitoring options	NTC (several PNs)	NTC (several PNs)	Temperature sensor integrated TSO (all PNs). NTC (STGIxyyCH60Tz)
Interlocking function	Yes	Yes	No
Lead options	Short leads	Short leads	Short leads and emitter forward. Long leads
V_{ISO}	2500 Vrms	2500 Vrms	1500 Vrms

Please refer to the relevant datasheets for more detailed device specifications and recommended operation conditions.

1.1 Product synopsis

The SLLIMM 2nd series family has been designed to satisfy the requirements of a wide variety of final applications in the 300 W-3.0 kW range, including:

- washing machines
- dish washers
- refrigerators
- air conditioning compressor drives
- sewing machines
- pumps
- tools

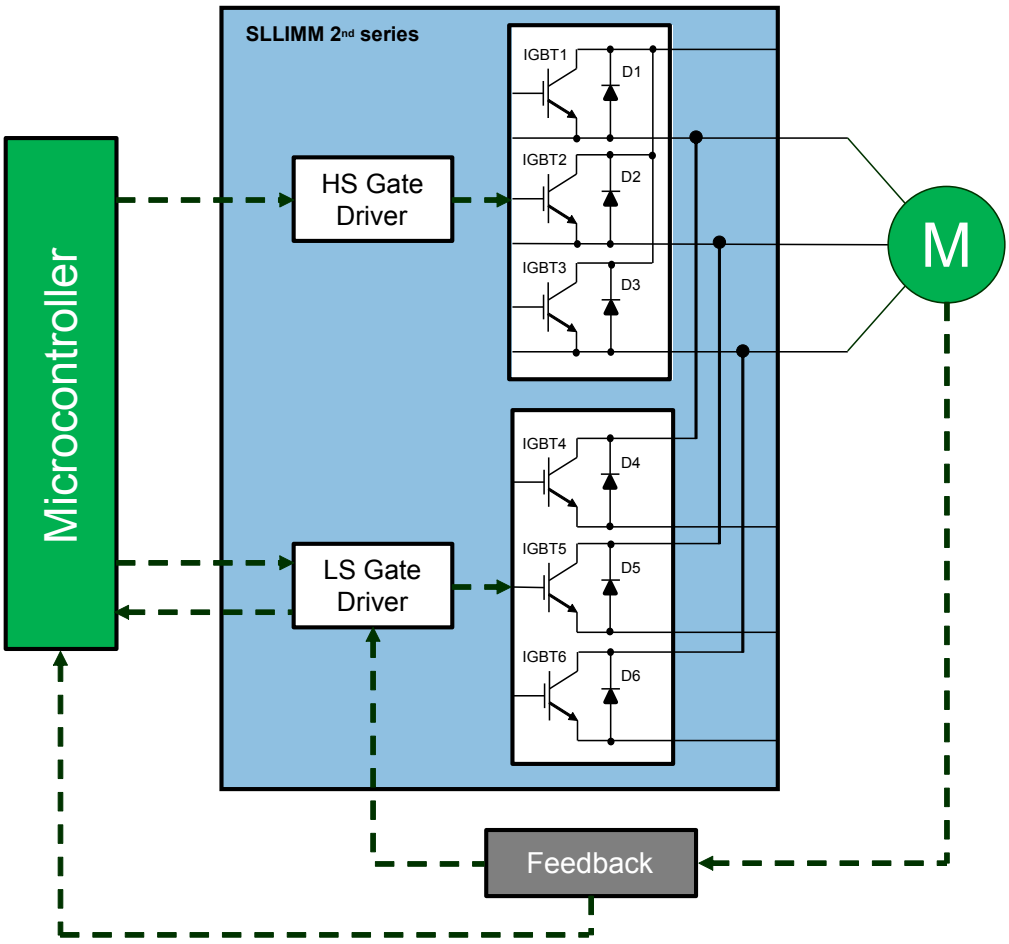
- low power industrial applications

The main features and integrated functions can be summarized as follows:

- 600 V, 8 - 35 A ratings
- 3-phase IGBT inverter bridge including:
  - six low-loss and short-circuit protected IGBTs
  - six low forward voltage drop and soft recovery freewheeling diodes
- two control ICs for gate driving and protection including:
  - three integrated bootstrap diodes
  - smart shutdown function
  - comparator for fault protection against overcurrent and short-circuit (on low-side gate driver IC)
  - undervoltage lockout on V_{CC} (on high and low-side gate driver ICs) and V_{boot} (on high-side gate driver ICs)
  - two fault signal outputs (on low-side gate driver IC): overcurrent protection and V_{CC} undervoltage (on low-side gate driver IC only)
- output thermal sensor (TSO) embedded on the low-side gate driver IC
- NTC thermistor for temperature monitor on the power stage (optional)
- open emitter configuration for individual phase current sensing
- DBC fully isolated package for enhanced thermal behavior and a cost-effective fully isolated full molded package
- isolation voltage rating of 1500 V_{RMS}/min

The figure below shows the block diagram of an inverter solution including a SLLIMM.

Figure 1. **SLLIMM block diagram**



1.2 Product line-up and nomenclature

The table below shows the products in production. Additional modules are being developed to extend the current range.

Table 2. **Product line-up**

Package	Part number	I_C (A) T_C @ 25°C [T_C @ 80°C]	Voltage (V)	V_{ISO} (Vrms)	Max T_j (°C)	Typical (W)
SDIP2F-26L	STGIF5CH60xy-z	8 [5]	600	1500	175	750
	STGIF7CH60xy-z	10 [7]	600	1500	175	800
	STGIF10CH60xy-z	15 [10]	600	1500	175	900
SDIP2B-26L	STGIB8CH60xy-z	12 [8]	600	1500	175	1500
	STGIB10CH60xy-z	15 [10]	600	1500	175	1500
	STGIB15CH60xy-z	20 [15]	600	1500	175	2000
	STGIB20M60xy-z	25 [20]	600	1500	175	2500
	STGIB30M60xy-z	35 [30]	600	1500	175	3000

Table 3. Synoptic table for full molded package option

Feature	STGIF5CH60xy-z	STGIF7CH60xy-z	STGIF10CH60xy-z
Voltage (V)	600	600	600
Continuous collector current each IGBT (A) (T_C = 25°C)	8	10	15
Continuous collector current each IGBT (A) (T_C = 80°C)	5	7	10
$R_{th(j-c)}$ max single IGBT (°C/W)	5	4.8	4.6
Package type	SDIP2F-26L	SDIP2F-26L	SDIP2F-26L
Number of pins	26 (NTC on board)	26 (NTC on board)	26 (NTC on board)
	25	25	25
Package size (mm) X, Y, Z	38.0x24.0x3.5	38.0x24.0x3.5	38.0x24.0x3.5
Integrated bootstrap diode	Yes	Yes	Yes
SD function	Yes	Yes	Yes
Comparator for fault protection	Yes (1 pin)	Yes (1 pin)	Yes (1 pin)
Smart shutdown function	Yes	Yes	Yes
Undervoltage lockout	Yes	Yes	Yes
Open emitter configuration	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)
3.3/5 V input interface compatibility	Yes	Yes	Yes
High and low-side IGBT input signal	Active high	Active high	Active high

Table 4. Synoptic table for DBC package option

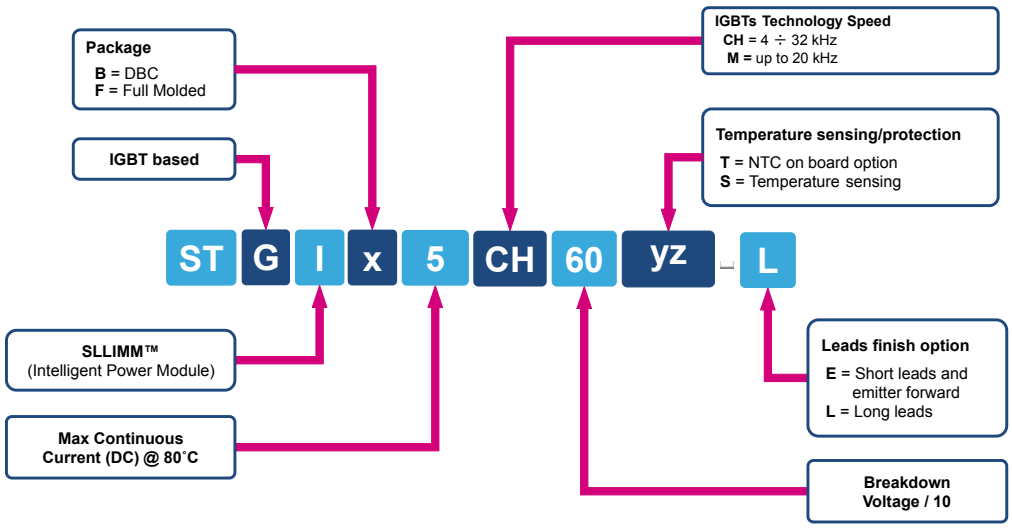
Feature	STGIB8CH60xy-z	STGIB10CH60xy-z	STGIB15CH60xy-z	STGIB20M60xy-z	STGIB30M60xy-z
Voltage (V)	600	600	600	600	600
Continuous collector current each IGBT (A) (T_C = 25°C)	12	15	20	25	35
Continuous collector current each IGBT (A) (T_C = 80°C)	8	10	15	20	30
$R_{th(j-c)}$ max single IGBT (°C/W)	3	2.26	1.85	1.4	1.2
Package type	SDIP2B-26L	SDIP2B-26L	SDIP2B-26L	SDIP2B-26L	SDIP2B-26L
Number of pins	26 (NTC on board)	26 (NTC on board)	26 (NTC on board)	26 (NTC on board)	26 (NTC on board)
	25	25	25	25	25
Package size (mm) X, Y, Z	38.0x24.0x3.5	38.0x24.0x3.5	38.0x24.0x3.5	38.0x24.0x3.5	38.0x24.0x3.5
Integrated bootstrap diode	Yes	Yes	Yes	Yes	yes
SD function	Yes	Yes	Yes	Yes	yes

Feature	STGIB8CH60xy-z	STGIB10CH60xy-z	STGIB15CH60xy-z	STGIB20M60xy-z	STGIB30M60xy-z
Comparator for fault protection	Yes (1 pin)	Yes (1 pin)	Yes (1 pin)	Yes (1 pin)	yes (1 pin)
Smart shutdown function	Yes	Yes	Yes	Yes	yes
Undervoltage lockout	yes	yes	yes	yes	yes
Open emitter configuration	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)	Yes (3 pins)	yes (3 pins)
3.3/5 V input interface compatibility	Yes	Yes	Yes	Yes	yes
High and low-side IGBT input signal	active high	active high	active high	active high	active high

Please refer to www.st.com for the complete product portfolio.

The figure below describes the 2nd series product family nomenclature.

Figure 2. SLLIMM 2nd series nomenclature



1.3 Internal circuit

SLLIMM 2nd series offers two internal circuit and number of leads options, based on the presence of the NTC thermistor (STGIxyyCH60Tz and STGIByyM60Tz with NTC on board).

Figure 3. **Internal circuit for SDIP2F-26L and SDIP2B-26L (without NTC)**

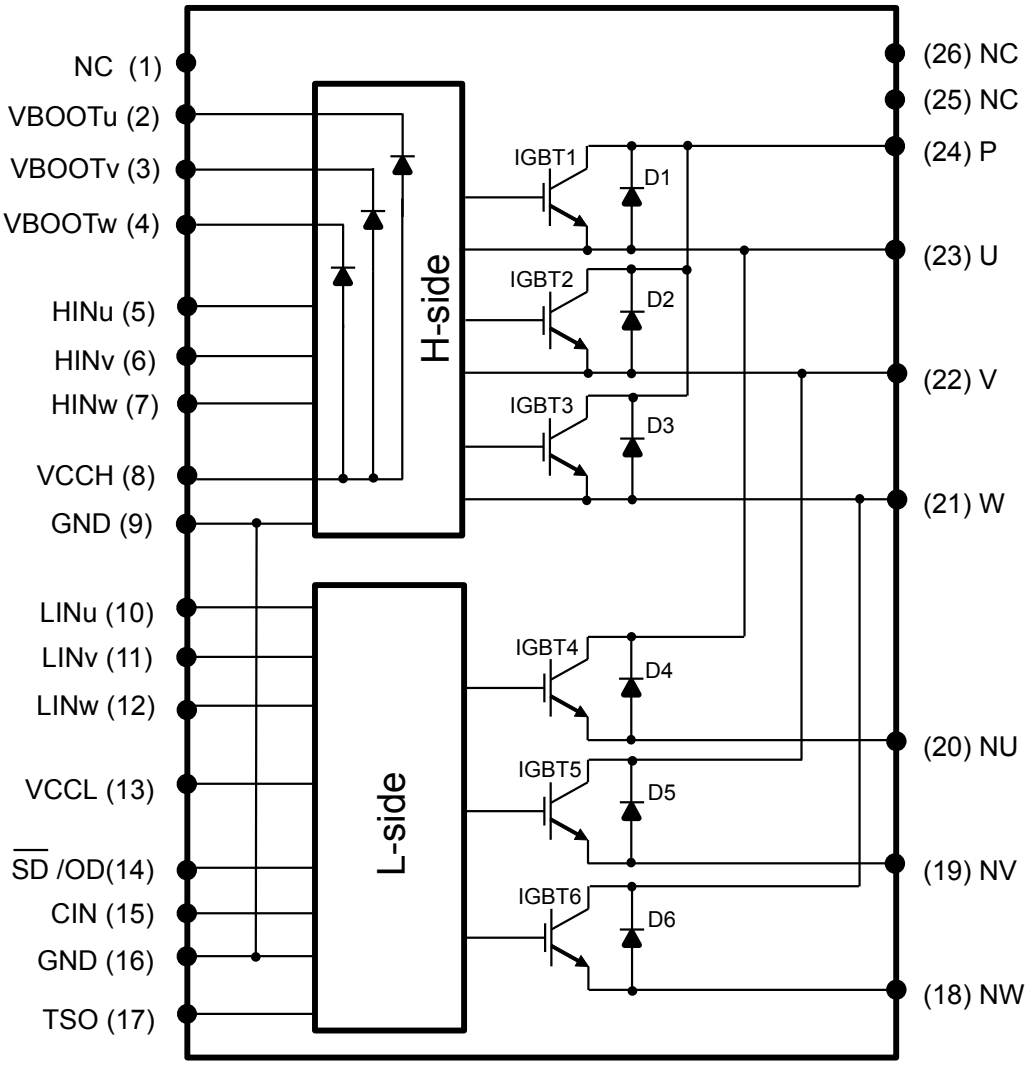
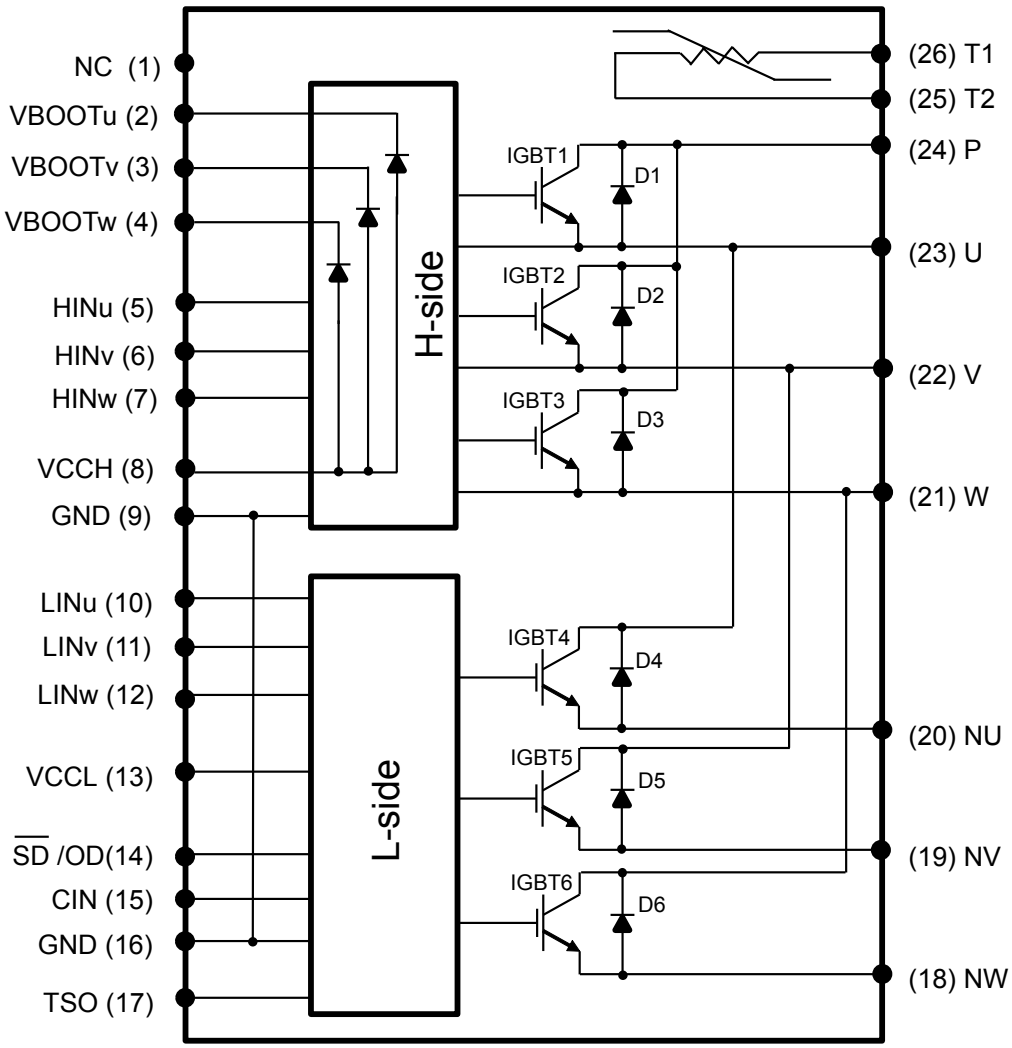


Figure 4. **Internal circuit for SDIP2F-26L and SDIP2B-26L (with NTC)**



1.4 Absolute maximum ratings

The absolute maximum ratings represent the extreme capabilities of the device and can be normally used to set the worst case design limit conditions.

Absolute maximum values are based on specific test parameters such as temperature, frequency and voltage. Device performance can change according to the applied condition.

The SLLIMM specifications are described below with the STGIF5CH60xy-z datasheet example. Please refer to the relevant product datasheets for detailed information regarding the other device types.

Table 5. **Inverter part of STGIF5CH60xy-z**

Symbol	Parameter	Value	Unit
V_{PN}	supply voltage applied between P - NU, NV, NW	450	V
$V_{PN(surge)}$	supply voltage surge between P - NU, NV, NW	500	V
V_{CES}	collector-emitter voltage each IGBT	600	V

Symbol	Parameter	Value	Unit
$\pm I_C$	each IGBT continuous collector current at T_j = 25 °C	8	A
	each IGBT continuous collector current at T_j = 80 °C	5	A
$\pm I_{CP}$	peak collector current each IGBT (less than 1ms)	16	A
P_{TOT}	each IGBT total dissipation at T_C = 25 °C	30	W
t_{SCW}	short circuit withstand time, V_{CE}= 300 V, T_J= 125 °C, V_{CC}= V_{boot} = 15 V, V_{IN}= 0 to 5 V	5	µs

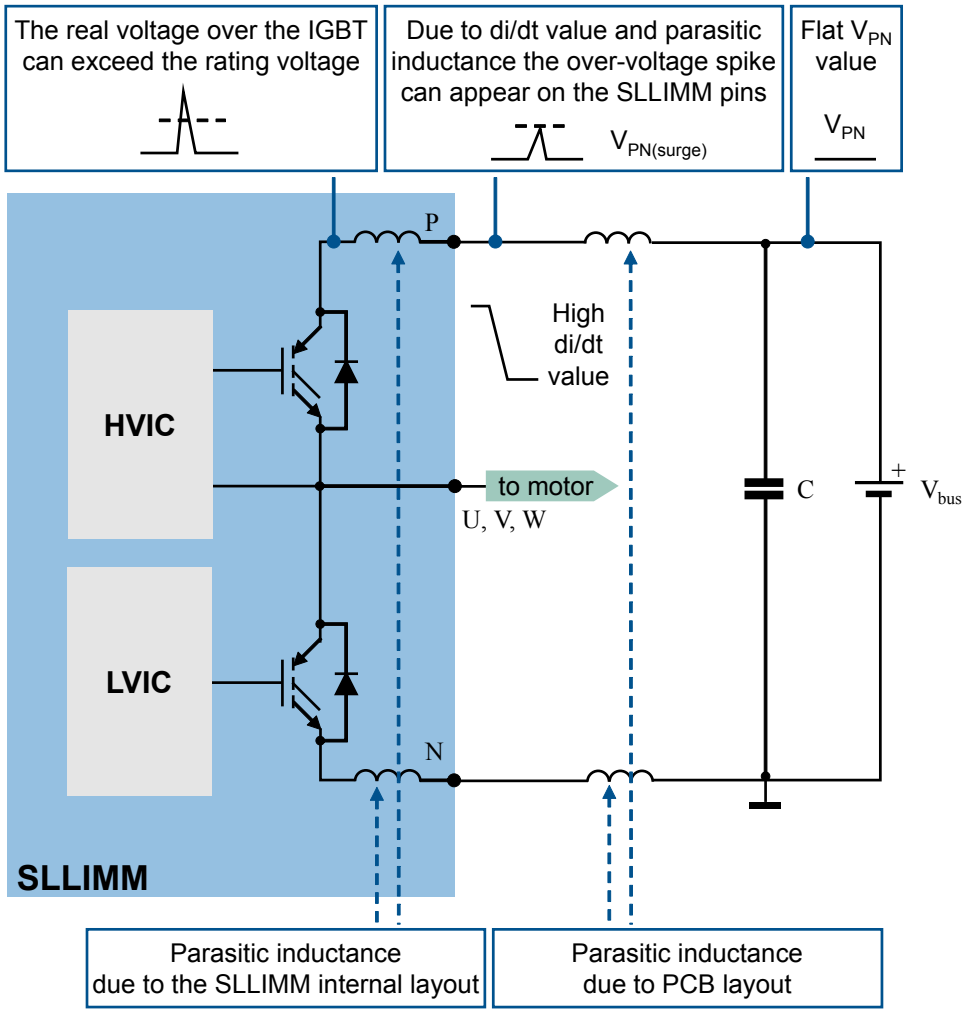
The power stage of SLLIMM is based on IGBTs (and freewheeling diodes) with a 600 V V_{CES} rating. Considering the SLLIMM internal stray inductance during the commutations, which can generate up to 100 V of surge voltage, the maximum surge voltage between P-N ($V_{PN(surge)}$) allowed is 500 V. At the same time, the maximum supply voltage (in steady-state) applied between P-N (V_{PN}) is limited to 450 V because of an additional 50 V surge voltage generated by the stray inductance between the SLLIMM and the DC-link capacitor.

$\pm I_c$ is the allowable DC current continuously flowing at the collector electrode of each IGBT (T_j = 25 °C and T_j = 80 °C).

t_{SCW} is the short-circuit, non repetitive withstand time.

The internal SLLIMM layout and board layout shown below are the two major components of parasitic inductance.

Figure 5. **Stray inductance components of output stage**



The IGBTs incorporated in the SLLIMM are tailored for motor control applications where short-circuit self-protection is one of the main module features. If the short-circuit conditions exceed the above specifications, the lifetime of the device is drastically shortened. We therefore strongly recommended not operating the SLLIMM under these conditions.

Table 6. **Control part of STGIF5CH60xy-z**

Symbol	Parameter	Min	Max	Unit
V_{CC}	supply voltage between V_{CCH}-GND, V_{CCL}-GND	-0.3	20	V
V_{BOOT}	bootstrap voltage	-0.3	619	V
V_{OUT}	output voltage between U, V, W and GND	V_{BOOT}- 21	V_{BOOT}+ 0.3	V
V_{CIN}	comparator input voltage	-0.3	20	V
V_{IN}	logic input voltage applied between HINx, LINx and GND	-0.3	15	V
$V_{\overline{SD/OD}}$	open-drain voltage	-0.3	7	V
$I_{\overline{SD/OD}}$	open-drain sink current	-	10	mA

Symbol	Parameter	Min	Max	Unit
V_{TSO}	temperature sensor output voltage	-0.3	5.5	V
I_{TSO}	temperature sensor output current	-	7	mA

V_{CC} represents the supply voltage of the control part for both high-side and low-side gate drivers. Local filtering is recommended to enhance the SLLIMM noise immunity. Generally, we suggest using one electrolytic capacitor (with a higher value and not negligible ESR) and a faster and smaller ceramic capacitor (in the order of hundreds of nF) to provide current.

Refer to the details in the table below to drive the SLLIMM properly.

Table 7. Supply voltage and operation behavior

V_{CC} voltage (typ. value)	Operating behavior
< 12 V	As the voltage is lower than the UVLO threshold, the control circuit is not fully turned on. Perfect functionality cannot be guaranteed.
12 V – 13.5 V	IGBTs can function, however conduction and switching losses increase due to low voltage gate signal.
13.5 V – 18 V	Recommended value (see relevant datasheets).
18 V – 20 V	IGBTs can function. Switching speed is faster and saturation current higher, increasing short-circuit broken risk and EMI issues.
> 20 V	Control circuit is destroyed. Absolute max. rating is 20V.

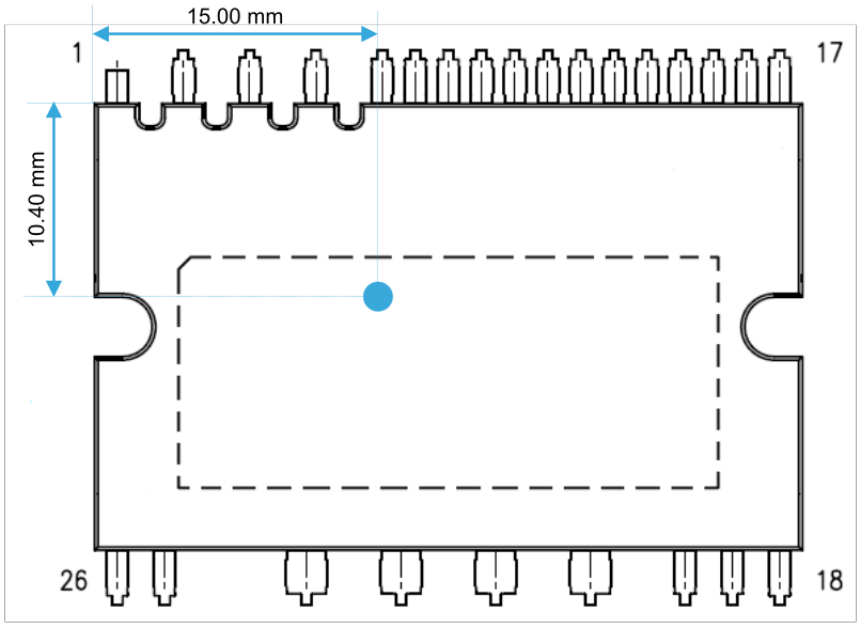
For further information, please refer to the relevant datasheet.

Table 8. Total STGIF5CH60xy-z system

Symbol	Parameter	Value	Unit
V_{ISO}	isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s)	1500	Vrms
T_j	power chip operating junction temperature	-40 to 175	°C
T_C	module case operation temperature	-40 to 125	°C

The figure below shows the case temperature measurement point for all package options, right above the power chip. To obtain accurate temperature information, mount a thermocouple on the heat sink surface at this specific location. For non-complementary switching schemes, the highest T_C point occur in a different position. In this case, the measurement location is over the point where the highest power chip temperature is generated.

Figure 6. T_C measurement point



1.5 SCSOA

Figure 7. SCSOA test circuit and Figure 8. SCSOA main data show the circuits for obtaining the SCSOA of SLLIMM 2nd series devices and the SCSOA main data, respectively.

Figure 7. **SCSOA test circuit**

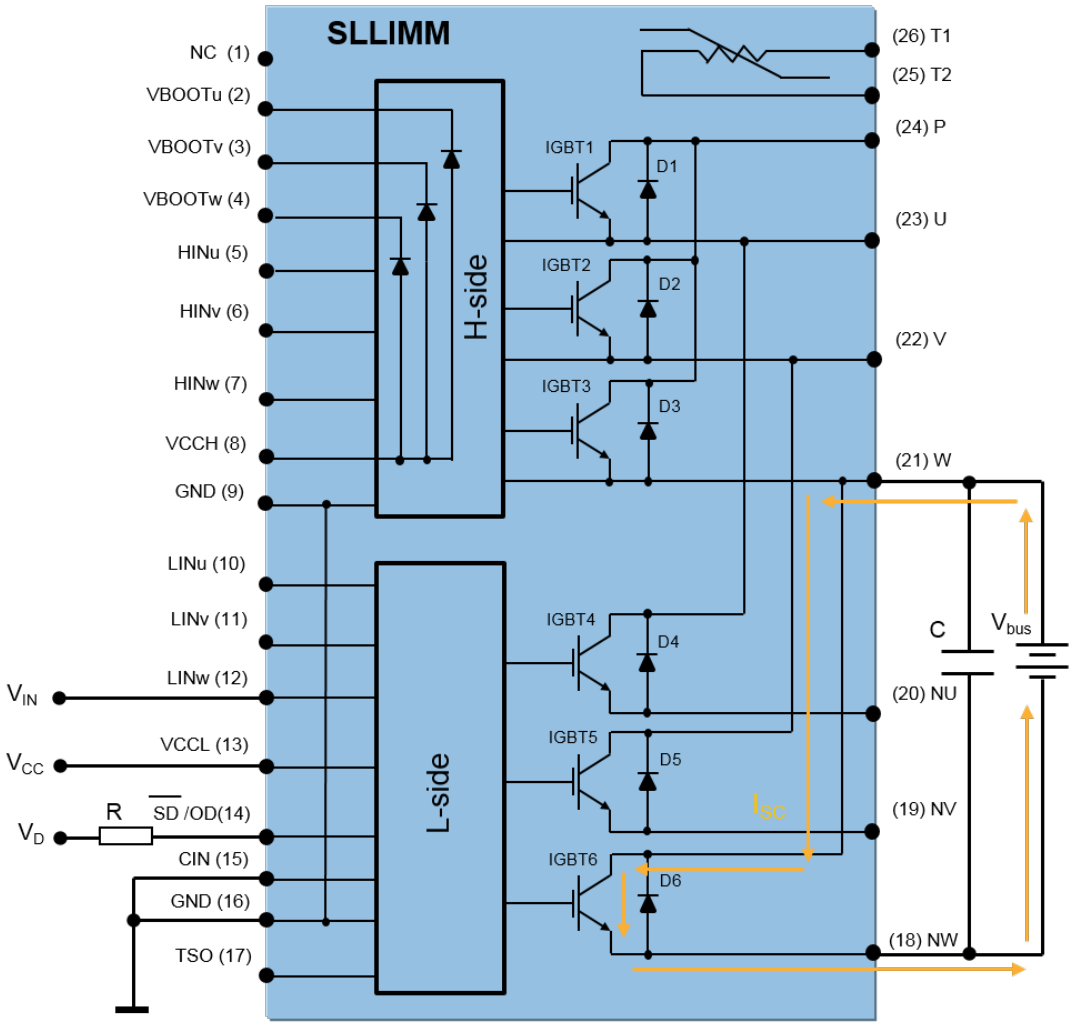
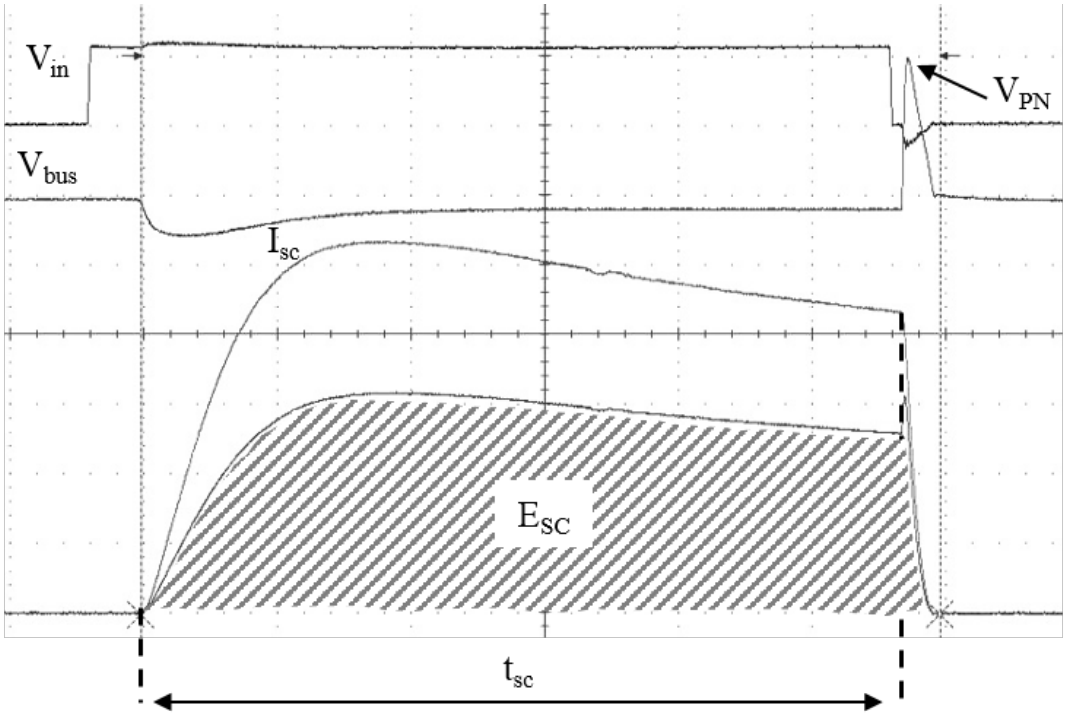


Figure 8. **SCSOA main data**



V_{PN} is the surge voltage generated at the end of the switching by the inductor wiring between the IPM and DC-Link capacitor.

E_{sc} is the total energy during the switch.

t_{sc} is the impulse width.

The following figures show the typical SCSOA performance curves of STGIF5CH60xy-z, STGIF7CH60xy-z, STGIFx10CH60xy-z, STGIB8CH60xy-z , STGIB15CH60xy-z, STGIB20M60xy-z and STGIB30M60xy-z devices.

The testing conditions for all the devices are: V_{bus} = 300 V, T_{case} = 125 °C, V_{IN} = 5 V, non-repetitive.

Figure 9. **Typical STGIF5CH60yy SCSOA curve**

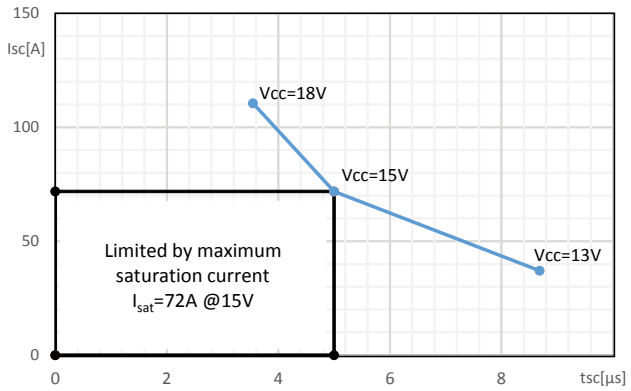


Figure 10. **Typical STGIF7CH60yy SCSOA curve**

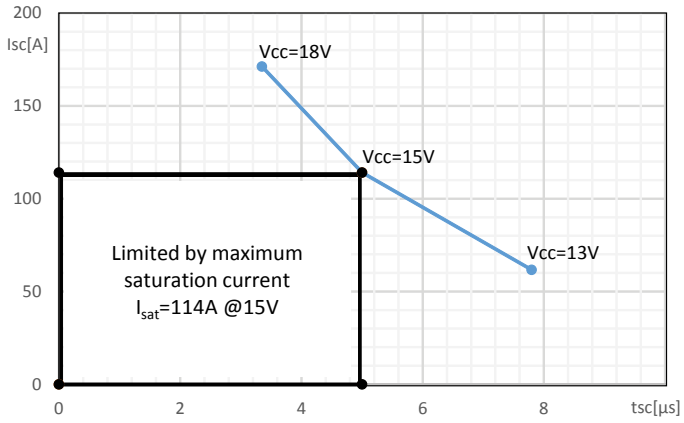


Figure 11. **Typical STGIx10CH60yy SCSOA curve**

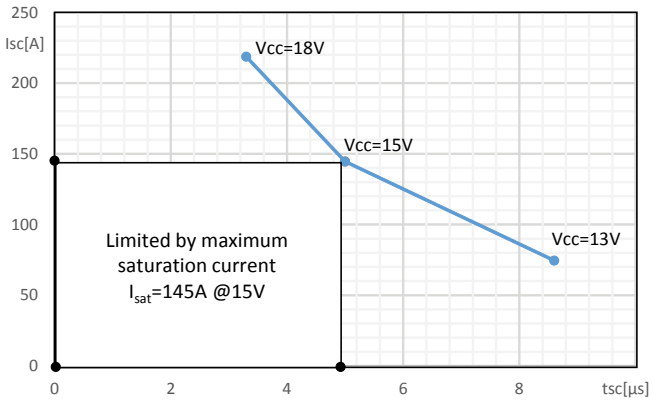


Figure 12. **Typical STGIB8CH60yy SCSOA curve**

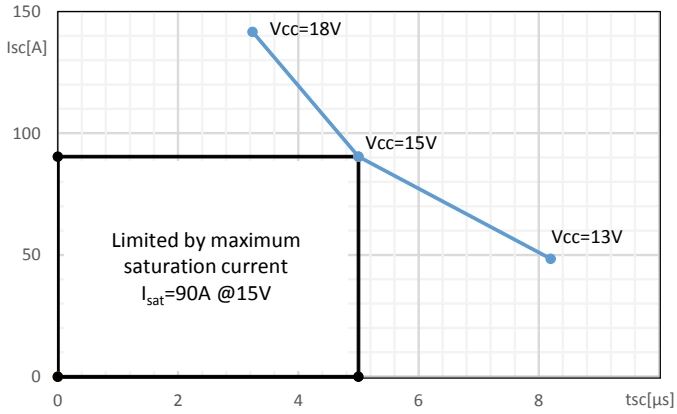


Figure 13. **Typical STGIB15CH60yy SCSOA curve**

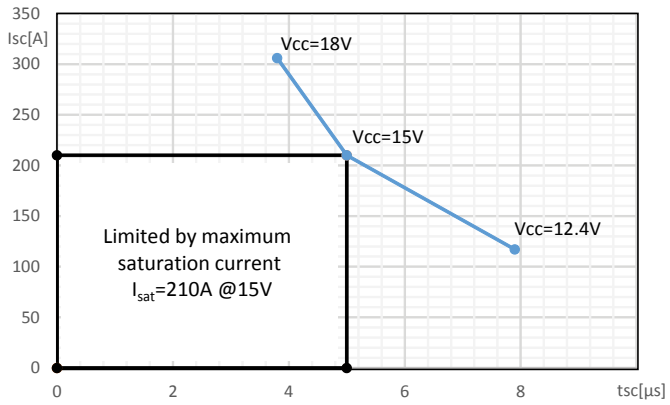


Figure 14. **Typical STGIB20M60yy SCSOA curve**

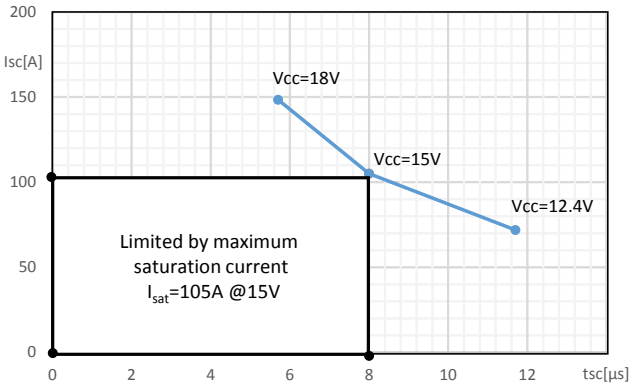
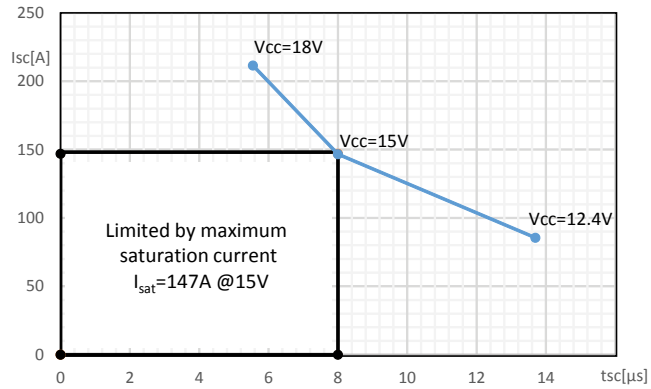


Figure 15. **Typical STGIB30M60yy SCSOA curve**



2 Electrical characteristics and functions

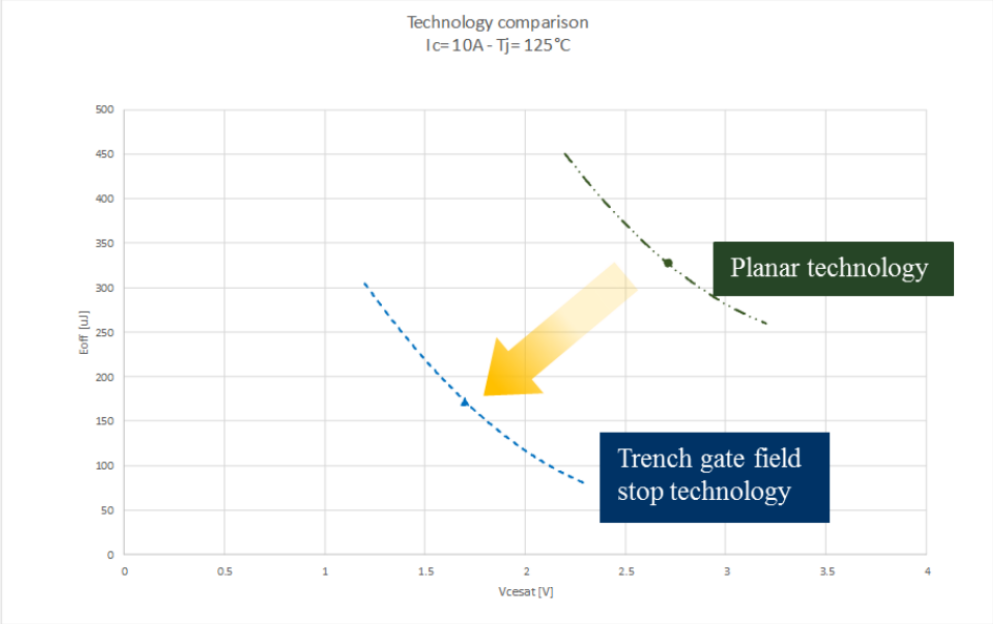
In this section, the main electrical characteristics of the power stage are discussed, together with a detailed description of the SLLIMM functions.

2.1 IGBTs

The 2nd version of the SLLIMM range combines the IGBTs with trench field stop (TFS) technology (in both H and M series), along with a new gate driver design to improve the system efficiency and allow new features.

These power devices, optimized for typical motor control switching frequencies, offer an excellent tradeoff between voltage drop ($V_{CE(sat)}$) and switching speed (t_{fall}) to therefore minimize the two major sources of energy loss, conduction and switching, thus reducing the environmental impact of daily-use equipment. Furthermore, the TFS technology offers significant improvement in terms of loss reduction over the previous generation based on planar technology. The figure below shows a comparison of $V_{CE(sat)}$ vs. E_{OFF} for both TFS and planar IGBT technologies with the same chip size.

Figure 16. TFS and Planar IGBT technology comparison



SLLIMM 2nd series devices are also capable of surviving short-circuits lasting up to 5 microseconds, as required by targeted applications. Furthermore M series devices (STGIB20M60xy-z and STGIB30M60xy-z) have a short circuit current withstand time of 8 microseconds.

2.2 Freewheeling diodes

The Turbo 2 ultrafast high voltage diodes have been appropriately selected for the SLLIMM family and carefully tuned to achieve the best t_{rr}/V_F tradeoff and softness as freewheeling diodes in order to further improve the total performance of the inverter and significantly reduce electromagnetic interference (EMI) in motor control applications, which are quite sensitive to this phenomena.

2.3 IC gate drivers

The new SLLIMM family is equipped with two different IC gate drivers: a triple low voltage gate driver for LS IGBTs and a triple high voltage gate driver for HS IGBTs. They are designed using BCD and BCD offline (Bipolar, CMOS, and DMOS) technologies respectively and are particularly suited to field oriented control (FOC) motor driving applications, able to provide all the functions and the proper current capabilities necessary for IGBT driving. The HS driver includes a patented internal circuitry which replaces the external bootstrap diode.

Figure 17. High-side gate driver block diagram

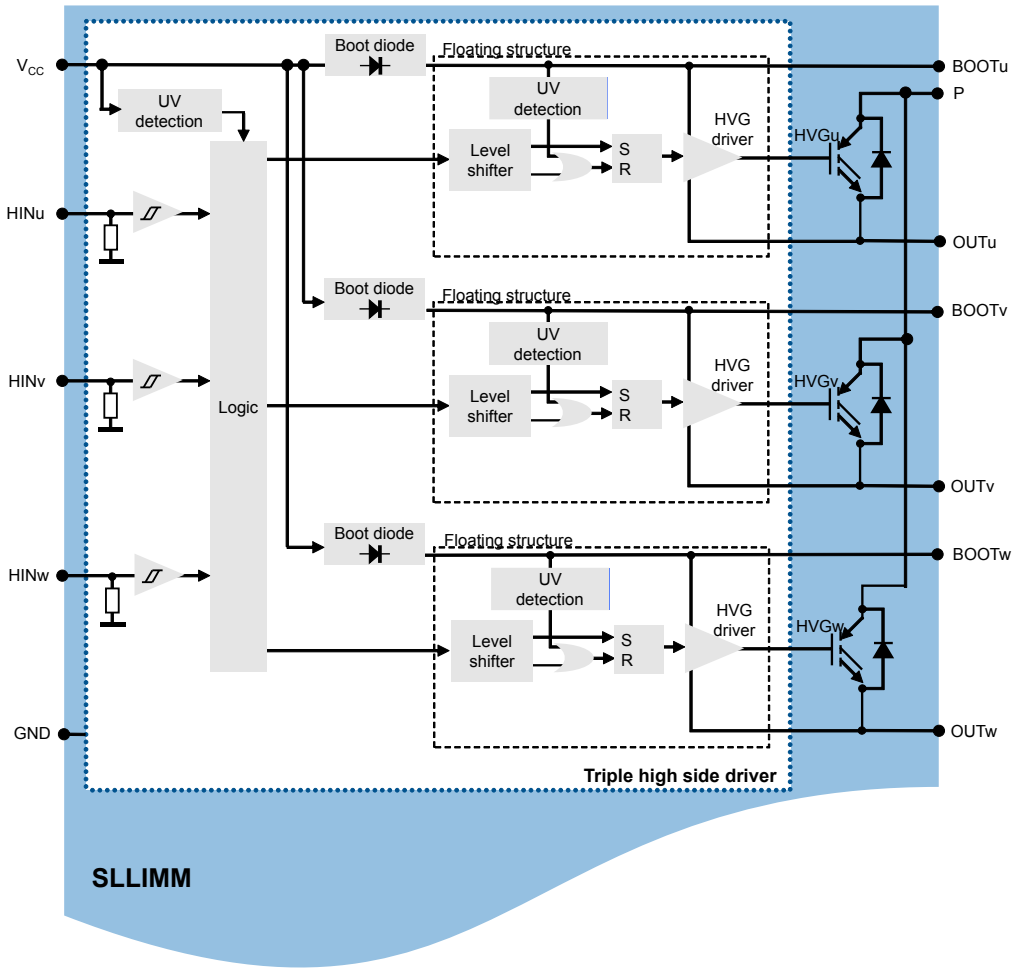
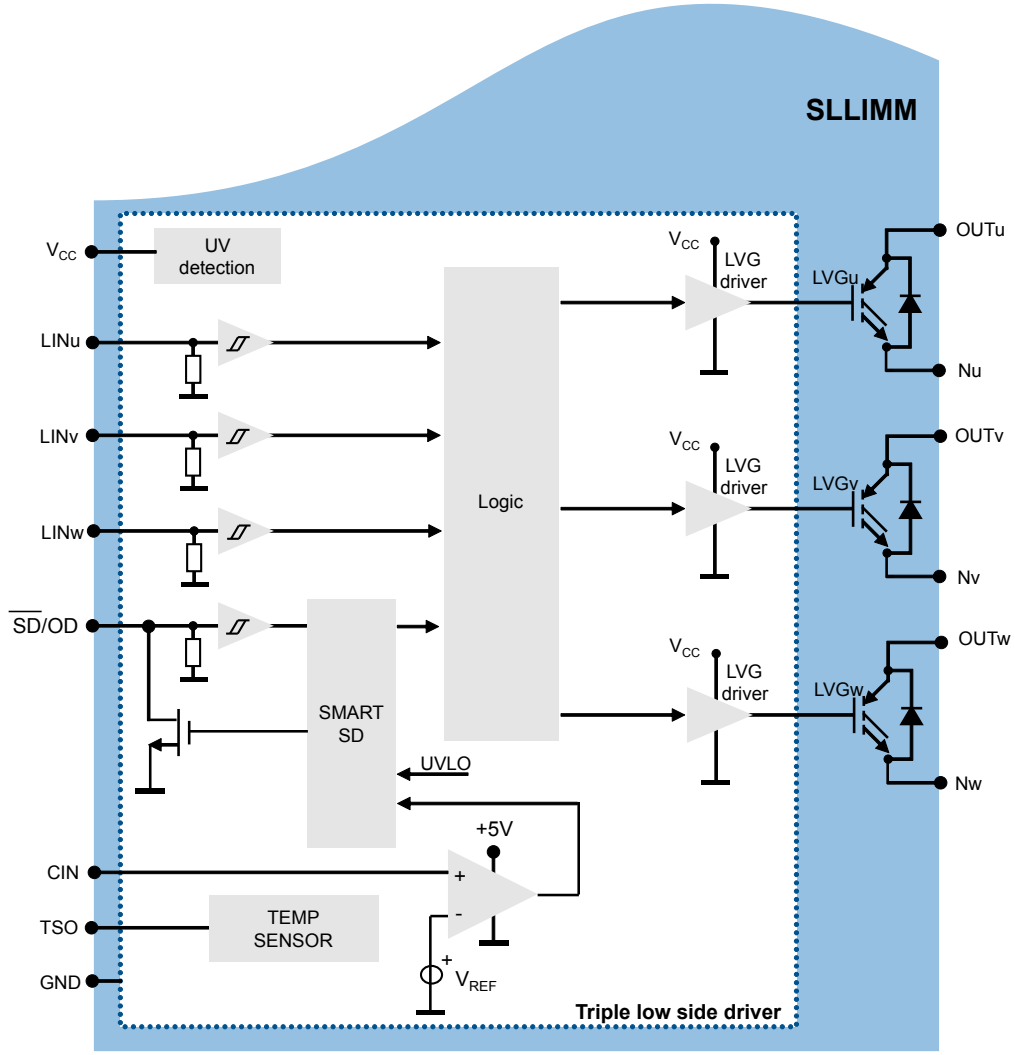


Figure 18. **Low-side gate driver block diagram**



For pin descriptions, refer to Section 3.4 Input and output pin descriptions.

2.3.1 Logic inputs

All the logic inputs include hysteresis (~1V) for low noise sensitivity and are TTL/CMOS-3.3-V compatible. Thanks to this low voltage interface logic compatibility, the SLLIMM can be used with any kind of high performance controller like microcontrollers, DSPs or FPGAs.

As shown in Figure 17. High-side gate driver block diagram and Figure 18. Low-side gate driver block diagram, the logic inputs have internal pull-down resistors in order to set the proper logic level in case of interruption in the logic lines. If logic inputs are left floating, the gate driver outputs LVG and HVG are set to low level. This simplifies the interface circuit by eliminating the six external resistors, therefore saving on cost, board space and number of components.

Table 9. Integrated pull-down resistor values

Input pin	Input pin logic	Internal pull-down
High-side gate driving HINu, HINv, HINw	active high	100 kΩ
Low-side gate driving LINu, LINv, LINw	active high	100 kΩ
$\overline{SD}$/OD shutdown	active low	100 kΩ

2.3.2 High voltage level shift

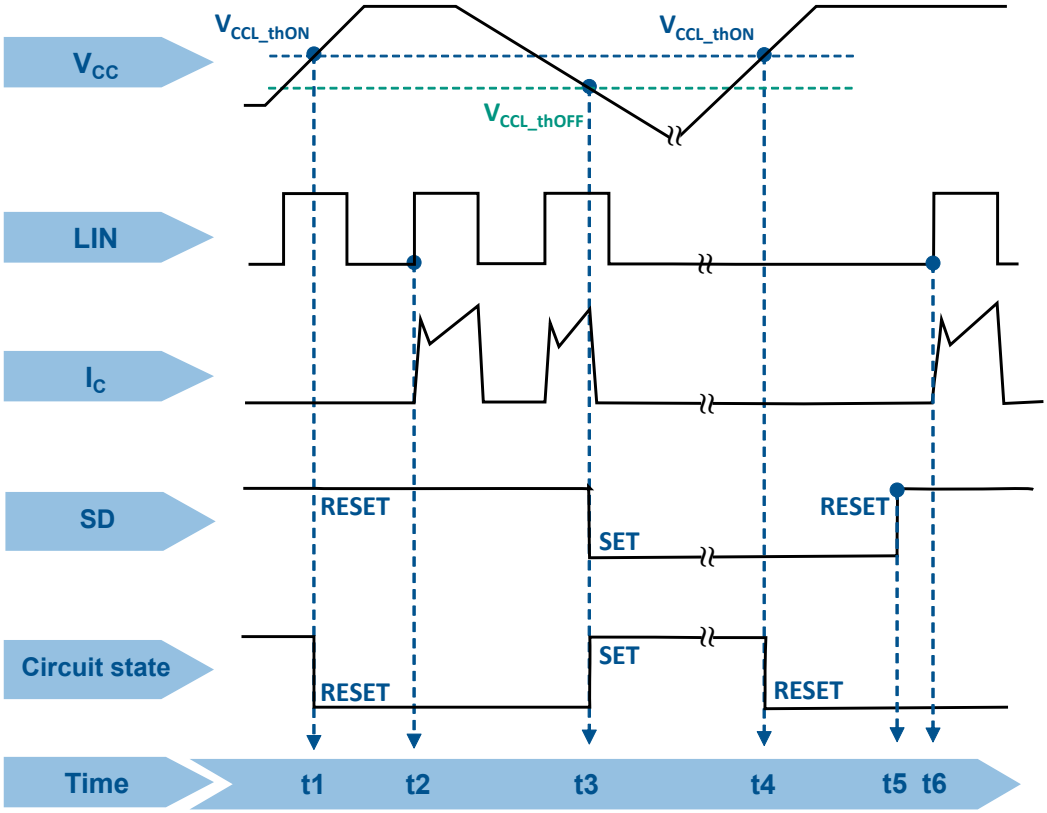
In the HS gate driver IC, the built-in high voltage level shift allows direct connection between the low voltage control inputs and the high voltage power half bridge in any power application up to 600 V. It is obtained thanks to the BCD offline technology which integrates, in the same die, low and medium voltage CMOS bipolar devices for analog and logic circuitry and high voltage DMOS transistors with a breakdown voltage in excess of 600 V. This key feature eliminates the need for external optocouplers, resulting in significant savings, component count and power losses. Other advantages are high-frequency operation and short input-to-output delays.

2.3.3 Undervoltage lockout

Both HS and LS gate driver IC supply voltages, V_{CCH} and V_{CCL} respectively, are continuously monitored by an undervoltage lockout (UVLO) circuit able to turn the low-side and high-side gate driver outputs off when the supply voltage falls below the V_{CCx_thOFF} threshold specified on the datasheet, and turns the IC on when the supply voltage rises above the V_{CCx_thON} voltage. A hysteresis of about 1.4 V is provided for noise rejection purposes. In addition, a fault signal on the $\overline{SD}$ pin is activated if an undervoltage is detected by the LS gate driver IC only. See Section 2.3.9 Fault management for further details.

Furthermore, in the HS gate driver IC, the high voltage floating supply V_{boot} is also provided with similar undervoltage lockout circuitry. In case of an UVLO condition on V_{boot}, the HVG outputs are set to low level.

Figure 19. **Timing chart of undervoltage lockout function on low-side section**



The timing chart is based on the following steps:

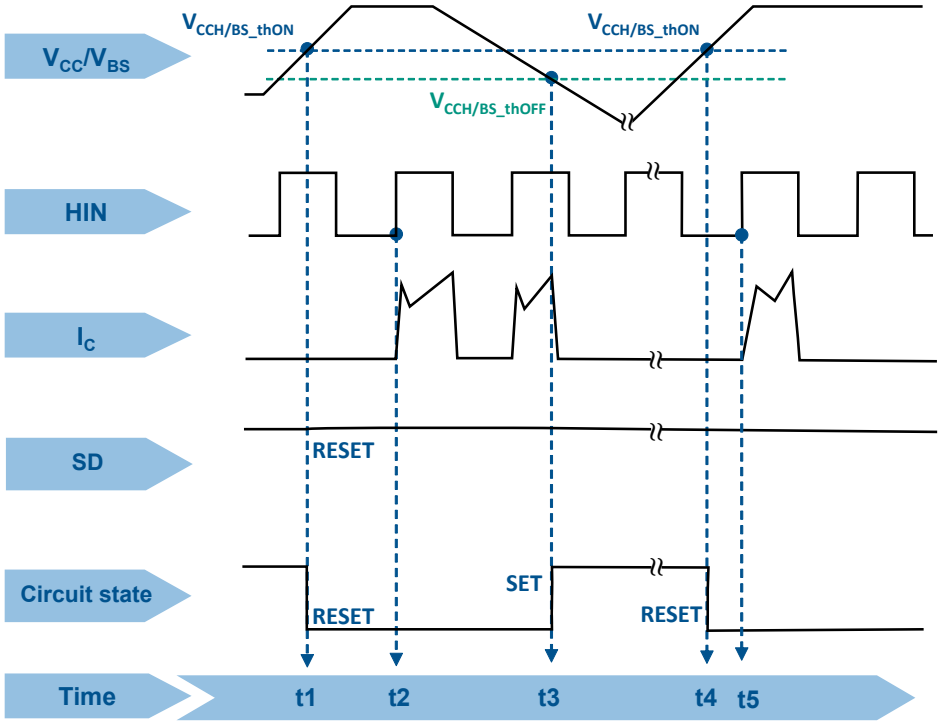
- t1: when the V_{CC} supply voltage rises above the V_{CCL_thON} threshold, the low-side gate driver starts operating after the next input signal LIN is on. The SD signal is in the pull up condition (RESET) from the external network and the circuit state is RESET.
- t2: input signal LIN is on and the related IGBT is turned on.
- t3: when the V_{CC} supply voltage falls below the V_{CCL_thOFF} threshold, an UVLO event is detected. The LS IGBTs are turned off even if the input signals LIN from the MCU are switching. The SD signal jumps to the SET condition and circuit is now in the SET state.
- t4: at this time, the V_{CC} supply voltage rises above the V_{CCL_thON} threshold again, but the driver is waiting for the SD reset. During this time, despite the V_{CC} having the right voltage, the LIN signals coming from the MCU are filtered. The SD is in the SET condition and fault information is sent to the MCU. The circuit state changes to RESET.
- t5: the LS gate driver re-starts when the SD jumps to the RESET condition.
- t6: the first useful input signal LIN now is able to turn on the LS IGBTs.

The undervoltage event on the LS gate driver enables a fault signal on the $\overline{SD}$ pin with a specific interval (t4 - t3):

- SD is SET for t_{UVLO} (70 µs) in case of short UVLO event (≤ 70 µs)
- SD is SET for t_{UVLO} (> 70 µs) in case of long UVLO event (> 70 µs)

Further details regarding SD timing can be found in Section 2.3.9 Fault management.

Figure 20. **Timing chart of undervoltage lockout function on high-side section**



The timing chart applies to the high-side gate driver for an undervoltage on V_{CC} or V_{boot}. It is based on the following steps:

- t1: when the V_{CC} (or V_{boot}) supply voltage rises above the V_{CCH_thON} (or V_{BS_thON}) threshold(s), the HS gate driver starts operating after the next input signal HIN is on. The SD signal is in the pull up condition (RESET) from the external network and the circuit state changes to RESET.
- t2: input signal HIN is on and the IGBTs are turned on.
- t3: when the V_{CC} (or V_{boot}) supply voltage falls below the V_{CCH_thOFF} (or V_{BS_thOFF}) threshold(s), an UVLO event is detected. The HS IGBTs are turned off even if the HIN input signals from the MCU are switching. The circuit changes to the SET state. During UVLO on the HS section, there is no fault signal so the SD remains in the RESET condition.
- t4: at this time, the V_{CC} (or V_{boot}) supply voltage again rises above the V_{CCH_thON} (or V_{BS_thON}) threshold and the gate driver restarts.
- t5: the first useful input signal HIN now is able to turn on the IGBT.

Table 10. SD duration time per event summarizes the possible UVLO events and their effect on the IGBTs and the SD pin.

2.3.4 Comparators for fault sensing

The SLLIMM family integrates one comparator intended for advanced fault protection such as overcurrent, over temperature or any other type of fault measurable via a voltage signal. The comparator has an internal reference voltage V_{REF}, specified in the datasheet, on its inverting input (see Low-side gate driver block diagram), while the non-inverting input is available on the CIN pin. The comparator input can be connected to an external shunt resistor to implement a simple overcurrent or short-circuit detection function, as discussed in the following section.

2.3.5 Short-circuit protection and smart shutdown function

The SLLIMM is able to monitor the output current and provide protection against overcurrent and short-circuit conditions in a very short time (comparator triggering to high/low-side driver turn-off propagation delay t_{isd} = 300 ns), thanks to the smart shutdown function.

This feature is based on patented circuitry which provides intelligent fault management and greatly reduces the protection intervention delay, regardless of the protection time duration which can be set by the user.

The comparator input can be connected to an external shunt resistor, R_{SHUNT}, in order to implement a simple overcurrent detection function.

An RC filter network (R_{SF} and C_{SF}) is necessary to prevent erroneous operation of the protection.

The output signal of the comparators is fed into an integrated MOSFET with the open drain available on the $\overline{SD}$/OD pin, shared with the input.

When the comparator triggers, the device is set to the shutdown state and all LS IGBTs are turned off. In common overcurrent protection architectures, the comparator output is connected to the $\overline{SD}$/OD input and an external RC network (R_{SD} and C_{SD}) is connected to this $\overline{SD}$/OD line in order to provide a mono-stable circuit which implements a protection time when a fault condition occurs.

Contrary to common fault detection systems, the smart shutdown structure allows immediate turn off of the LS gate driver output in the event of a fault, without having to wait for the external capacitor to discharge.

This strategy minimizes the propagation delay between the fault detection event and the actual switching off of the outputs. In fact, the time delay between the fault and output disabling is not dependent on the RC value of the external SD circuitry but, thanks to the internal architecture, it has a preferential internal path in the LS driver.

As shown in Figure 22. Timing chart of smart shutdown function, the device immediately turns off the LS driver outputs (with a propagation delay of 300 ns) and simultaneously latches the turn-on of the open drain switch (with propagation delay t_{CIN_SD}). The SD signal decreases to its unlatch threshold V_{SSD} and holds the open drain on until t_{OC} (24 µs) has elapsed. This time interval (taken from the V_{il} threshold) distinguishes the overcurrent fault event from other fault events like UVLO. The driver outputs restart following the input pins as soon as the voltage at the $\overline{SD}$ pin reaches the higher threshold of the SD logic input V_{ih}.

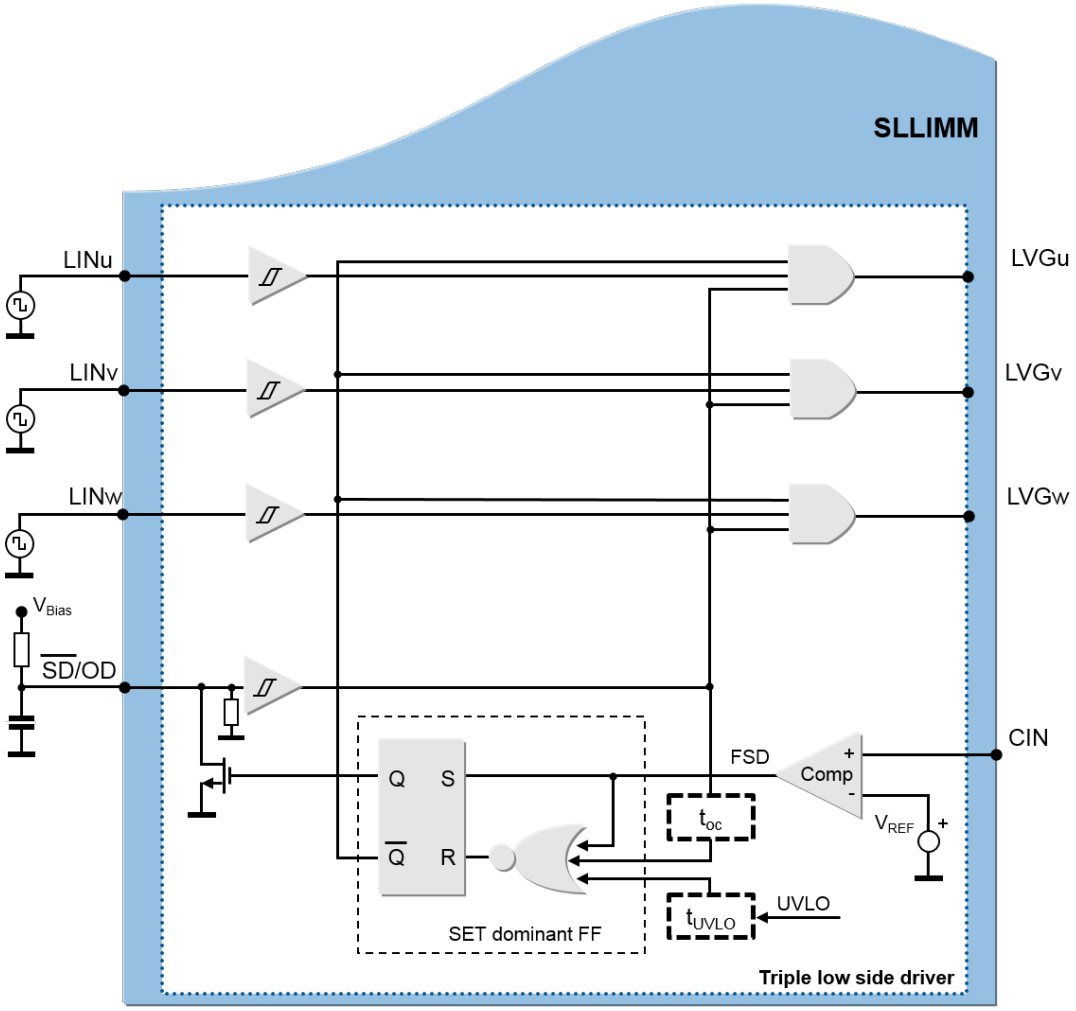
If the short-circuit is present during restart, the IPM enters a smart shutdown phase again.

Important: *Repeated short-circuit operations will stress the device.*

The smart shutdown system allows increasing the value of the external RC network across the $\overline{SD}$ pin over the time t_{OC} (sized to fix the disable time generated after the fault event) as much as desired by the user without compromising the intervention time delay of the SLLIMM protection.

The figure below shows a block diagram of the smart shutdown architecture inside the low-side driver.

Figure 21. **Smart shutdown equivalent circuitry**



In normal operation, the outputs follow the commands received from the respective input signals.

When a fault detection event occurs, the fault signal (FSD) is set to high by the fault detection circuit output and the FF receives a SET input signal. Consequently, the FF outputs set the low-side output signals to low level and simultaneously turn on the open drain MOSFET which works as an active pull-down for the SD signal.

Note that the low-side gate driver outputs remain at the low level until the $\overline{SD}$ pin has experienced both a falling edge and a rising edge, although the fault signal could be returned to low level immediately following fault sensing. In fact, even if the FF is reset by the falling edge of the $\overline{SD}$ input, the SD signal also acts as the enable for the outputs, thanks to the AND ports.

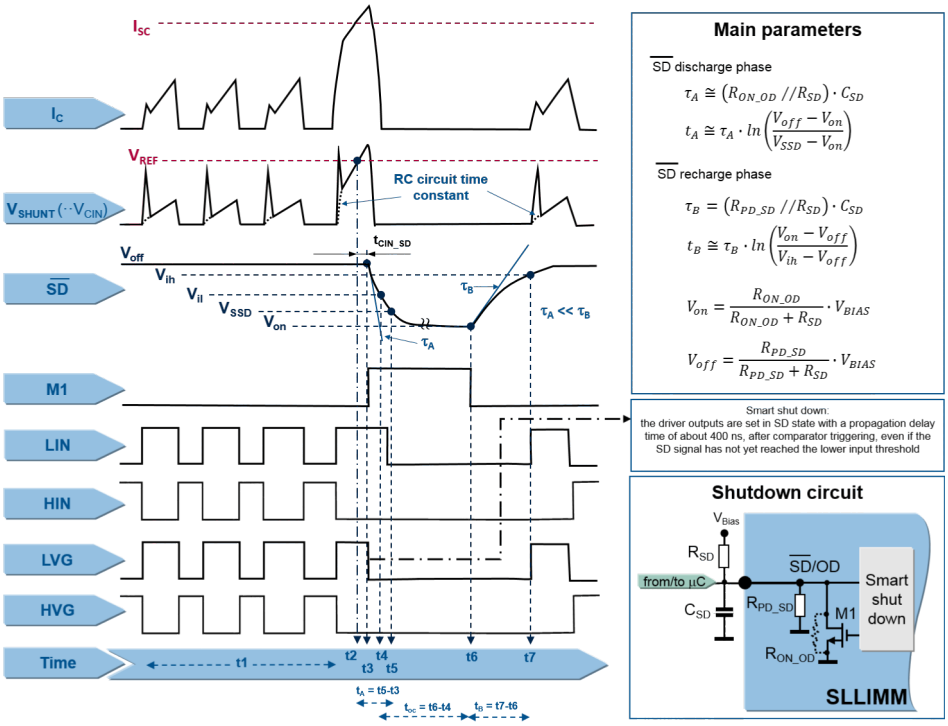
Moreover, once the internal open drain transistor has been activated, due to the latch, it cannot be turned off until the $\overline{SD}$ pin voltage reaches V_{SSD} and t_{OC} has elapsed.

Note: As the FF is SET dominant, oscillations of the $\overline{SD}$ pin are disregarded if the fault signal remains steady at the high level.

2.3.6 Timing chart of short-circuit protection and smart shutdown function

The figure below shows the timing chart during an overcurrent or short circuit event.

Figure 22. **Timing chart of smart shutdown function**



The timing chart is based on the following steps:

- t1: when the output current is lower than the max. allowed level, the SLLIMM functions normally.
- t2: when the output current reaches the max. allowed level (I_{SC}), the overcurrent/short-circuit event is detected and the protection is activated. The voltage across the shunt resistor, and then on the CIN pin (V_{CIN}), reaches the V_{REF} value; the comparator triggers and the shutdown phase begins.
- t3: after t_{cin_SD} time, the M1 internal open-drain MOSFET is switched on, the SD starts the discharge phase (with a time constant according to Equation 1) and the smart shutdown switches off the low-side IGBTs gate (LVG) through a preferential path (400 ns as typical internal delay time).

Equation 1

$$\tau_A \cong \left(R_{ON_{OD}} // R_{SD}\right) \cdot C_{SD}$$

- t4: at this time, the SD signal reaches the low voltage logic level (V_{il}) and, starting from this point, an internal timer fixes the t_{OC} time (20 µs for an overcurrent or short-circuit event).
- t5: the SD signal reaches the Smart SD unlatch threshold (V_{SSD}). In the meantime, the MCU detects the fault and it switches the input signals LIN and HIN off. The open drain MOSFET M1 remains on.
- t6: when the t_{OC} has elapsed, the SD can rise with a time constant given by following equation:

Equation 2

$$\tau_B \cong \left(R_{PD\_SD} // R_{SD}\right) \cdot C_{SD}$$

- t7: the SD signal reaches the upper threshold V_{ih} (in the worst case) and the system is ready to be re-enabled.

The discharging time t_A and the charging time t_B are the time intervals between t5-t3 and t7-t6, respectively.

2.3.7 Current sensing shunt resistor selection

As previously discussed, the shunt resistors R_{SHUNT} externally connected between the N pins and ground are used in the overcurrent detection circuitry.

When the output current exceeds the short-circuit reference level (I_{SC}), the CIN signal overtakes the V_{REF} value and the short-circuit protection is activated. For reliable and stable operation, the current sensing resistor should be a high quality, low tolerance non-inductive type. In fact, stray inductance in the circuit due to the layout, the RC filter, and even the shunt resistor, must be minimized in order to avoid undesired short-circuit detection.

For these reasons, the shunt resistor and the filtering components must be placed as close as possible to the SLLIMM pins. Refer to layout suggestions

The value of the current sense resistor can be calculated according to different guidelines, functions of the design specifications, or requirements. A common criterion is presented here based on the following steps:

- Define of the overcurrent threshold value (I_{OC_th}). This value can, for example, be set by considering the IGBT typical working current in the application and adding 20-30% as overcurrent.
- Calculation of the shunt resistor value according to the conditioning network.
- Selection of the closest shunt resistor commercial value.
- Calculation of the power rating of the shunt resistor, taking into account that this parameter is strongly temperature dependent. Therefore, the power derating ratio of the shunt resistor, ΔP(T)%, shown in the manufacturer's datasheet, must be considered, as shown in the formula below:

Equation 3

$$P_{SHUNT}(T) = \frac{R_{SHUNT} \cdot I_{RMS}^2}{\Delta P(T)\%}$$

Where I_{RMS} is the IGBT RMS working current.

For proper selection of the shunt resistor, a safety margin of at least 30% is recommended on the calculated power rating.

Below is an example for STGIF5CH60xy-z IPM.

The value of shunt resistor is calculated by the following equation:

Equation 4

$$R_{SH} = \frac{V_{ref}}{I_{OC}}$$

Where V_{ref} is the internal comparator (CIN) (0.51 V typ.) and I_{OC} is the OC trigger level.

The maximum OC protection level should be set less than the pulsed collector current in the datasheet. In this design, the overcurrent threshold level is fixed at 30% more than the nominal current at 80 °C (5 A). Therefore the shunt resistor value is:

Equation 5

$$R_{SH} = \frac{V_{\text{ref}}}{I_{OC}} = \frac{0.51}{1.3\text{x}5} = 0.078\ \Omega$$

For the power rating of the shunt resistor, these parameters must be considered:

- maximum load current of inverter (85% of I_{nom} (A_{rms})): I_{load}(max).
- shunt resistor value at T_C=25°C.
- power derating ratio of shunt resistor at T_{SH} = 100 °C
- safety margin.

The power rating is calculated with following equation:

Equation 6

$$P_{SH} = \frac{1}{2} \cdot \frac{I_{load(\max)}^2 \cdot R_{SH} \cdot margin}{Derating\ ratio}$$

For STGIF5CH60xy-z and R_{SH}= 0.08 Ω (commercial value):

Equation 7

$$I_{nom} = 5\text{A}(@80°\text{C}) \rightarrow I_{nom[rms]} = \frac{I_{nom}}{\sqrt{2}} \rightarrow I_{load}(\max) = 85\%\left(I_{nom[rms]}\right) = 3A_{rms}$$

- power derating ratio of shunt resistor at T_{SH} =100 °C: 80% (from datasheet manufacturer)
- safety margin: 30%

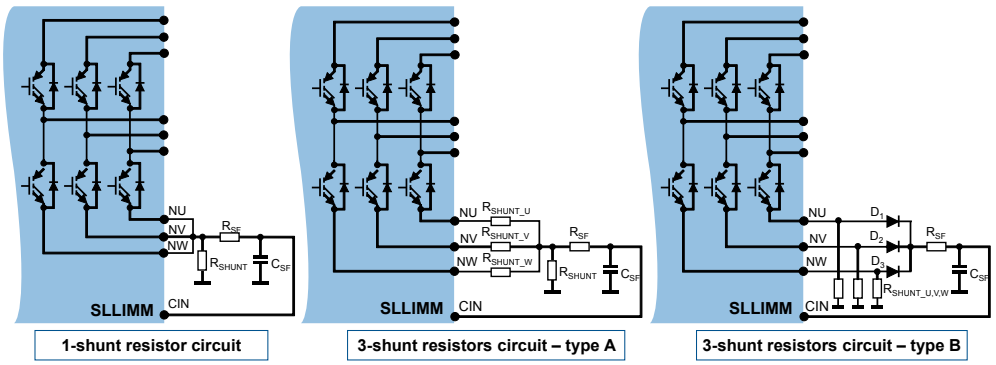
Equation 8

$$P_{SH} = \frac{1}{2} \cdot \frac{3^2 \cdot 0.08 \cdot 1.3}{0.8} = 0.58W$$

2.3.8 RC filter network selection

Two options of shunt (1- or 3-shunt) resistor circuits can be adopted for different control and short-circuit protection techniques. For 3-shunt resistor configurations, the following figure shows two simple overcurrent protection variants: type A, using an additional shunt resistor (R_{SHUNT}) and type B, using a diode OR gate circuit.

Figure 23. Examples of SC protection circuits



An RC filter network is required to prevent undesired short-circuit operation due to noise on the shunt resistor.

All the solutions allow detection of the total current in all the three phases of the inverter. The filter is based on the R_{SF} and C_{SF} network and its time constant is given by:

Equation 9

$$t_{SF} = R_{SF} \cdot C_{SF}$$

In addition to the RC time constant, the turn-off propagation delay of the gate driver, t_{CIN_LVG} (specified in the datasheet) and the IGBT turn-off time (in the order of tens of ns), must be considered in the total delay time (t_{Total}), which is the time necessary to completely switch the IGBT off once the short-circuit event is detected. Therefore, t_{Total} is calculated as follows:

Equation 10

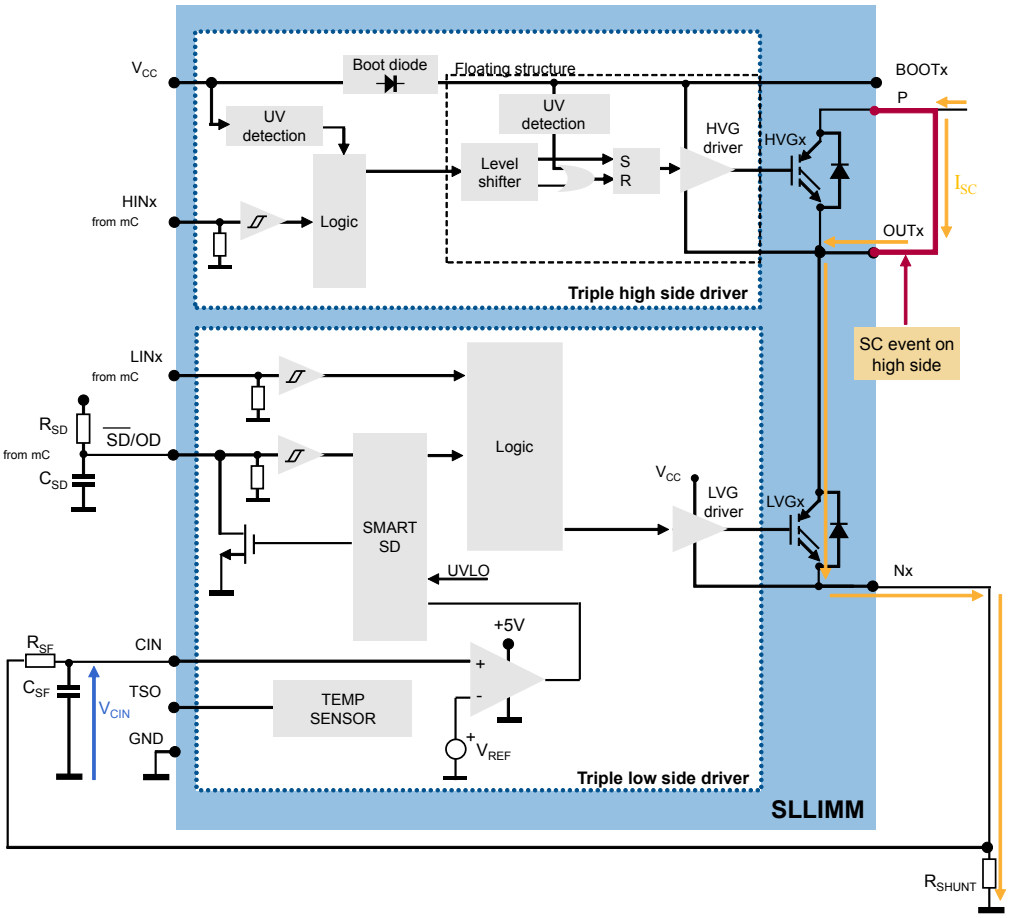
$$t_{Total} = t_{SF} + t_{CIN\_LVG} + t_{off}$$

Considering that the IGBT short-circuit withstand time (t_{SC}) is 5 µs, t_{SF} should be set to the 1-2 µs range.

In a 3-shunt resistor circuit, a specific control technique can be implemented by using the three shunt resistors (R_{SHUNT_U}, R_{SHUNT_V} and R_{SHUNT_W}) to monitor each phase current.

An example short-circuit event during normal operation, between P and OUTx when LINx is high, is shown in the figure below.

Figure 24. **Example of a short-circuit event**



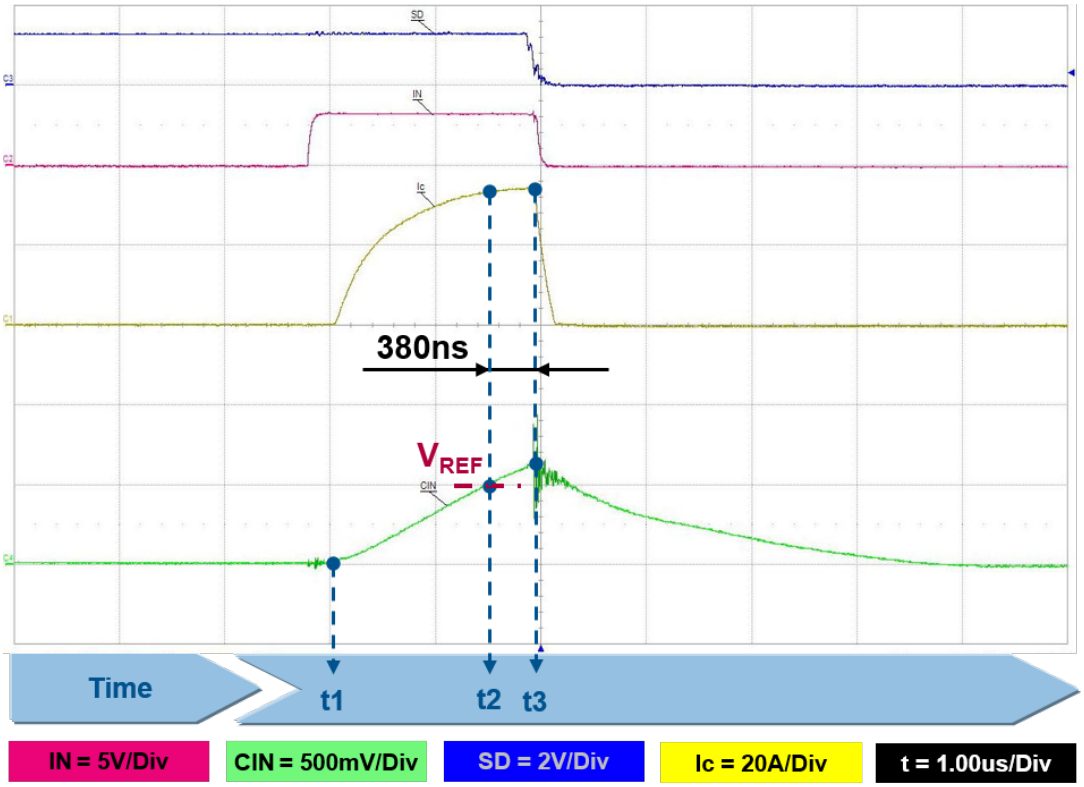
Smart shutdown operation clearly demonstrates the highly rapid protection offered by the smart shutdown function for an overcurrent fault event occurring on an HS IGBT.

The main steps are, shown in the figure below, are:

- t1: collector current I_C starts to rise. An SC event is not detected yet due to the RC network on the CIN pin
- t2: voltage on V_{CIN} reaches V_{REF}. An SC event is detected and the smart shutdown starts turning off the LS IGBTs. The SD signal is enabled (for 24 µs) so the MCU can stop the PWM signals and as consequence of this, even the HS IGBTs are turned off.
- t3: the SLLIMM is definitively turned off in less than 400 ns (including the $t_{d(off)}$ time of IGBT) from SC detection.

In summary, the total disable time is t3-t2 and the total SC action time is t3-t1.

Figure 25. **Smart shutdown operation**



2.3.9 Fault management

The SLLIMM 2nd series integrates a specific kind of fault management, useful when the $\overline{SD}$ pin acts as output and is able to identify the type of fault event.

As previously described, as soon as a fault occurs, the open-drain (DMOS) is activated and LVG outputs are forced low and consequently the LS IGBTs.

Two types of fault can be identified:

- Overcurrent (OC) sensed by the internal comparator (C_{IN})
- Undervoltage (UVLO) on LS gate driver supply voltage (V_{CCL})

During an UVLO event, the supply voltage must in any case be higher than 4 V to ensure the full functionality of fault management logic.

Each fault event enables the $\overline{SD}$ open drain for a different time interval to allow the type of failure event to be identified. Actually, the device remains in a fault condition for a total duration time also depending on RC network connected to the $\overline{SD}$ pin. The network generates a time contribution that is added to the internal value shown in the table below.

Table 10. SD duration time per event

Symbol	Parameter	Event time	SD open-drain enable time result
OC	Overcurrent event	≤ 24 µs (1)	24 µs (1)(2)
		> 24 µs (1)	OC time
UVLO	Undervoltage lock out even	≤ 70 µs (1)	70 µs (1)(2)
		> 70 µs (1) until the V_{CC_LS} exceeds the V_{CC_LS} UV turn ON threshold	UVLO time

1. *typical value (Tj= - 40 °C to 125 °C)*
2. *without contribution of RC network on SD*

The table below summarizes the fault events and the effect on the IGBTs and $\overline{SD}$ pin.

Table 11. Fault event summary effect on IGBT and SD

Fault event	HS IGBTs	LS IGBTs	$\overline{SD}$/OD
OC	ON	OFF	Low (SET) (for t_{OC}) (2)
UVLO V_{CCH}	OFF	Operative	High (RESET)
UVLO V_{CCL}	Operative	OFF	Low (SET) (for t_{UVLO}) (2)
UVLO V_{boot}	OFF	Operative	High (RESET)

The following figures demonstrate device behavior during OC and UVLO events.

Figure 26. **OC event**

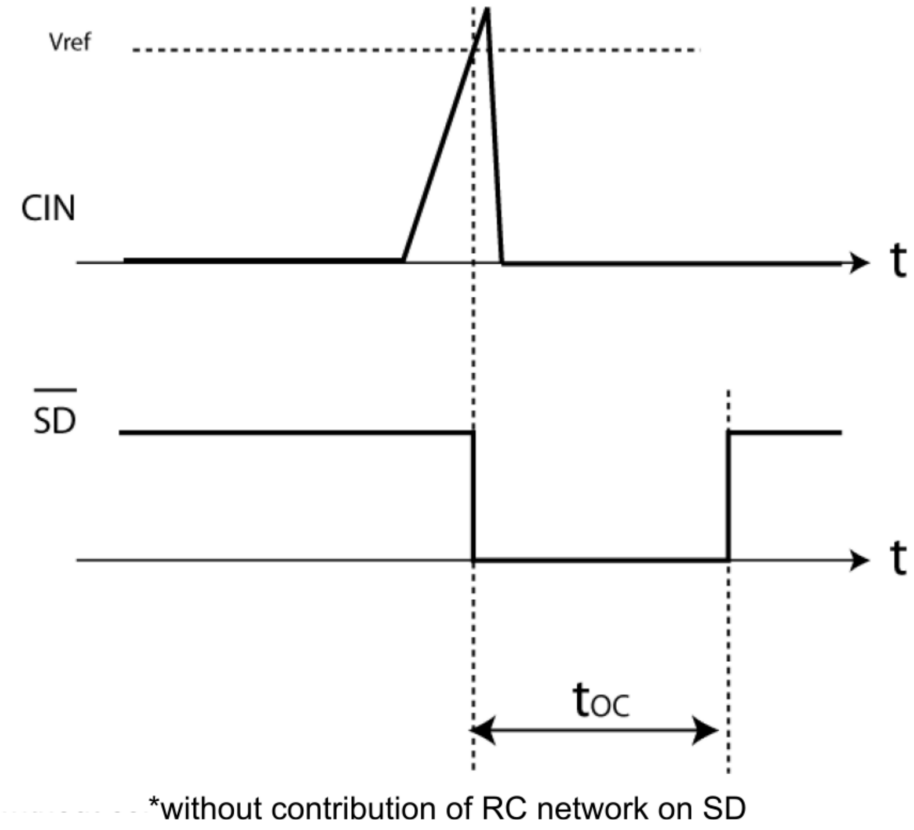
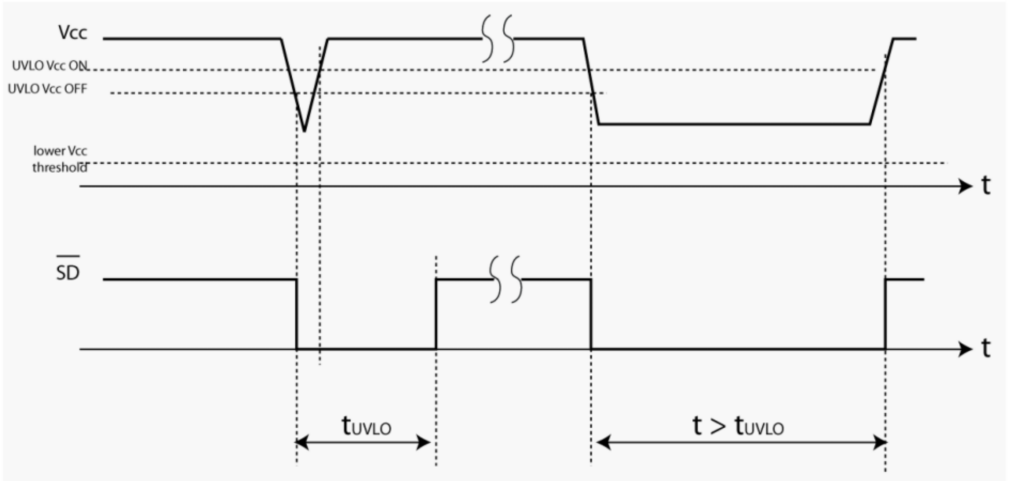


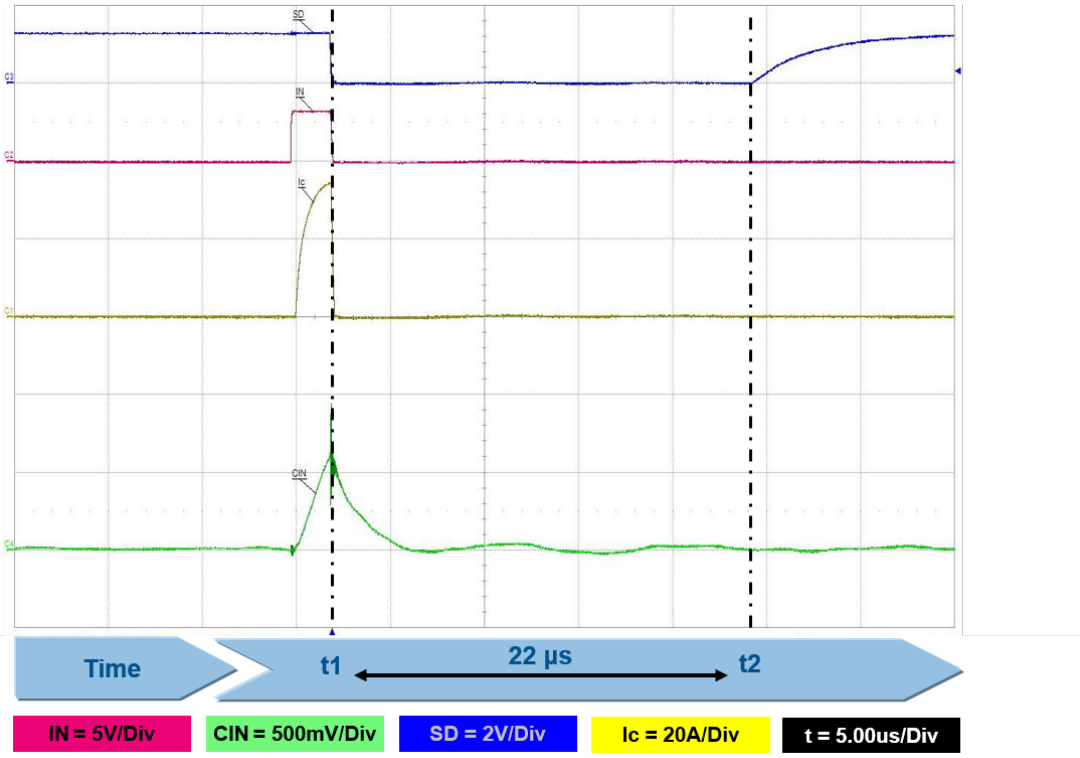
Figure 27. **UVLO event**



*without contribution of RC network on SD

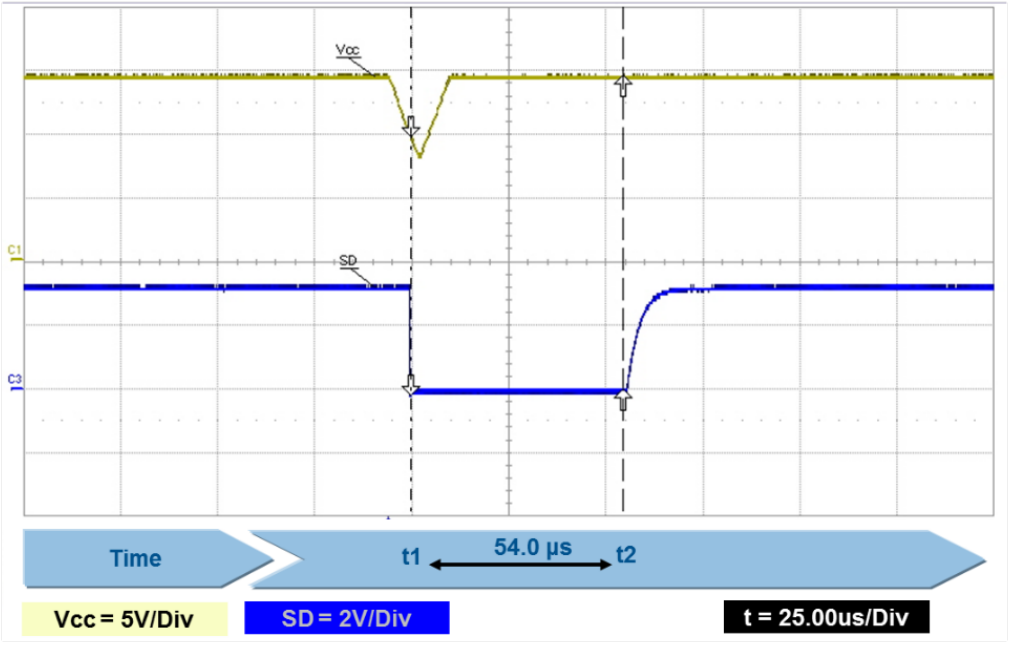
The figure below shows a shutdown as the result of an overcurrent event. During the overcurrent, the voltage on the comparator (CIN) exceeds the threshold (0.51 V typ.) and the shutdown is able to stop the application. In this case, the SD event time is about 24 µs (1) (for OC event less than 24 (1) µs).

Figure 28. **SD duration for OC event**



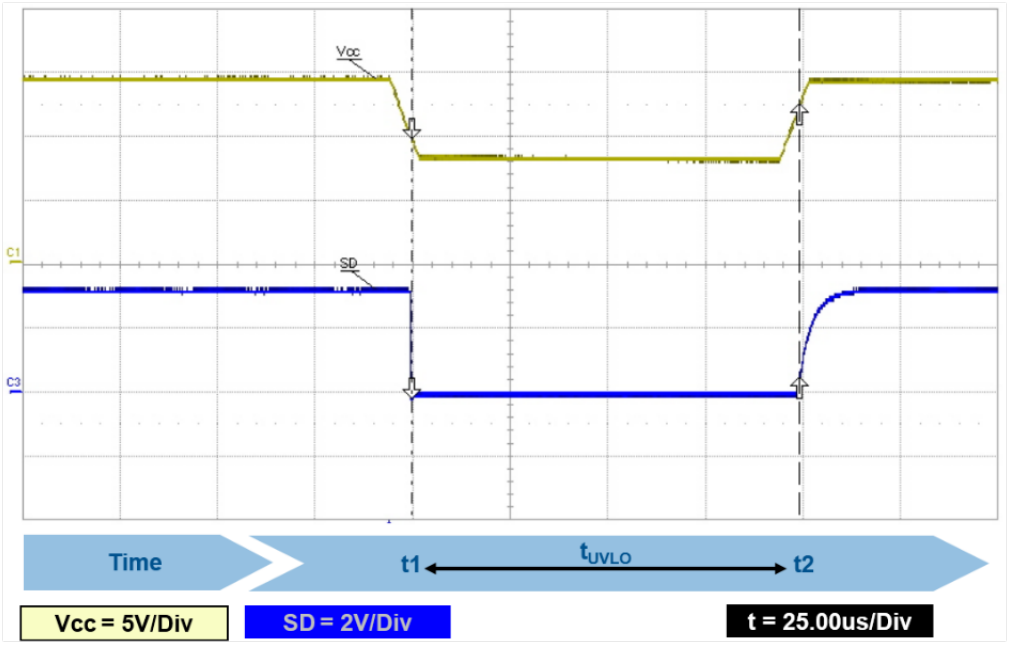
The following figure shows real acquisition data for a short UVLO event (≤ 70 [1] µs) on the V_{CCL} (yellow waveform) supply voltage (V_{CCL} > 4 V). When this voltage drops to the undervoltage threshold ($V_{CC\_th(off)}$), the SD (blue waveform) is SET. The figure clearly shows an SD duration of about 70 µs [1] (for a UVLO event less than 70 µs).

Figure 29. **SD duration for short UVLO event (≤ 50 µs)**



The following figure shows real acquisition data for a long UVLO event (> 70 µs [1]) on the V_{CCL} (yellow waveform) supply voltage (V_{CCL} > 4 V). In this case, V_{CCL} remains in the UVLO condition for more than 70 µs [1] and the SD duration is the same as the UVLO duration.

Figure 30. SD duration for long UVLO event (> 70 µs)



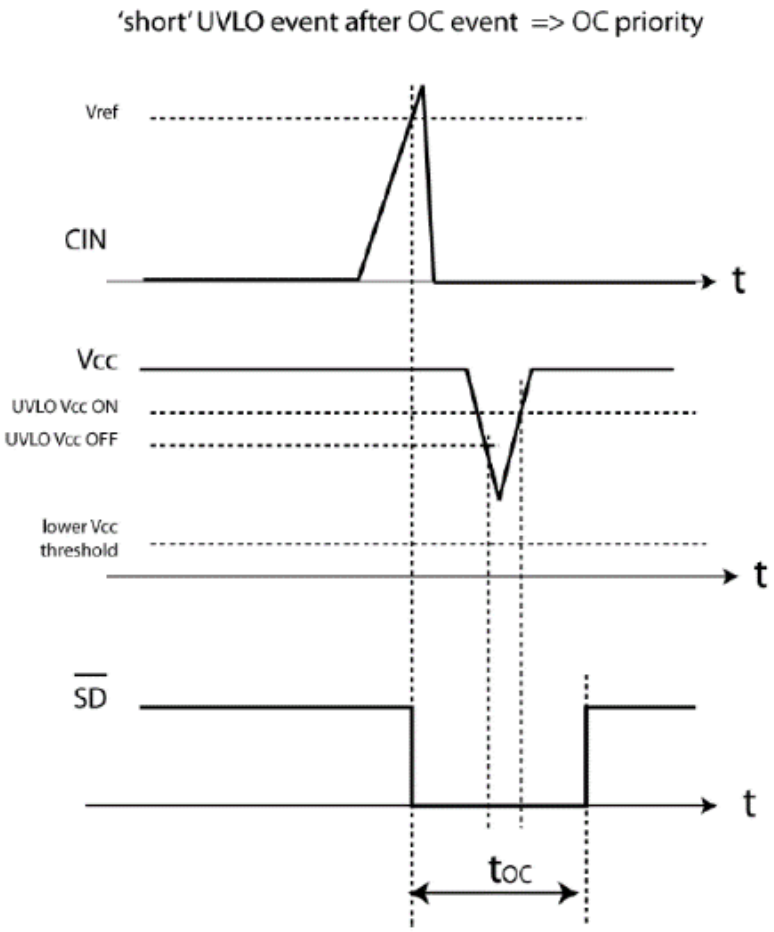
The following simultaneous fault events are in any case highly unlikely:

Figure 31. Short UVLO event after OC event shows a short (≤ 24 µs [1]) UVLO event within an OC event. In this case, the fault duration is t_{OC} (24 µs).

Figure 32. Long UVLO event after OC event shows a long (> 24 µs [1]) UVLO event while the IPM is an OC event. In this case, the fault signal only elapses when UVLO terminates (> 70 µs [1]).

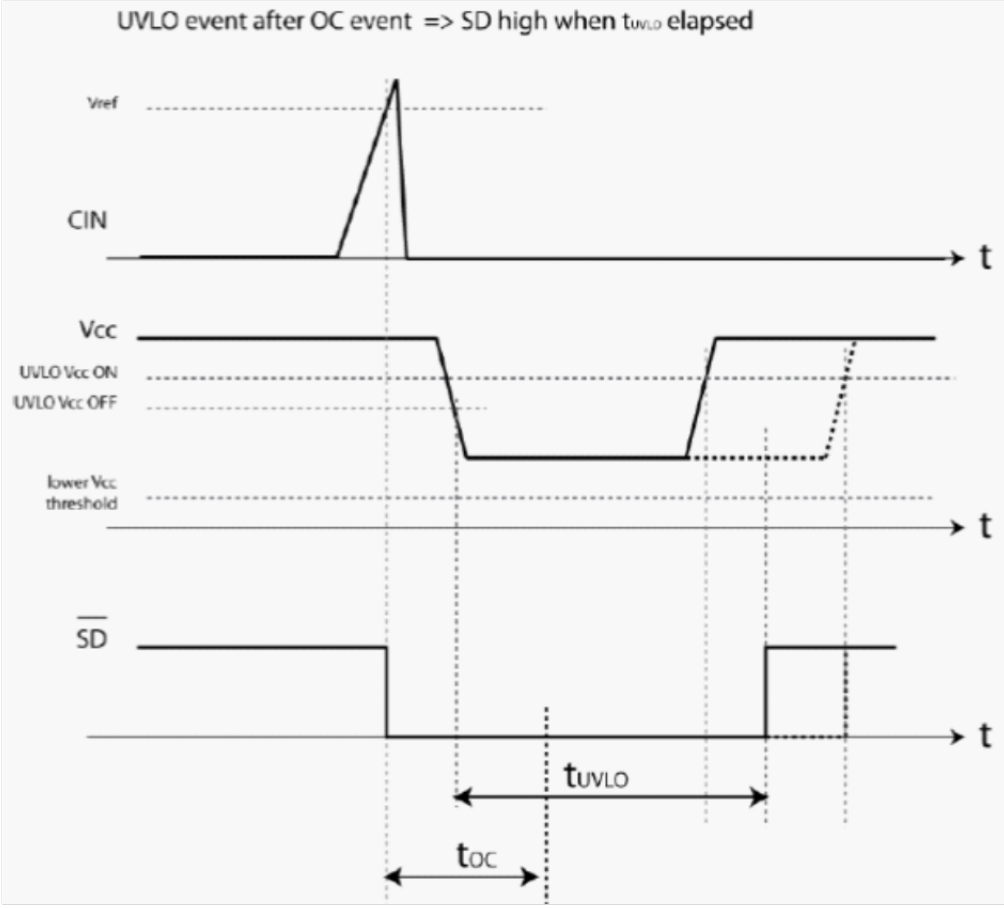
If the internal comparator is not used for overcurrent protection, comparator triggering may occur when the device is in a UVLO state, as shown in Figure 33. Comparator triggering in UVLO condition. In this case the fault duration is given by the overlap between t_{OC} and t_{UVLO}.

Figure 31. **Short UVLO event after OC event**



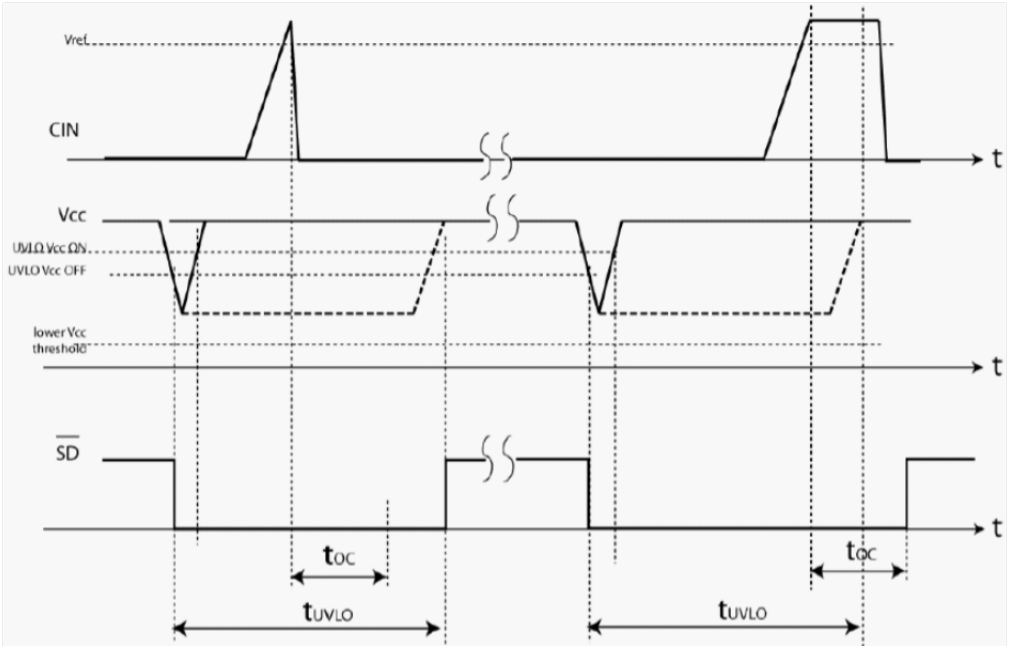
*without contribution of RC network on SD

Figure 32. **Long UVLO event after OC event**



*without contribution of RC network on SD

Figure 33. **Comparator triggering in UVLO condition**

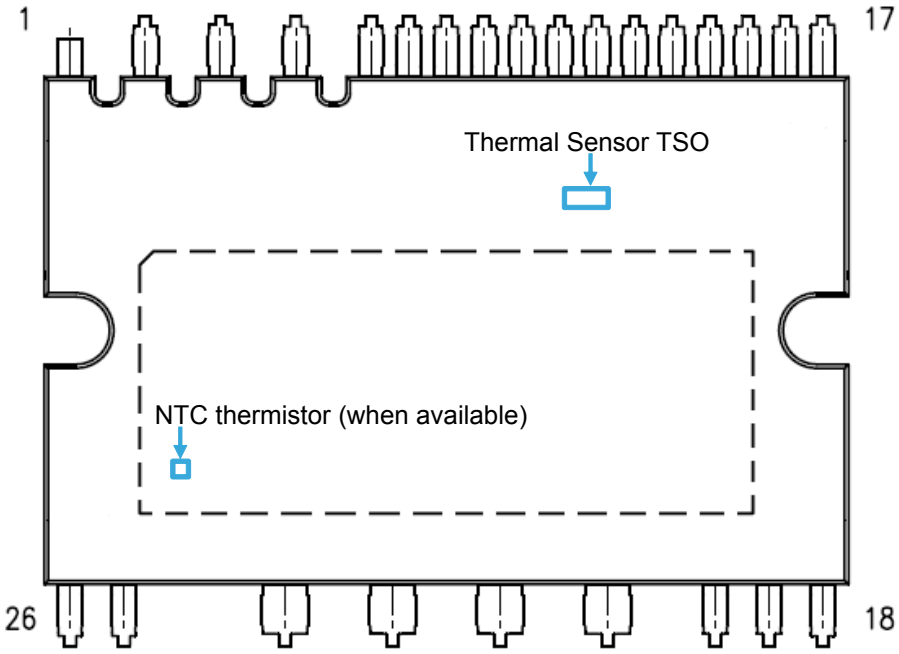


*without contribution of RC network on SD

2.3.10 Temperature monitoring

The SLLIMM 2nd series family integrates a thermal sensor (TSO) on the low-side gate driver and an NTC thermistor (optional) placed near the power stage for internal IPM temperature monitoring.

Figure 34. **Temperature detection points (top view)**



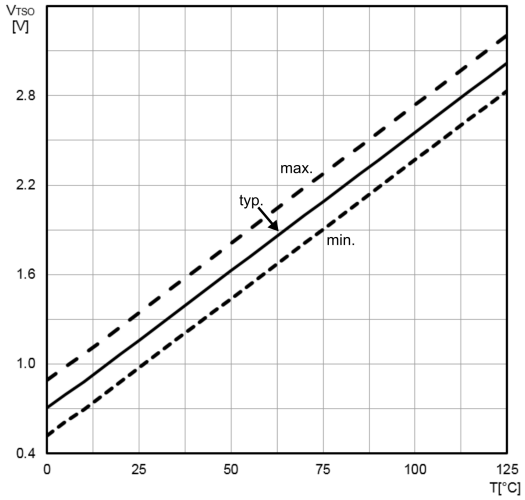
2.3.10.1 *Thermal sensor (TSO)*

The SLLIMM 2nd series family includes a temperature sensor integrated on the LS gate driver. The internal heat generated during normal operation is transferred to the sensor through the internal resin and heatsink. Temperature and consequent voltage variation is therefore not immediate. For this reason, we recommend using this function for monitoring and eventual protection when slow temperature increases are detected in cases such as during continuous overload. A voltage proportional to the temperature is available on TSO pin (17) and the sensor does not need any pull down resistor. To increase the noise immunity, a capacitor filter of 1 to 10 nF must be placed on this pin.

This function cannot shut the SLLIMM down directly if the temperature rises above safe temperatures, but the output voltage can be sent to a circuit (such as a comparator) to provide feedback to the MCU which can in turn halt the IPM.

The figure below shows a typical voltage variation with temperature graph. For specific device information, please refer to the relevant datasheet.

Figure 35. **Thermal sensor voltage vs temperature**



The output voltage is a linear characteristic compatible with the 3.3 V MCU supply voltage. If a safety margin is required, a 3.3 V clamp circuit at can be used. The following figures show typical circuits that can be used to monitor internal temperature and provide relevant information to the MCU, which can halt the IPM if necessary.

Figure 36. **Normal voltage controller (MCU)**

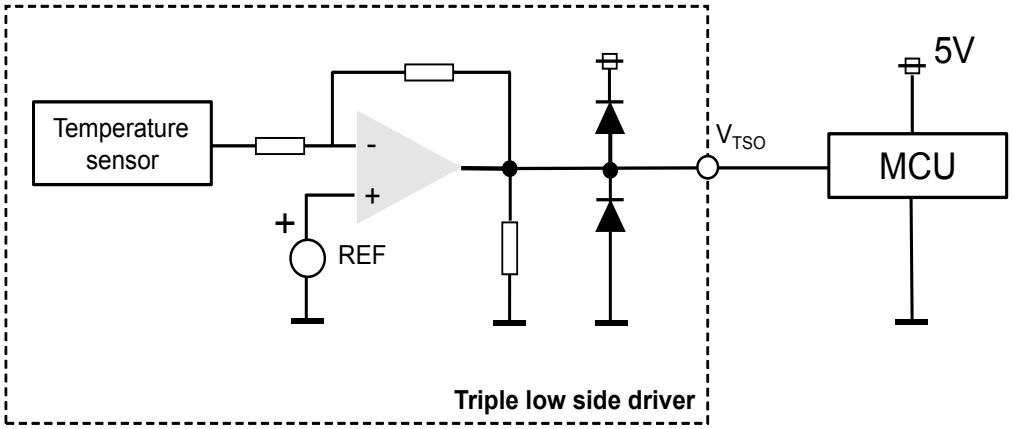
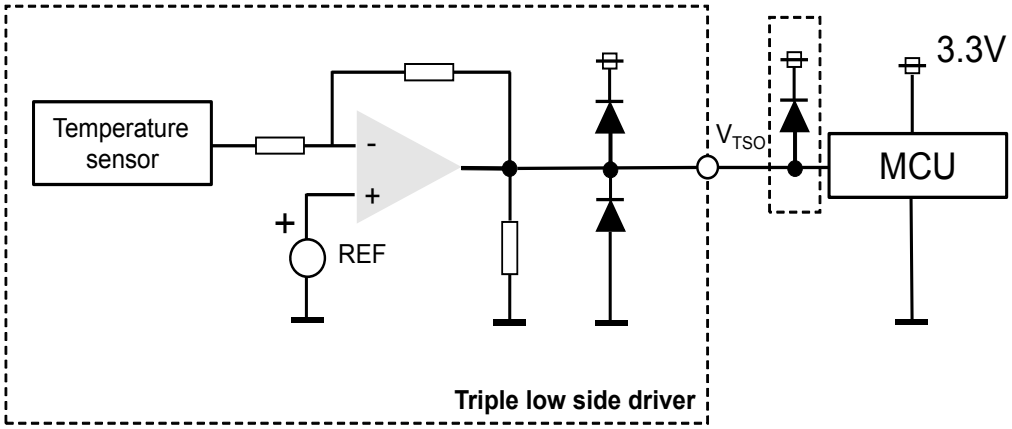


Figure 37. **Low voltage controller (MCU): optional clamping**



The internal circuit consists of a temperature sensor, an amplification network to amplify the signal and ESD protection. Its current capability is 4 mA min. source (I_{TSO_SRC}) and 0.1 mA typ. (I_{TSO_SNK}).

When this function is not used, the TSO pin can be left floating.

2.3.10.2 *NTC Thermistor*

The SLLIMM 2nd series can be optionally equipped with a negative temperature coefficient (NTC) thermistor for easy over temperature protection, by sending the microcontroller real-time temperature data.

Due to the thermal impedance of SLLIMM and its own time constant, the NTC thermistor is not suited to detecting rapid junction temperature rises directly in the power devices. Therefore, it cannot be used for short-circuit or overcurrent protection, but only to monitor gradual changes in temperature.

The NTC thermistor is placed very close to the power stage for accurate junction temperature monitoring of power chips.

The resistance versus temperature characteristic of NTC thermistor is non-linear and it is described by the following expression:

Equation 11

$$R\left(T\right) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

Where T is the temperature in Kelvin, B is a constant in the SLLIMM operating range and R25 is the resistance at 25 °C; these last two parameters are shown in the datasheet.

The built-in thermistor (85 kΩ at 25 °C) is inside the IPM and connected between T1 and T2 pins (26, 25).

Figure 38. **NTC resistance vs temperature**

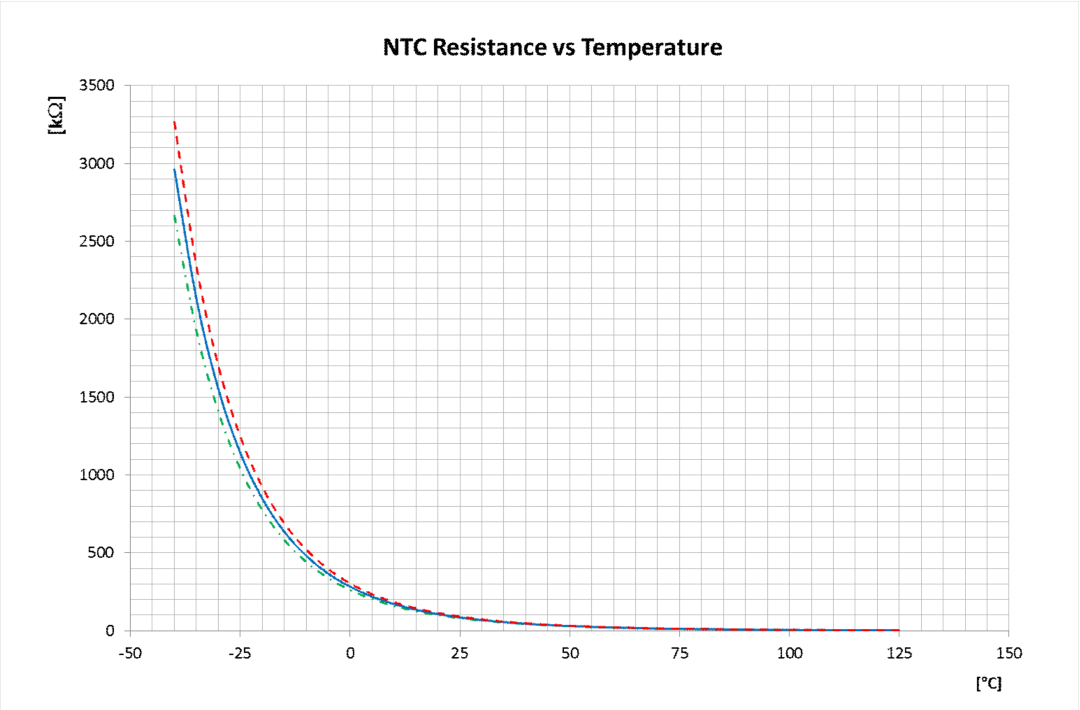
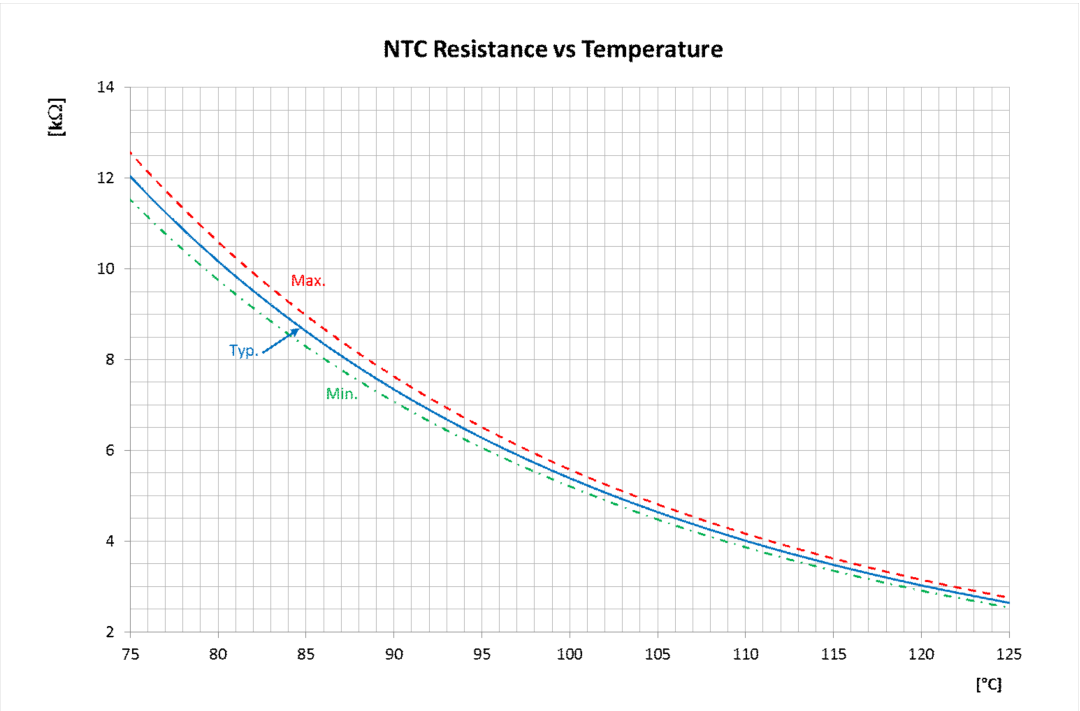
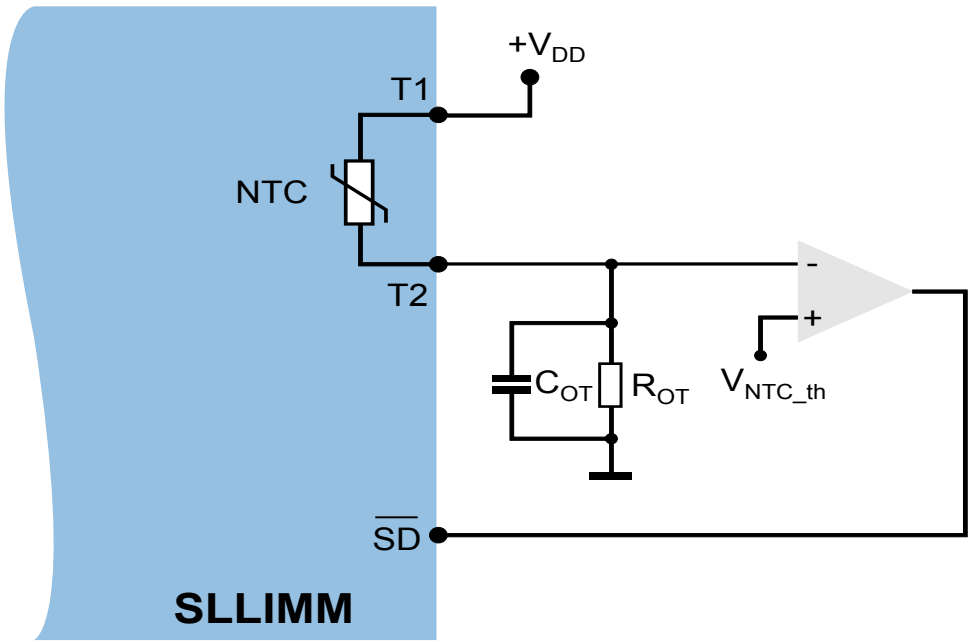


Figure 39. **NTC resistance vs temperature – zoom**



The following figure shows a simple circuit using a voltage divider for both overtemperature protection and temperature monitoring.

Figure 40. **Sample overtemperature protection circuit**



The external comparator is used to send a shutdown signal to the SLLIMM in case of over temperature. V_{NTC_th} is a threshold voltage, fixed by design, and connected to the non-inverting input, while the inverting input is connected to a voltage divider based on the NTC and R_{OT} resistors. When the voltage on the inverting input exceeds the V_{NTC_th} value, the comparator triggers, pulling down the $\overline{SD}$ pin and consequently switching off the LS IGBTs.

For a proper sizing of the voltage divider, the maximum allowed temperature level (T_{OT_Max}) must first be set and the thermistor resistance derived from Equation 11, as well as from Figure 38. NTC resistance vs temperature and Figure 39. NTC resistance vs temperature – zoom. The value of resistance R_{OT} can be calculated with the voltage divider formula:

Equation 12

$$V^{-}(T) = \frac{R_{OT}}{R_{NTC}(T) + R_{OT}} \cdot V_{DD}$$

considering that, if T = T_{OT_Max} then V-(T_{OT_Max}) = V_{NTC_th}.

The maximum allowed power on the thermistor should not exceed 5 mW across the entire operating range in order to guarantee safe operation and avoid power consumption affecting the temperature measurement through self-heating.

Therefore, for T = T_{OT_Max}:

Equation 13

$$R_{NTC} \cdot I^2 = R_{NTC} \cdot \left(\frac{V_{DD}}{R_{NTC}+R_{OT}}\right)^2 \leq 5mW$$

Finally, to increase the noise immunity of the NTC thermistor, we recommend placing a decoupling capacitor (C_{OT}) in parallel, whose value must be between 10 and 100 nF.

The following figures show two sample pull up and pull down resistor configurations and corresponding voltage output graphs as function of temperature. Both curves include the maximum spread according to the tolerance of the NTC and RPU / RPD resistances.

Figure 41. V_{NTC} vs temperature (pull up configuration)

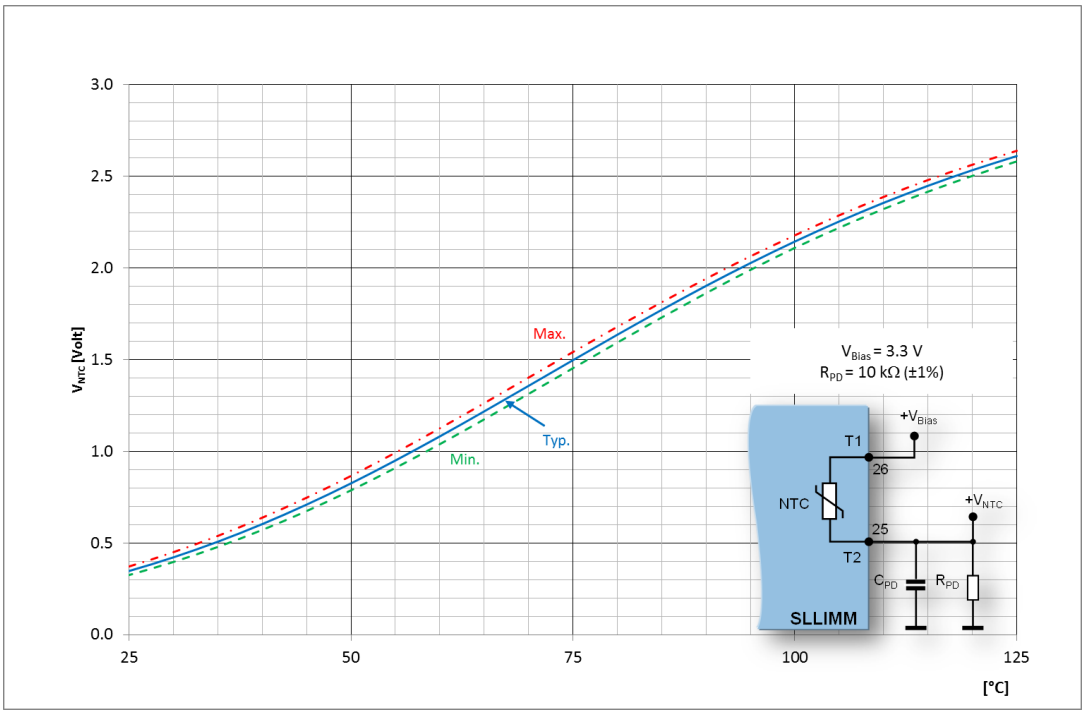
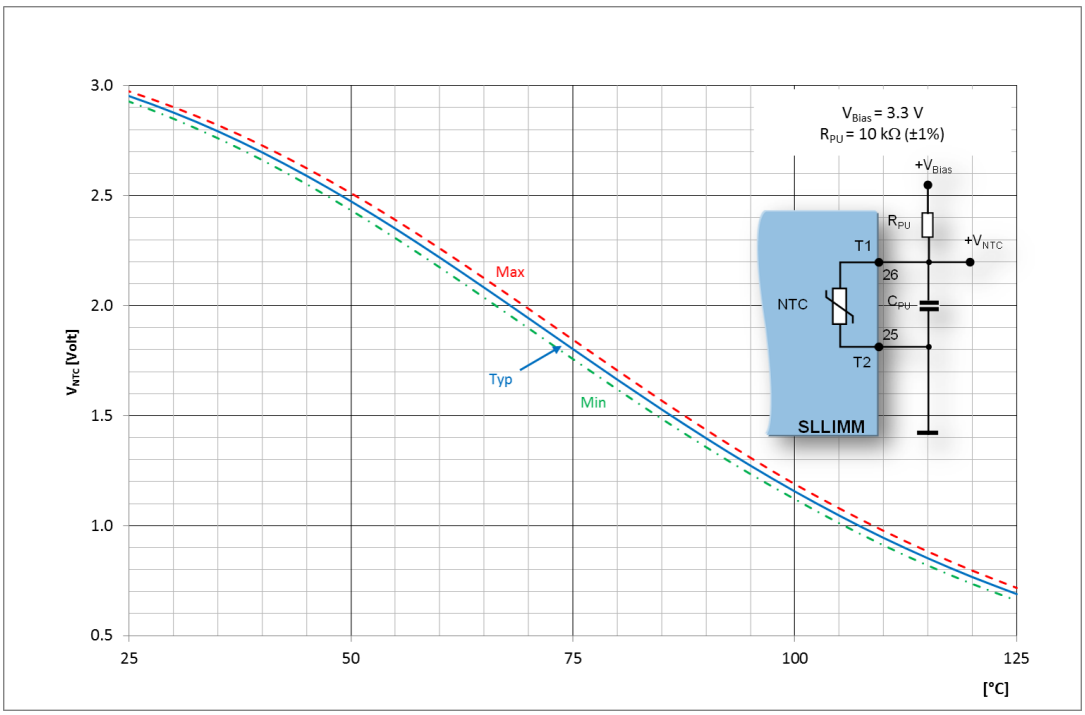


Figure 42. V_{NTC} vs temperature (pull down configuration)



2.3.11 Bootstrap circuit

In the 3-phase inverter, the emitters of the low-side IGBTs are connected to the negative DC bus (VDC-) as the common reference ground, which allows all low-side gate drivers to share the same power supply, while the emitter of the high-side IGBTs is alternately connected to the positive (VDC+) and negative (VDC-) DC bus during operation.

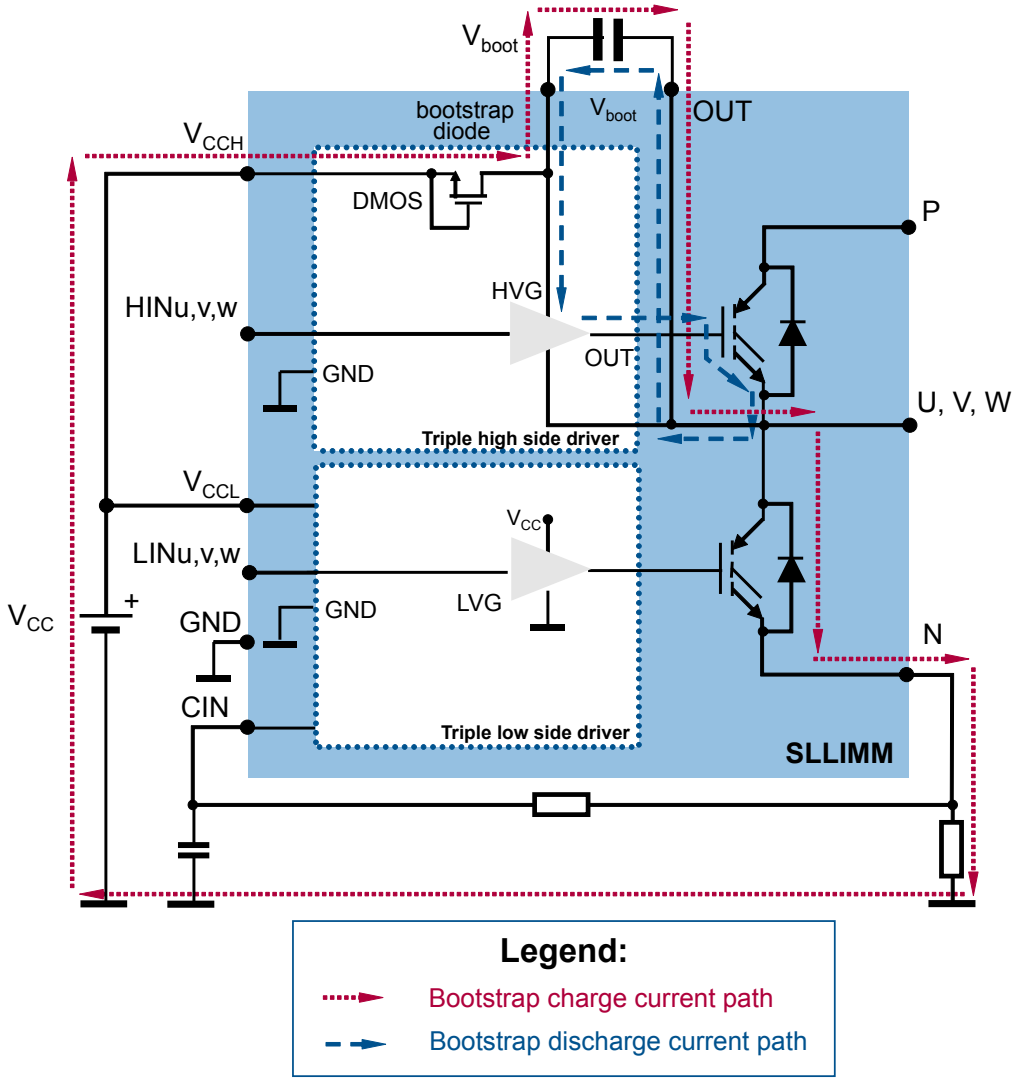
A bootstrap method is a simple and cheap solution to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode.

The SLLIMM family includes a patented integrated structure that replaces the external diode. It is realized with a high voltage DMOS working as a diode with a series resistor.

The new bootstrap diode structure used in the 2nd series offers further benefits compared to previous series. As it is no longer synchronized with its low-side input signal, the bootstrap capacitor can be recharged regardless of which LS IGBT is on and even during the low-side freewheeling recirculation phase. This avoids using the external bootstrap diode even in non-complementary switching schemes such as the 6-step modulation.

The operation of the bootstrap circuit is shown in the figure below. The floating supply capacitor C_{BOOT} is charged by the V_{CC} supply when V_{OUT} is lower than V_{CC} through the bootstrap diode and the DMOS path with reference to the “bootstrap charge current path”. During the high-side IGBT on phase, the bootstrap circuit provides the right gate voltage to properly drive the IGBT (see “bootstrap discharge current path”). This circuit is iterated for all the three half-bridges.

Figure 43. Bootstrap circuit



The value of the C_{BOOT} capacitor should be calculated according to the application condition and must take the following into account:

- The voltage across C_{BOOT} must be maintained at a value higher than the undervoltage lockout level (V_{BS_th}). This enables the high-side IGBT to work with the correct gate voltage (lower dissipation and better overall performances).
- The voltage across C_{BOOT} is affected by different components such as drops across the integrated bootstrap structure, drops across the low-side IGBT, and others.
- When the high-side IGBT is on, the C_{BOOT} capacitor discharges mainly to provide the right IGBT gate charge, but other phenomena must be considered such as leakage currents, quiescent current, etc.
- Bear in mind that if a voltage below the UVLO threshold is applied on the bootstrap channel, the HS gate driver disables its output without a fault signal.

2.3.11.1 *Bootstrap capacitor selection*

A simple method to properly size the bootstrap capacitor involves considering only the amount of charge that is needed when the high voltage side of the driver is floating and the IGBT gate is driven once. This approach takes neither the duty cycle of the PWM nor the fundamental frequency of the current into account. Observations regarding the PWM duty cycle, kind of modulation (6-step, 12-step and sine-wave) must be considered according to their individual specifics to achieve best bootstrap circuit sizing.

During the bootstrap capacitor charging phase, the low-side IGBT is on and the voltage across C_{BOOT} (V_{CBOOT}) can be calculated as follows:

Equation 14

$$V_{CBOOT} = V_{CC} - V_F - V_{DS(on)} - V_{CE(sat)\max}$$

Where:

- V_{CC}: supply voltage of gate driver
- V_F: bootstrap diode forward voltage drop
- $V_{CE(sat)max}$: maximum emitter collector voltage drop of low-side IGBT
- $V_{DS(on)}$: DMOS driving voltage drop

The magnitude of the bootstrap capacitance C_{BOOT} value is based on the minimum voltage drop (ΔV_{CBOOT}) to guarantee when the high-side IGBT is on, and must be:

Equation 15

$$\Delta V_{CBOOT} = V_{CC} - V_F - V_{DS(on)} - V_{GE}(\min) - V_{CE(sat)\max}$$

Under the condition:

Equation 16

$$V_{BOOT}(\min) > V_{BS\_thON}$$

Where:

- $V_{GE(min)}$: minimum gate emitter voltage of high-side IGBT
- V_{BS_thON}: bootstrap turn on undervoltage threshold (maximum value, see datasheet).

Considering the factors contributing to V_{CBOOT} decreasing, the total charge supplied by the bootstrap capacitor (during high-side on phase) is:

Equation 17

$$Q_{TOT} = Q_{GATE} + \left(I_{LKGE} + I_{QBO} + I_{LK} + I_{LKDiode} + I_{LKCap}\right) \cdot t_{Hon} + Q_{LS}$$

Where:

- Q_{GATE}: total IGBT gate charge
- I_{LKGE}: IGBT gate emitter leakage current
- I_{QBO}: bootstrap circuit quiescent current
- I_{LK}: bootstrap circuit leakage current
- $I_{LKDiode}$: bootstrap diode leakage current
- I_{LKCap}: bootstrap capacitor leakage current (relevant when using an electrolytic capacitor but can be ignored if other types of capacitors are used)
- t_{Hon}: high-side on time
- Q_{LS}: charge required by the internal level shifters

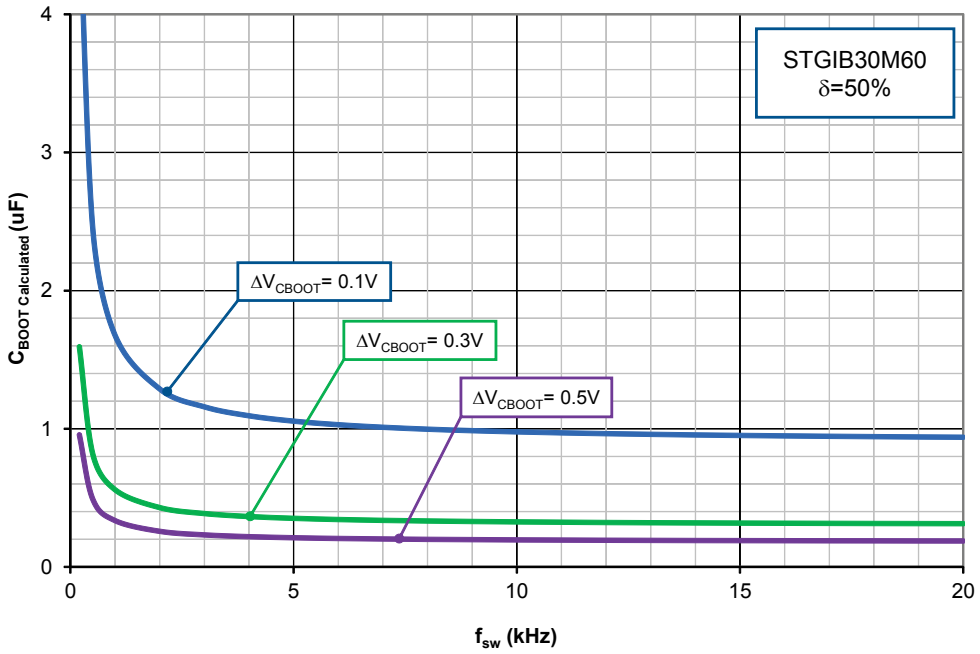
Finally, the minimum size of the bootstrap capacitor is:

Equation 18

$$C_{BOOT} = \frac{Q_{TOT}}{\Delta V_{CBOOT}}$$

To aid in the selection of the bootstrap capacitor, the figure below shows the behavior of C_{BOOT} (calculated) versus switching frequency (f_{sw}), with different values of ΔV_{CBOOT}, corresponding to Equation 18 for a continuous sinusoidal modulation and for STGIB30M60xy-z(worst case) and a duty cycle δ = 50%. For all the other devices, the bootstrap capacitor can be calculated using the same curve.

Figure 44. Bootstrap capacitor vs. switching frequency



Considering the extreme cases during PWM control and further leakage and dispersion in the board layout, the capacitance value for the bootstrap circuit should be two or three times higher than C_{BOOT} derived from Figure 44. Bootstrap capacitor vs. switching frequency. The bootstrap capacitor should have a low ESR value for good local decoupling; therefore, if an electrolytic capacitor is used, a parallel ceramic capacitor placed directly on the SLLIMM pins is highly recommended.

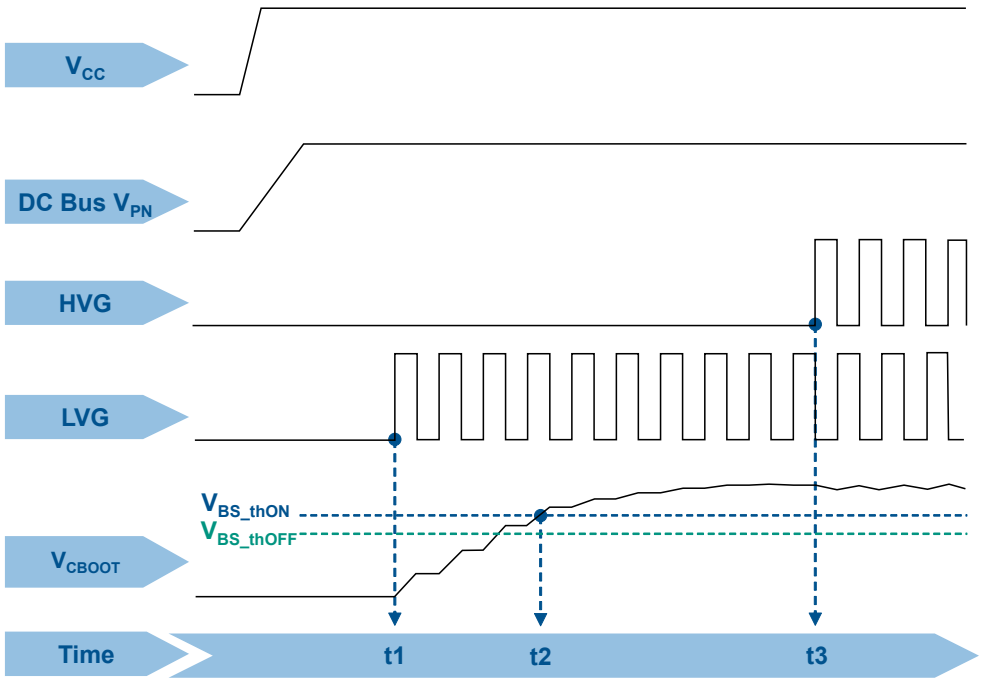
2.3.11.2 *Initial bootstrap capacitor charging*

During the startup phase, the bootstrap capacitor must be charged long enough to complete the initial charging time (t_{CHARGE}), which is at least the time V_{CBOOT} needs to exceed the turn-on undervoltage threshold V_{BS_thON}, as already stated in Equation 14.

For normal operation, the voltage across the bootstrap capacitor must never drop down to the turn-off undervoltage threshold V_{BS_thOFF}.

During startup, only the low-side IGBT is switched on and the PWM is run immediately after tgis phase, as shown by the sequence in the following figure.

Figure 45. **Initial bootstrap charging time**



The timing chart is based on the following steps:

- t1: the bootstrap capacitor starts to charge through the low-side IGBT (LVG)
- t2: the voltage across the bootstrap capacitor (V_{CBOOT}) reaches its turn-on undervoltage threshold V_{BS_thON}
- t3: the bootstrap capacitor is fully charged, this enables the high-side IGBT and the C_{BOOT} capacitor starts discharging in order to provide the right IGBT gate charge. The bootstrap capacitor recharges during the on state of the low-side IGBT (LVG).

The initial charging time is given by Equation 19 and must, for safety reasons, be at least three times longer than the calculated value.

Equation 19

$$t_{CHARGE} \geq \frac{C_{BOOT} \cdot R_{DS(on)}}{\delta} \cdot ln\left(\frac{V_{CC}}{\Delta V_{CBOOT}}\right)$$

Where δ is the duty cycle of the PWM signal and $R_{DS(on)}$ is 150 Ω typical value, as per the datasheet.

A practical example can be analyzed by considering a motor drive application where the PWM switching frequency is 12.5 kHz, with a duty cycle of 50%, and ΔV_{CBOOT} = 0.1 V (hence a gate driver supply voltage V_{CC} = 17.6 V). From the graph in Figure 44. Bootstrap capacitor vs. switching frequency, the bootstrap capacitance is 1.5 µF so C_{BOOT} can be chosen between 3.0 and 4.5 µF. We shall adopt the commercially available 3.3 µF capacitor.

From Equation 19, the initial charging time is:

Equation 20

$$t_{CHARGE} \geq \frac{3.3 \cdot 10^{-6} \cdot 150}{0.5} \cdot ln\left(\frac{17.6}{0.1}\right) = 5\ ms$$

For safety reasons, the initial charging time must be at least 15 ms.

2.3.12 Output safe clamp

Both HS and LS gate driver ICs are designed with an output safe clamp to guarantee the low impedance of the IGBT driving network (V_{LVG}, V_{HVG} = 1V @ I_{sink} = 10 mA, V_{CC} > 3 V) even in the shutdown condition. This feature guarantees the off state of the IGBT and avoids any undesired turning on due to the Miller effect, for example.

3 Package

The SLLIMM 2nd series benefits from a more compact package while providing high power density, the best thermal performance, and good electrical isolation (>1500 V_{RMS}).

The SDIP2x-26L is a dual-in-line transfer mold package available in two technology options: full molded type for an optimized cost/performance tradeoff and DBC (Direct Bonded Copper) type for best performance.

Both package technologies have the same physical size and are available in 26-lead versions (SDIP2F-26L, SDIP2B-26L) with or without an additional on board NTC thermistor. A vacuum soldering process is used to avoid the inclusion of any gas (voids) during the soldering process that could cause potential hot spots. This results in a further increase in the reliability of the SLLIMM family due to the improved thermal and electrical conductivity.

The full molded technology is oriented towards cost effectiveness and represents an ideal choice for low/medium power platforms.

The DBC technology allows extremely low thermal resistance values, high stability in thermal cycling and high quality.

All the versions are also available in two different configurations as short leads with emitter forward (suffix -E) and log leads (suffix -L).

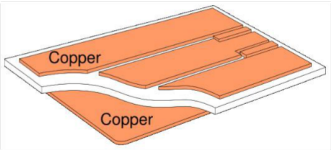
3.1 Full molded structure

The full molded package consists of a copper lead frame with power stage and control stage soldered on it and housed using the transfer molding process. The excellent thermal properties of the copper allows good heat spread and heat transfer, furthermore, the thickness of transfer mold resin and the layout of the lead frames has been optimized in order to further reduce the thermal resistance, while providing targeted electrical isolation level and overall reliable performance.

3.2 DBC structure

DBC stands for direct bonded copper, a process in which copper and a ceramic material are directly bonded, as shown in the figure below. Direct bonded copper substrates are a proven, high performance solution for the electrical isolation and thermal management of high power semiconductor modules.

Figure 46. DBC structure



The advantages of DBC substrates are:

- high current-carrying capability, due to thick copper metallization
- a thermal expansion coefficient close to the silicon value at the copper surface.

DBC has two layers of copper that are directly bonded onto an aluminum-oxide (Al_2O_3) ceramic base. The DBC process yields a super-thin base and eliminates the need for the thick, heavy copper bases used prior to this process.

Because SLLIMM with DBC bases has fewer layers, it has much lower thermal resistance values than those one based on different materials.

The main properties of DBC include:

- high mechanical strength
- mechanically stable dimensions

- good adhesion
- corrosion resistance
- excellent electrical isolation
- high thermal conductivity
- a thermal expansion coefficient similar to that of the silicon, so no interface layers are required
- good heat diffusion
- can be structured just like printed circuit boards or "IMS substrates"
- environmentally friendly

The DBC package consists of a DBC substrate for the power stage and a lead frame structure for the control stage, both housed using the transfer molding process.

Thanks to the new DBC substrate enhancement, the new SLLIMM 2nd series shows significant thermal resistance reduction up to 20% less than the SLLIMM 1st series. The following figure and corresponding table show an R_{th} comparison of SLLIMM 2nd series in DBC and full molded packages, and SLLIMM 1st series available only in DBC.

Figure 47. Thermal resistance comparison

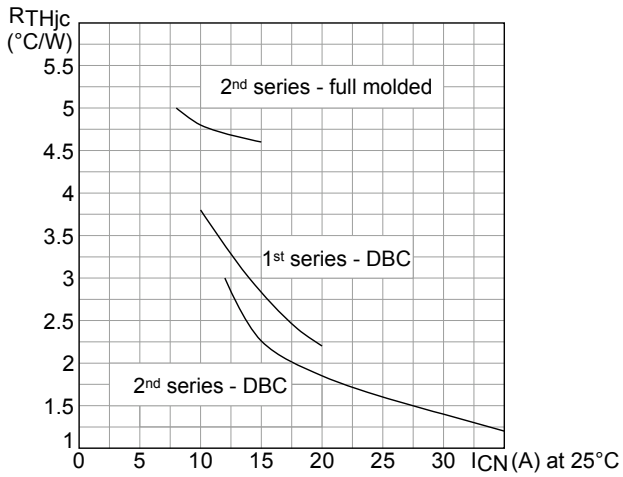


Table 12. $R_{th(j-c)}$ comparison

PN	SLLIMM series		I_{CN}	$R_{TH(J-C)}$ IGBT
STGIF5CH60x	2nd	FM	8 A	5.0 °C/W
STGIF7CH60x			10 A	4.8 °C/W
STGIF10CH60x			15 A	4.6 °C/W
STGIB8CH60x		DBC	12 A	3.0 °C/W
STGIB10CH60x			15 A	2.26 °C/W
STGIB15CH60x			20 A	1.85 °C/W
STGIB20M60x			25 A	1.40 °C/W
STGIB30M60x			35 A	1.20 °C/W

PN	SLLIMM series		I_{CN}	$R_{TH(J-C)}$ IGBT
STGIPS10K60	1st	DBC	10 A	3.8 °C/W
STGIPS14K60			14 A	3 °C/W
STGIPS20K60			18 A	2.4 °C/W
STGIPL20K60			20 A	2.2 °C/W

3.3 Package structure

The following two figures illustrate both the external internal structures of the SDIP2F-26L and SDIP2B-26L packages.

Figure 48. SDIP2F-26L external and internal representation

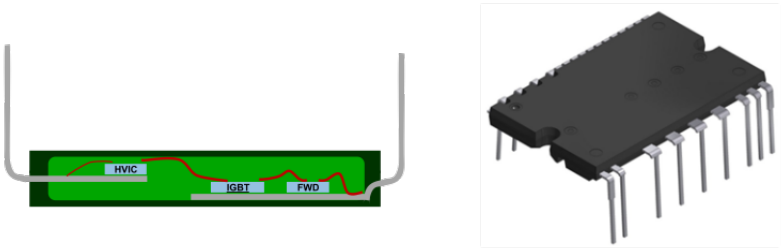
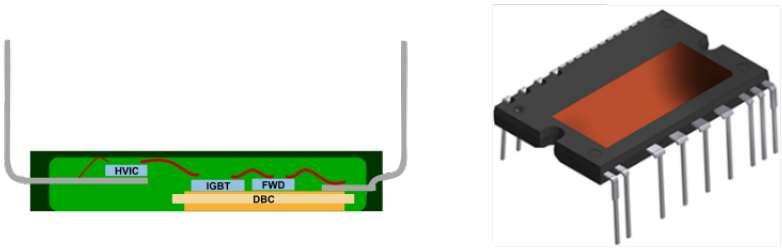
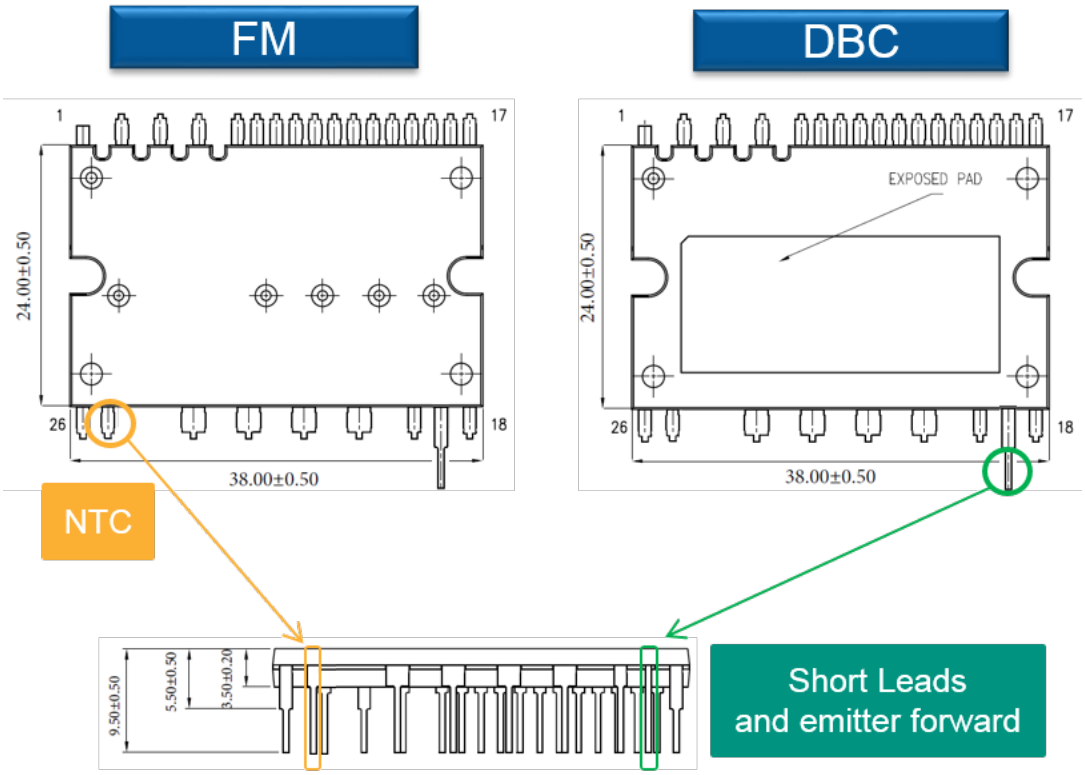


Figure 49. SDIP2B-26L external and internal representation



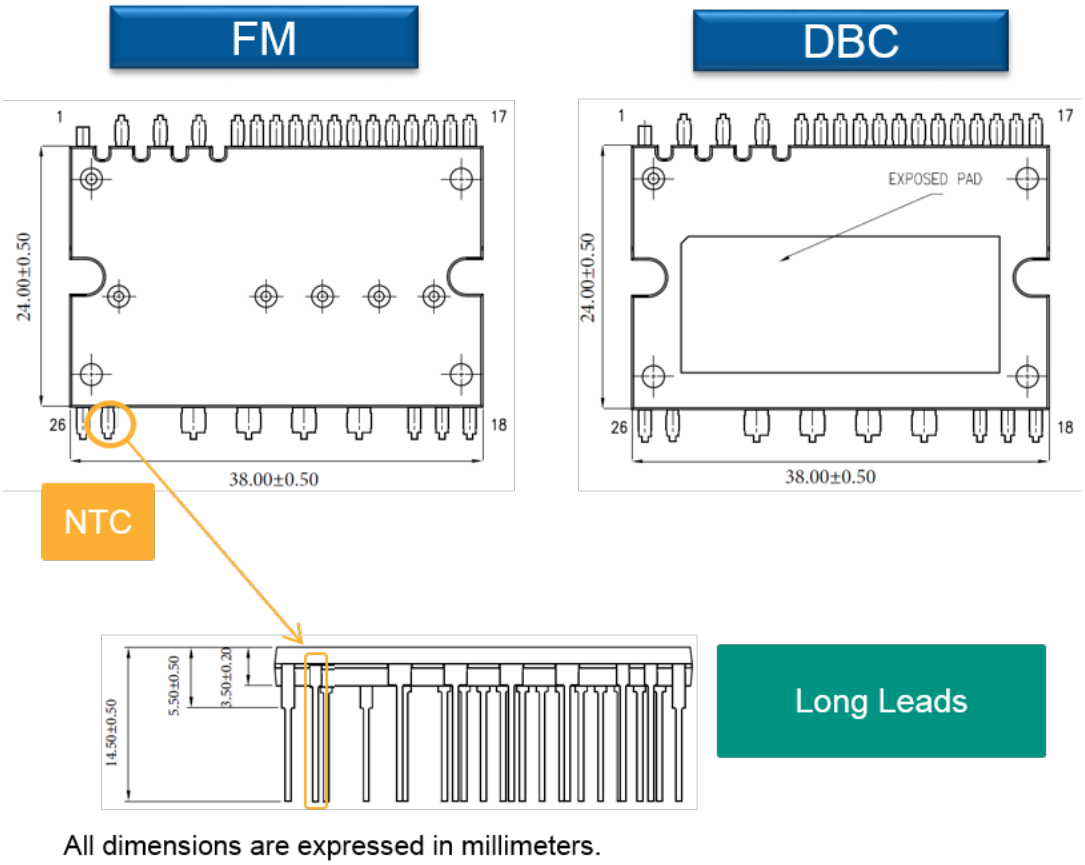
The following two figures show different package types in relation to lead length and emitter configuration of the SDIP2F-26L and SDIP2B-26L.

Figure 50. **SDIP2F-26L and SDIP2B-26L – short leads and emitter forward package**



All dimensions are expressed in millimeters.

Figure 51. **SDIP2F-26L and SDIP2B-26L – long leads package**



For further package outline details and dimensions, refer to the relevant datasheet.

3.4 Input and output pin descriptions

This section defines the SLLIMM 2nd series input and output pins. For a more accurate description and layout suggestions, please consult the relevant sections.

Table 13. **SDIP2x-25/26L input and output pins**

Pin	Name	Description
1	-	NC
2	VBOOTu	bootstrap voltage for U phase
3	VBOOTv	bootstrap voltage for V phase
4	VBOOTw	bootstrap voltage for W phase
5	HINu	high-side logic input for U phase
6	HINv	high-side logic input for V phase
7	HINw	high-side logic input for W phase
8	VCCH	high-side low voltage power supply
9	GND	Ground
10	LINu	low-side logic input for U phase

Pin	Name	Description
11	LINv	low-side logic input for V phase
12	LINw	low-side logic input for W phase
13	VCCL	Low-side low voltage power supply
14	SD	shutdown logic input (active low) / open-drain (comparator output)
15	CIN	comparator input
16	GND	Ground
17	TSO	temperature sensor output
18	NW	negative DC input for W phase
19	NV	negative DC input for V phase
20	NU	negative DC input for U phase
21	W	phase output
22	V	phase output
23	U	phase output
24	P	positive DC input
25	T2	NTC thermistor terminal 2 (STGIxyyCH60Tz and STGIByyM60Tz only)
	NC	NC only
26	T1	NTC thermistor terminal 1 (STGIxyyCH60Tz and STGIByyM60Tz only)
	NC	NC only

3.4.1 High-side bias voltage pins / high-side bias voltage reference

Pins: VBOOTu, VBOOTv, VBOOTw

- The bootstrap section is designed to facilitate a simple and efficient floating power supply, in order to provide the gate voltage signal to the high-side IGBTs.
- The SLLIMM family integrates the bootstrap diodes to save on cost, board space and number of components.
- The advantage of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
- Each bootstrap capacitor is charged from the V_{CC} supply.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.
- The size of the bootstrap capacitor is strictly related to the application conditions. See Section 2.3.11 Bootstrap circuit for more information.

3.4.2 Gate driver bias voltage

Pin: VCCH, VCCL

- Control supply pin for the built-in ICs.
- Separate supply.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to this pin.

3.4.3 Gate driver supply ground

Pin: GND

- Ground reference pin for the built-in ICs.
- Two pins internally connected
- To avoid being affected by noise, the main power circuit current should not be allowed to flow through this pin See Section 5.2 Layout suggestions.

3.4.4 Signal input

Pins: HINU, HINV, HINW; LINU, LINV, LINW;

- These pins control the operation of the built-in IGBTs.
- The signal logic of HINU, HINV, HINW, LINU, LINV, and LINW pins is active high. The IGBT associated with each of these pins is turned on when a sufficient logic (higher than a specific threshold) voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the SLLIMM against noise.

3.4.5 Internal comparator non-inverting

Pin: CIN

- The current sensing shunt resistor connected on each phase leg may be used by the internal comparator (pin CIN) to detect short-circuit current.
- The shunt resistor should be selected to meet the detection level requirements for the specific application.
- An RC filter (typically ~1us) should be connected to the CIN pin to eliminate noise.
- The connection length between the shunt resistor and CIN pin should be minimized.
- If a voltage signal higher than the specified V_{REF} (see datasheet) is applied to this pin, the SLLIMM automatically shuts down and the $\overline{SD}$ / OD pin is pulled down (to inform the microcontroller).

3.4.6 Shutdown / open-drain

Pin: $\overline{SD}$ / OD

- The $\overline{SD}$ / OD pin acts as an enable/disable pin.
- The signal logic of the $\overline{SD}$ / OD pin is active low. The SLLIMM shuts down if a voltage lower than a specific threshold is applied to this pin, leading each half bridge in tri-state.
- The $\overline{SD}$ / OD status is also connected to the internal comparator status (Section 2.3.5 Short-circuit protection and smart shutdown function). When the comparator triggers, the $\overline{SD}$ / OD pin is pulled down and acts as a FAULT pin.
- When pulled down by the comparator, the $\overline{SD}$ / OD pin is open drain configured. The $\overline{SD}$ / OD voltage should be pulled up to the 3.3 V or 5 V logic power supply through a pull-up resistor.

3.4.7 Thermistor

Pins: T1, T2

- A co-packaged NTC (optional) is available for temperature monitoring purposes.
- A simple voltage divider can be made with an external resistor in order to create a temperature-dependent voltage signal.
- The NTC is not able to sense rapid variations in IGBT junction temperature (due to the slow thermal dynamics).

3.4.8 Thermal sensor

Pin: TSO

- A voltage proportional to the temperature inside the package is available on the TSO pin. It does not need any pull down resistor. To improve noise immunity, a capacitor filter between 1 and 10 nF should be placed on this pin. When this function is not used, the TSO pin can be left floating.

3.4.9 Positive DC-link

Pin: P

- This is the DC-link positive power supply pin of the inverter and is internally connected to the collectors of the high-side IGBTs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a snubber capacitor close to this pin (typically, high voltage, metal film capacitors of about 0.1 or 0.22 µF).

3.4.10 Negative DC-link

Pins: NU, NV, NW

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of each phase.
- The power ground of the application should be separated from the logic ground of the system and reconnected at one specific point (star connection).

3.4.11 Inverter Power Output

Pins: U, V, W

- Inverter output pins for connection to the inverter load (e.g., motors).

4 Power loss and dissipation

The total power loss in an inverter derives from conduction losses, switching losses and off-state losses and is essentially generated by the power devices of the inverter stage, such as the IGBTs and the freewheeling diodes. The conduction losses (P_{cond}) are the on-state losses generated during the conduction phase. The switching losses (P_{sw}) are the dynamic losses encountered during turn-on and turn-off. Off-state losses deriving from blocking voltage and leakage current can be ignored.

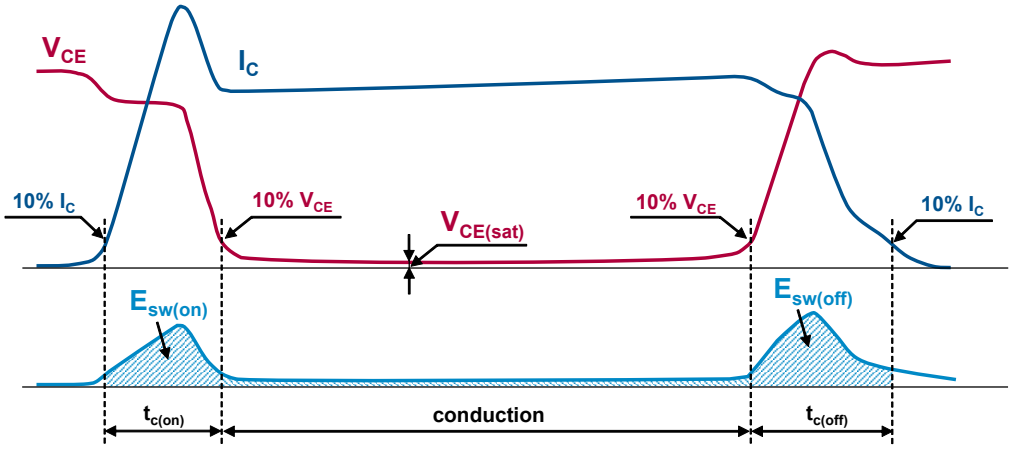
Total power loss is given by:

Equation 21

$$P_{tot} \approx P_{cond} + P_{sw}$$

The figure below shows a typical waveform and the major sources of power loss of an inductive hard switching application such as a motor drive.

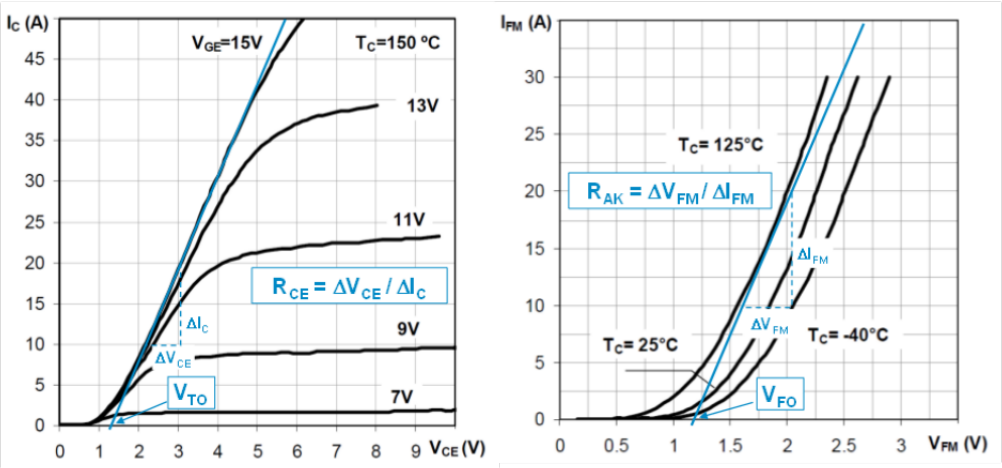
Figure 52. Typical IGBT power losses



4.1 Conduction power losses

Conduction losses are caused by IGBT and freewheeling diode forward voltage drops at rated currents. They can be calculated using a linear approximation of the forward characteristics for both IGBT and diode, in a series connection with a DC voltage source representing the threshold voltage, V_{TO} for IGBT, (and V_{FO} for diode) and a collector emitter on-state resistance, R_{CE} (and R_{AK} anode cathode on-state resistance), as shown in the figure below for reference purposes.

Figure 53. **IGBT and diode approximate output characteristics**



Both forward characteristics are temperature dependent, and so must be considered with respect to a specific temperature.

The linear approximations for IGBTs can be translated into the following equation:

Equation 22

$$v_{ce}(i_c) = V_{TO} + R_{CE} \cdot i_c$$

...and for freewheeling diodes:

Equation 23

$$v_{fm}(i_{fm}) = V_{FO} + R_{AK} \cdot i_{fm}$$

The conduction losses of IGBT and diode can be derived as the time integral of the product of conduction current and voltage across the devices, as such:

Equation 24

$$P_{cond\_IGBT} = \frac{1}{T}\int_0^T v_{ce} \cdot i_c(t)dt = \frac{1}{T}\int_0^T \left(V_{TO} \cdot i_c(t) + R_{ce} + i_c^2(t)\right)dt$$

Equation 25

$$P_{cond\_DIODE} = \frac{1}{T}\int_0^T v_f \cdot i_f(t)dt = \frac{1}{T}\int_0^T \left(V_{FO} \cdot i_f(t) + R_{AK} + i_f^2(t)\right)dt$$

Where T is the fundamental period.

As differing SLLIMM utilization modes, modulation techniques and operating conditions complicate power loss estimation, it is necessary to set some initial conditions.

Assuming that:

- the application is a variable voltage variable frequency (VVVF) inverter based on sinusoidal PWM technique.
- the switching frequency is high and therefore the output currents are sinusoidal
- the load is ideal inductive

Under these conditions, the output inverter current is given by:

Equation 26

$$i = \hat{I}cos(\theta - \phi)$$

Where Î is the current peak, θ represents ωt and ϕ is the phase angle between output voltage and current.

The conduction power losses can be obtained from:

Equation 27

$$P_{cond\_IGBT} = \frac{V_{TO} \cdot \hat{I}}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi\cos(\theta - \phi)d\theta + \frac{R_{CE} \cdot \hat{I}}{2\pi}\int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \xi cos^2(\theta - \phi)d\theta$$

Equation 28

$$P_{cond\_DIODE} = \frac{V_{FO} \cdot \hat{I}}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (1-\xi)\cos(\theta-\phi)d\theta + \frac{R_{AK} \cdot \hat{I}^2}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} \left(1-\xi\right)cos^2(\theta-\phi)d\theta$$

Where ξ is the duty cycle for this PWM technique given by:

Equation 29

$$\xi = \frac{1 + m_a \cdot cos\theta}{2}$$

Where m_a is the PWM amplitude modulation index.

Finally, solving for Equation 27 and Equation 28, we obtain:

Equation 30

$$P_{cond\_IGBT} = V_{TO} \cdot \hat{I}\left(\frac{1}{2\pi} + \frac{m_a \cdot cos\phi}{8}\right) + R_{CE} \cdot \hat{I}^2\left(\frac{1}{8} + \frac{m_a \cdot cos\phi}{3\pi}\right)$$

Equation 31

$$P_{cond\_DIODE} = V_{FO} \cdot \hat{I}\left(\frac{1}{2\pi} - \frac{m_a \cdot cos\phi}{8}\right) + R_{AK} \cdot \hat{I}^2\left(\frac{1}{8} - \frac{m_a \cdot cos\phi}{3\pi}\right)$$

and therefore, the conduction power loss for a single device (IGBT and diode) is:

Equation 32

$$P_{cond} = P_{cond\_IGBT} + P_{cond\_DIODE}$$

Of course, the total conduction loss for an inverter is six times this value.

4.2 Switching power losses

The switching loss is the power consumption during the turn-on and turn-off transients. As already shown in Figure 53. IGBT and diode approximate output characteristics, it is given by the pulse of power dissipated during turn-on (t_{on}) and turn-off (t_{off}).

Experimentally, it can be calculated by the time integral of the product of the collector current and collector-emitter voltage for the switching period. In any case, the dynamic performance is heavily dependent on several parameters including voltage, current temperature, so it is necessary to employ the same assumptions in Section 4.1 Conduction power losses to simplify the calculations.

Under these conditions, the switching energy losses are given by:

Equation 33

$$E_{on}(\theta) = \hat{E}_{on}\cos(\theta-\phi)$$

Equation 34

$$E_{off}(\theta) = \hat{E}_{off}\cos\left(\theta-\phi\right)$$

Where Êon and Êoff are the maximum values taken at T_{jmax} and $\hat{I}_C$, θ equals ωt and ϕ is the phase angle between output voltage and current.

Finally, the switching power loss per device depends on the switching frequency (f_{sw}) and is calculated as follows:

Equation 35

$$P_{sw} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}+\phi}^{\frac{\pi}{2}+\phi} (E_{IGBT} + E_{Diode}) \cdot f_{sw} d\theta = \frac{(E_{IGBT} + E_{Diode}) \cdot f_{sw}}{\pi}$$

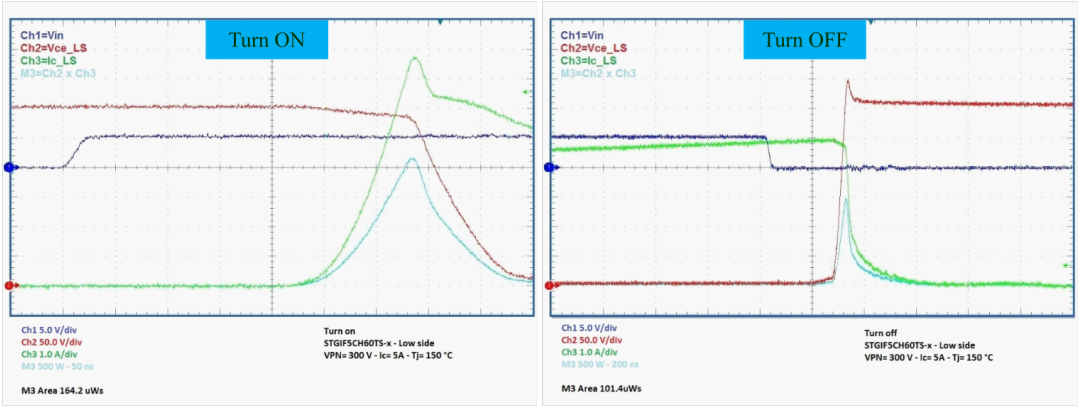
Where E_{IGBT} and E_{Diode} are the total switching energy for IGBT and freewheeling diode, respectively. Also in this case, the total switching loss per inverter is six times this value.

The figure below shows the real turn-on and turn-off waveforms of STGIF5CH60xy-z under the following conditions:

V_{PN} = 300 V, I_C = 5 A, T_j = 150 °C with inductive load on full bridge topology, taken on the low-side IGBT.

The light blue plots represent instantaneous power as the product of I_C (in green) and V_{CE} (in red) waveforms during the switching transitions. The areas under these plots are the switching energies computed by graphic integration thanks to the digital oscilloscope.

Figure 54. **STGIF5CH60xy-x typical switching waveforms**



Eon and Eoff are the areas below the light blue waveforms

4.3 Thermal impedance overview

During operation, power losses generate heat which elevates the temperature in the internal SLLIMM semiconductor junctions, limiting its performance and lifetime. To ensure safe and reliable operation, the junction temperature of power devices must be kept below the limits defined in the datasheet, therefore, the generated heat must be conducted away from the power chips and into the environment using an adequate cooling system.

The most common schemes are based on one heatsink designed for free conventional air flow or, in some cases, for forced air circulation. Free conventional air flow systems require larger heatsinks (about 50% bigger) than a forced air based heatsink, for a given thermal resistance. Therefore, the choice of the cooling system becomes the starting point for the application designer and the thermal aspect of the system is one of the key factors in designing high efficiency and high reliability equipment. In this respect, the package and its thermal resistance play a fundamental role.

Thermal resistance quantifies the ability of a given thermal path to transfer heat in the steady-state and is generally expressed as the ratio between the temperature increase above the reference and the relevant power flow:

Equation 36

$$R_{th} = \frac{\Delta T}{\Delta P}$$

The thermal resistance specified in the datasheet is the junction-case $R_{th(j\text{-}c)}$, defined as the temperature difference between the junction and case reference divided by the power dissipation per device:

Equation 37

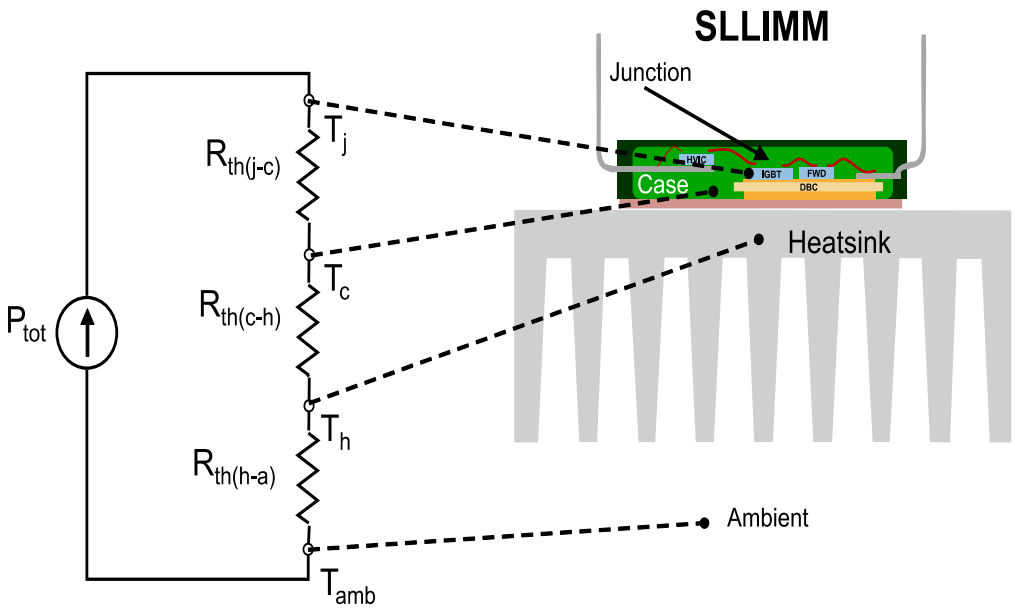
$$R_{th(j-c)} = \frac{T_j - T_c}{P_D}$$

The SLLIMM 2nd series (DBC package) benefits from a state of the art DBC substrate offering a very low $R_{th(j\text{-}c)}$ value. The backside of the DBC substrate and the full molded package are used as the cooling interface to the heatsink.

Thermal grease or some other thermal interface material between the backside and the heatsink is used to reduce the thermal resistance of the interface ($R_{th(c\text{-}h)}$) and, of course, depends on the material and its thickness.

Basically, the sum of the three thermal resistance components above gives the thermal resistance between junction and ambient $R_{th(j\text{-}a)}$, as shown in the figure below.

Figure 55. **Equivalent thermal circuit with heatsink single IGBT**



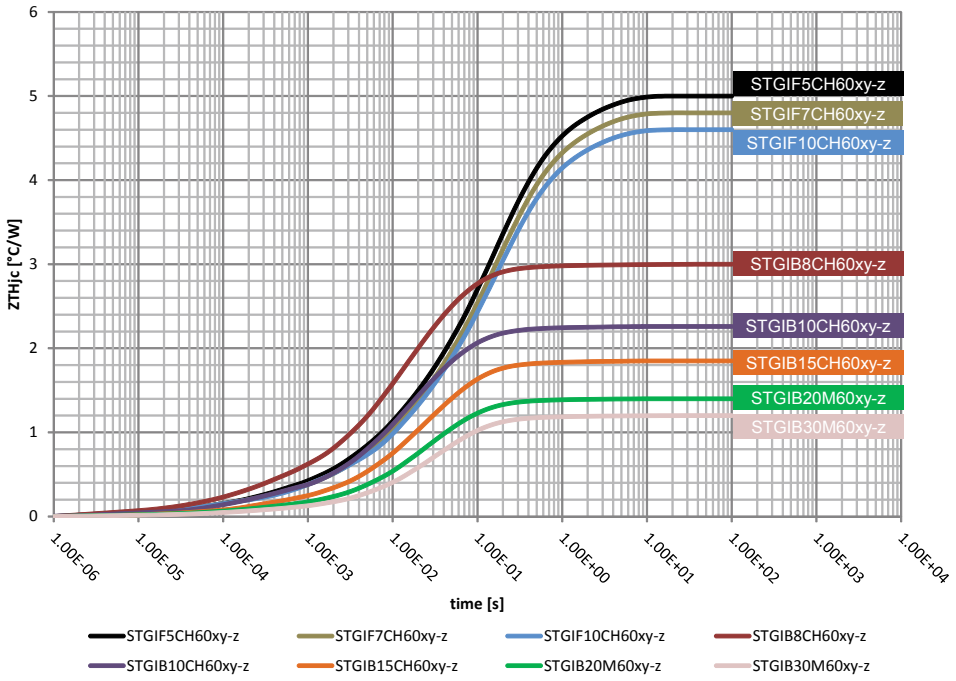
As the power loss P_{tot} is cyclic, the transient thermal impedance must also be considered. It is defined as the ratio of the time dependent temperature increase ΔT(t) above the reference and the relevant heat flow:

Equation 38

$$Z_{th}(t) = \frac{\Delta T(t)}{\Delta P}$$

Contrary to what we have already seen regarding thermal resistance, thermal impedance is typically represented by an RC equivalent circuit. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature and therefore the advantage of this behavior is the short-term overload capability of the SLLIMM.

Figure 56. **Thermal impedance curves**



More generally, in the case of the device, power is time dependent too. The device temperature can be calculated via the convolution integral method applied to the following equation thus:

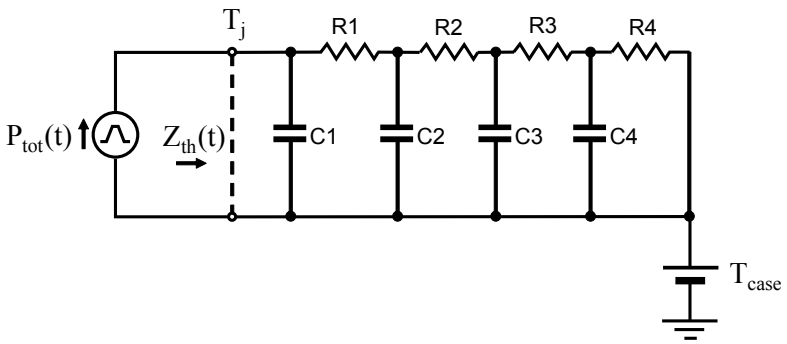
Equation 39

$$\Delta T(t) = \int_0^t Z_{th}(t-\tau) \cdot P(\tau) d\tau$$

An alternative and very useful method for simulator tools, is the transient thermal impedance model, which provides a simple method for estimating the junction temperature rise under a transient condition.

By using the thermo-electrical analogy, the transient thermal impedance Zth(t) can be transformed into an electrical equivalent RC network. The number of RC sections increases the model detail, therefore a fourth order model based on the Cauer network has been adopted to improve the accuracy of the model, as shown in the figure below.

Figure 57. **Thermal impedance RC Cauer thermal network**



Temperatures inside the electrical RC network represent voltages, power flows represent currents, electrical resistances and capacitances represent thermal resistances and capacitances respectively. The case temperature is represented with a DC voltage source and can be interpreted as the initial junction temperature.

Transient thermal impedance models are derived by curve fitting an equation to the measured data. Values for the individual resistors and capacitors are the variables from this equation and are defined for each device in the table below.

Table 14. RC Cauer thermal network elements by device

Element	STGIF5CH60	STGIF7CH60	STGIF10CH60	STGIB8CH60	STGIB10CH60	STGIB15CH60	STGIB20M60	STGIB30M60
R1 (°C/W)	0.11	0.15	0.11	0.125	0.097	0.07112	0.055	0.048
R2 (°C/W)	0.55	0.55	0.50	0.315	0.24	0.1752	0.149	0.110
R3 (°C/W)	2.8	2.2	2.09	1.196	1.04	0.824	0.526	0.447
R4 (°C/W)	1.54	1.9	1.90	1.365	0.878	0.7696	0.643	0.571
C1 (W·s/°C)	1.50E-04	2.20E-04	3.50E-04	1.05E-04	2.46E-04	3.93E-04	4.06E-04	5.54E-04
C2 (W·s/°C)	1.70E-03	2.80E-03	2.80E-03	4.07E-04	8.79E-04	2.34E-03	3.63E-03	5.68E-03
C3 (W·s/°C)	1.60E-02	2.20E-02	2.20E-02	3.05E-03	5.86E-03	6.93E-03	1.08E-02	1.43E-02
C4 (W·s/°C)	5.10E-01	3.00E-01	2.00E-01	2.96E-02	4.85E-02	7.70E-01	6.89E-02	8.70E-02

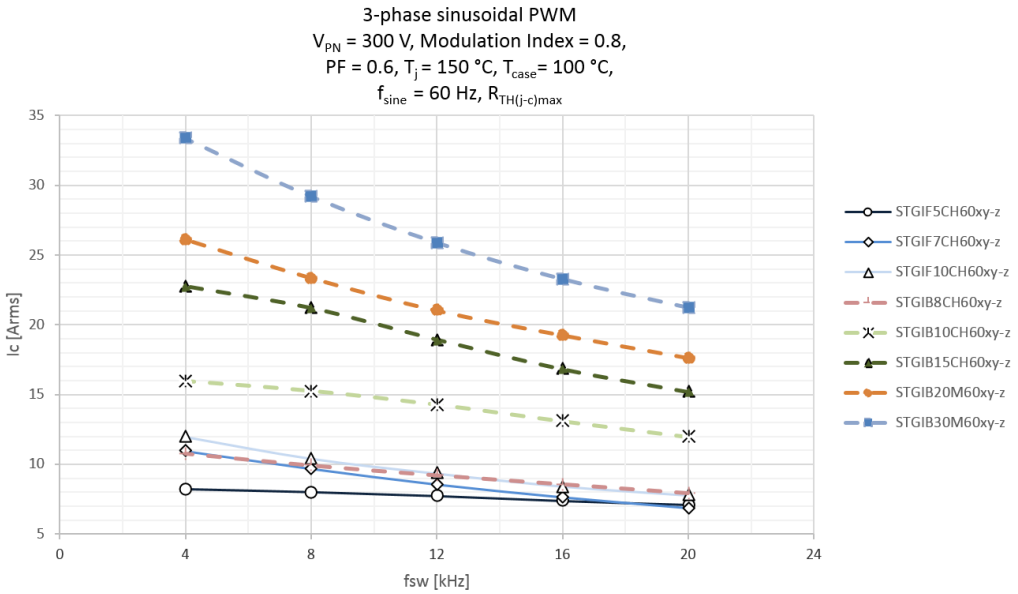
4.4 Power loss calculation example

From the power loss calculation and thermal aspects detailed in the previous sections, we can simulate the maximum $I_{C(RMS)}$ current versus switching frequency curves for an inverter using a 3-phase continuous PWM modulation to synthesize sinusoidal output currents.

The curves in Figure 58. Maximum $I_{C(RMS)}$ current vs. f_{sw} simulated curves represent the maximum current managed by the SLLIMM under safe conditions, when the junction temperature rises to 50 °C (maintaining a good margin from the 175 °C maximum junction temperature for SLLIMM 2nd) and the case temperature is 100 °C, which is a typical operating condition to guarantee the reliability of the system.

These curves, functions of the motor drive typology and control scheme, are simulated under the conditions reported in the figure below, with typical power loss.

Figure 58. Maximum $I_{C(RMS)}$ current vs. f_{sw} simulated curves



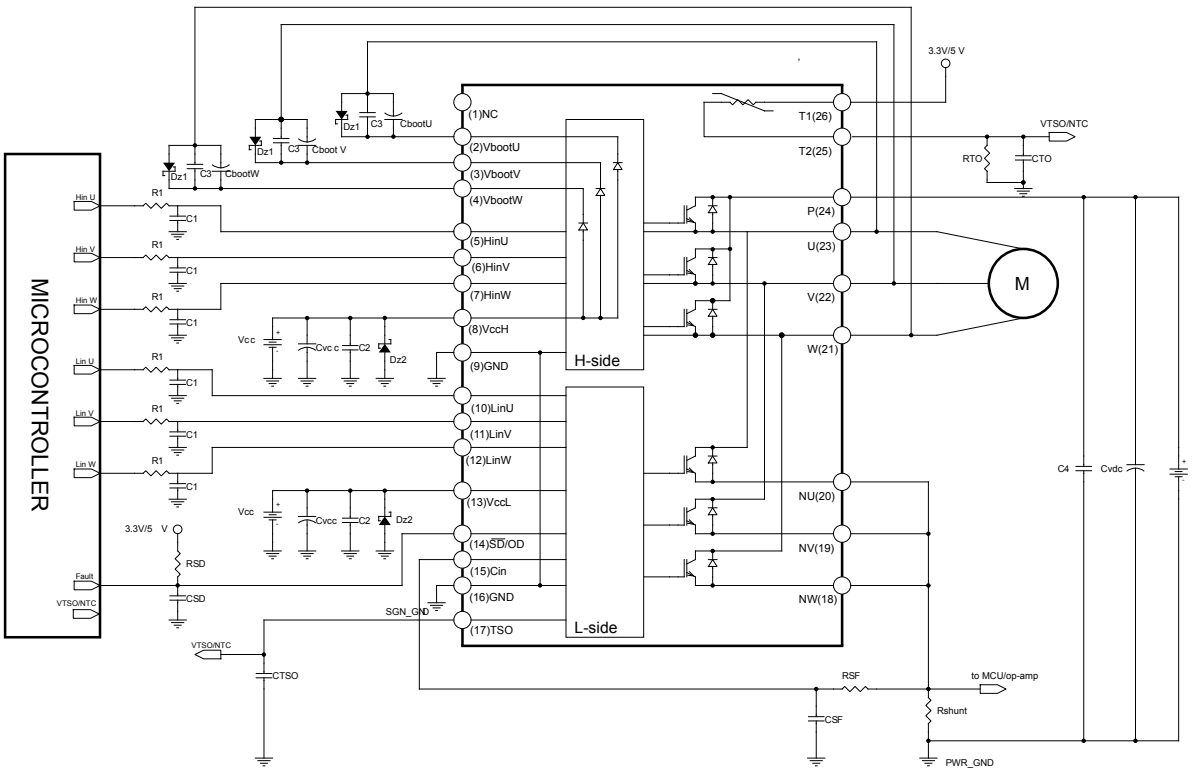
5 Design and mounting guidelines

This section provides suggestions regarding typical circuits, optimized design layouts and important mounting recommendations to aid in the appropriate handling and assembly of the SLLIMM 2nd series family.

5.1 Typical circuit and recommendations

The figure below shows a typical application circuit using SLLIMM 2nd series with signal interfaces with the MCU.

Figure 59. Typical application circuit



Below are some hardware and PCB layout recommendations:

1. Input signals HIN, LIN are active-high logic. A 100 kΩ (typ.) pull-down resistor is built-in for each input pin. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R_1, C_1) on each input signal is suggested. The filters should be done with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
2. The use of a bypass capacitor C_{VCC} (aluminum or tantalum) can help reduce the transient circuit demand on the power supply. Also, to reduce high frequency switching noise distributed on the power lines, placing a decoupling capacitor C_2 (100 to 220 nF, with low ESR and low ESL) as close as possible to each Vcc pin and in parallel with the bypass capacitor is suggested.
3. The use of RC filter (R_{SF}, C_{SF}) for preventing protection circuit malfunction is recommended. The time constant (R_{SF} x C_{SF}) should be set to 1 µs and the filter must be placed as close as possible to the CIN pin.
4. The $\overline{SD}$ is an input/output pin (open-drain type if used as output). It is recommended that it be pulled up to a power supply (i.e., MCU bias at 3.3/5 V) by a resistor value able to keep the I_{od} no higher than 5 mA (V_{OD} ≤ 500 mV when open-drain MOSFET is ON). The filter on $\overline{SD}$ should be sized to get a desired re-starting time after a fault event and placed as close as possible to the $\overline{SD}$ pin.

5. A decoupling capacitor C_{TSO} between 1 nF and 10 nF can be used to increase the noise immunity of the TSO thermal sensor; a similar decoupling capacitor C_{OT} (between 10 nF and 100 nF) can be implemented if the NTC thermistor is available and used. In both cases, their effectiveness is improved if the capacitors are placed close to the MCU.
6. The decoupling capacitor C_3 (100 to 220 nF with low ESR and low ESL) in parallel with each C_{boot} is useful to filter high frequency disturbances. Both C_{boot} and C_3 (if present) should be placed as close as possible to the U,V,W and V_{boot} pins. Bootstrap negative electrodes should be connected to U,V,W terminals directly and separated from the main output wires.
7. To prevent overvoltage on the V_{CC} pin, a Zener diode (D_{z1}) can be used. Similarly on the V boot pin, a Zener diode(D_{z2}) can be placed in parallel with each C_{boot} .
8. The use of the decoupling capacitor C_4 (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor C_{vdc} is useful to prevent surge destruction. Both capacitors C_4 and C_{vdc} should be placed as close as possible to the IPM (C_4 has priority over C_{vdc}).
9. By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an opto-coupler is possible.
10. Low inductance shunt resistors should be used for phase leg current sensing.
11. In order to avoid malfunction, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
12. The connection of SGN_GND to PWR_GND at only one point (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.

5.2 Layout suggestions

PCB layout optimization for high voltage, high current and high switching frequency applications is a critical factor. PCB layout is a complex matter involving several aspects such as track length and width and circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application function properly and achieve expected performance. On the other hand, PCBs without careful layout can generate EMI issues (both induced and perceived by the application), can provide overvoltage spikes due to parasitic inductances along the PCB traces, and can produce higher power loss and even malfunction in the control and sensing stages.

The compactness of the SLLIMM solution, which offers an optimized gate driving network and reduced parasitic elements, allows designers to concentrate on other issues such as the ground or noise filter. In any case, to avoid the aforementioned conditions, the following general PCB layout guidelines and suggestions should be followed for 3-phase applications.

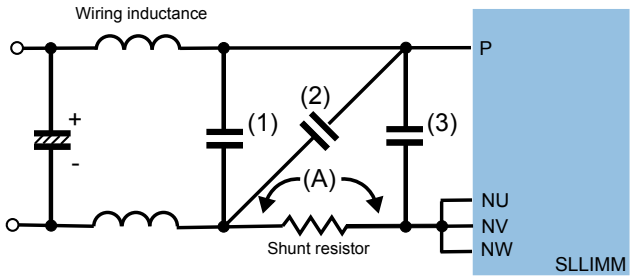
For more information please refer to application note AN4694.

5.3 General suggestions

1. PCB traces should be designed as short as possible and the area of the circuit (power or signal) minimized to reduce the sensitivity of such structures to surrounding noise.
2. Ensure a good distance between switching lines with high voltage transitions and the signal lines sensitive to electrical noise. Specifically, the tracks of each OUT phase carrying significant currents and voltages should be separated from logic lines and analog op amp and comparator sensing circuits.
3. Place the R_{SENSE} resistors as close as possible to the low-side pins of the SLLIMM (NU, NV and NW). Parasitic inductance can be minimized by connecting the ground line (also called driver ground) of the SLLIMM directly to the cold terminal of sense resistors. Use a low inductance type resistor, such as an SMD resistor instead of long-lead type resistors, to help further decrease parasitic inductance. The total parasitic inductance (including the shunt resistor) should be lower than 15 nH.
4. Avoid any ground loop. Only a single path must connect two different ground nodes.
5. Place each RC filter as close as possible to the SLLIMM pins in order to increase their efficiency.
6. Fixed voltage tracks such as GND or HV lines can be used to shield the logic and analog lines from electrical noise produced by the switching lines (e.g., OUTu, OUTv and OUTw).

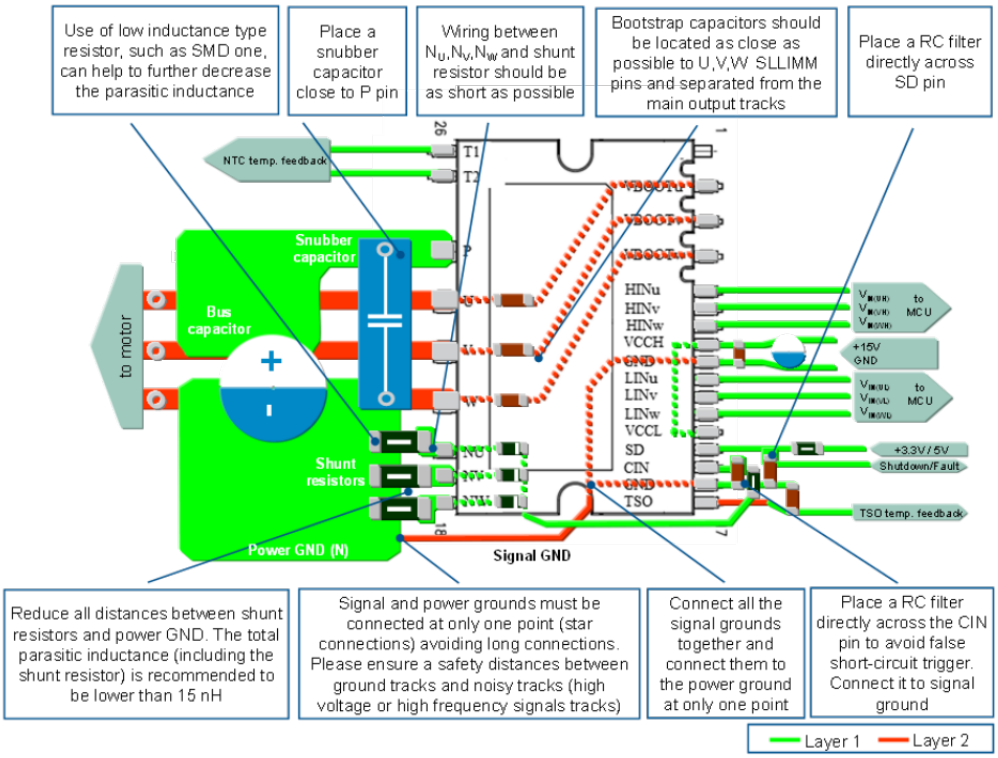
7. Generally, it is recommended to connect each half bridge ground in a star configuration and the three R_{SENSE} very close to each other and to the power ground.
8. In order to prevent surge destruction, the wiring between the snubber capacitor and the P N pins should be as short as possible. The use of a high frequency, high voltage non-inductive capacitor of about 0.1 or 0.22 µF is recommended. In order to effectively suppress the surge voltage, the snubber capacitor has to be placed in position (2) in Figure 60. Recommended snubber capacitor position. The position (1) is incorrect for effective surge voltage suppression. If the capacitor is placed on the position (3), the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor with possible undesired protection activation, even if the surge suppression effect is the greatest. Finally, position (2) is the right compromise. The parasitic inductance on the A tracks (including that of the shunt resistor) should be as small as possible in order to suppress the surge voltage.

Figure 60. Recommended snubber capacitor position



The general suggestions for all SLLIMM products are summarized in the following figure.

Figure 61. PCB layout general suggestions



6 Mounting and handling instructions

Some basic assembly rules must be followed in order to limit thermal and mechanical stress and optimize the thermal conduction and electrical isolation for both SDIP2F-26L and SDIP2B-26L packages when mounting a heatsink.

Moreover, semiconductors are normally electrostatic discharge sensitive devices (ESDS) requiring specific precautionary measures regarding handling and processing. Static discharges caused by human touch or by processing tools may cause high-current and/or high-voltage pulses which may damage or even destroy sensitive semiconductor structures. Integrated circuits (ICs) may also be charged by static during processing. If discharging takes place too quickly (“hard” discharge), it may cause peak loads and consequent damage.

Make careful choices regarding workspaces, personal equipment and processing and assembly equipment.

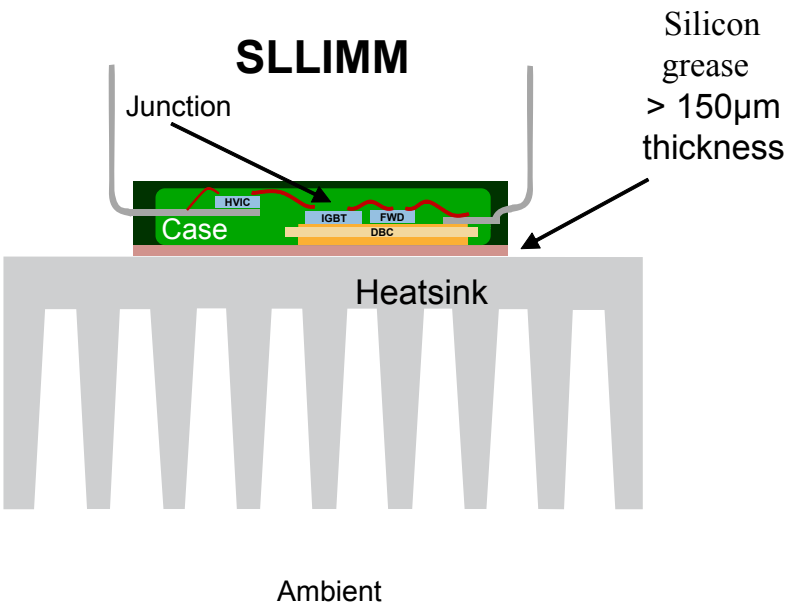
6.1 Heatsink mounting

When attaching a heatsink to a SLLIMM, do not apply excessive force to the device for assembly. Drill holes for screws in the heatsink exactly as specified. Smooth the surface by removing burrs and protrusions Do not touch the heat-sink when the SLLIMM is operational to avoid burn injury.

To get the most effective heat dissipation, enlarge the contact area as much as possible to minimize the contact thermal resistance. Properly apply thermal-conductive grease over the contact surface between modules and heatsinks, is also useful for preventing contact surfaces from corrosion. Apply a minimum 150 µm layer of thermal grease to the module base plate or to the heatsink, as shown in Figure 62. Recommended silicon grease thickness and positioning. Use a torque screwdriver to fasten up to the max specified torque rating. Exceeding the maximum torque may lead to module damage or degradation. Remove any dirt from the contact surface.

Ensure the grease quality remains constant over time and is able to perform long-term over a wide operating temperature range.

Figure 62. Recommended silicon grease thickness and positioning



6.1.1 Mounting torque

Mounting torque and heatsink flatness specifies the correct fastening torque. Inappropriate mounting can damage the device and over tightening the screws may cause DBC substrate or molding compound cracks. Avoid mechanical stress due to tightening on one side only. It is recommended to first lightly fasten both screws fastening them permanently to the specified torque value with a torque wrench.

Table 15. Mounting torque and heatsink flatness

Item	Condition		Min.	Typ.	Max.	Unit
Mounting torque	Mounting screw: M3	Recommended 0.55 N•m	0.40	0.55	0.70	N•m
Device flatness	See Figure 63. Device flatness specification		0		150	µm
Heatsink flatness	See Figure 64. Heatsink flatness specification		-50		100	µm

The following two figures provide device and heatsink flatness details, respectively.

Figure 63. Device flatness specification

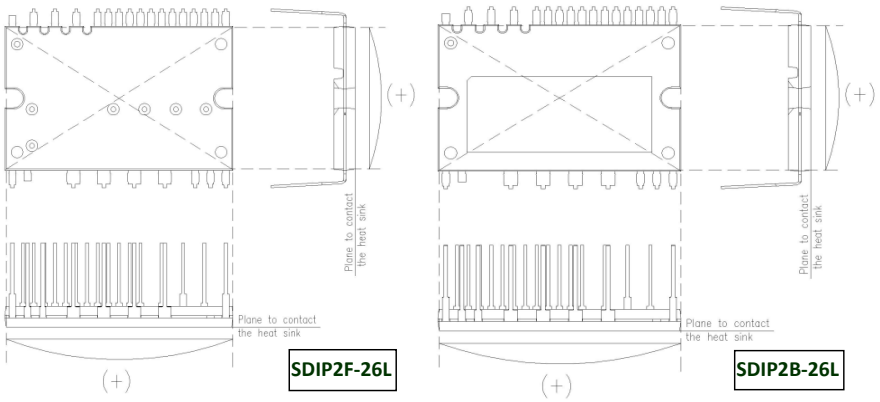
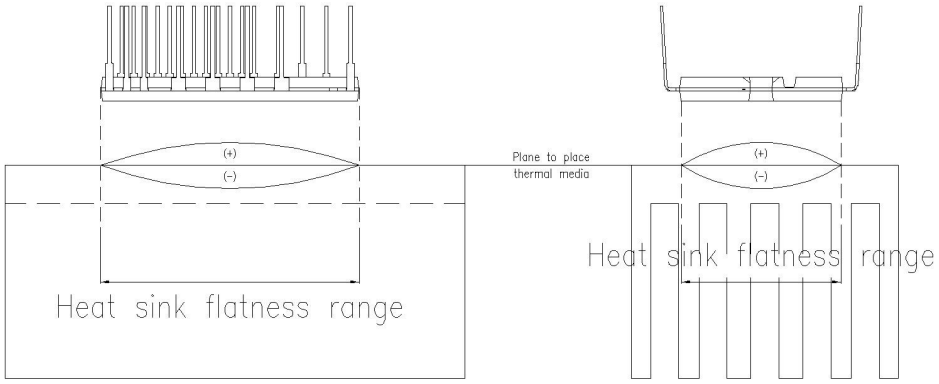


Figure 64. Heatsink flatness specification



Do not exceed the specified fastening torque. Over tightening the screws may cause ceramic or molding compound cracks and heat-fin threaded hole destruction.

Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance.

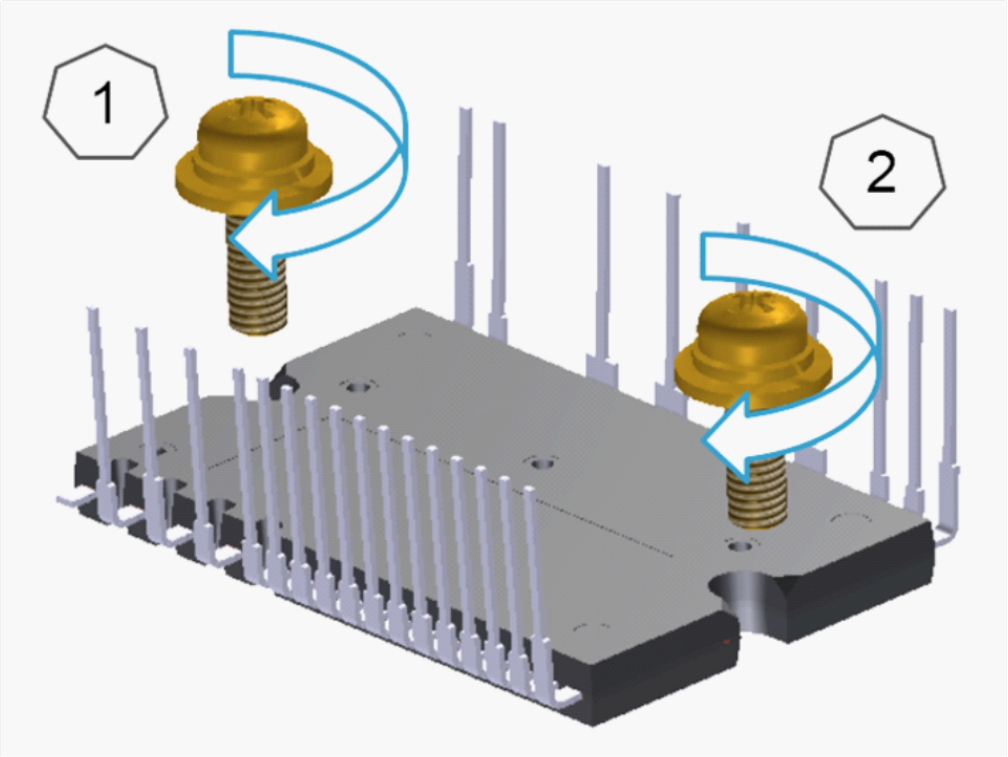
Figure 65. Recommended mounting screw fastening sequence shows the recommended fastening sequence for mounting screws. ST recommends temporarily tightening mounting screws with the fixing torque set at 0.1/0.2 Nm and then permanently screwing them with a torque 0.55 Nm (0.70 Nm max.) crosswise.

1. Fasten temporarily in the sequence 1 → 2

2. Screw down permanently in the sequence 1 → 2

When using electrical or pneumatic screwdrivers, ST suggests limiting the revolution to 200 rpm as the rapid impact of the screw may damage the module plastic body.

Figure 65. Recommended mounting screw fastening sequence



Many other precautions regarding handling and contamination, ESD, storage, transportation and soldering should be considered, and further details are available in technical note TN1220.

7 Motor control power board based on the ST SLLIMM 2nd series

The STEVAL-IPMnmx interface demo board is a reference design compact motor drive power board based on the full SLLIMM 2nd series product portfolio.

It provides an easy-to-use solution for driving high power motors for a wide range of applications such as domestic appliances, air conditioning, compressors, power fans, high-end power tools and generally, 3-phase inverters for motor drives.

The main characteristics of this evaluation board are small size, minimal BOM list and easily testable and scalable. It consists of an interface circuit (BUS and VCC connectors), bootstrap capacitors, snubber capacitor, hardware short-circuit protection, fault event signal and temperature monitoring. In order to increase flexibility, it is designed to work in single or three shunt configurations and with double current sensing options such as three dedicated op-amps onboard or op-amps embedded on the MCU. The Hall/encoder part completes the circuit.

Thanks to these advanced characteristics, the system has been specially designed to achieve accurate and fast conditioning of the current feedback, matching the typical requirements for field oriented control (FOC).

The STEVAL-IPMnmx is compatible with ST's control board based on STM32, so as to provide a complete platform for motor control.

Features:

- input voltage: 125 to 400 VDC
- nominal power: up to 3000 W (1)
- input auxiliary voltage: up to 20V DC
- single- or three-shunt resistors for current sensing (with sensing network)
- two options for current sensing: dedicated op-amps or through MCU
- overcurrent hardware protection
- IPM temperature monitoring and protection
- Hall sensor or encoder input
- scalable for the whole SLLIMM 2nd series product portfolio
- motor control connector (32pins) interfacing with ST MCU boards
- universal conception for further evaluation with bread board and testing pins
- very compact size

1. *Board extension on going*

The following table shows the order code for the power board equipped with STGIF5CH60xy-z.

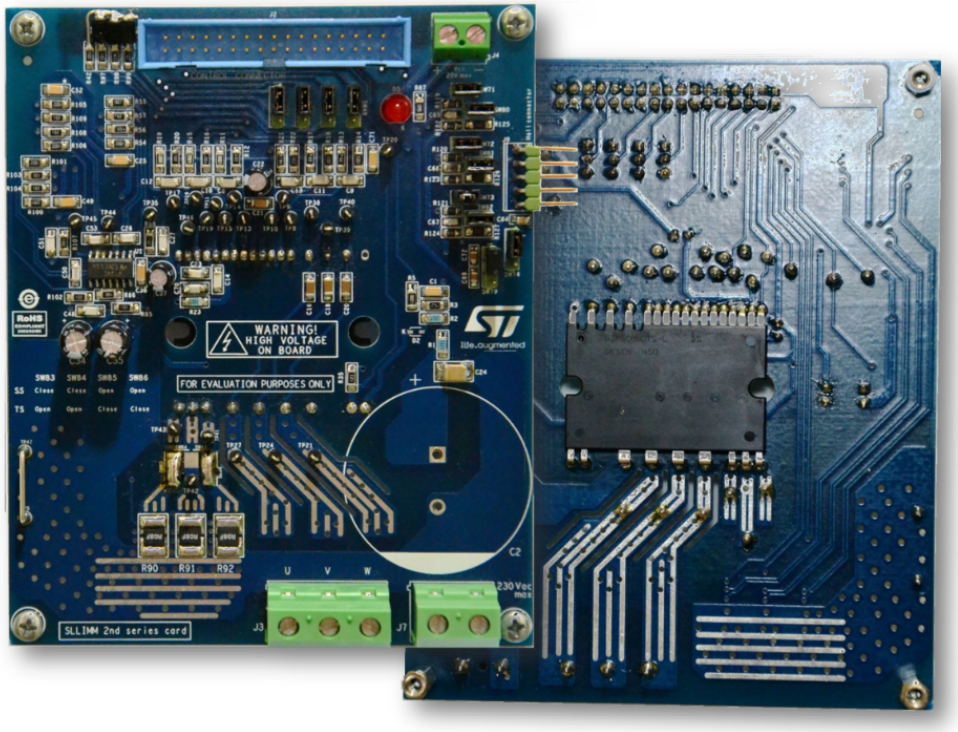
Table 16. SLLIMM 2nd series power board order code

Reference	STEVAL-IPMnmx(1)		
SLLIMM mounted	n	m	x
STGIF5CH60xy-z	0	5	F
STGIF7CH60xy-z	0	7	F
STGIF10CH60xy-z	1	0	F
STGIB8CH60xy-z	0	8	B
STGIB10CH60xy-z	1	0	B
STGIB15CH60xy-z	1	5	B

1. *Board extension on going*

The following figure shows a top and bottom view of STEVAL-IPM05F mounting the full molded package STGIF5CH60xy-z, for 700 W power level applications.

Figure 66. Top and bottom view of STEVAL-IPM05F



8 References

STGIF5CH60xy-z datasheet
STGIF7CH60xy-z datasheet
STGIF10CH60xy-z datasheet
STGIB8CH60xy-z datasheet
STGIB10CH60xy-z datasheet
STGIB15CH60xy-z datasheet
STGIB20M60xy-z datasheet
STGIB30M60xy-z datasheet
STEVAL-IPM05F evaluation board
STEVAL-IPM07F evaluation board
STEVAL-IPM10F evaluation board
STEVAL-IPM08B evaluation board
STEVAL-IPM10B evaluation board
STEVAL-IPM15B evaluation board
AN3338 – “SLLIMM”
AN4694 – “EMC design guides for motor control applications”
TN1220 – “Mounting instruction for SLLIMM™ 2nd series”

Revision history

Table 17. **Document revision history**

Date	Revision	Changes
22-Oct-2015	1	First release.
30-Oct-2015	2	In Undervoltage lockout: - Timing chart of undervoltage lockout function on low-side section and relevant steps below figure. In Motor control power board based on the ST SLLIMM 2nd series: - changed text "...STGIF5CH60xy-z, for 500 W power level applications..." to "...STGIF5CH60xy-z, for 700 W power level applications..."
09-Jan-2017	3	Minor text and formatting changes throughout document. Added text content between F*igure 5: "Stray inductance components of output stage"* and *Table 6: "Control part of STGIF5CH60xy-z"* Added *Section 1.5: "SCSOA"* In *Section 2.3.5: "Short-circuit protection and smart shutdown function"* - added sentence: "If the short-circuit is present during restart..." and corresponding note. - updated *Figure 18: "Smart shutdown equivalent circuitry"* Updated *Figure 19: "Timing chart of smart shutdown function"* and *corresponding descriptions for t1 to t7* Updated *Figure 22: "Smart shutdown operation"*, *Figure 25: "SD duration for OC event"*, *Figure 32: "Thermal sensor voltage vs temperature"*, *Figure 35: "NTC resistance vs temperature"*, *Figure 36: "NTC resistance vs temperature – zoom"* Added *Figure 38: "VNTC vs temperature (pull up configuration)"* and *Figure 39: "VNTC vs temperature (pull down configuration)"* Updated *Figure 47: "SDIP2F-26L and SDIP2B-26L – short leads* and *emitter forward package"* and *Figure 48: "SDIP2F-26L and SDIP2B-26L – long leads package"* Updated *Equation 29* In *Section 5.1: "Typical circuit and recommendations"* - updated point 1 In *Section 5.3: "General suggestions"* - updated point 8 Updated *Table 16: "SLLIMM 2nd series power board order code"*

Date	Revision	Changes
17-May-2018	4	Updated Section "Introduction" (delete note a). Updated curves in Section 1.5 SCSOAand Table 1. SLLIMM 1st and 2nd series differences. Updated Section 1.2 Product line-up and nomenclature and Table 4. Synoptic table for DBC package option. Updated Section 1.3 Internal circuit and Section 2.1 IGBTs section. Updated Section 2.3.5 Short-circuit protection and smart shutdown function. Updated Table 10. SD duration time per event and Section 2.3.9 Fault management. Updated Section 2.3.10 Temperature monitoring and Figure 1. Updated Figure 47. Thermal resistance comparison and Table 12. $R_{th(j-c)}$ comparison. Updated Table 13. SDIP2x-25/26L input and output pins Updated Figure 2 and Table 2. Updated Figure 58. Maximum $I_{C(RMS)}$ current vs. f_{sw} simulated curves. Updated Table 16. SLLIMM 2nd series power board order code. Updated Section 8 References. Minor text and formatting changes throughout document.

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