AN4829
Application note

Fishbone diagrams for a forward converter

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Introduction

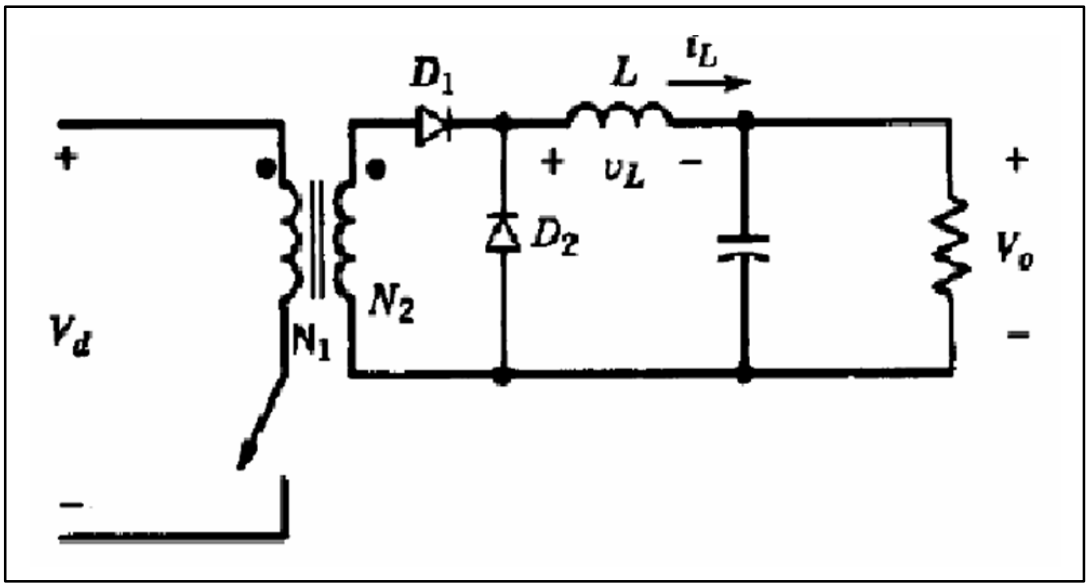
The purpose of this application note is to highlight all of the critical conditions affecting power MOSFET devices when they are used as switches in forward converters. This note will describe the principle of the forward-converted and reset configuration used to dispose of the magnetic energy stored inside of the transformer. Finally, a series of forward coverter fishbone diagrams will be presented.

Contents

1 The forward converter

In this converter, the flyback is used to reduce the V_{main} voltage, bringing it to values able to feed the several applications for which the converter is used. Looking at the schematic below, we can observe that the use of an appropriate transformer permits isolation of the V_{main} from the output.

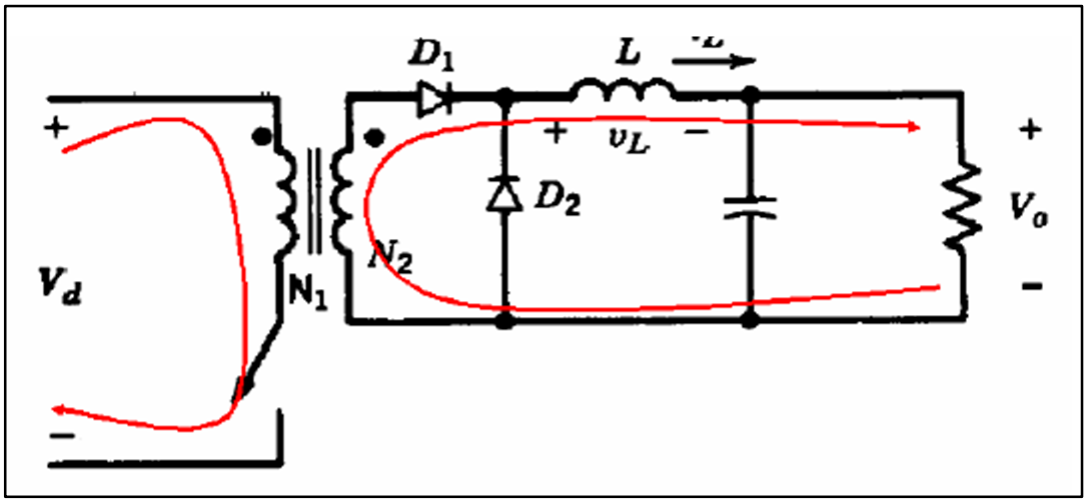
Figure 1: Schematic diagram of the forward converter



1.1 Functioning of the forward converter

T_{on}: During T_{on}, the switch is closed; the polarity of the transformer allows current conduction through diode D1, while diode D2 is blocked.

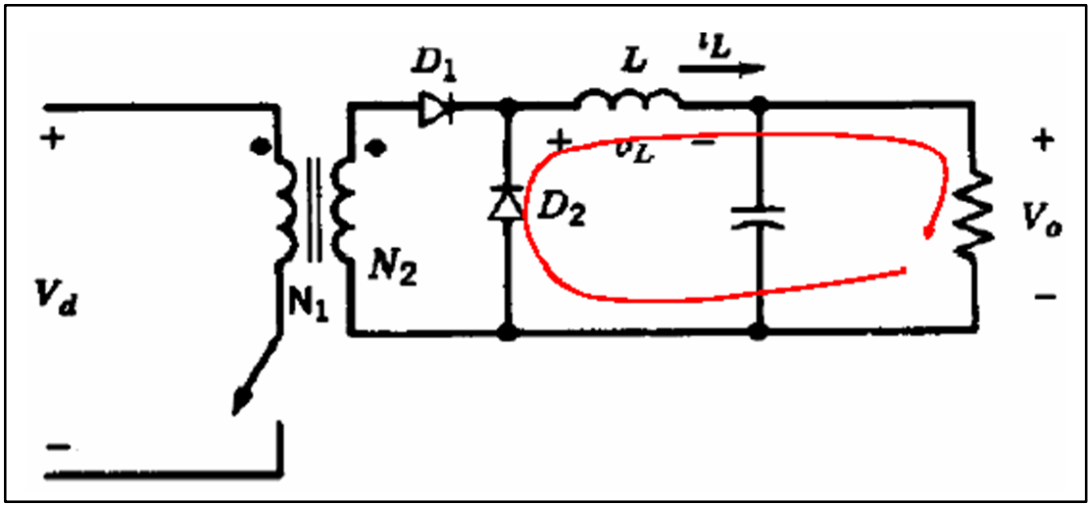
Figure 2: The circuit during the ON state



T_{off}: As soon as the switch turns off, an extra voltage is generated across its pin. This voltage is higher than the V_{main}, causing charging of the polarity on the secondary side of the transformer. This condition causes the blocking of D1, while diode D2 starts

conducting. In this situation, the load current holds up through D2, maintaining the correct direction.

Figure 3: The circuit during the OFF state



The following conditions are verified:

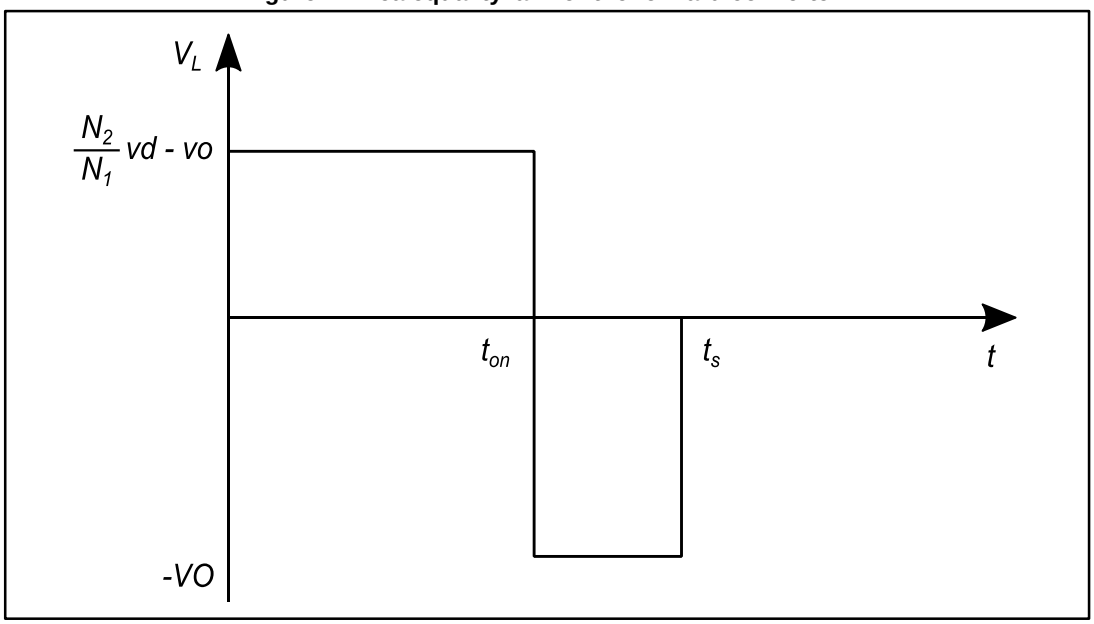
Equation 1

$$0 < t < t_{on} -> V_1 = V_2 - V_0 = \frac{N_2}{N_1} V_d - V_0$$

Equation 2

$$t_{on} < t < T_s -> V_1 = -V_0$$

Figure 4: Area equality law for the forward converter



From the two equations above, it is possible to calculate the input-output relation:

Equation 3

$$\left(V_d \cdot \frac{N_2}{N_1} - V_0\right) t_{on} - V_0 t_{off} = 0$$

Equation 4

$$V_d \cdot \frac{N_2}{N_1} \cdot t_{on} = V_0\left(t_{on} + t_{off}\right) \rightarrow V_d \cdot \frac{N_2}{N_1} \cdot DT_s = V_0 \cdot T_s$$

Equation 5

$$\frac{V_0}{V_d} = \frac{N_2}{N_1} \cdot D$$

This is the typical relation of a buck converter on which the ratio N2/N1, due to the impact of the transformer, is included.

1.2 Considerations

The schematic functioning previously described is the standard. Due to its intrinsic characteristics, the forward converter requires an appropriate reset circuit. In fact, due to the transformer's magnetization inductance, the magnetic energy stored during the conduction phase is not completely transferred to the secondary side. If the stored energy is not wasted, each commutation adds a quantity of energy and this undesirable condition can induce transformer saturation; therefore the primary winding behaves as a short-circuit, inducing a high current to be absorbed by the switch.

In the next section several reset circuits will be shown and the critical conditions will be discussed.

2 Reset circuits

As described previously, a suitable reset circuit is necessary to dispose of the magnetic energy linked to the magnetization inductance (L_m). For this purpose, several reset circuits will be shown. The main condition to be verified in each circuit is that $T_{reset} \leq T_{off}$

T_{reset}: The time necessary to dispose of the magnetic energy.

T_{off}: The switch-off time.

Figure 5: Base description of the reset method

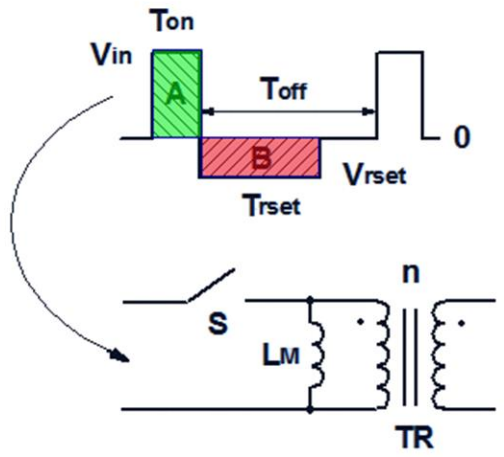


Figure 6: Area equality principle

$$V_{in} \cdot T_{on} = V_{rset} \cdot T_{rset}$$

$$T_{rset} \leq T_{off}$$

area A = area B

2.1 Reset by tertiary winding

The presence of an additional winding on the primary side allows energy recovery when the switch is off, and the two main windings are not working.

Referring to the schematic diagram below, we can observe how the discharge current can flow only in the direction allowed by the D3 diode, closing the circuit to V_{main}.

Figure 7: Reset by tertiary winding

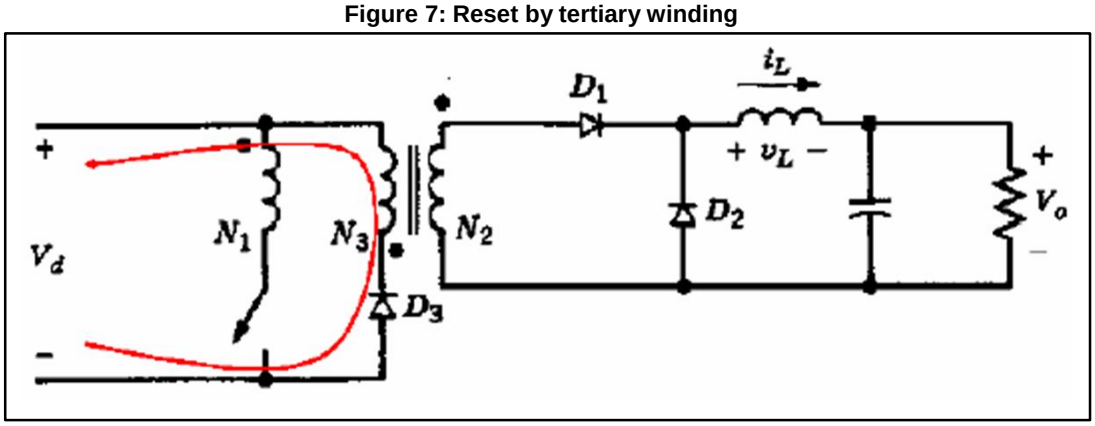
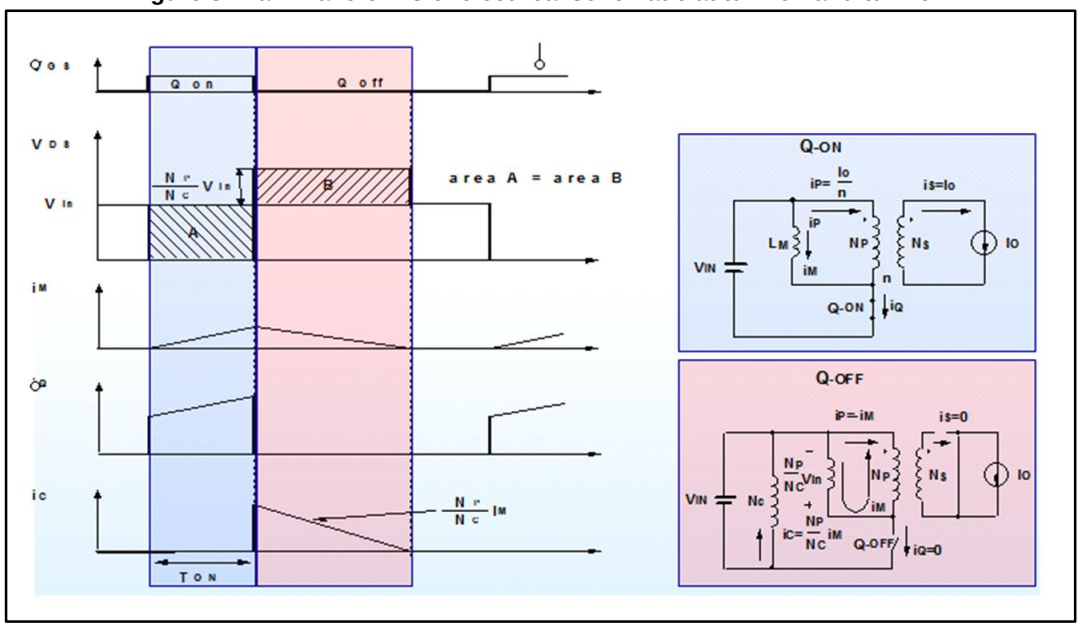


Figure 8: Main waveforms of electrical schematic at turn-on and turn-off



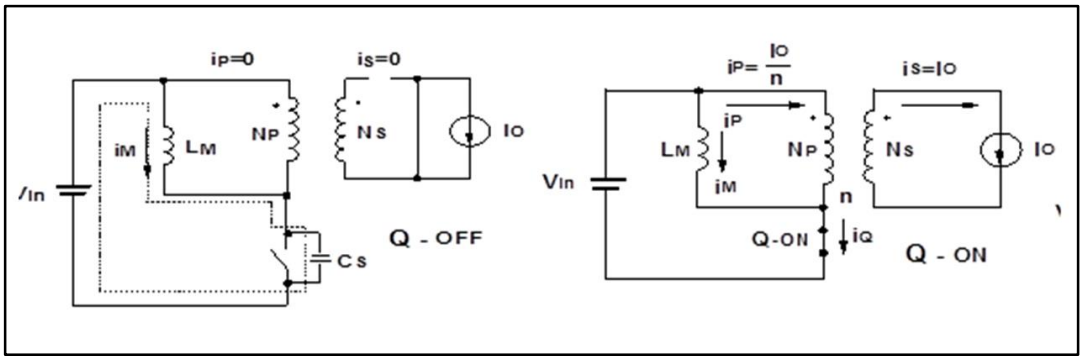
Stress condition

- As soon as the switch turns off, it is necessary to discharge the residual magnetization imposed on the switch to withstand stress voltage applied to the primary. The device used as a switch must have a wide BV_{DSS} tolerance in order to withstand the high values reached.
- Still, the T_{reset} must satisfy the following condition: $T_{reset}<T_{off}$.

2.2 Resonant reset

The illustration below shows the circuit used for the resonant reset, mainly used in applications with relatively low voltage.

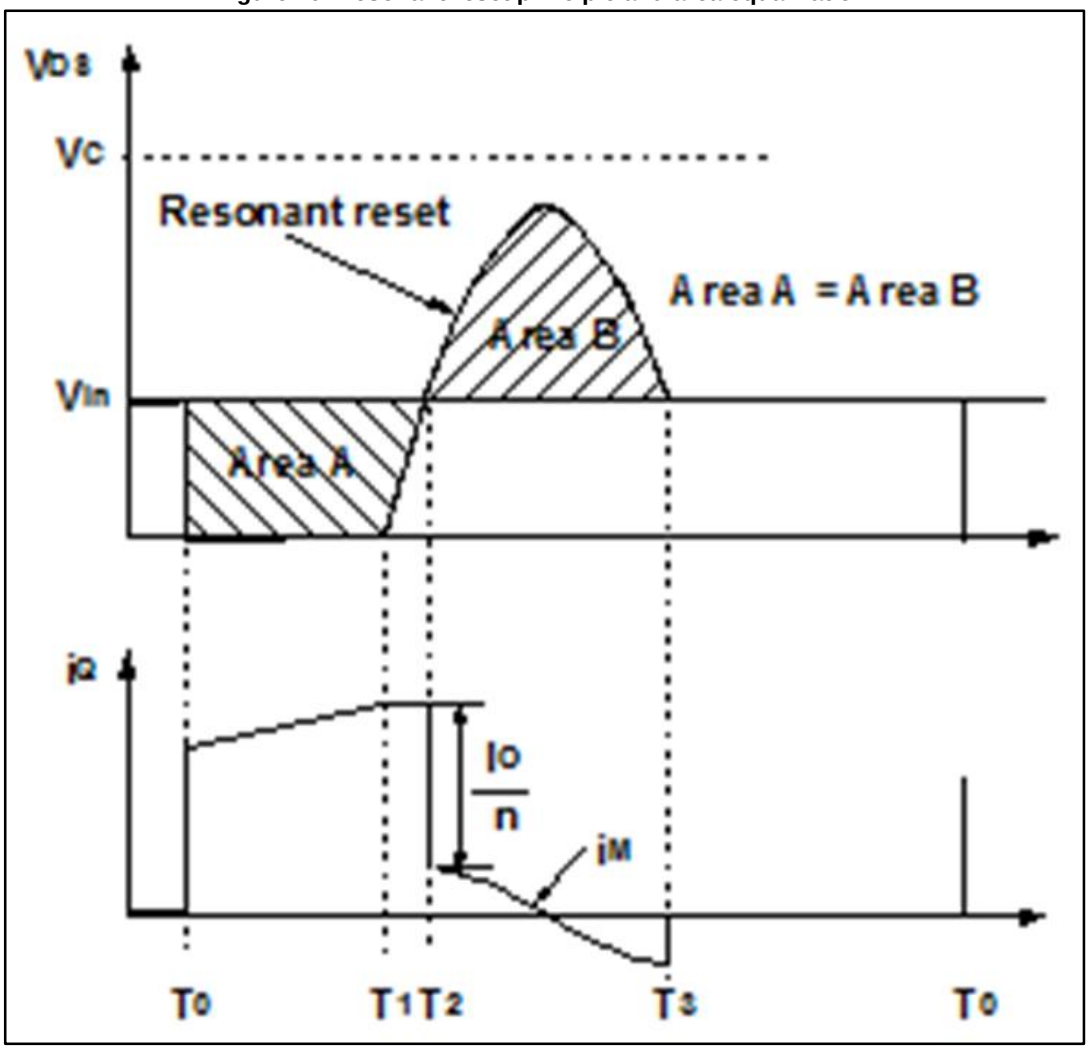
Figure 9: Resonant reset circuit



This reset uses the intrinsic capacitance of the power MOSFET and the parasitic external capacitance ($C_s=C_{oss}+C_{ext}$).

During turn-off, the capacitance C_s resonating with the magnetization inductance permits the dissipation of magnetic energy.

Figure 10: Resonant reset principle and area equalization



Looking at the diagram above, we can observe the sinusoidal shape of the V_{ds} voltage during turn-off.

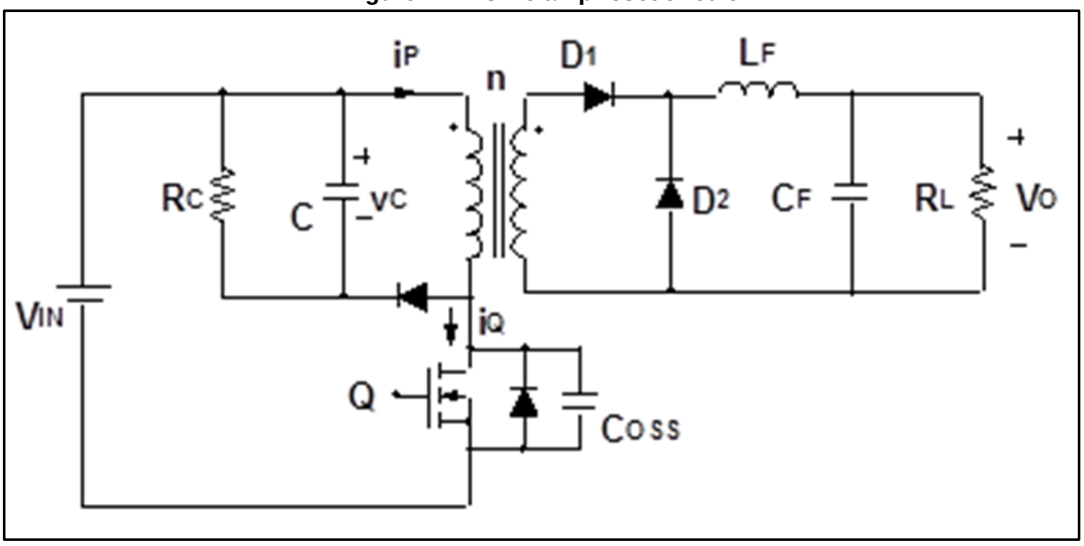
Stress condition

- High peak voltage due to the resonance effect.
- Still, the T_{reset} must satisfy the following condition: $T_{reset}<T_{off}$

2.3 RCD clamp reset

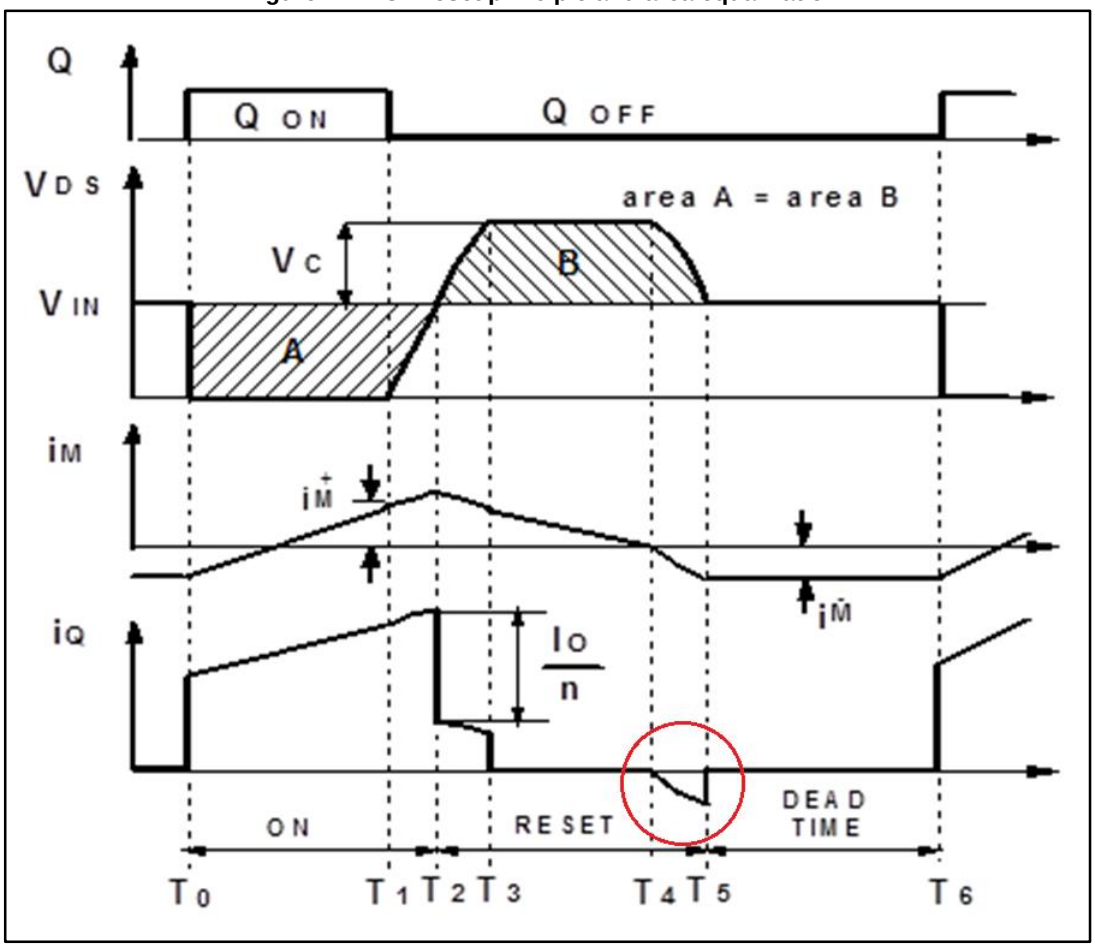
A schematic diagram of the the most popular reset circuit is shown below:

Figure 11: RCD clamp reset circuit



The magnetic energy is dissipated mainly by means of the RCD net, which also provides the voltage spike clamp. A small amount of energy is dissipated by the C_{oss} capacitor, as in the previous case.

Figure 12: RCD reset principle and area equalization

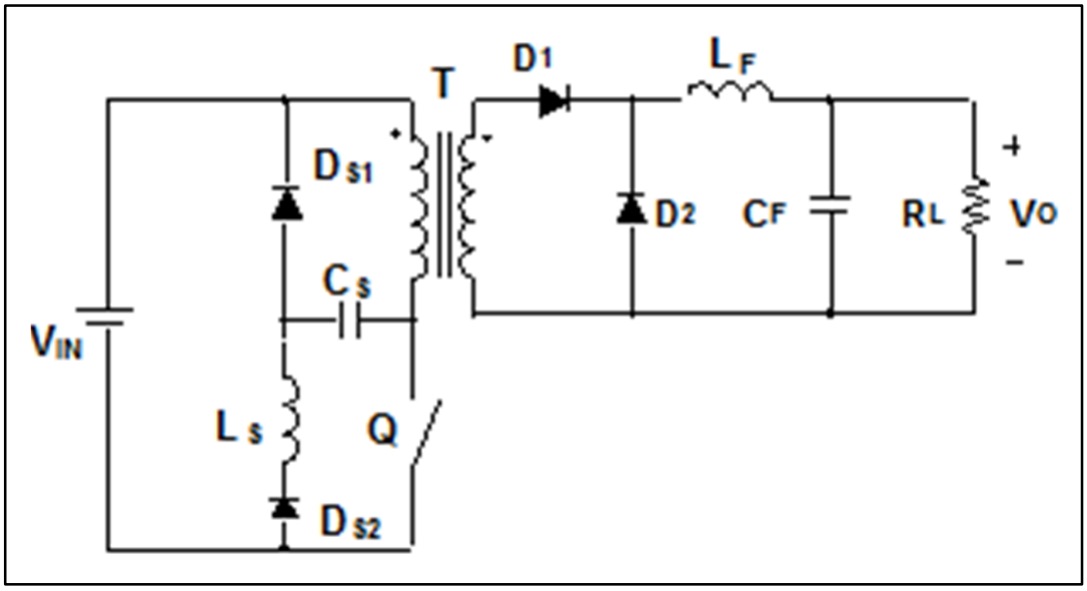


Stress condition

- The delay in the intervention time of the diode does not clamp the voltage, with consequences both for the discharge of the magnetic energy and for the power MOSFET, which can go into an avalanche condition.
- Observing the I_Q waveform, the red circle highlights the presence of a reverse current that flows through the body diode of the power MOSFET. If T_{reset} is close to T_{off}, this phenomenon can induce dv/dt stress.
- Still, the T_{reset} must satisfy the following condition: $T_{reset}<T_{off}$.

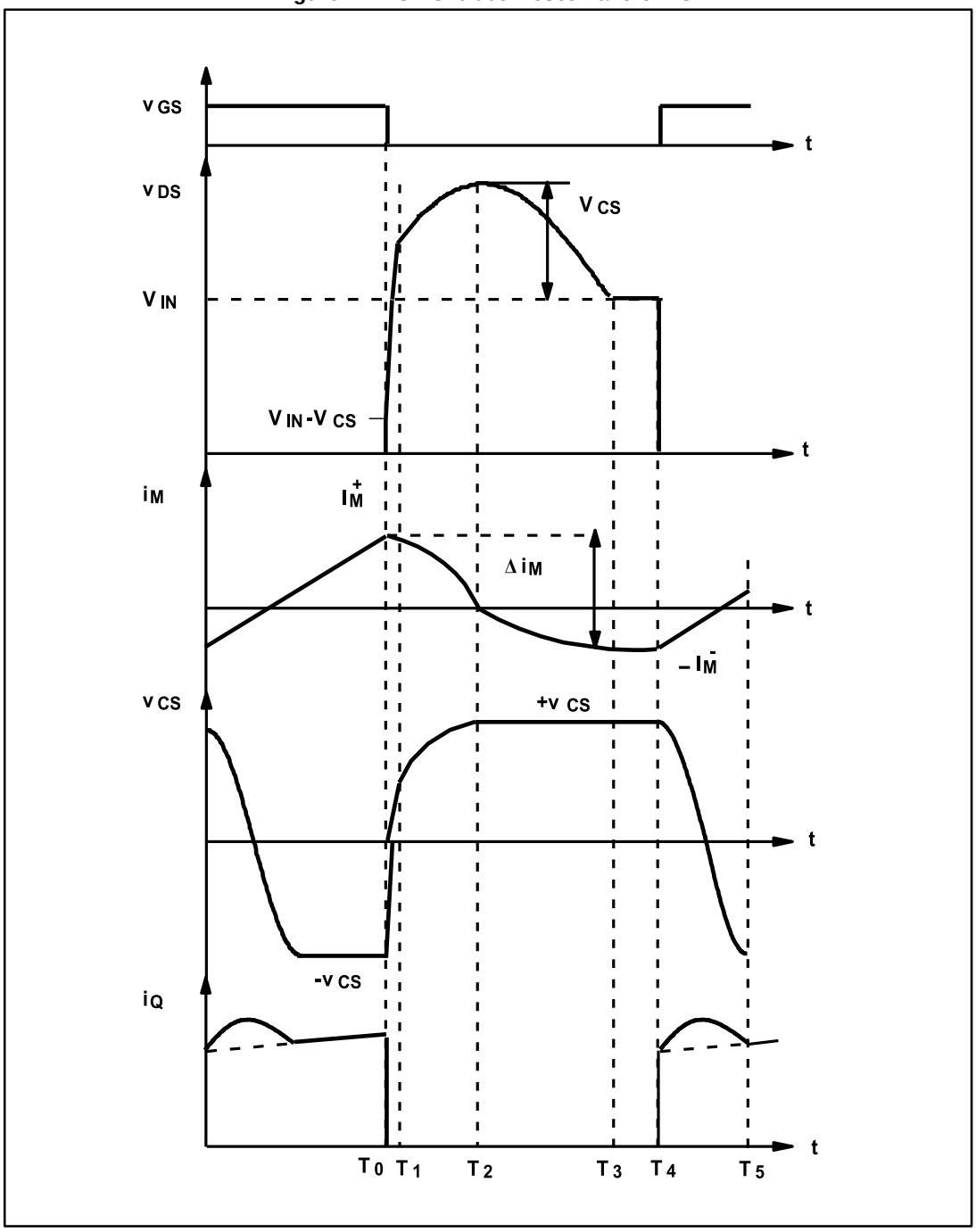
2.4 LCD snubber reset

Figure 13: LCD snubber reset schematic diagram



The use of a net composed of an external capacitor C_s and an inductor L_s permits recycling of part of the magnetization current. This behavior is typical of a resonant net. The effect of the net is to minimize energy losses by eliminating hot spots.

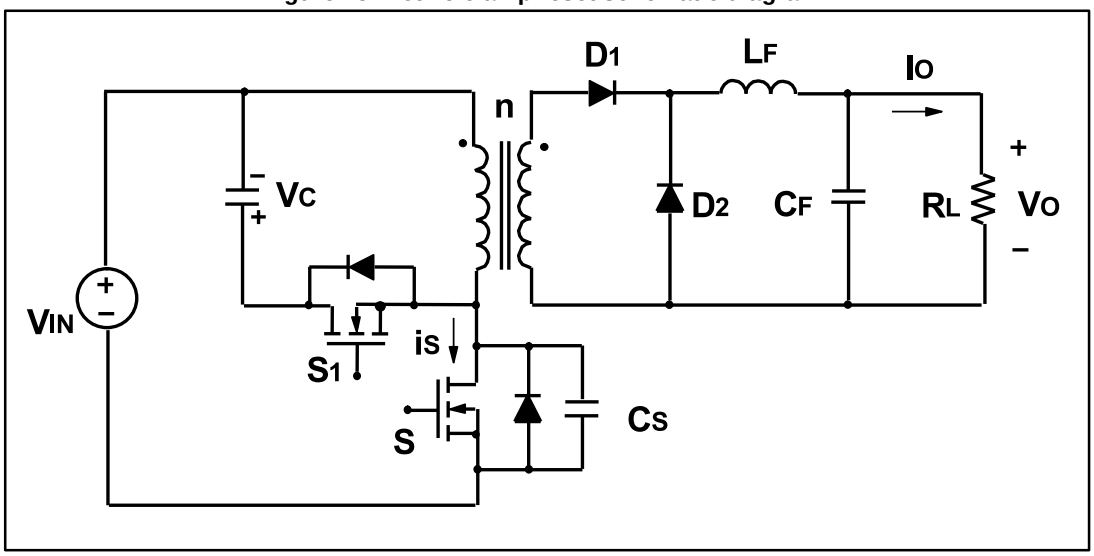
Figure 14: LCD snubber reset waveforms



2.5 Active clamp reset

This circuit implements the same behavior as the RCS net previously explained; the only difference is linked to the use of a power MOSFET instead of a diode. The main advantage of this approach consists in the minimization of the voltage stress on the main switch S. This because synchronization of the two power MOSFET is implemented. Moreover, it uses the entire off-time for reset (with a decrease in the voltage peak).

Figure 15: Active clamp reset schematic diagram



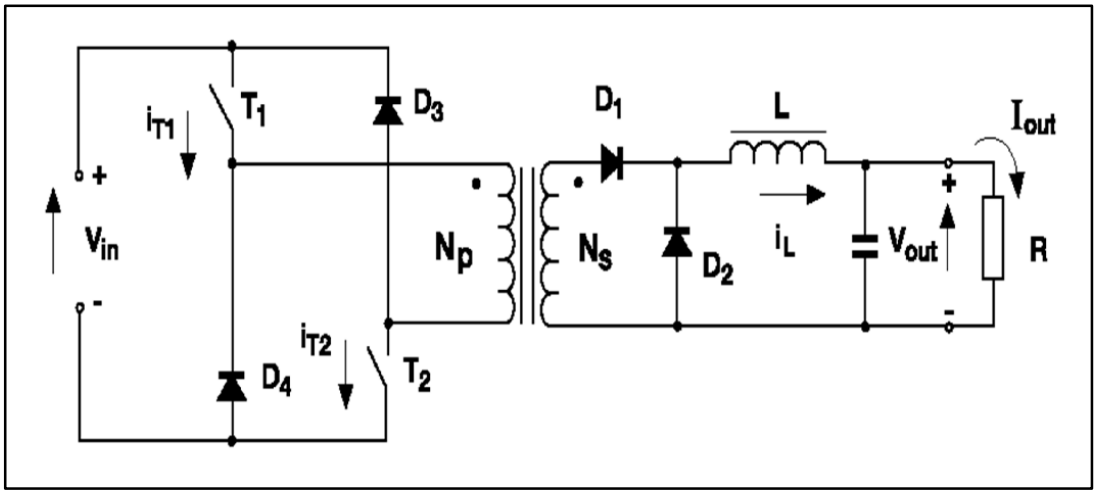
Critical condition

The poor synchronization of the two switches emphasizes the stress induced on the switch S by the intrinsic net characteristic.

2.6 Two switch forward converter

This converter is mainly used on applications which require high power. This is because devices with lower BV_{DSS} values can be used (each device must be able to withstand half the voltage compared to a single transistor converter).

Figure 16: Two switch forward converter schematic diagram



Critical condition:

The difference in switching time for each MOSFET is dangerous because the V_{IN} both during the turn-on and turn-off is applied to only one switch.

3 Fishbone diagrams

In this section, the critical conditions described previosuly will be summarized in causes-and-effect (fishbone) diagrams.

The first shows the fishbone diagram for the most general forward converter. The successive diagrams show the critical conditions induced by the reset circuit on the power MOSFET used as switch.

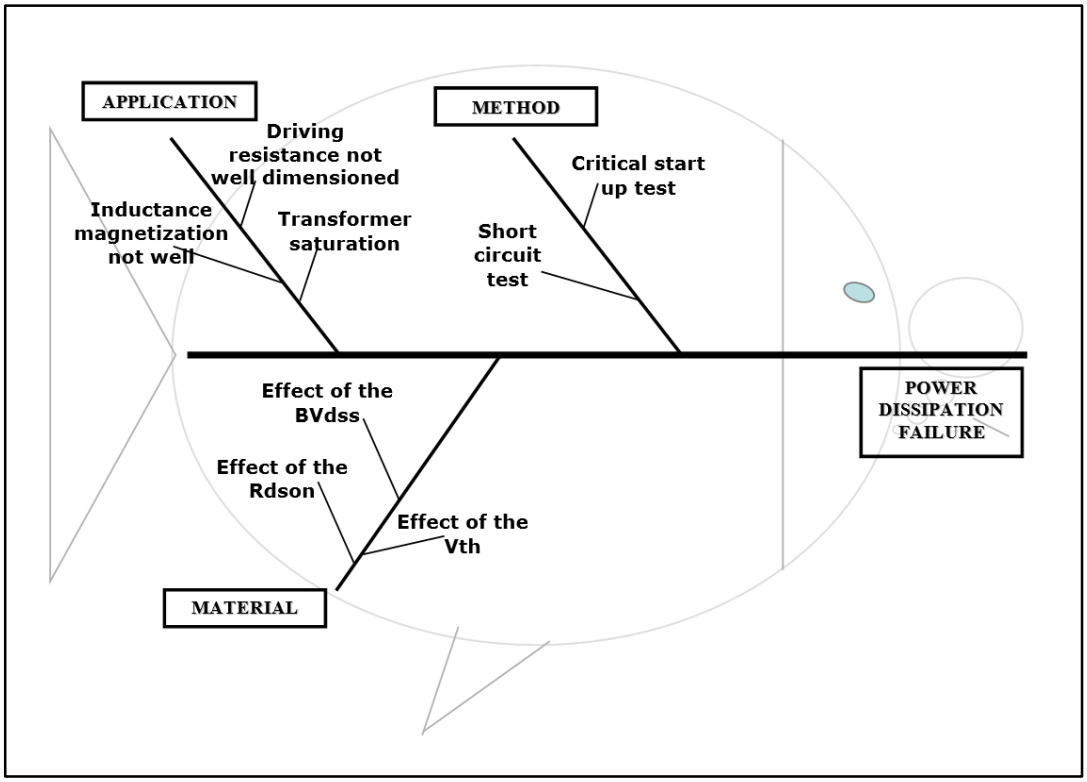
3.1 Fishbone diagrams for the forward converter

Two different failure types can be highlighted:

1. Failure due to power dissipation
2. Current stress failure

3.1.1 Failure due to power dissipation

Figure 17: Failure due to power dissipation



Causes linked to the application:

- Driving gate resistance not well dimensioned (high value).

A too high driving resistance can cause a slow turn-off that determines higher power dissipation during the transition from the on state to the off state.

- Transformer saturation.

During the startup phase, if transformer saturation occurs I_d current reaches higher values than what is reached during the steady-state phase. Subsequently, the transformer primary wing will no longer absolve the function of coil, but will be assimilated into a short-circuit,

and therefore the I_d current slope will increase also. This condition implies an increase of the power dissipation (given by the product $P=V_{ds}$*Id and uncontrolled peak current value). If the heatsink is not properly sized, the temperature reached will exceed the maximum guaranteed value and the device will be forced into thermal runaway. In any case, the device can exhibit early failure if the I_d current reaches values higher than the maximum ratings supported.

- Leakage inductance effect and spread of the leakage inductance.

Each transformer is characterized by a proper leakage inductance.

Leakage inductance couples with the magnetization inductance and their main effect consists in increasing the voltage spike present on the drain of the power MOSFET during turn-off. The higher the value of the leakage inductance, the higher the leakage effect in terms of peak voltage and duration with an increase of power dissipation. A considerable spread of leakage inductance, for instance of 10%, could cause a heavy overvoltage effect on the device, causing possible failure.

- Magnetization inductance not well disposed of

During the off-state, the absence of the reset circuit causes the magnetization inductance not to dispose the energy accumulated during the previous phase. This condition leads to pre-saturation of the transformer. The consideration related to transformer saturation previously discussed can be considered also for this case.

Causes linked to the method:

- Critical startup test

Generally, this kind of test has the purpose to evaluate the performances of the board submitted to over electrical stress in terms of current and voltage. If the stress isn't linked to a single parameter, it can be due to their combination then it can be due summarized like thermal stress.

The board is forced to work for a certain period of time in abnormal working condition. This condition could cause an overheating of the transformer. Subsequently, in a short interval of time, the board is switched off and quickly is switched on again. Being transformer saturation current related to the temperature with a reverse relation, in these cases, it is possible to observe a pre-saturation effect for the transformer. At this point the condition to analyze is that just explained for the transformer saturation.

- Short-circuit test

In this test the load is a short circuit. Some SMPS makers perform this kind of test in different ways. The increase of the output current implies an increase of the V_{ds} voltage due to the high current value . Also in this case this condition imposes an increase of the power to be dissipated. If this test is not well fitted with the device electrical characteristics, the power dissipated can induce thermal runaway.

Causes linked to the material:

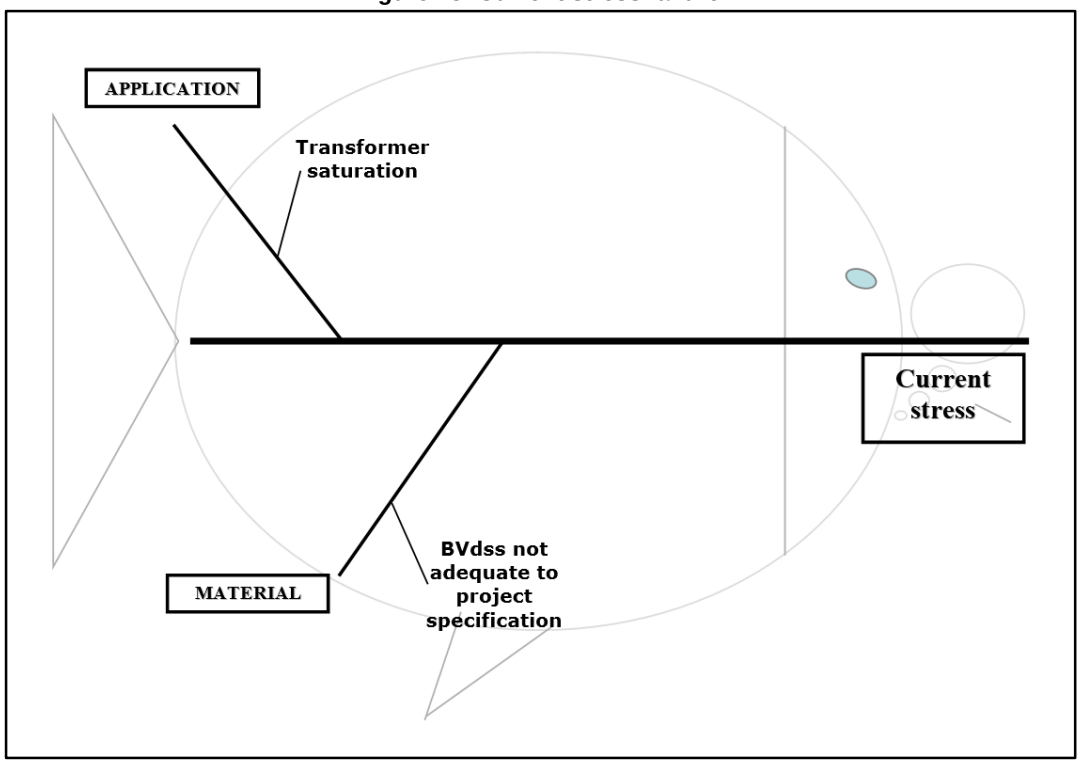
Each parameter, like for instance the $R_{DS(on)}$, V_{th} is single electrical characterized by a typical variation inside the datasheet limits. Marginal devices with values close to these limits can cause also the below described issues problems.

- Parameter not well dimensioned:
  a. **$R_{DS(on)}$** : A value of $R_{DS(on)}$ higher respect that requested by the design determines a temperature increasing that can bring to the failure for thermal runaway.
  b. **V_{th}** : A device with a V_{th} value lower with respect to the typical values causes a turn off delay, that increasing the power dissipation can bring the device in thermal runaway.

c. **BV_{dss}**: If the device used is not well marginated in terms of BV_{dss}, during the turn off. BV_{dss} peaks able to bring the device in Avalanche can occur (the peaks are not able to turn on the parasitic bipolar). This condition causes an overheating of the unit that in some cases can bring the device in thermal runaway.

3.1.2 Current stress failure (parasitic bipolar turn-on)

Figure 18: Current stress failure



Causes linked to the application

- Transformer saturation

If transformer saturation occurs and the voltage spike is able to bring the device into avalanche, the current that flows through the unit is too high to activate the parasitic bipolar, causing failure due to uncontrolled overcurrent flow.

Causes linked to the material

- BV_{DSS} not adequate for the project specification

Avalanche can occur also if the BV_{DSS} is not adequate based on the project specification or if the BV_{DSS} value is close to the lower distribution limit (marginality case).

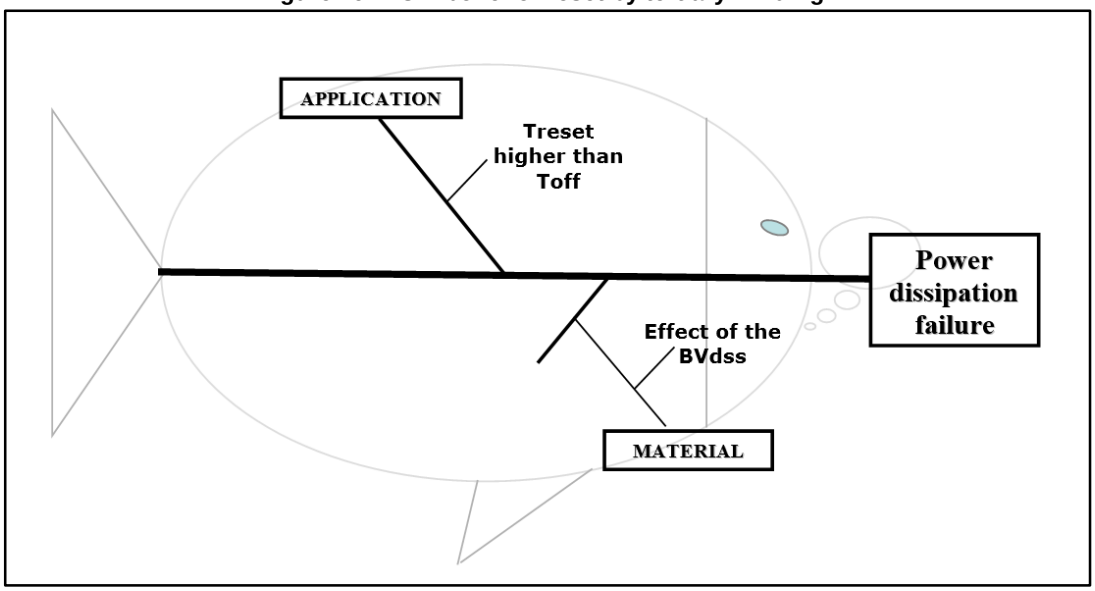
3.1.3 Fishbone for reset circuit by tertiary winding

In this paragraph, for each reset circuit analyzed, the several causes able to bring about to the failure of the power MOSFET will be analyzed.

On each diagram only the critical condition induced by the particular reset circuit will be discussed, the ones just discussed in the previous paragraph remain valid and will not be put in the diagrams.

The first circuit analyzed is the reset by tertiary winding.

Figure 19: Fishhbone for reset by tertiary winding



Causes linked to the application

- T_{reset} higher than T_{off}

During the transition from turn on to turn off, the T_{off} time must be well marginated with respect to the T_{off}. The condition on which the T_{reset} is higher than T_{off} does not allow to the magnetization inductance to dispose of the magnetic energy. The accumulation this magnetic energy can induce transformer saturation.

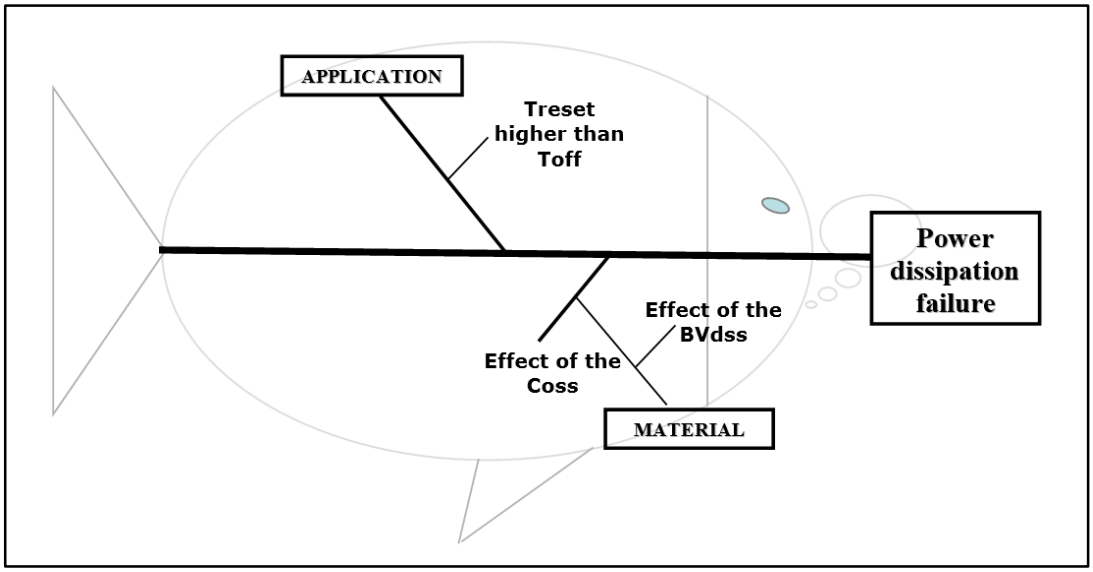
Causes linked to the material

- Effect of the BV_{DSS}

As previously explained, during the transition from turn-on to turn-off, the voltage applied to the drain of the transistor can reach high values. This condition is caused by the presence of the diode in the tertiary winding. This effect, coupled with the effect of the leakage inductance, determines the voltage spike which could be higher than the breakdown voltage of the power MOSFET (BV_{DSS}). In particular, if the device used is characterized by a BV_{DSS} voltage close to the minimum specification limit, the high voltage reached could determine the failure of the device.

3.1.4 Fishbone for resonant reset

Figure 20: Fishbone for resonant reset



Causes linked to the application

- T_{reset} higher than T_{off}

The same consideration discussed for the previous case remains valid for this one.

- Effect of the BV_{DSS}

Due to the resonant effect, a consistent voltage peak is present in the drain of the power MOSFET. Also in this case, the use of devices with BV_{DSS} values close to the minimum guaranteed limit can cause failure of the power MOSFET.

- Effect of the C_{oss}

During the transition from turn-on to turn-off, the energy accumulated inside the coil charges the capacitor. The use of devices with low C_{oss}, due to a decrease of the time constant, determines the reduction of T_{reset}, with a consequent increase in the voltage peak. For the same consideration, the use of C_{oss} with a higher value has the advantage of decreasing the voltage peak; but unfortunately T_{reset} increases.

It is possible to summarize the above in the following table:

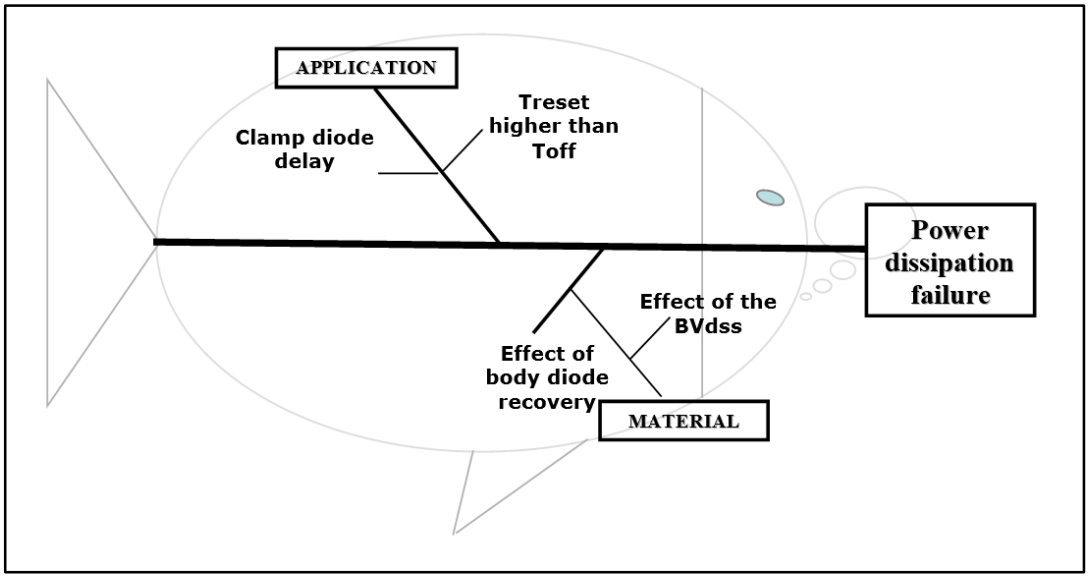
Table 1: Effect of the Coss - summary

C_{oss} value	Influence	Possible failures
Low	Increases the voltage peak	If the BV_{DSS} value is close to the minimum specification limit, the avalanche phenomenon can occur
High	Increases T_{reset}	If $T_{reset}>T_{off}$, transformer saturation can occur

Based on these considerations, the device must be characterized with a suitable C_{oss} value.

3.1.5 Fishbone for the RCD reset net

Figure 21: Fishbone for the RCD reset net



Caused linked to the application

- Clamp diode relay

The delay in the intervention time of the clamp diode determines the voltage applied on the drain of the power MOSFET to reach high values. This condition induces two stresses:

a. If the voltage is able to overcome the device breakdown voltage, the device going in avalanche could fail.
b. The increase in the voltage determines an increase in the power dissipation; this is because the crossing point between the voltage and current rises with respect to the normal condition.

- T_{reset} higher than T_{off}

The same consideration discussed for the previous case remains valid for this one.

Causes linked to the material

- Effect of the BV_{DSS}

The condition in which a delay in the intervention time of the diode occurs, as explained above, determines an increase of the voltage on the drain terminal.

Also in this case, if the device is characterized by a BV_{DSS} voltage close to the minimum specification limit, the same two stress conditions previously explained can occur.

- Effect of body diode recovery

As explained in the relevant paragraph, a decrease in the magnetization current determines, as soon as it reaches the zero, an inversion in the polarity of the inductance which determines an inverse current to flow through the body diode. The condition in which T_{reset} is close to T_{off} determines an incomplete disposal of the minority charges that can induce turn-on of the parasitic bipolar.

3.1.6 Fishbone for the active clamp reset

The circuital topology is the same as that of the previous one, but referring to *Figure 15: "Active clamp reset schematic diagram"*, if the S1 and S diodes are not properly synchronized, the critical conditions mentioned above are maximized.

4 Revision history

Table 2: Document revision history

Date	Version	Changes
03-Mar-2016	1	Initial release.

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