AN4857
Application note

STEVAL-ISA179V1 15 V/2.25 W 60 kHz buck demo with VIPer0P

Introduction

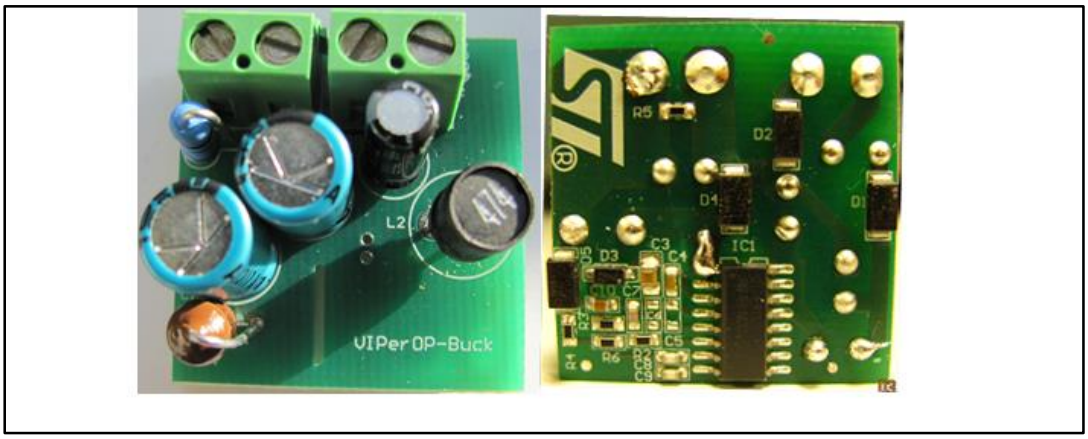
The STEVAL-ISA179V1 is a 15 V – 0.15 A power supply set in buck topology using the new VIPer0P off-line high voltage converter by STMicroelectronics, specifically developed for non-isolated SMPS.

The device features:

- an 800 V avalanche rugged power section
- on-board soft-start
- safe auto-restart after faults
- PWM operation at 60 kHz with frequency jittering for lower EMI
- pulse skipping frequency to limit DRAIN peak current at startup
- low standby power consumption

Thermal shutdown and delayed overload protections are included; all protections involve auto-restart mode.

Figure 1: STEVAL-ISA179V1 demo board



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1 Adapter features

Table 1: STEVAL-ISA179V1 electrical specifications

Parameter	Symbol	Value
Input voltage range	V_{IN}	85 to 265 V_{AC}
Output voltage	V_{OUT}	15 V
Max output current	I_{OUT}	0.15 A
Precision of output regulation	ΔV_{OUT_LF}	±5%
High frequency output voltage ripple	ΔV_{OUT_HF}	50 mV
Max ambient operating temperature	T_{AMB}	60 ºC

2 Circuit description

Referring to *Figure 2: "Application schematic diagram"*, the FB pin is the inverting input of the internal transconductance error amplifier, internally referenced to V_{REF_FB} (1.2 V typ.). This allows setting the voltage across capacitor C10 (actually a replica of the output voltage) through the voltage divider made up of resistors (R4+R6) and R3, according to:

Equation 1

$$V_{OUT} = V_{FB\_REF} \cdot (1 + \frac{R4 + R6}{R3})$$

The compensation network is connected between the COMP pin (the output of the error amplifier) and the SGND pin.

The bleeder resistor R5 provides a 1 mA approximate minimum load to avoid overvoltage when the output load is disconnected. It is a tradeoff between overvoltage containment and increase of power consumption under no load.

At power-up, as V_{DRAIN} exceeds $V_{HVSTART}$, the internal HV current generator charges the VCC capacitor, C3, to V_{CCon}, the Power MOSFET starts switching, the current generator is turned off and the IC is powered by C3.

When V_{OUT} reaches its steady-state value, the IC is biased from the output through diode D3. This is referred to as "external biasing" and can be applied because the output voltage is high enough to keep the C3 voltage above the V_{CSon} threshold, whose maximum value V_{CSon_max} is 4.5 V. With this setting, the V_{CC} voltage shape during steady-state operation is constant, following the output voltage, the HV current generator is never activated and very low input power consumption under light or no load conditions is possible (less than 40 mW at 230 V_{AC} under no load with an appropriate design), thanks to the low consumption of the internal blocks of the VIPer0P.

The VIPer0P can also be operated without diode D_3 or any other external biasing network. In this case, V_{CC} is not sustained by the output and whenever it decays to V_{CCson} due to internal IC consumption, the HV current generator is automatically turned on and charges V_{CC} to V_{CCon}, upon which it is switched off. This repeated operation produces a saw tooth V_{CC} voltage shape. This setting, referred to as "self-biasing", leads to higher power dissipation and worse standby performance with respect to external biasing, but reduces the overall BOM cost, minimizing the number of external components. Moreover, it allows the designer to generate output voltages below the UVLO (e.g., 3.3V) without complicating the power inductor design.

Only external biasing is considered herein.

3 Schematic diagram and bill of materials

Figure 2: Application schematic diagram

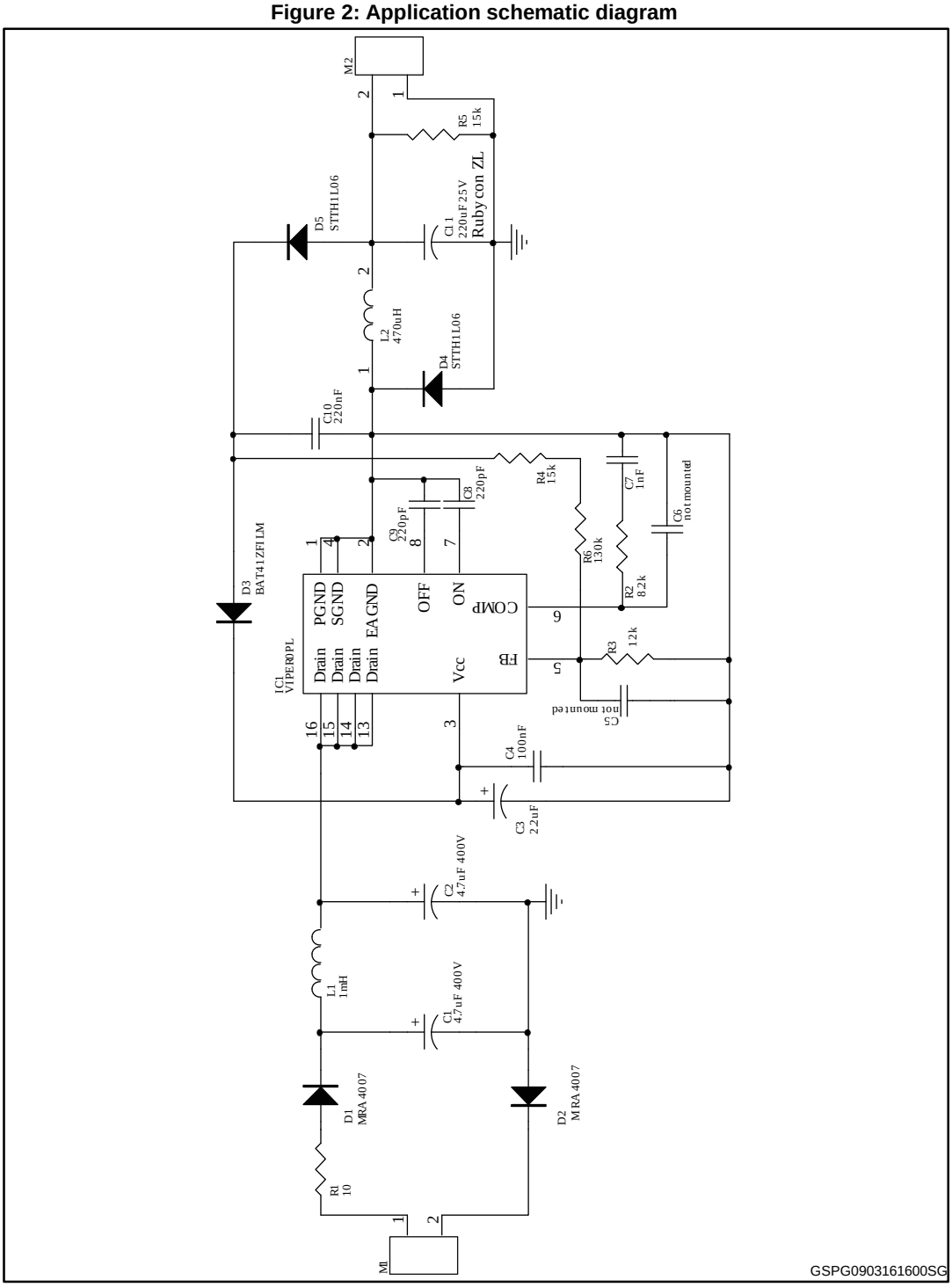


Table 2: Bill of materials

Ref	Part number	Manufacturer	Description	Package
D1	MRA4007T3G	ON semiconductor	1 A-1000 V power rectifier diode	SMA
D2	MRA4007T3G	ON semiconductor	1 A-1000 V power rectifier diode	SMA
D3	BAT41ZFILM	STMicroelectronics	0.15 A-100 V signal Schottky diode	SOD-123
D4	STTH1L06A	STMicroelectronics	DIODE ULTRA FAST 600V 1A	SMA
D5	STTH1L06A	STMicroelectronics	DIODE ULTRA FAST 600V 1A	SMA
L1	B82144A2105J	Epcos	1 mH axial inductor	Axial
L2	DR0810-474L	COILCRAFT	470 µH ± 10% radial inductor (Isat=0.66A)	Radial
C1		SAMXONN	4.7µF, 400 V electr. cap.	Ø8 mm - p3.5 mm - h11 mm
C2		SAMXONN	4.7µF, 400 V electr. cap.	Ø8 mm - p3.5 mm - h11 mm
C3	GRM21BR61H225KA73L	Murata	2.2 µF, 50V ceramic multilayer cap	0805
C4	GRM188R71H104KA93D	Murata	100 nF, 50V ceramic multilayer cap	0603
C5	- - -	- - -	not mounted ceramic multilayer cap	0603
C6	- - -	- - -	not mounted ceramic multilayer cap	0603
C7	C1608C0G1H102J080AA	TDK	1 nF, 50 V ceramic multilayer cap	0603
C8	C0603C221J5GACTU	Kemet	220 pF, 50V ceramic multilayer cap	0603
C9	C0603C221J5GACTU	Kemet	220 pF, 50V ceramic multilayer cap	0603
C10	CGA3E3X7R1H224K080AB	TDK	220 nF, 50V ceramic multilayer cap	0603
C11		Rubycon	220 µF, 25V Elcap ultra-low ESR ZL series	Ø8 mm - p3.5 mm - h11 mm
R1	ROX1SJ10R	TE Connectivity	10 Ω axial metal film resistor	Ø3 mm - p9mm
R2	ERJP03F8201V	Panasonic	8.2 kΩ ±1% - 0.2 W resistor	0603
R3	ERJP03F1202V	Panasonic	12 kΩ ±1 % - 0.2 W resistor	0603

Ref	Part number	Manufacturer	Description	Package
R4	ERJP03F1502V	Panasonic	15 kΩ ±1% - 0.2 W resistor	0603
R5	ERJP03F1502V	Panasonic	15 kΩ ±1% - 0.2 W resistor	0603
R6	ERJP03F1303V	Panasonic	130 kΩ ±1% - 0.2 W resistor	0603
IC1	VIPer0PL	STMicroelectronics	High voltage converter	SO-16N

4 Board layout

Figure 3: Layout (complete)

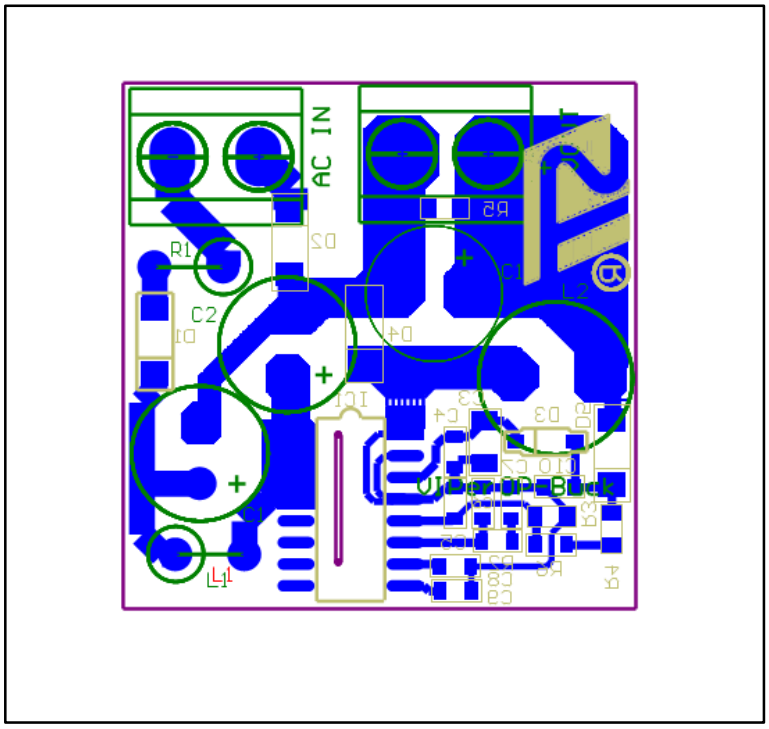


Figure 4: Layout (top layer)

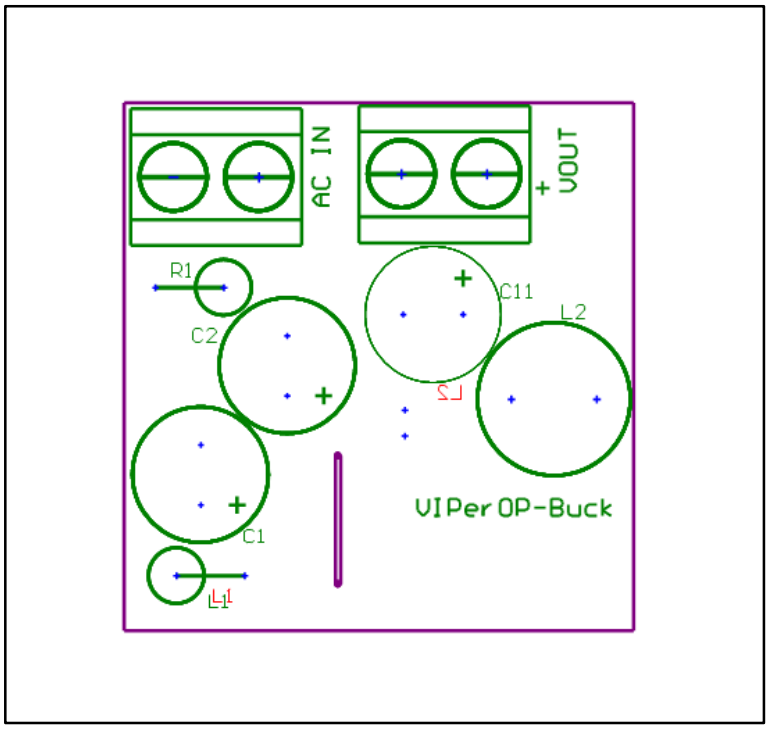
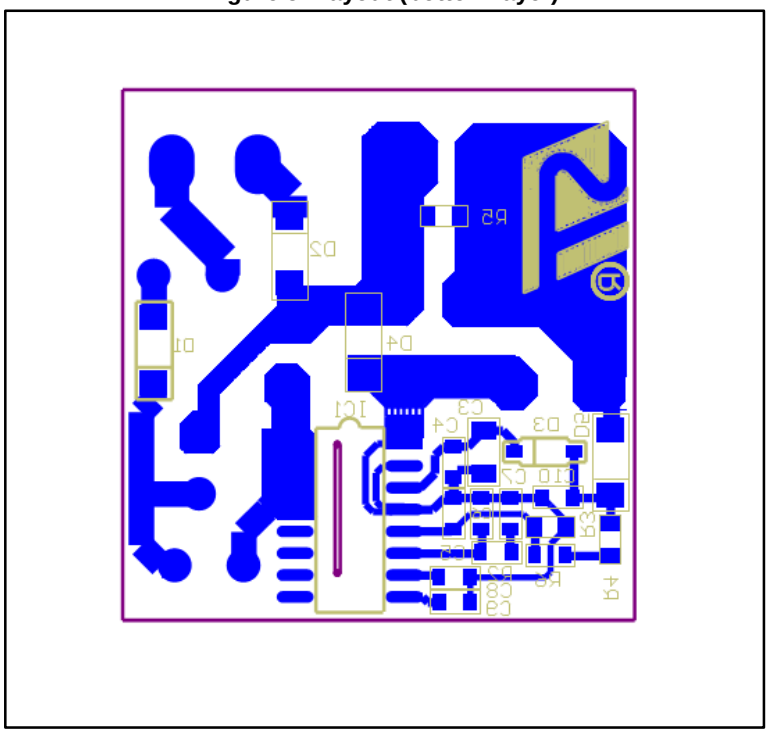


Figure 5: Layout (bottom layer)



5 Testing the board

5.1 Typical waveforms

Voltage and current waveforms under full load in *Figure 6: "waveforms at 115 VAC, full load"* and *Figure 7: "waveforms at 115VAC, full load (zoom)"* (at V_{IN} =115 V_{AC}) and in figures *Figure 8: "waveforms at 230VAC, full load"* and *Figure 9: "waveforms at 230VAC, full load (zoom)"* (at V_{IN} = 230 V_{AC}).

Figure 6: waveforms at 115 V_{AC}, full load

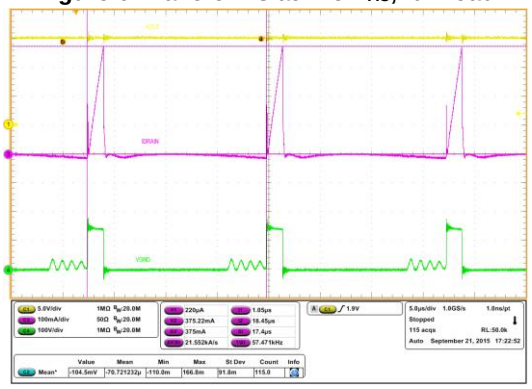


Figure 7: waveforms at 115 V_{AC}, full load (zoom)

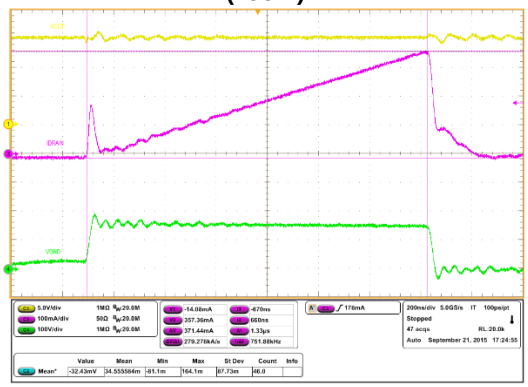


Figure 8: waveforms at 230 V_{AC}, full load

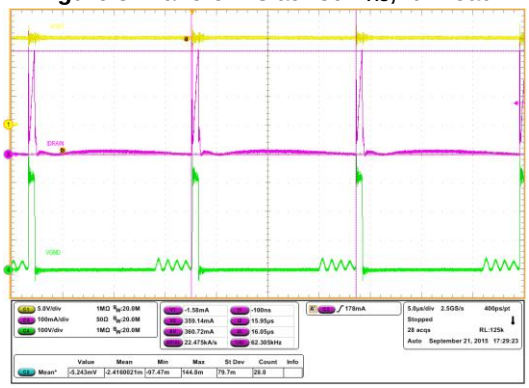
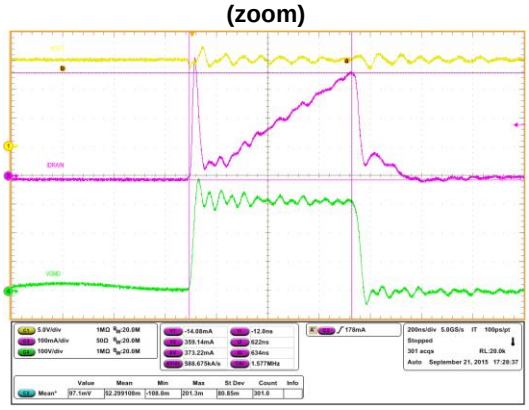


Figure 9: waveforms at 230 V_{AC}, full load (zoom)



5.2 Line and load regulation

The output voltage of the board was measured under different line and load conditions, with the results shown in the figures below.

Figure 10: Line regulation

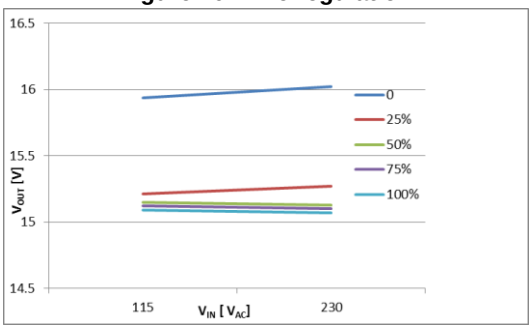
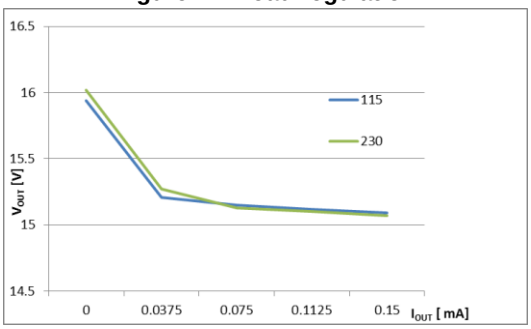


Figure 11: Load regulation



5.3 Efficiency

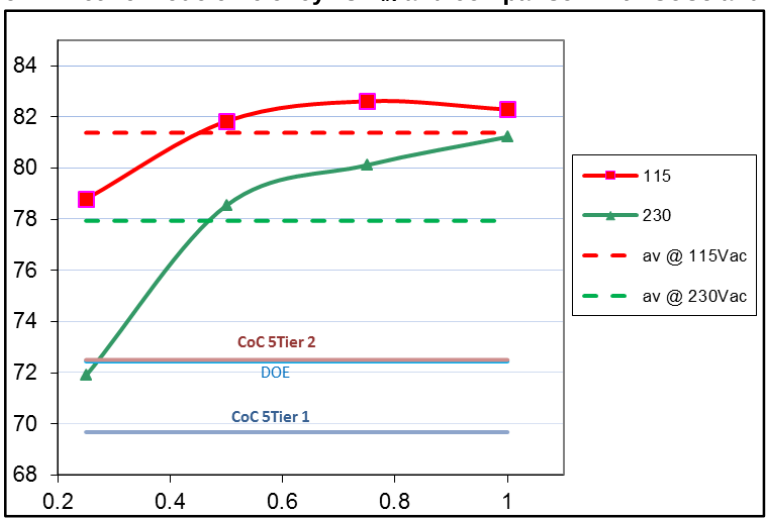
The active mode efficiency is defined as the average of the efficiencies measured at 25%, 50%, 75% and 100% maximum load at V_{IN} = 115 V_{AC} and V_{IN} = 230 V_{AC} nominal input voltages.

External power supplies (those housed separately from the end-use devices they are powering) need to comply with the Code of Conduct, version 5 "Active mode efficiency" criterion, whereby the active mode efficiency must be above 72.5% for a power throughput of 2.25 W (CoC5 tier2, January 2016).

The DOE (Department of Energy) recommendation is another standard whose active mode efficiency requirement for the same power throughput is 72.4%.

Figure 12: "Active mode efficiency vs Vand comparison with CoC5 and DOE" demonstrates the compliance of the STEVAL-ISA179V1 with the above standards: the DOE and CoC5 limits are indicated in solid lines; average efficiencies at 115 V_{AC} and 230 V_{AC} (81.4% and 77.9% respectively) in dotted lines; markers on the curves represent efficiency at 25%, 50%, 75% and 100% maximum load for both input voltages.

Figure 12: Active mode efficiency vs V_{IN} and comparison with CoC5 and DOE



5.4 Light load performance

In version 5 of the Code of Conduct, the power consumption of the power supply when it is not loaded is also considered.

Table 3: Energy consumption criteria for no load

Nameplate output power (Pno) [W]	Maximum power under no load for AC-DC EPS [W]	
	Tier 1	Tier 2
0.3 < Pno ≤ 49	0.15	0.075
50 < Pno < 250	0.25	0.15

The STEVAL-ISA179V1 no load performance measured at 115 V_{AC} and 230 V_{AC} nominal input voltages are well above Tier 1 and Tier 2 requirements, as shown in the following table.

Table 4: Demo board input power consumption under no load

V_{IN} [V_{AC}]	No load	
	V_{OUT} [V]	P_{IN} [mW]
115	15.94	30.1
230	16.02	35.0

CoC5 also includes requirements on the active mode efficiency when the output load is 10% of the nominal output power. Comparison of the requirement for an external power supply with a power throughput of 2.25 W and STEVAL-ISA179V1 performance in the following table shows that the demo board is compliant with Tier 1 and Tier 2 requirements.

Table 5: CoC5 requirement and performance at 10% output load

V_{IN} [V_{AC}]	STEVAL-ISA179V1 performance [%]	CoC5 requirements for P_{OUT} = 2.25 W	
		Tier 1	Tier2
115	71.8	59.7	62.5
230	66.5		

Depending on the equipment supplied, there are several criteria to measure the performance of a converter. In particular, one requirement for light load performance (EuP lot 6) is that the input power should be less than 500 mW when the converter is loaded with 250 mW.

The following table shows how the STEVAL-ISA179V1 board satisfies this requirement, along with consumption figures for P_{OUT} = 25 mW and P_{OUT} = 50 mW light load conditions.

Table 6: Light load performance against output power

V_{IN} [V_{AC}]	efficiency [%]		
	at P_{OUT} = 25 mW	at P_{OUT} = 50 mW	at P_{OUT} = 250 mW
115	62.0	94.8	342
230	67.8	100.7	367

The following table provides data for other light load comparisons, where the parameter is the input power consumption.

Table 7: Light load performance against input power

V_{IN} [V_{AC}]	efficiency [%]		
	at P_{IN} = 25 mW	at P_{IN} = 50 mW	at P_{IN} = 1 W
115	70.2	76.7	81.2
230	64.2	70.3	75.2

6 Functional check

6.1 Startup

The startup phase at maximum load and 115 V_{AC} and 230 V_{AC} nominal input voltages are shown in *Figure 13: "startup at 115 VAC, full load"* and *Figure 15: "startup at 115 VAC, full load"*.

An internal soft-start function progressively increases the cycle-by-cycle current limitation set point from zero to I_{DLIM} in 8 steps. This limits drain current during the output voltage rise, thus reducing the stress on the secondary diode. The t_{SS} soft-start time needed for the current limitation to reach its final value is internally set at 8 ms. This function is activated for any converter start-up attempt or after a fault event. The IC has a “pulse skipping” feature which skips a switching cycle whenever the OCP comparator is triggered within the minimum on-time. The switching frequency is thus halved, down to the minimum allowed value of F_{OSC_MIN} (15 kHz typ.).

By allowing a longer inductor discharge time, this feature helps prevent current runaway: the possible uncontrolled increase in drain current during the very first cycles of converter startup due to the initial inability of the system to maintain the volt-second balance when there is a large input-to-output voltage differential.

Whenever the OCP comparator is not triggered inside the minimum on-time, a switching cycle is restored, thus doubling the switching frequency up to the nominal frequency F_{OSC}.

Pulse skipping and F_{OSC} restoration are evident in *Figure 14: "startup at 115VAC, full load (zoom)"* and *Figure 16: "startup at 115VAC, full load (zoom)"*.

Figure 13: startup at 115 V_{AC}, full load

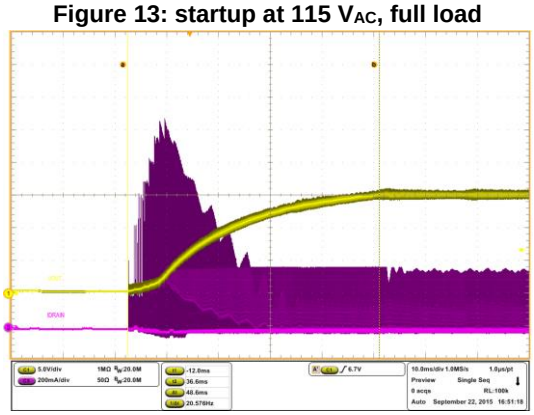


Figure 14: startup at 115 V_{AC}, full load (zoom)

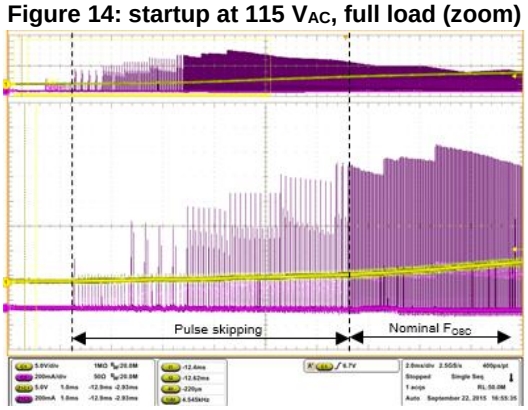


Figure 15: startup at 115 V_{AC}, full load

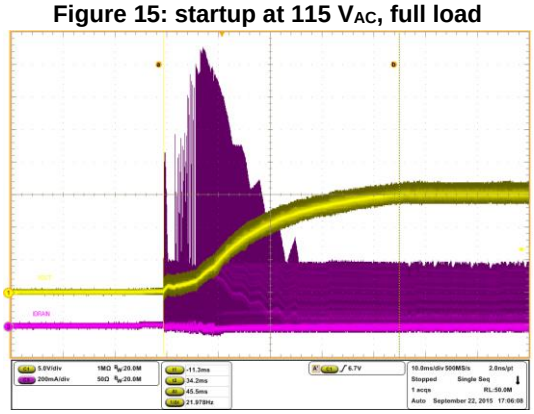
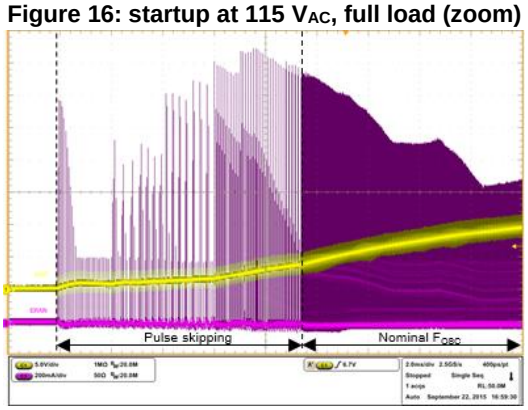


Figure 16: startup at 115 V_{AC}, full load (zoom)



The effect of pulse skipping feature is shown in *Figure 17: "Max. peak current at VIN = 115 VAC, startup under full load"* and *Figure 18: "Max. peak current at VIN = 230 VAC, startup under full load"*, where the maximum value reached by the peak current at startup is quite low for both 115 V_{AC} and 230 V_{AC}.

Figure 17: Max. peak current at V_{IN} = 115 V_{AC}, startup under full load

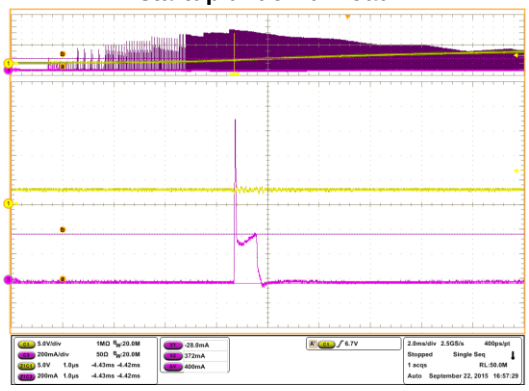
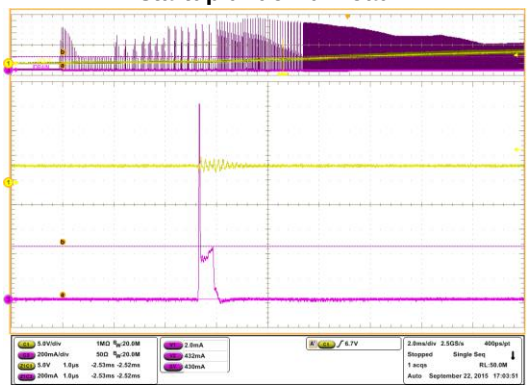


Figure 18: Max. peak current at V_{IN} = 230 V_{AC}, startup under full load



6.2 Overload protection (OLP)

During an overload or short circuit, the drain current reaches I_{DLIM} (see *Figure 19: "Output overload applied: OLP tripping"*). For every cycle that this condition is met, an internal OCP counter is incremented and the protection is tripped if the fault is maintained for a set time, which ranges from a minimum of 50 ms when pulse skipping is never invoked and the switching frequency is always the nominal 60 kHz F_{OSC}, to a maximum of 200 ms when pulse skipping is always invoked, and the OCP counter is incremented at ¼ of the nominal F_{OSC}.

The approximate overload duration in the figures below is 180 ms, with the magnified *Figure 23: "Output overload maintained: skipping frequency"* showing both 15 and 30 kHz cycles.

If the short is removed before the protection is tripped, the counter decrements each cycle down to zero and the protection is not tripped.

On protection tripping, the power section is turned off and the converter is disabled for $t_{RESTART}$ (1 s typ.), after which the IC resumes switching and, if the fault persists, continues

triggering the protection in the same way (see *Figure 20: "Output overload maintained: OLP steady-state"*). This lowers the restart attempt rate to ensure safe operation with extremely low power throughput and avoids IC overheating. Furthermore, every time the protection is tripped, the internal soft-start function is invoked at restart.

If the short circuit is removed during $t_{RESTART}$, the IC waits for the $t_{RESTART}$ period to elapse before resuming switching (*Figure 24: "Output overload removal and converter restart"*).

Figure 19: OVL applied: OLP tripping

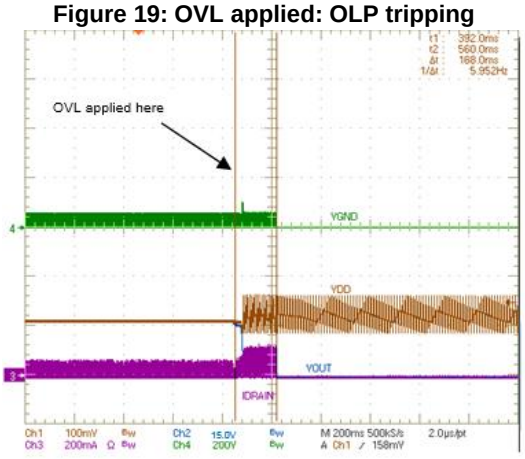


Figure 20: OVL maintained: OLP steady-state

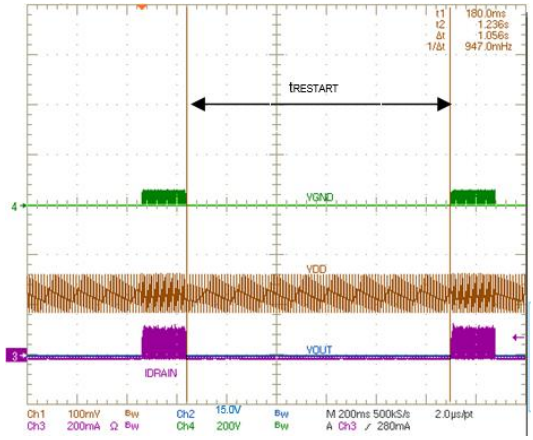


Figure 21: OVL maintained: OLP steady-state (zoom 1)

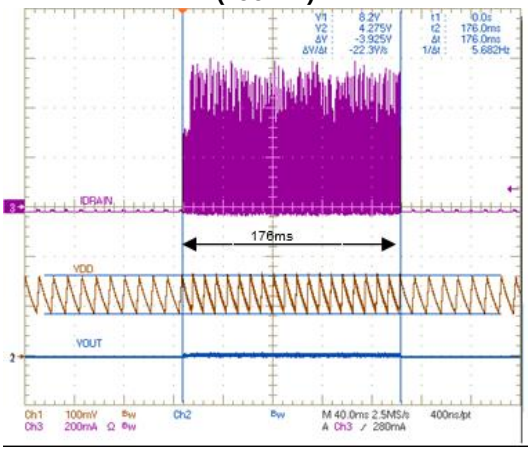


Figure 22: OVL maintained: OLP steady-state (zoom 2)

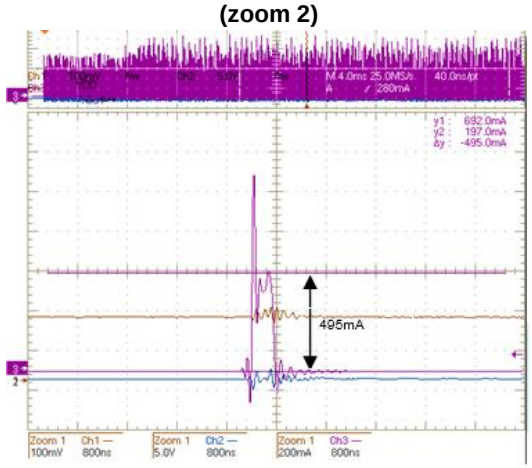


Figure 22: "OVL maintained: OLP steady-state (zoom 2)" shows how the pulse skipping feature limits the highest DRAIN current peak to below 500 mA.

Figure 23: OVL maintained: skipping frequency

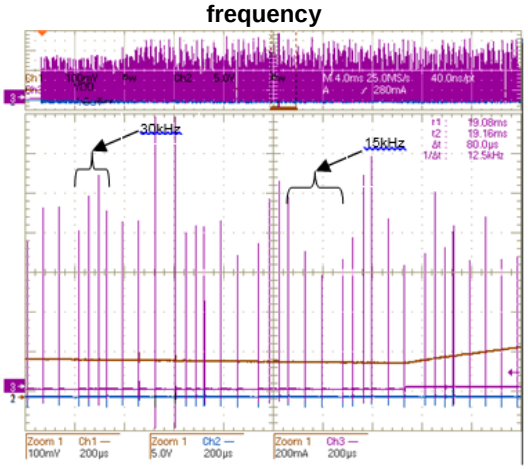
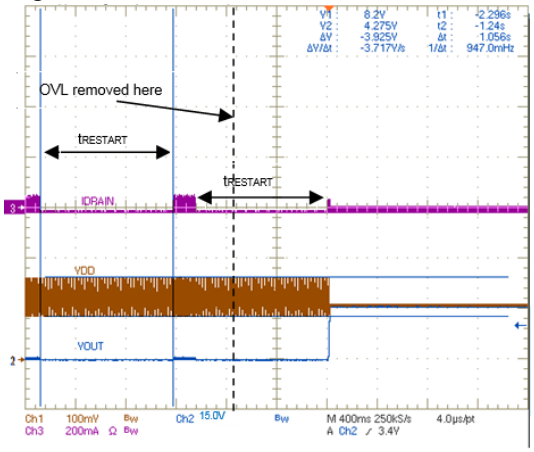


Figure 24: OVL removal and converter restart

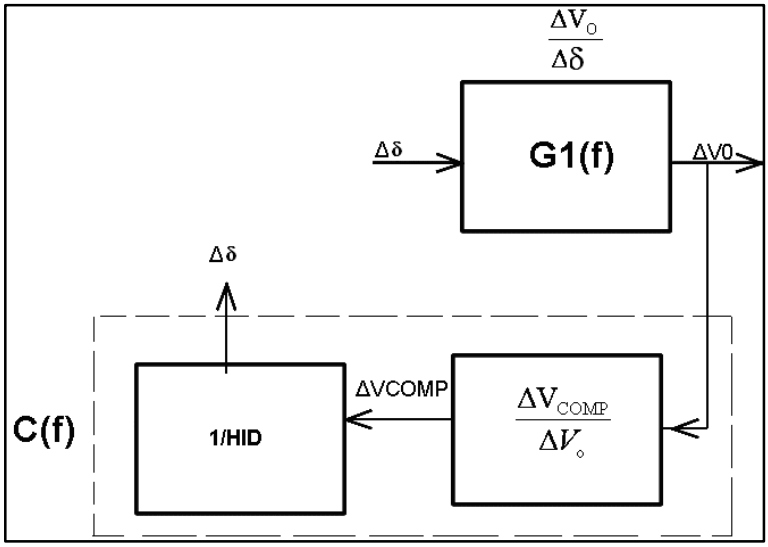


7 Feedback loop calculation guidelines

7.1 Transfer function

In the following figure, G1(f) represents the set PWM modulator plus power stage, while C(f) is the “controller” network which ensures system stability.

Figure 25: Control loop block diagram



The mathematical expression for the power plant G1(f) in DCM is:

Equation 2

$$G1(f) = \frac{\Delta V_{OUT}}{\Delta \partial} = G10 \cdot \frac{1 + \frac{j \cdot f}{fZ}}{1 + \frac{j \cdot f}{fP}}$$

where fz is the zero due to the ESR of the output capacitor:

Equation 3

$$fz = \frac{1}{2 \cdot \pi \cdot Cout \cdot ESR}$$

and fp is the pole due to the output load:

Equation 4

$$fp = \frac{1 + ß \cdot Rout}{2 \cdot \pi \cdot Cout \cdot (ESR + Rout + ESR \cdot ß \cdot Rout)}$$

with:

Equation 5

$$a = \frac{V_{IN} + V\gamma}{(V_{OUT} + V\gamma)} \cdot \frac{Ipk}{2}$$

Equation 6

$$ß = \frac{V_{IN} + V\gamma}{(V_{OUT} + V\gamma)^2} \cdot \frac{Ipk}{2} \cdot \partial$$

Equation 7

$$G10 = \frac{a \cdot Rout}{1 + ß \cdot Rout} = \frac{(V_{OUT} + V\gamma) \cdot (V_{IN} + V\gamma) \cdot \frac{Ipk}{2} \cdot Rout}{(V_{OUT} + V\gamma)^2 + (V_{IN} + V\gamma) \cdot \frac{Ipk}{2} \partial \cdot Rout}$$

In the above formulas, Cout and ESR are the capacitance and the equivalent series resistance of the output capacitor respectively, Vy is the forward drop of the free-wheeling diode, Rout = Vout/Iout is the output load, Ipk is the drain peak current at full load and δ = Ton•fsw is the duty cycle.

If the compensation network consists of an RC series only as shown in *Figure 2: "Application schematic diagram"* (C5 and C6 not mounted), the mathematical expression for the compensator C(f) is:

Equation 8

$$C(s) = \frac{C_0}{H_{COMP}} \cdot \frac{(1 + \frac{j \cdot f}{fzc})}{j \cdot 2 \cdot \pi \cdot f}$$

where:

Equation 9

$$C_0 = \frac{L \cdot fsw}{V_{in} - V_{OUT}} \cdot (\frac{-G_M}{C7}) \cdot \frac{R3}{R3 + R4 + R6}$$

and…

Equation 10

$$fzc = \frac{1}{2 \cdot \pi \cdot R2 \cdot C7}$$

are chosen in order to ensure the stability of the overall system.

G_M is the VIPer0P transconductance specified in the datasheet; H_{COMP} = (V_{COMPH} - V_{COMPL})/(I_{DLIM} – I_{DLIM_PFM}) is the slope of the V_{COMP} vs I_{DRAIN} characteristic.

7.2 Compensation procedure for a DCM buck

The first step is to choose the pole and zero of the compensator and the crossing frequency.

In this case C(f) has only a zero (fzc) and a pole at the origin, thus a possible setting is:

fzc = x•fp

fcross = fcross_sel ≤ fsw/10

where “x” can be chosen arbitrarily

After setting fcross, G1(fcross_sel) can be calculated from *Equation 2* and, since by definition it is $\left| C(fcross\_sel)*G1(fcross\_sel) \right| = 1$, C_0 can be calculated as follows:

Equation 11

$$C_0 = \frac{|j \cdot 2 \cdot \pi \cdot fcross\_sel|}{|1 + \frac{j \cdot fcross\_sel}{fzc}|} \cdot \frac{H_{COMP}}{|G1(fcross\_sel)|}$$

At this point the Bode diagram for G1(f)*C(f) can be plotted to check the phase margin for stability.

If the margin is not high enough, choose new fzc and fcross_sel values and repeat the procedure.

When the stability is ensured, the next step is to find the values of the schematic components, which can be calculated as follows.

From *Equation9*:

Equation 12

$$C7 = \frac{L \cdot fsw}{V_{in} - V_{OUT}} \cdot \left(\frac{|-G_M|}{C_0}\right) \cdot \frac{R3}{R3 + R4 + R6}$$

and from *Equation10*:

Equation 13

$$R2 = \frac{1}{2 \cdot \pi \cdot fzc \cdot C7}$$

The quantities found in equations *Equation12* and *Equation13* are suggested values. Using commercial values we will call C7_act and R2_act, results in fzc_act:

Equation 14

$$fzc\_act = \frac{1}{2 \cdot \pi \cdot R2\_act \cdot C7\_act}$$

Also the value of C_0 will be recalculated from (9):

Equation 15

$$C_0\_act = \frac{L \cdot fsw}{V_{in} - V_{OUT}} \cdot \left(\frac{-G_M}{C7\_act}\right) \cdot \frac{R3}{R3 + R4 + R6}$$

And the compensator becomes:

Equation 16

$$C\_act(\mathrm{f}) = \frac{C_0\_\mathrm{act}}{H_{COMP}} \cdot \frac{\left(1 + \frac{f}{f\mathrm{zc\_act}}\right)}{\mathrm{j} \cdot 2 \cdot \pi \cdot \mathrm{f}}$$

At this point the Bode diagram for G1(f)*C_act(f) should be plotted to determine whether the phase margin for stability is maintained.

8 Thermal measurements

Thermal analysis of the board was performed using an IR camera at 85 V_{AC}, 115 V_{AC}, 230 V_{AC} and 265 V_{AC} mains input, full load condition and external biasing. The results are shown in the following figures, where “A” indicates the highest temperature point (VIPer0P) and “B” represents ambient temperature.

Figure 26: Thermal measurements by IR camera at V_{IN} = 85 V_{AC}, full load, T = 25°C

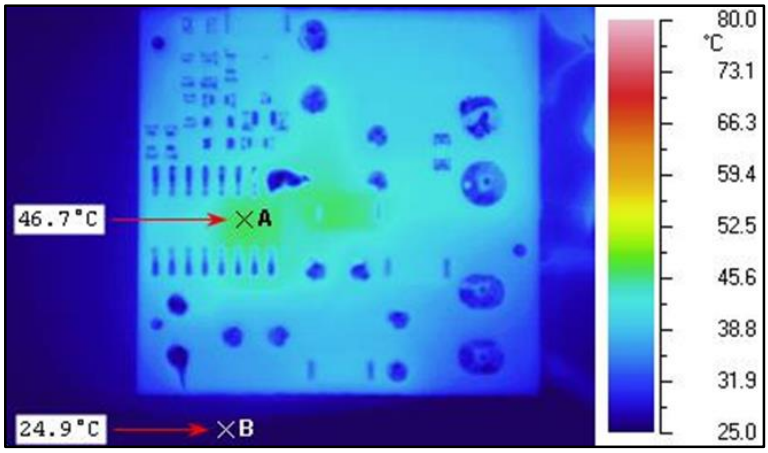


Figure 27: Thermal measurements by IR camera at V_{IN} = 115 V_{AC}, full load, T = 24°C

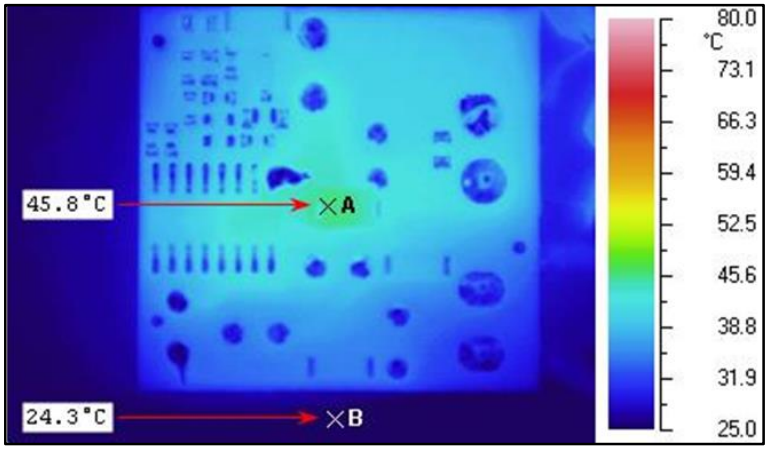


Figure 28: Thermal measurements by IR camera at V_{IN} = 230 V_{AC}, full load, T = 24°C

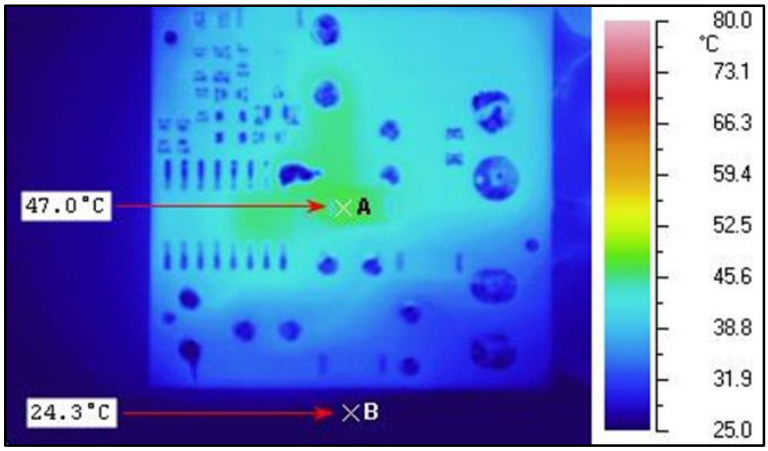
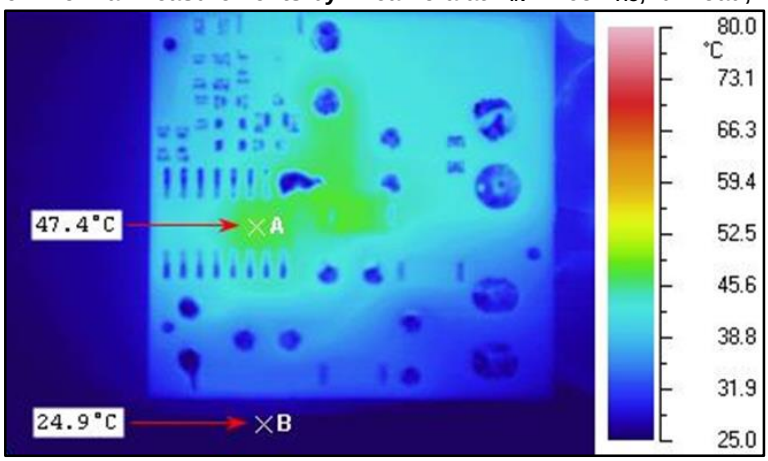


Figure 29: Thermal measurements by IR camera at V_{IN} = 265 V_{AC}, full load, T = 25°C



9 EMI measurements

A pre-compliance test for European normative EN55022 (Class B) was performed using an EMC analyzer with average detector and a line impedance stabilization network (LISN).

Figure 30: EMI measurements with average detector at 115 V_{AC}, full load, supply from output, T = 25°C

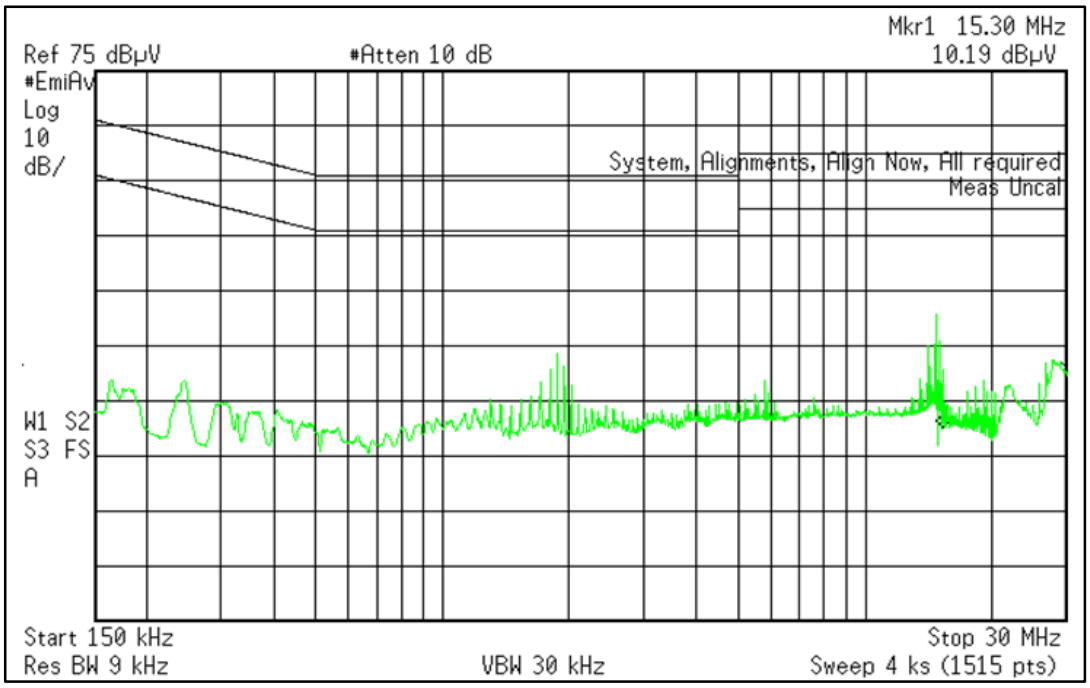
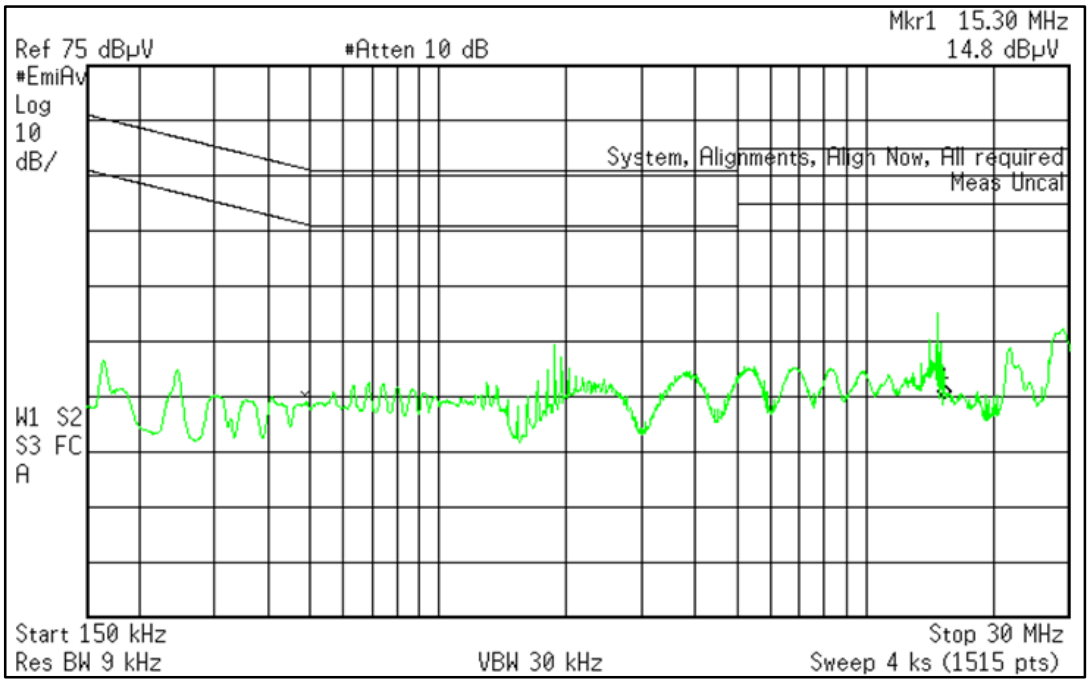


Figure 31: EMI measurements with average detector at 230 V_{AC}, full load, supply from output, T = 25°C



10 Conclusions

The VIPer0P simplifies the design of non-isolated converters and reduces the amount of external components required.

We have described and characterized a buck converter, with particular focus on light load performance. The resulting empirical data compared favorably with the energy star program (version 2.0) requirements for external AC/DC adapters, as measured active mode efficiency always exceeded minimum requirements.

11 Revision history

Table 8: Document revision history

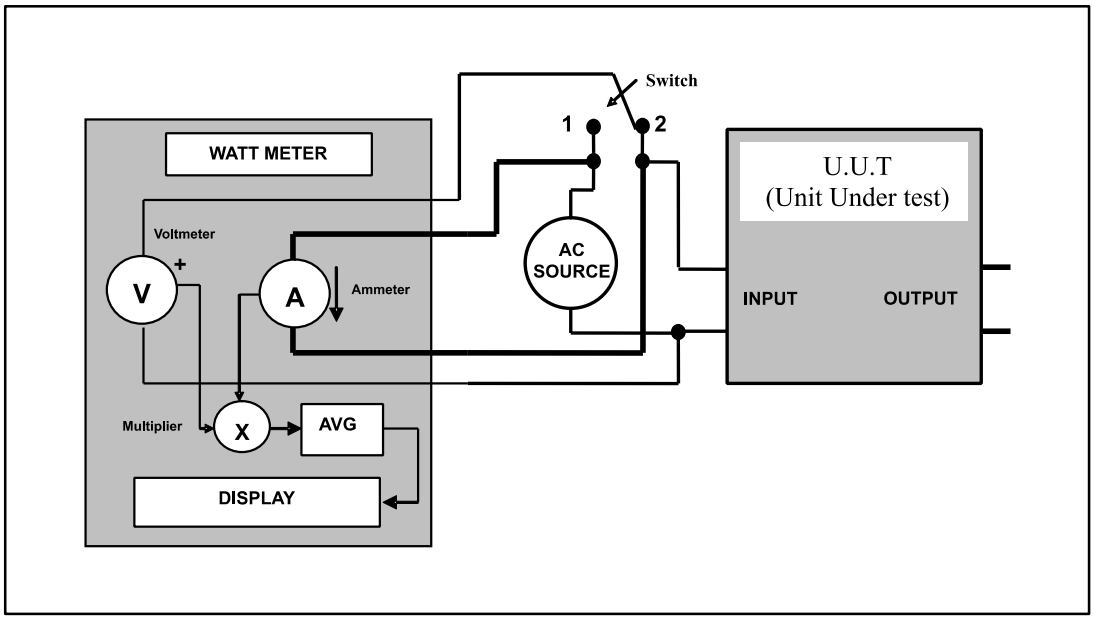
Date	Version	Changes
03-May-2016	1	Initial release.

Appendix A Test equipment and measurement of efficiency and low load performance

The converter input power is measured using a wattmeter. The wattmeter simultaneously measures the converter input current (using its internal ammeter) and voltage (using its internal voltmeter). The digital wattmeter samples the current and voltage and converts them in digital formats, which are then multiplied to give the instantaneous measured power. The sampling frequency is in the range of 20 kHz or higher and the average measured power over a short interval (1 s typ.) is displayed.

The following figure shows the wattmeter connection to the UUT (unit under test) and AC source, as well as the wattmeter internal block diagram.

Figure 32: Connections of the UUT to the wattmeter for power measurements



An electronic load is connected to the output of the power converter (UUT), allowing the converter load current to be set and measured, while the output voltage is measured by a voltmeter. The output power is the product between load current and output voltage.

The ratio between the above output power calculation and the input power measured by the wattmeter is the converter's efficiency, measured under different input/output conditions.

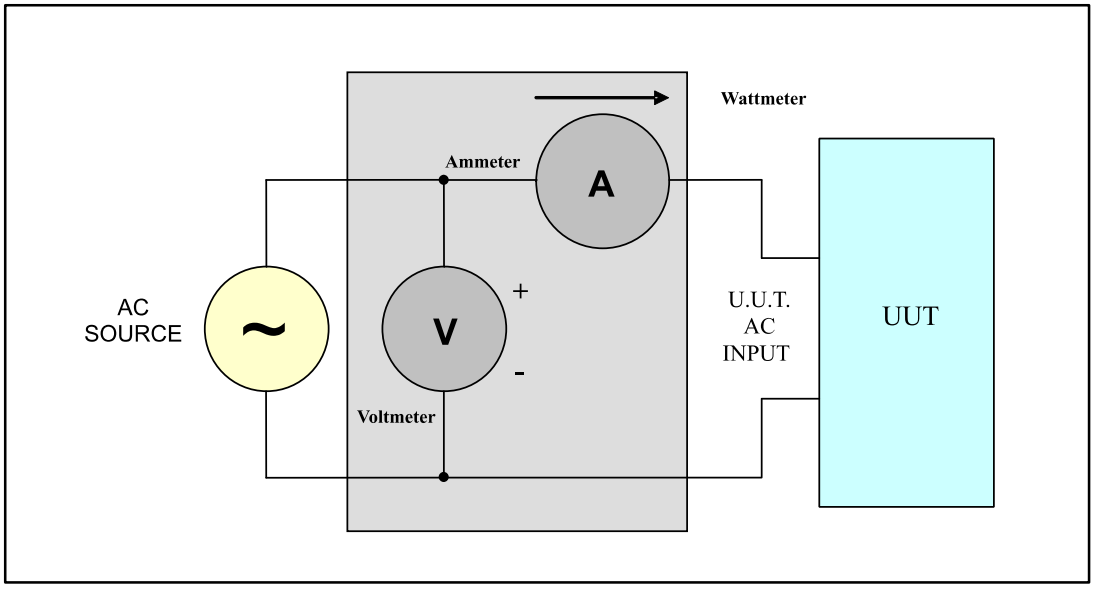
Considerations when measuring input power

With reference to *Figure 32: "Connections of the UUT to the wattmeter for power measurements"*, the UUT input current causes a voltage drop across the ammeter internal shunt resistance (the ammeter is not ideal as it has an internal resistance higher than zero) and across the cables connecting the wattmeter to the UUT.

If the switch in *Figure 32: "Connections of the UUT to the wattmeter for power measurements"* is in position 1 (see the simplified schematic below) this voltage drop causes an input measured voltage higher than the input voltage at the UUT input, which of

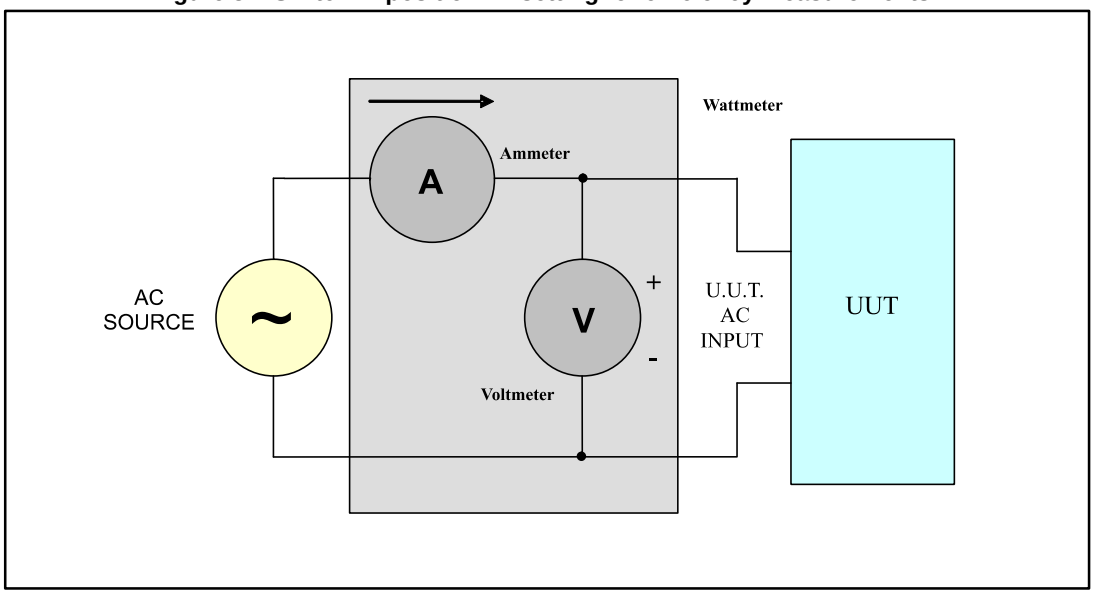
course distorts the measured power. The voltage drop is generally negligible if the UUT input current is low (e.g., the input power of UUT under low load condition).

Figure 33: Switch in position 1 - setting for standby measurements



For high UUT input currents (e.g., heavy load conditions), the voltage drop compared to the UUT real input voltage can become significant. In this case, the switch in *Figure 32: "Connections of the UUT to the wattmeter for power measurements"* should be set to position 2 (see the simplified schematic below), where the UUT input voltage is measured directly at the UUT input terminal and the input current does not affect the measured input voltage.

Figure 34: Switch in position 2 - setting for efficiency measurements



On the other hand, the arrangement in *Figure 34: "Switch in position 2 - setting for efficiency measurements"* may introduce a relevant error during light load measurements, when the UUT input current is low and the leakage current inside the voltmeter itself (not having infinite input resistance) is not negligible. This is why it is better to use the *Figure*

33: "Switch in position 1 - setting for standby measurements" arrangement for light load measurements and *Figure 34: "Switch in position 2 - setting for efficiency measurements"* for heavy loads.

If you are not certain which arrangement distorts the result less, try both and record the lower input power value.

As noted in IEC 62301, instantaneous measurements are appropriate when power readings are stable. The UUT shall be operated at 100% of nameplate output current output for at least 30 minutes (warm up period) immediately prior to conducting efficiency measurements.

After this warm-up period, the AC input power shall be monitored for a period of 5 minutes to assess the stability of the UUT. If the power level does not drift by more than 5% from the maximum value observed, the UUT can be considered stable and the measurements can be recorded at the end of the 5 minute period. If AC input power is not stable over a 5 minute period, the average power or accumulated energy shall be measured over time for both AC input and DC output.

Some wattmeter models allow integrating the measured input power over a time range and measuring the energy absorbed by the UUT during the integration time. Dividing by the integration time itself gives the average input power.

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