SLLIMM™-nano MOSFET small low-loss intelligent molded modules

Introduction

The SLLIMM™-nano (small low-loss intelligent molded module) MOSFET series is ST's new family of very compact, high-efficiency, dual-in-line intelligent power modules with optional extra features. This series is provided in the NDIP (SLLIMM-nano) and N2DIP (SLLIMM-nano 2nd series) packages, and targets appliances such as dishwashers, refrigerator compressors, air conditioning fans, dryers, ceiling fans, drain and recirculation pumps as well as low-power industrial applications, for instance small fans, pumps and tools.

This new series combines optimized silicon chips, integrated in three main inverter blocks:

- Power stage
  - six MOSFETs with fast body diode
- Driving network
  - three high-voltage gate drivers
  - dedicated turn-on and turn-off gate driving network
  - three bootstrap diodes
- Protection and optional features
  - op-amp for advanced current sensing
  - comparator for fault protection against overcurrent and short-circuit
  - NTC thermistor
  - dead-time, interlocking function and undervoltage lockout

Thanks to their great compactness, the fully isolated packages (NDIP and N2DIP) are the ideal solution for applications requiring reduced assembly space even with heatsink, without sacrificing thermal performance and reliability.

The aim of this application note is to provide a detailed description of the SLLIMM-nano UltraFAST MOSFET and SLLIMM-nano 2nd series MDmesh™ DM2 MOSFET products, providing the guidelines to motor drive designers for an efficient, reliable, and fast design when using this new ST SLLIMM-nano series.

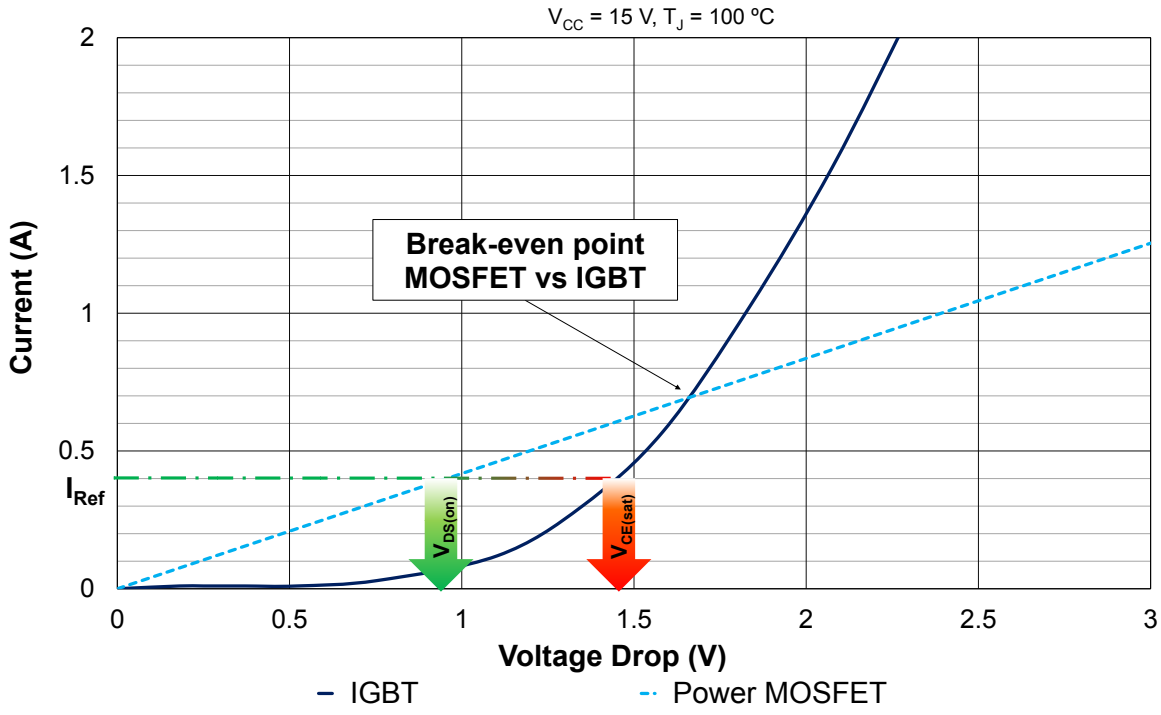
1 Major advantages of the MOSFET technology

The emergence of MOSFET-based intelligent power modules is the result of continuous improvements in the development of more efficient, low-loss MOSFET switching transistors.

The main household appliances target the best energy class to increase energy saving. One of the most important requirements in these applications is the power loss reduction during the steady state operation. This leads designers to select power switches which offer low loss mainly at low-load conditions, but are still capable of providing the necessary current under high-load conditions.

The MOSFET technology benefits of a forward voltage ($V_{DS(on)}$) which decreases linearly with the drain current, whilst in the IGBT the voltage drop ($V_{CE(sat)}$) is not linear with the collector current. It shows a threshold voltage (knee) before getting the on-state, and saturates with an almost constant forward drop above a certain collector current. Thanks to their static characteristics, Power MOSFETs offer lower conduction loss than IGBTs at a low-current level, as shown in the following figure.

Figure 1. MOSFETs and IGBTs static characteristics comparison



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Furthermore, MOSFETs offer very fast turn-off commutation since they are unipolar devices without minority carriers and their intrinsic body diode has been optimized to significantly reduce the reverse recovery energy, which is one of the main sources of power loss impacting also the MOSFET turn-on energy.

The intrinsic body diode of the MOSFETs replaces the need for a separate freewheeling diode, as required for IGBT-based modules. This reduces the complexity of the module assembly and improves overall reliability.

Finally, MOSFETs can offer lower conduction loss, mainly at low-current level, very low turn-off energy and minimal turn-on energy depending on the technology process used to make the body diode fast.

1.1 Product synopsis and block diagram

The SLLIMM-nano MOSFET series has been designed to satisfy the requirements of a wide range of final applications up to 300 W, such as:

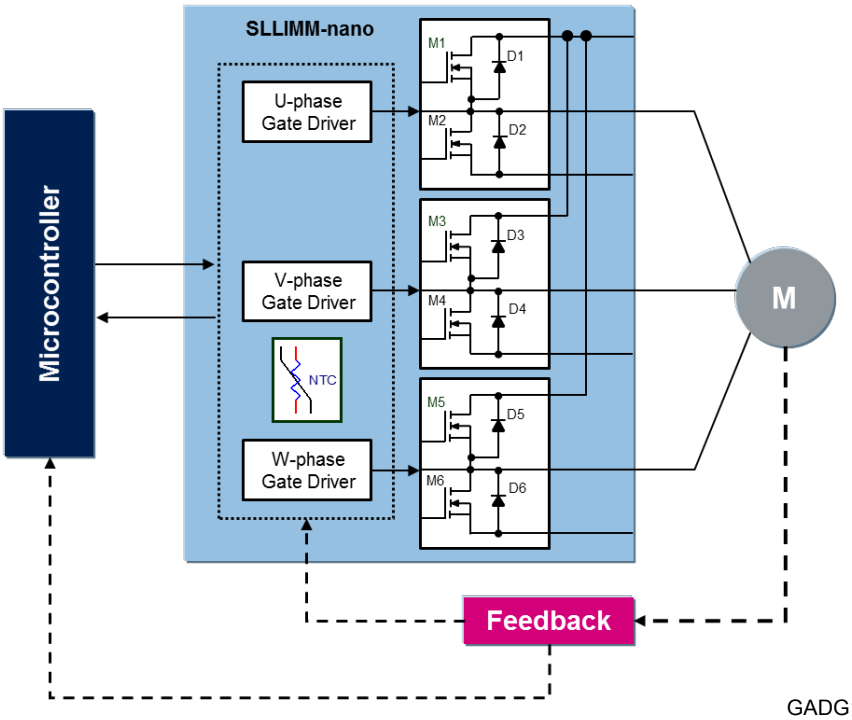
- refrigerator compressors
- dishwashers
- air conditioning fans
- dryers
- draining and recirculation pumps
- low-power industrial applications
- small fans, pumps and tools

The main features and integrated functions can be summarized as follows:

- 500 V, 1 and 2 A ratings (SLIMM-nano in NDIP package)
- 600 V, 3 and 5 A ratings (SLLIMM-nano 2nd series in N2DIP package)
- 3-phase MOSFET inverter bridge including:
  - six MOSFETs with fast body diode
- three control ICs for gate driving and protection including:
  - comparator for fault protection against overcurrent and short-circuit
  - op-amp for advanced current sensing
  - three integrated bootstrap diodes
  - interlocking function
  - undervoltage lockout
  - NTC thermistor (optional)
- open emitter configuration for individual phase current sensing
- very compact and fully isolated package
- integrated gate driving network for optimum MOSFET switching speed setting
- proper biasing of gate driver

The following figure shows the block diagram of the SLLIMM-nano included in the inverter solution.

Figure 2. SLLIMM-nano block diagram



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The MOSFETs incorporated in the half-bridge block are tailored for motor drive applications, delivering the greatest overall efficiency, thanks to the optimized trade-off between conduction and switching power loss, and limiting EMI generation.

The IC gate drivers are of a fully featured version which provides advanced options for a sophisticated control method and protection. The fully isolated NDIP/N2DIP packages offer a high level of compactness, very useful applications with reduced space, while maintaining a high thermal performance and reliability level.

1.2 Product line-up and nomenclature

Table 1. **SLLIMM-nano MOSFET in NDIP package line-up**

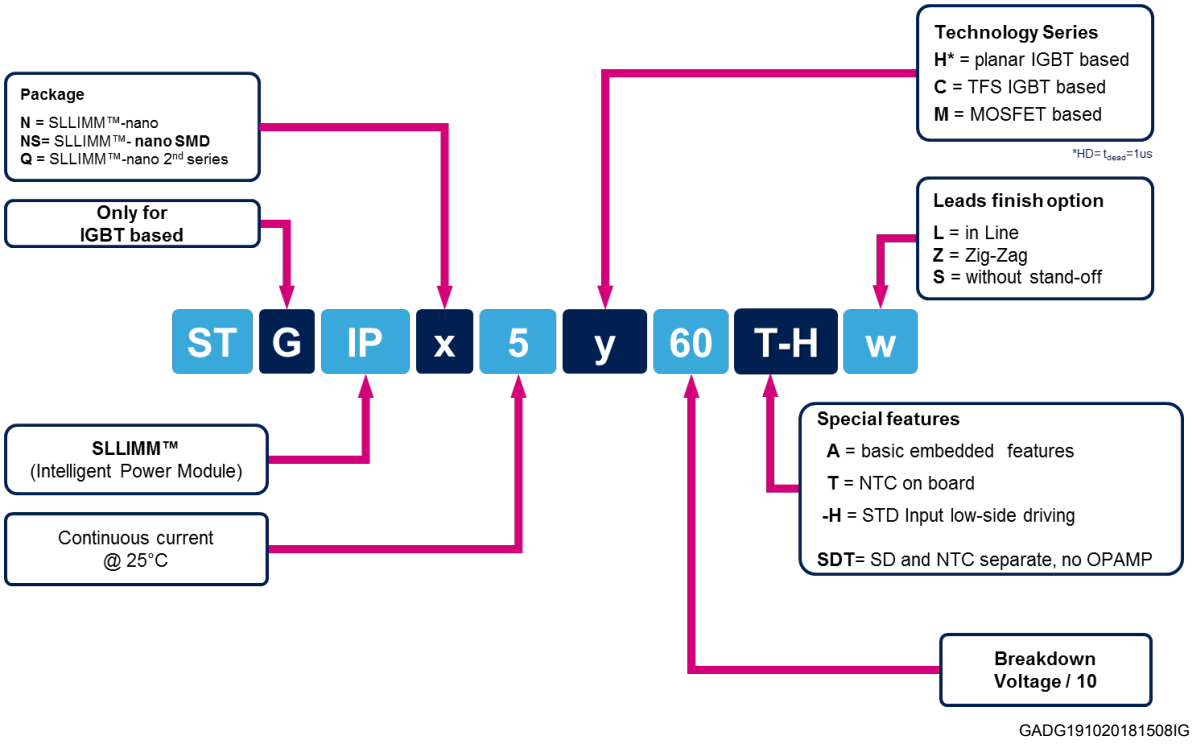
Features	STIPN1M50x-Hy	STIPN2M50x-Hy
Powerswitch technology	Ultrafast MOSFET	Ultrafast MOSFET
Voltage (V)	500	500
Current @ T_C = 25 °C (A)	1	2
$R_{th(j-c)}$ max (°C/W)	13	12
Package type	NDIP-26L	NDIP-26L
Package size (mm) X, Y, Z	29.15x12.45x3.1	29.15x12.45x3.1
Integrated bootstrap diode	Yes	Yes
SD function	Yes	Yes
Comparator for fault protection	Yes	Yes
Op-amp for advanced current sensing	Yes	Yes
Interlocking function	Yes	Yes
Undervoltage lockout	Yes	Yes
Open emitter configuration	Yes (3 pins)	Yes (3 pins)
NTC thermistor	Yes (except for STIPN1M50-H)	Yes (except for STIPN2M50-H)
3.3/5 V input interface compatibility	Yes	Yes
High-side IGBT input signal	Active high	Active high
Low-side IGBT input signal	Active high	Active high
V_{ISO} (V) (AC voltage, t = 60 s)	1000	1000
Lead option	Zig-zag (STIPN1M50x-H)	In-line (STIPN2M50x-HL) Zig-zag (STIPN2M50x-H)

Table 2. SLLIMM-nano 2nd series MOSFET in N2DIP package line-up

Features	STIPQ3M60T-Hx	STIPQ5M60T-Hx
Power switch type	MDmesh™ DM2 MOSFET	MDmesh™ DM2 MOSFET
Voltage (V)	600	600
Current @ T_C = 25 °C (A)	3	5
$R_{th(j-c)}$ max (°C/W)	10.7	9.8
Package type	N2DIP-26L	N2DIP-26L
Package size (mm) X, Y, Z	32.15x12.45x4.1	32.15x12.45x4.1
Integrated bootstrap diode	Yes	Yes
SD function	Yes	Yes
Comparator for fault protection	Yes	Yes
Op-amp for advanced current sensing	Yes	Yes
Interlocking function	Yes	Yes
Undervoltage lockout	Yes	Yes
Open emitter configuration	Yes (3 pins)	Yes (3 pins)
NTC thermistor	Yes	Yes
3.3/5 V input interface compatibility	Yes	Yes
High-side IGBT input signal	Active high	Active high
Low-side IGBT input signal	Active high	Active high
V_{ISO} (V) (AC voltage, t = 60 s)	1500	1500
Lead option	In-line (STIPQ3M60T-HL) Zig-zag (STIPQ3M60T-HZ)	In-line (STIPQ5M60T-HL) Zig-zag (STIPQ5M60T-HZ)

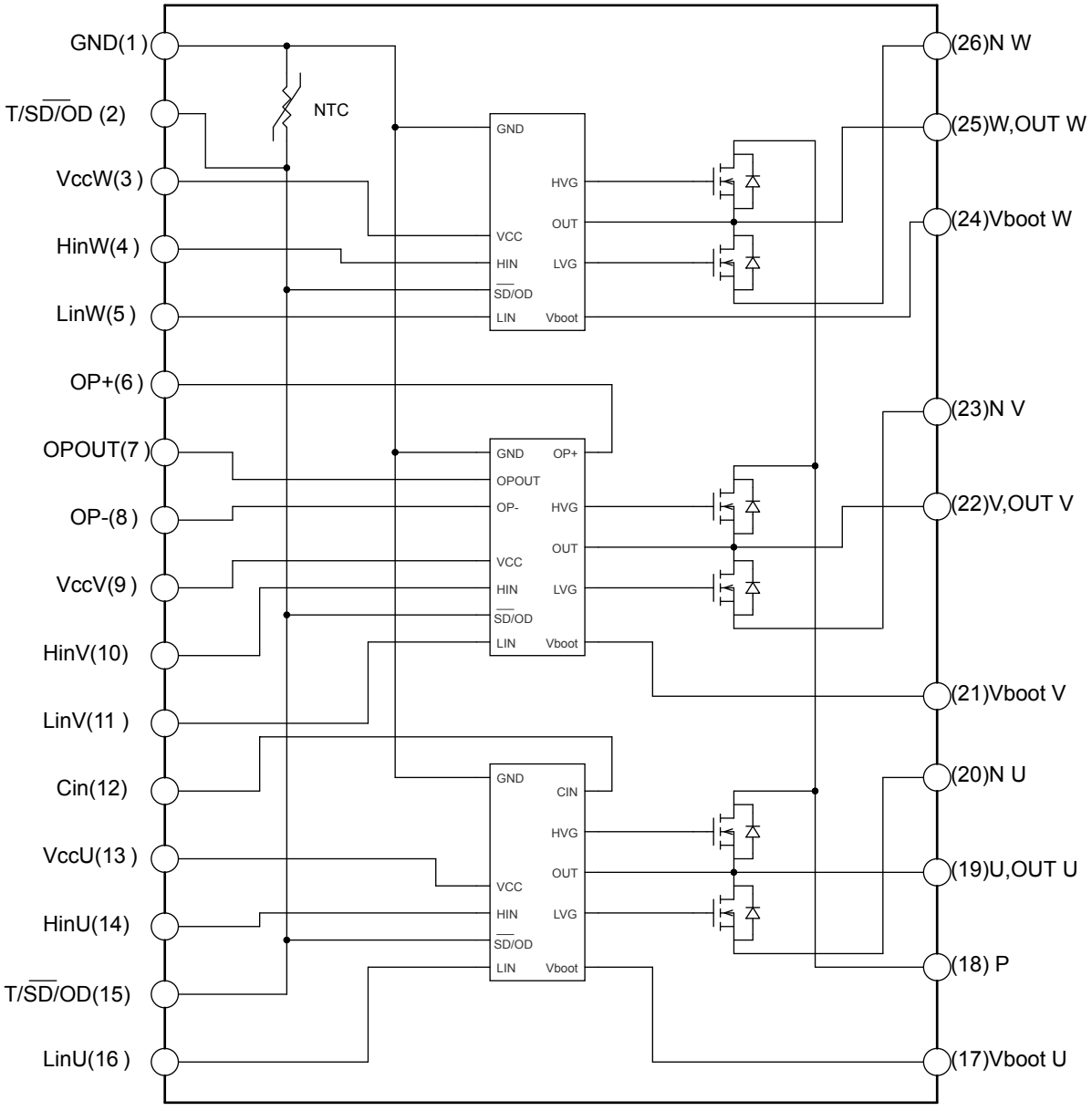
Note: Please refer to www.st.com for the complete product portfolio.

Figure 3. **SLLIMM-nano nomenclature**



1.3 Internal circuit

Figure 4. Internal circuit



Note: STIPN1M50-H and STIPN2M50-H do not have an internal NTC.

1.4 Absolute maximum ratings

The absolute maximum ratings represent the extreme capability of the device and can be normally used as a worst case design limit condition. It is important to note that the absolute maximum values are given according to a set of testing conditions such as temperature, frequency, voltage. The device performance can change according to the applied condition.

For the specifications described below, the STIPQ5M60T-Hx datasheet has been used as an example. Please refer to the respective product datasheets for a detailed description of all types.

Table 3. Inverter part

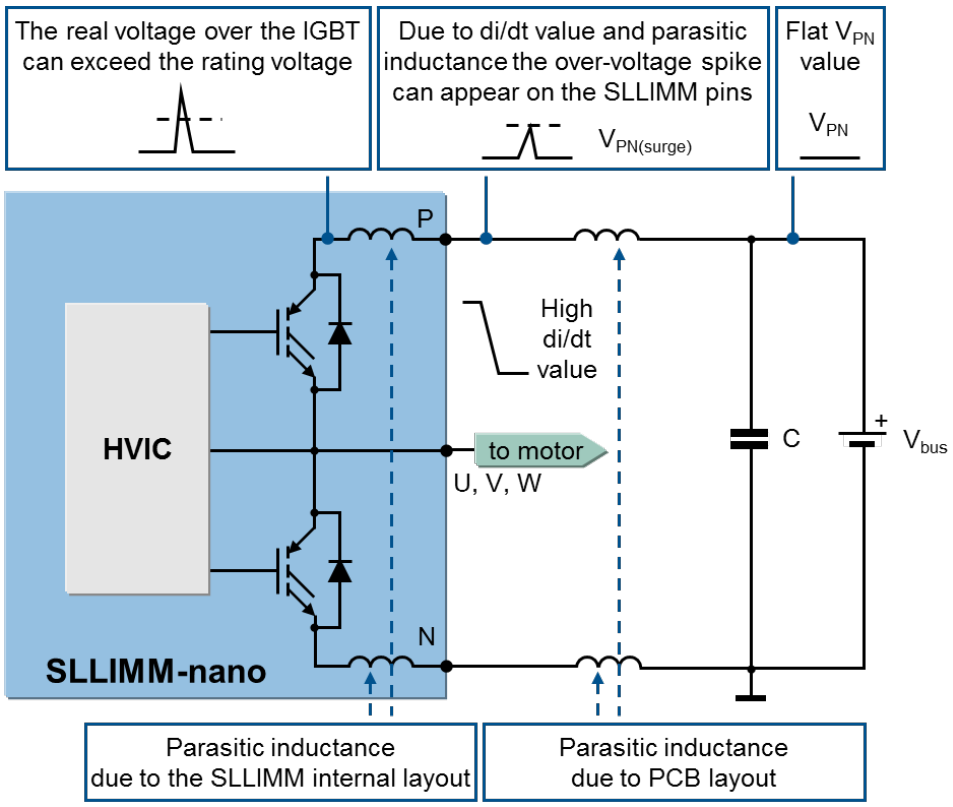
Symbol	Parameter	Value	Unit
V_{DSS}	MOSFET blocking voltage (or drain-source voltage)(1)	600	V
± I_D	Continuous current for each MOSFET	5	A
± I_{DP} (2)	Peak drain current for each MOSFET (less than 1 ms)	10	A
P_{TOT}	Total power dissipation at T_C = 25 °C for each MOSFET	12.8	W

1. *Applied among HINx, LINx and GND for x = U, V, W.*
2. *Pulse width limited by maximum junction temperature.*

- V_{DSS}: MOSFET blocking voltage (or drain-source voltage) for each MOSFET

The power stage is based on MOSFETs having 500-600 V_{DS} rating. Generally, considering the intelligent power module's internal stray inductances during commutations which can generate surge voltages, the maximum allowed surge voltage between P-N ($V_{PN(surge)}$) is lower than V_{DS}, as shown in the figure belows. At the same time, considering also the surge voltage generated by the stray inductance between the device and the DC-link capacitor, the maximum supply voltage (in steady-state) applied between P-N (V_{PN}) must be even lower than $V_{PN(surge)}$.Thanks to the small package size and the lower working current, this phenomenon is less marked in the SLLIMM-nano series than in the larger intelligent power modules.

Figure 5. Stray inductance components of the output stage



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- I_D: Continuous drain current for each MOSFET

  I_D is the allowable DC current continuously flowing at the drain electrode.

Table 4. Control part

Symbol	Parameter	Value	Unit
V_{CC}	Low voltage power supply	-0.3 to 21	V
V_{boot}	Bootstrap voltage	-0.3 to 620	V
V_{OUT}	Output voltage applied between OUT_U, OUT_V,OUT_W and GND	V_{boot} -21 to V_{boot} + 0.3	V
V_{CIN}	Comparator input voltage	-0.3 to V_{CC} + 0.3	V
V_{IN}	Logic input voltage applied among HINx, LINx and GND	-0.3 to 15	V
$V_{T/\overline{SD}/OD}$	Open drain voltage	-0.3 to 15	V
$\Delta V_{OUT/dT}$	Allowed output slew rate	50	V/ns

- V_{CC}: Low voltage power supply

V_{CC} represents the supply voltage of the control part. Local filtering is recommended to enhance noise immunity.

Generally, the use of one electrolytic capacitor (with a greater value, but not negligible ESR) and one smaller ceramic capacitor (hundreds of nF), which is faster than the electrolytic capacitor to provide current, is recommended. Please refer to Table 5. Supply voltage and operating behavior below in order to properly drive the SLLIMM-nano.

Table 5. Supply voltage and operating behavior

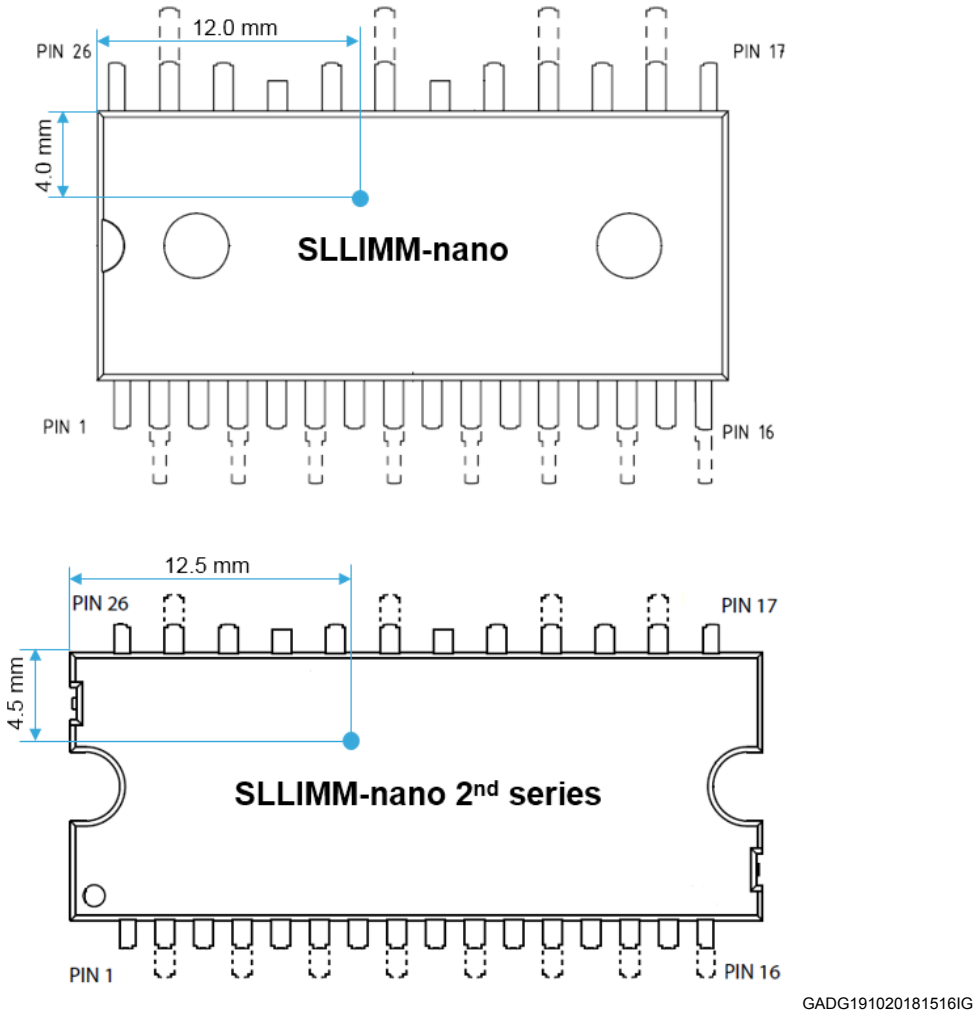
V_{CC} voltage (typical value)	Operating behavior
<12 V	As the voltage is lower than the UVLO threshold, the control circuit is not fully turned on. Perfect functionality cannot be guaranteed.
13.5 V – 18 V	Typical operating conditions
>21 V	Control circuit is destroyed

Table 6. Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 s)	1500	Vrms
T_J	Power chips operating junction temperature	-40 to 150	°C
T_C	Module case operation temperature	-40 to 125	°C

The following figure shows the case temperature measurement point for all package lead options, right above the power chip. To obtain accurate temperature information, mount a thermocouple on the heatsink surface at this specific location. For non-complementary switching schemes, the highest T_C point occurs at a different position. In this case, the measurement location is over the point where the highest power chip temperature is generated.

Figure 6. T_C measurement point (top view)



2 Electrical characteristics and functions

This section presents the main electrical characteristics of the power stage and offers a detailed description of all the MOSFET-based SLLIMM-nano functions.

2.1 MOSFETs with fast body diode

The SLLIMM-nano achieves power savings in the inverter stage thanks to the use of MOSFETs manufactured with proprietary advanced processes. These power devices are optimized for typical motor control switching frequency and offer an excellent trade-off between voltage drop (V_{DS}) and switching energy (E_{on} and E_{off}), therefore minimizing the two major sources of energy loss (conduction and switching) and reducing the environmental impact of daily-use equipment.

The improved lifetime killing process makes the intrinsic body diode faster, with good softness, and more robust. Finally, it offers very low recovery charge (Q_{rr}) and time (t_{rr}) combined with very low $R_{DS(on)}$, making it suitable for high-efficiency bridge topologies converters. A full analysis on the power loss of the complete system is reported in Section 4 Power loss and dissipation.

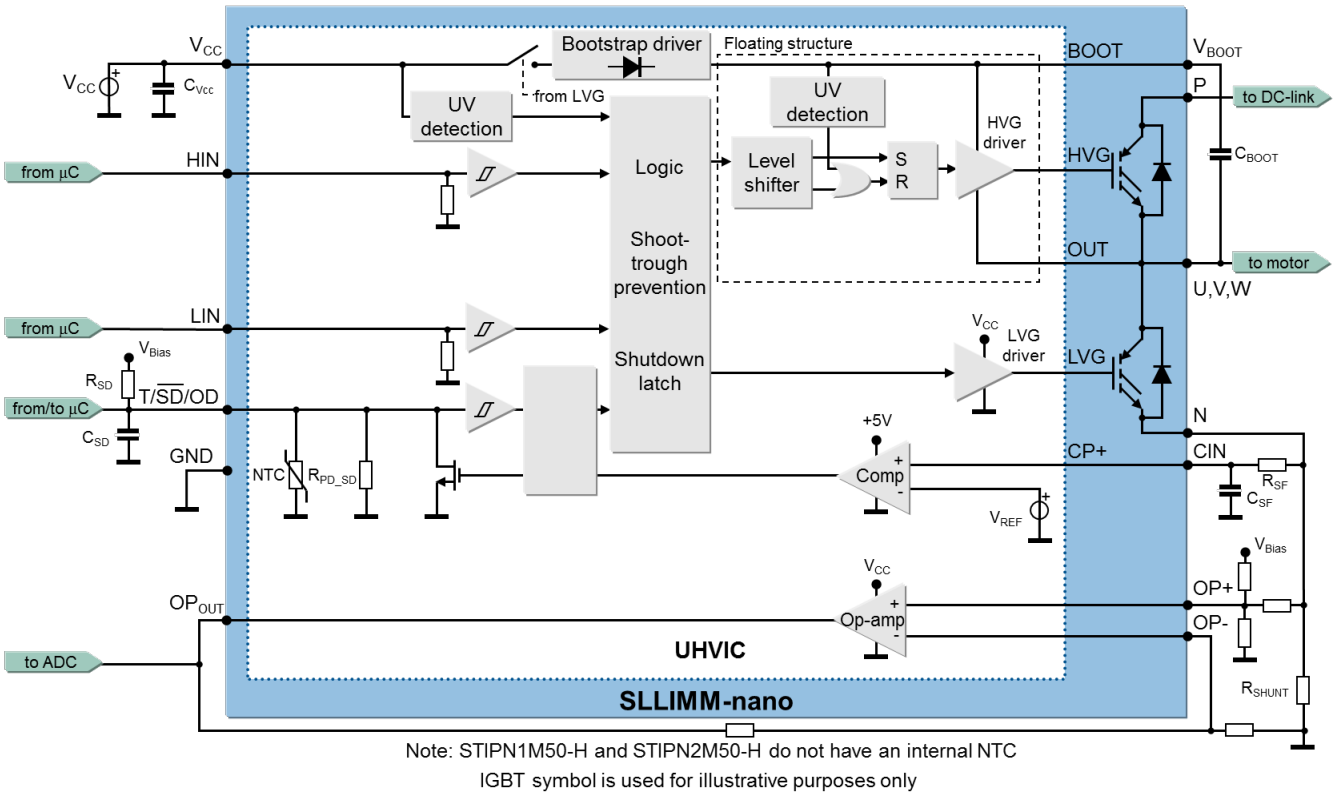
2.2 High-voltage gate drivers

The SLLIMM-nano is equipped with a versatile high-voltage gate driver IC (HVIC), which is designed using BCD offline (bipolar, CMOS and DMOS) technology and is particularly suited to field oriented control (FOC) motor driving applications. It can also provide all of the functions and the current capability required for high- and low-side MOSFET driving. This driver includes patented internal circuitry which replaces the external bootstrap diode.

Each high-voltage gate driver chip controls two MOSFETs in half-bridge topology, offering basic functions such as interlocking and an integrated bootstrap diode, but also advanced features such as the shutdown function, a fault comparator and a dedicated high-performance op-amp for advanced current sensing. Table 1. SLLIMM-nano MOSFET in NDIP package line-up and Table 2. SLLIMM-nano 2nd series MOSFET in N2DIP package line-up provide a schematic summary of the features by device.

This application note describes the main characteristics of a high-voltage gate drive related to the SLLIMM-nano. For further information, please refer to application note AN2738, available on www.st.com.

Figure 7. **High-voltage gate driver block diagram**



Note: STIPN1M50-H and STIPN2M50-H do not have an internal NTC
IGBT symbol is used for illustrative purposes only

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2.2.1 Logic inputs

All the HINx and LINx logic inputs are provided with hysteresis (~1 V) for low noise sensitivity and are TTL/CMOS 3.3 V compatible. Thanks to this low-voltage interface logic compatibility, the SLLIMM-nano can be used with any type of high-performance controller, such as microcontrollers, DSPs or FPGAs. As shown in the block diagram in Figure 7. High-voltage gate driver block diagram, the logic inputs have internal pull-down resistors in order to set a proper logic level in case of interruption in the logic lines. If logic inputs are left floating, the gate driver outputs LVG and HVG are set to low level. This simplifies the interface circuit by eliminating the six external resistors, thereby reducing costs, board space and component count.

The typical values of the integrated pull-down resistors are shown in the following table:

Table 7. **Integrated pull-down resistor values**

Input pin	Input pin logic	Internal pull-down
High-side gate driving HIN_U, HIN_V, HIN_W	Active high	375 kΩ
Low-side gate driving LIN_U, LIN_V, LIN_W	Active high	375 kΩ
T/$\overline{SD}$/OD shutdown	Active low	50 kΩ

2.2.2 High-voltage level shift

The built-in high-voltage level shift allows direct connection between the low-voltage control inputs and the high-voltage power half bridge in any power application up to 600 V. It is obtained thanks to the BCD offline technology which integrates, in the same die, bipolar devices, low- and medium- voltage CMOS for analog and logic circuitry and high-voltage DMOS transistors with a breakdown voltage in excess of 600 V. This key feature eliminates the

need for external optocouplers, resulting in a significant reduction in component count and power loss. Other advantages are high-frequency operation and short input-to-output delays.

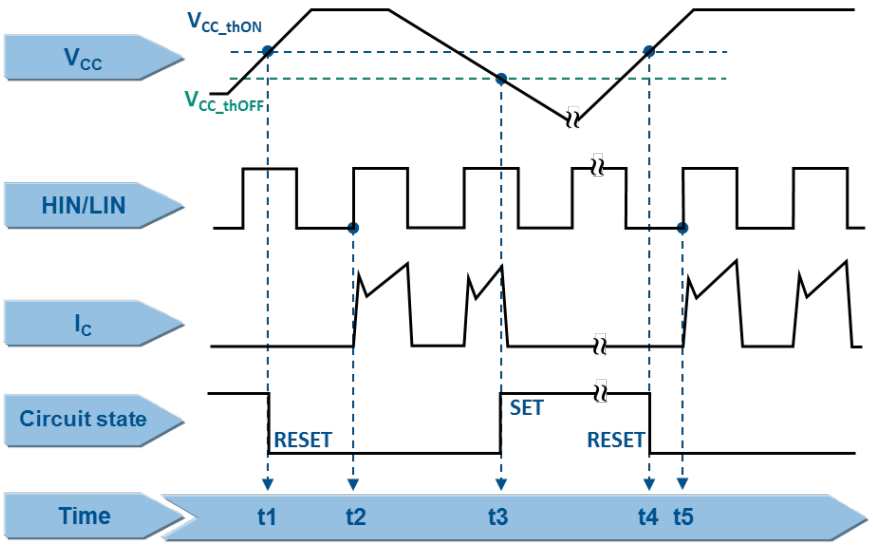
2.2.3 Undervoltage lockout

The SLLIMM-nano supply voltage (V_{CC}) is continuously monitored by the undervoltage lockout (UVLO) circuitry which turns off the gate driver outputs when the supply voltage goes below the $V_{CCH\_th(off)}$ threshold specified in the datasheet, and turns on the IC when the supply voltage goes above the $V_{CCH\_th(on)}$ voltage value. An hysteresis of about 1.5 V is provided for noise rejection purposes. A high-voltage floating supply (V_{boot}) is also provided with similar undervoltage lockout circuitry. When the driver is in the UVLO condition, both of the gate driver outputs are set to low level, setting the half-bridge power stage output to high impedance.

The timing chart of the undervoltage lockout is plotted in the figure below and is based on the following steps:

- t1: when the V_{CC} supply voltage reaches the the $V_{CCH\_th(on)}$ threshold, the gate driver starts to work after the next input signal HIN/LIN is on. The circuit state becomes RESET.
- t2: input signal HIN/LIN is on and the MOSFET is turned on.
- t3: when the V_{CC} supply voltage goes below the $V_{CCH\_th(off)}$ threshold, the UVLO event is detected. The MOSFET is turned off regardless of the status of the input signal HIN/LIN. The state of the circuit is now SET.
- t4: the gate driver re-starts once the V_{CC} supply voltage rises again to the $V_{CCH\_th(on)}$ threshold.
- t5: The input signal HIN/LIN is on and the MOSFET is turned on again.

Figure 8. Timing chart of the undervoltage lockout function



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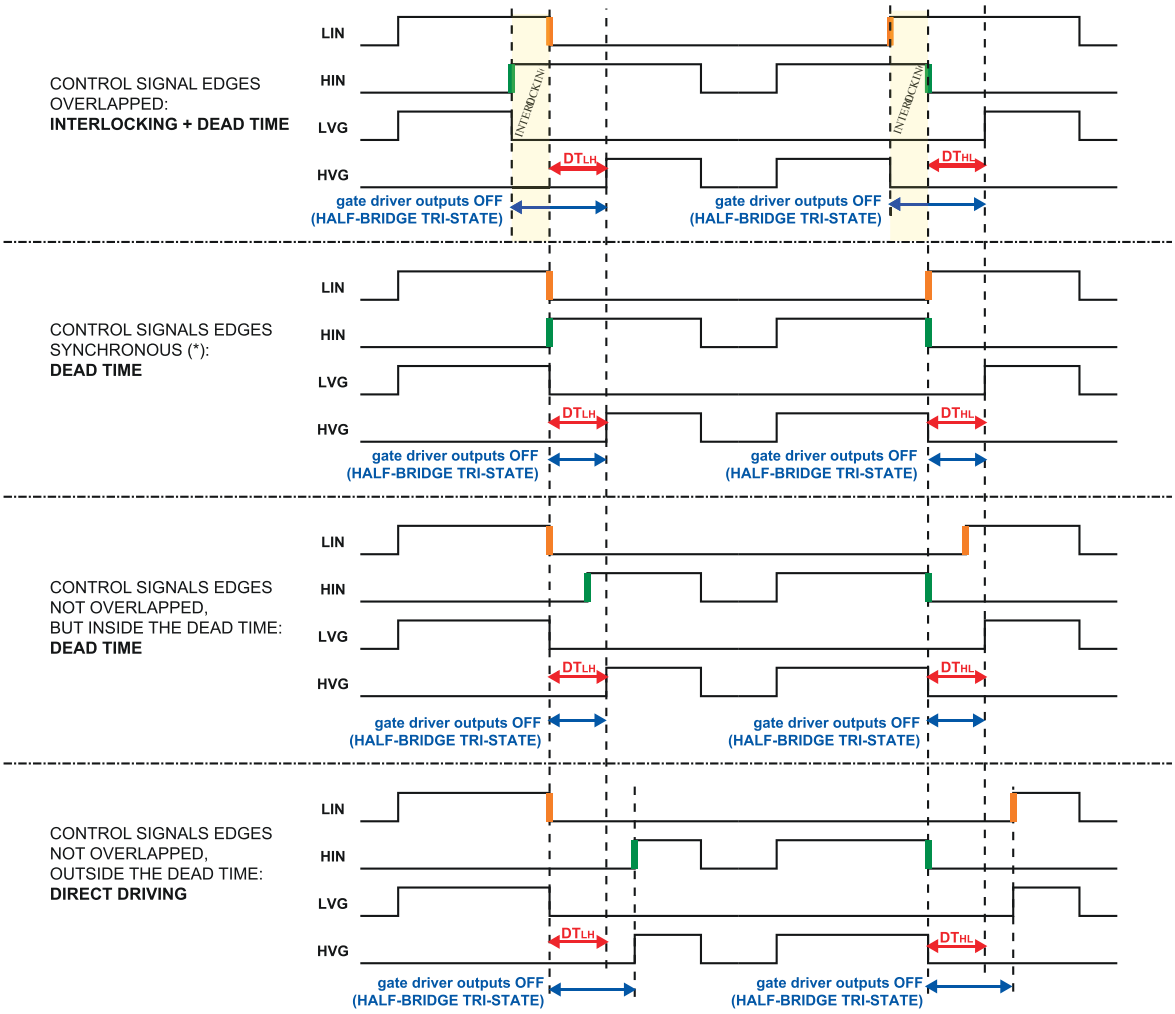
2.2.4 Interlocking function and dead time

In order to prevent possible cross-conduction between high-side and low-side MOSFETs, the SLLIMM-nano provides an interlocking function, which is a logic operation setting both of the outputs to low level when the inputs are simultaneously active, as shown in the table below. Even if an internal dead time is fixed as a default (180 ns typ.) between the falling edge transition of one driver output and the rising edge of the other output, the external dead time value set by the application firmware is mandatory to avoid cross-conduction. External dead time is dominant over internal dead time, and it is recommended to set it in accordance with the datasheet value.

Table 8. Interlocking function truth table

Condition	Logic input (V_I)		Outputs	
	LIN	HIN	LVG	HVG
Interlocking half-bridge tri-state	H	H	L	L
0 “logic state” half-bridge tri-state	L	L	L	L
1 “logic state” low-side direct driving	H	L	H	L
1 “logic state” high-side direct driving	L	H	L	H

Figure 9. Timing chart of dead time function



2.2.5 Comparators for fault sensing

The SLLIMM-nano integrates one comparator (embedded in the U IC gate driver) intended for fault protection such as overcurrent, overtemperature or any other type of fault measurable via a voltage signal. The comparator has an internal reference voltage, V_{REF}, specified in the datasheet, on its inverting input (see Figure 7. High-voltage gate driver block diagram) while the non-inverting input is available on the CIN pin. The comparator input can be connected to an external shunt resistor, in order to implement a simple overcurrent or short-circuit detection function, as discussed in detail in Section 2.2.6 Short-circuit protection and shutdown function.

2.2.6 Short-circuit protection and shutdown function

The SLLIMM-nano is able to monitor the output current and provide protection against overcurrent and short-circuit conditions.

Considering the internal schematic diagram of this product family, the comparator is directly connected on the U IC gate driver, whilst the V and W gate drivers are internally connected to the U one through the T/$\overline{SD}$/OD pin. Therefore, the overcurrent protection of the whole IPM depends on the external RC network connected to the T/$\overline{SD}$/OD pin.

As already mentioned in Section 2.2.5 Comparators for fault sensing and as shown in Figure 7. High-voltage gate driver block diagram, the comparator input can be connected to an external shunt resistor, R_{SHUNT}, in order to implement a simple overcurrent detection function. An RC filter network (R_{SF} and C_{SF}) is necessary to prevent erroneous operation of the protection. The output signal of the comparator is fed to an integrated MOSFET with the open drain available on the T/$\overline{SD}$/OD pin, shared with the $\overline{SD}$ input. When the comparator triggers, the U IC gate driver is set to shutdown state and its outputs are set to low level, leaving the half bridge in tri-state. In common overcurrent protection architectures, the comparator output is usually connected to the $\overline{SD}$ input and an external RC network ($R_{\overline{SD}}$ and $C_{\overline{SD}}$) is connected to this $\overline{SD}$/OD line in order to provide a mono-stable circuit which implements a protection time when a fault condition occurs.

Also, the outputs of the V and W IC gate drivers are set to low level, but not before the $\overline{SD}$ voltage reaches its low level threshold.

Finally, the shutdown structure allows to turn off the gate drivers' outputs in case of fault, latching the turn-on of the open drain MOSFET, until the $\overline{SD}$ signal has reached its lower threshold. After the $\overline{SD}$ signal goes below the lower threshold, the open drain is switched off (see Figure 14. Timing chart of shutdown function).

Since the protection of the V and W phases is linked to the $\overline{SD}$ level, a delay time, mainly due to the R_{SD}-C_{SD} network, is added for the shutdown of their outputs. Therefore, in order to implement effective protection, the $\overline{SD}$ network must be designed with special attention. For further details please refer to Section 2.2.7 Timing chart of short-circuit protection and shutdown function.

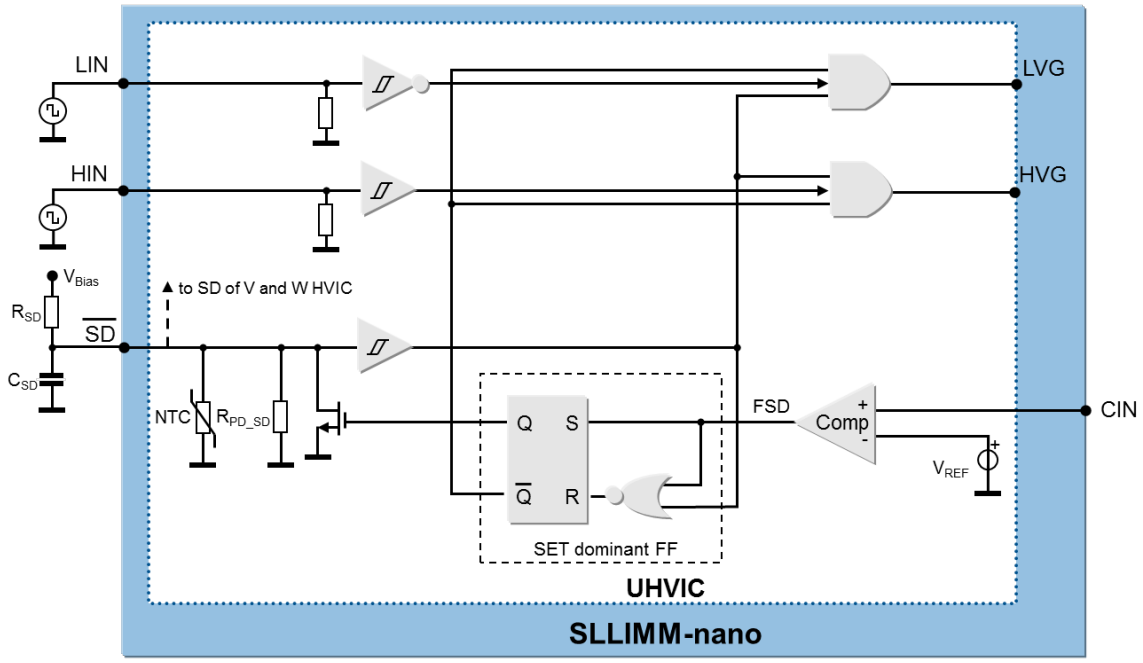
An NTC thermistor for temperature monitoring is internally connected in parallel to the $\overline{SD}$ pin in order to perform temperature monitoring using the same T/$\overline{SD}$/OD pin. The NTC thermistor is in parallel with the internal pull-down resistor (RPD_SD) and the equivalent resistance is shown in Figure 11. Equivalent resistance (NTC//R_{PD_SD}) below. Both temperature monitoring and the SD function can coexist on the same pin if a proper external pull-up resistor R_{SD} is designed (refer to Figure 7. High-voltage gate driver block diagram).

Therefore, to avoid any undesired shutdown, the T/$\overline{SD}$/OD voltage should be kept higher than the high-level logic threshold by setting the R_{SD} to 1 kΩ or 2.2 kΩ for the 3.3 V or 5 V MCU power supplies, respectively (see Figure 12. Voltage of T/$\overline{SD}$/OD pin according to NTC temperature).

Note: STIPN1M50-H and STIPN2M50-H do not have an internal NTC feature.

The block diagram of the shutdown architecture is depicted in Figure 10. Shutdown equivalent circuitry.

Figure 10. Shutdown equivalent circuitry



Note: STIPN1M50-H and STIPN2M50-H do not have an internal NTC

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Figure 11. Equivalent resistance (NTC//R_{PD_SD})

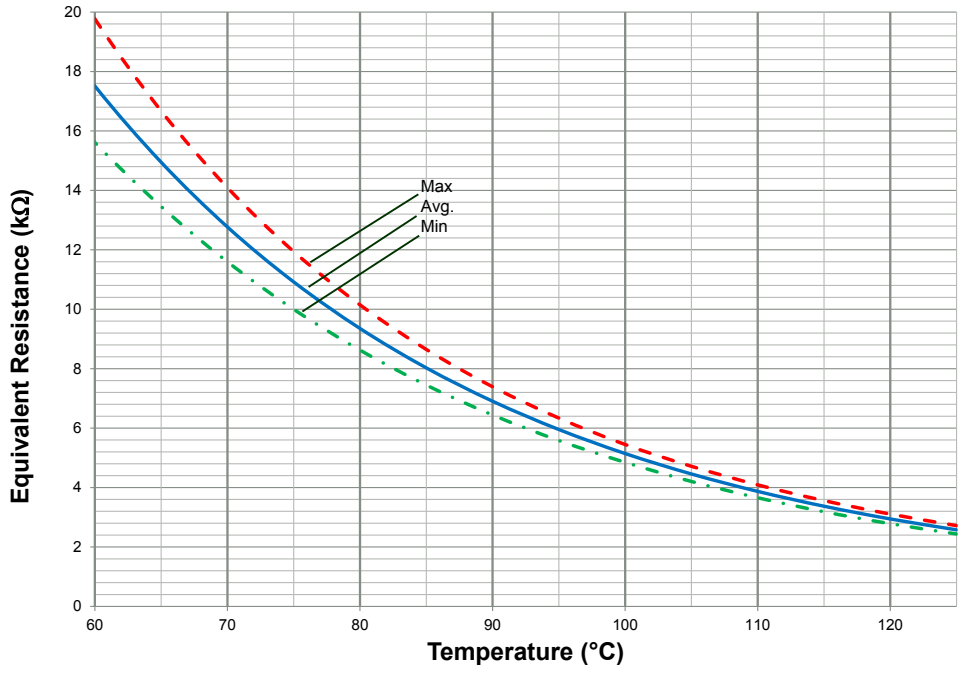

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Figure 12. Voltage of T/$\overline{SD}$/OD pin according to NTC temperature

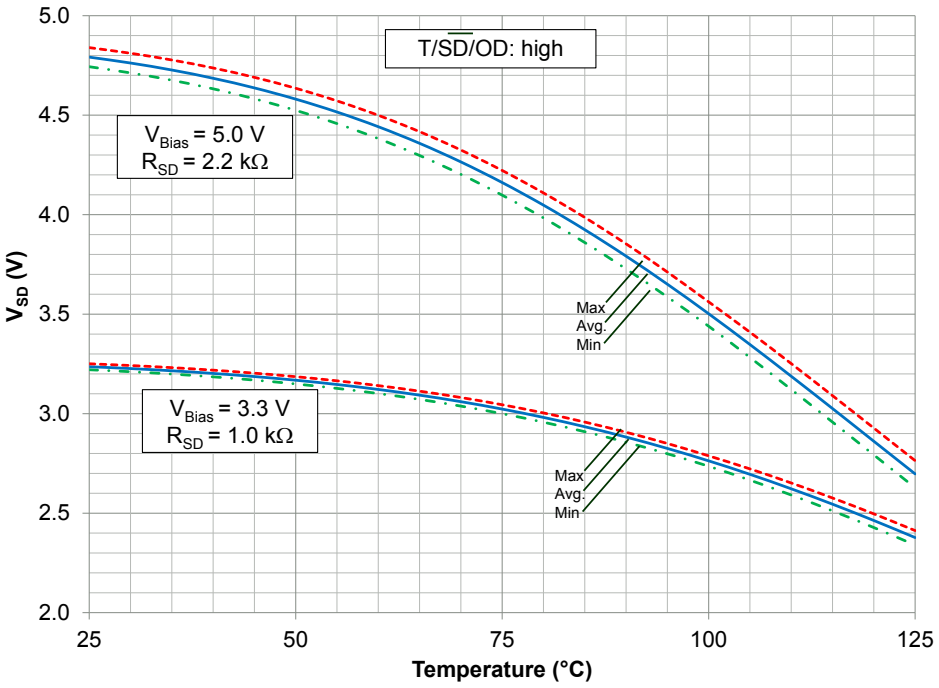

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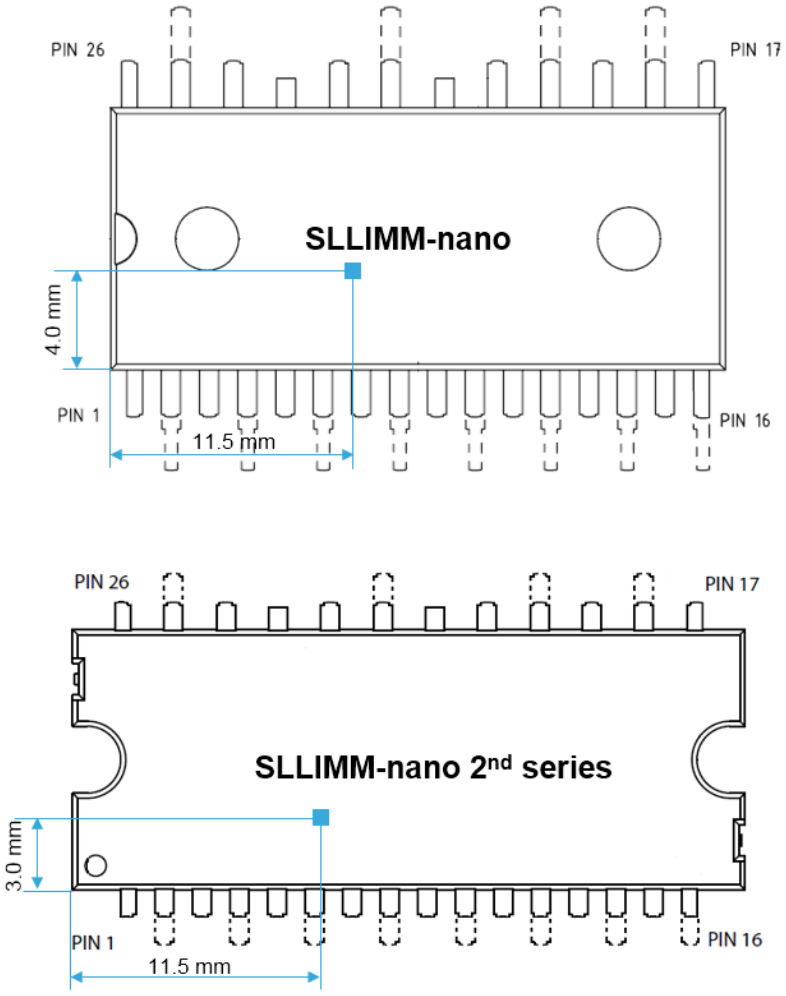
Figure 13. NTC thermistor position (top view) shows the NTC thermistor position inside the SLLIMM-nano (NDIP) and SLLIMM-nano 2nd series (N2DIP).

Figure 13. NTC thermistor position (top view)



In normal operation, the outputs follow the commands received from the respective input signals.

When a fault detection event occurs, the fault signal (FSD) is set to high by the fault detection circuit output and the FF receives a SET input signal. Consequently, the FF outputs set the SLLIMM-nano output signals to low level and, at the same time, turn on the open drain MOSFET which works as active pull-down for the $\overline{SD}$ signal. Note that the gate driver outputs stay at low level until the $\overline{SD}$ pin has experienced both a falling edge and a rising edge, although the fault signal could be returned to low level immediately after the fault sensing. In fact even if the FF is reset by the falling edge of the $\overline{SD}$ input, the $\overline{SD}$ signal also works as enable for the outputs, thanks to the two AND ports. Moreover, once the internal open drain transistor has been activated, due to the latch, it cannot be turned off until the $\overline{SD}$ pin voltage reaches the low logic level. Note that since the FF is SET dominant, oscillations of the $\overline{SD}$ pin are avoided if the fault signal remains steady at high level.

2.2.7 Timing chart of short-circuit protection and shutdown function

With reference to Figure 14. Timing chart of shutdown function, the short-circuit protection is based on the following steps:

- t1: when the current is lower than the maximum allowed level, the SLLIMM-nano works in normal operation.
- t2: when the current reaches the maximum allowed level (I_{SC}), an overcurrent/short- circuit event is detected and the protection is activated. The voltage across the shunt resistor, and then on the CIN pin, exceeds the V_{REF} value, the comparator triggers, setting the U IC gate driver in shutdown state and both its outputs are set to low level leading the half bridge into tri-state. The U phase MOSFETs gates (HVG, LVG) are switched off in 200 ns (typical internal delay time) and at the same time the M1 MOSFET is switched on. The $\overline{SD}$ signal starts the discharge phase and its value drops with a time constant τ_A (SD activation time constant). The time constant of τ_A is given by the following equation:

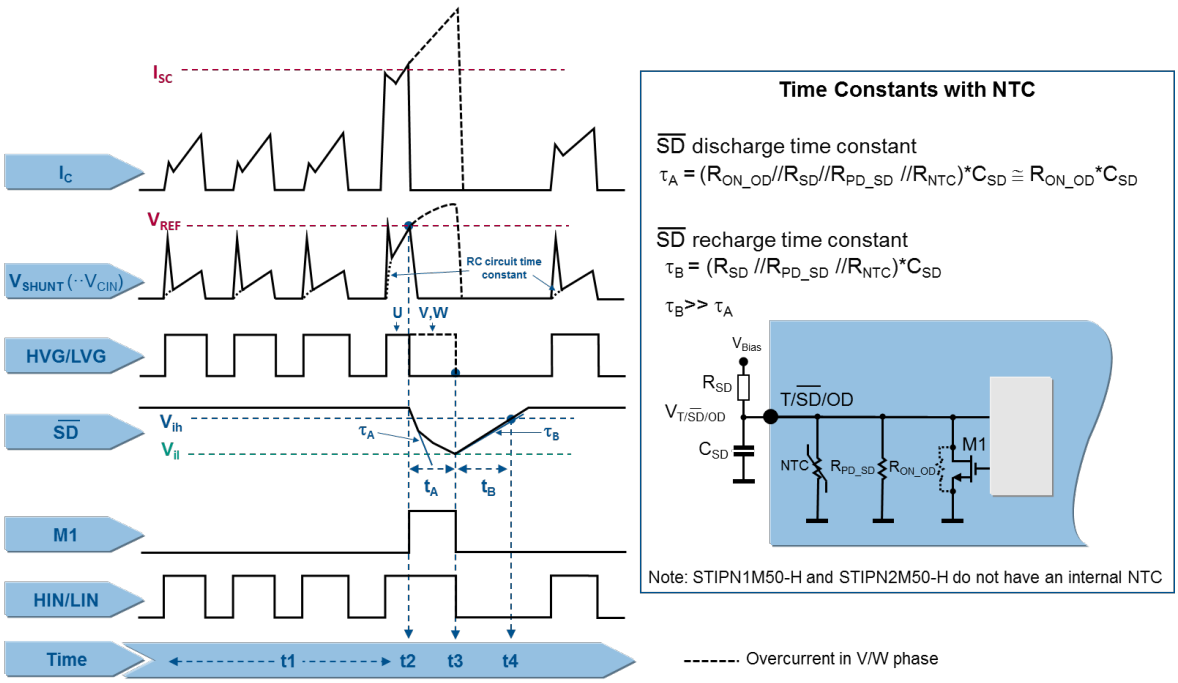
$$\tau_A = \left(R_{ON\_OD} \,//\, R_{SD} \,//\, R_{PD\_SD} \,//\, R_{NTC}\right) \cdot C_{SD} \cong R_{ON\_OD} \cdot C_{SD} \quad (1)$$

- t3: the $\overline{SD}$ signal reaches the lower threshold $V_{sd\_L\_THR}$, even the outputs of the V and W IC gate drivers are set to low and the control unit switches off all the HIN and LIN input. The M1 MOSFET is switched off and $\overline{SD}$ can rise with a time constant τ_B (SD re-enabling time constant), given by the following equation:

$$\tau_B = \left(R_{SD} \,//\, R_{PD\_SD} \,//\, R_{NTC}\right) \cdot C_{SD} \quad (2)$$

- t4: when the $\overline{SD}$ signal reaches the upper threshold $V_{sd\_H\_THR}$, the system is re-enabled.

Figure 14. Timing chart of shutdown function



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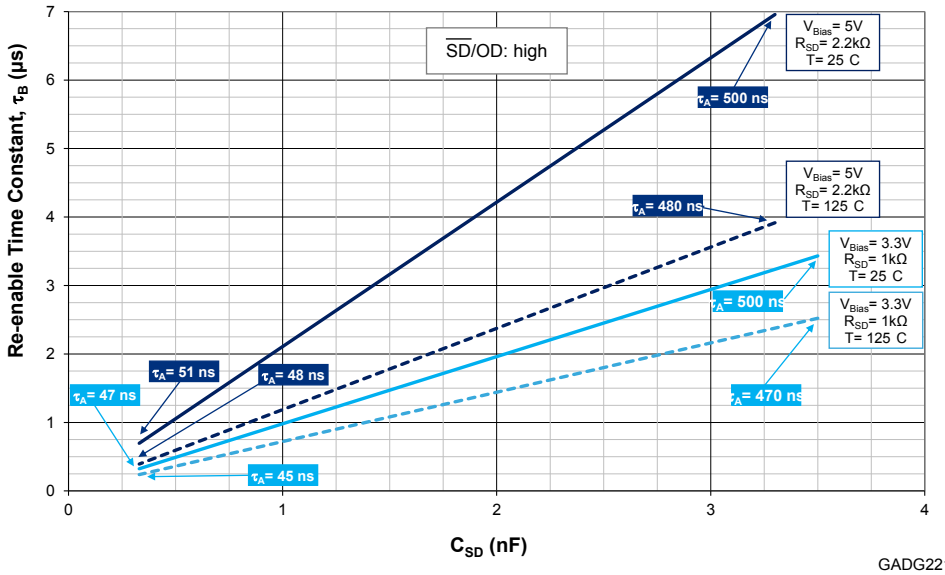
As shown in Eq. (1) and Eq. (2), the time constants τ_A and τ_B are even functions of the NTC resistor value which depends on temperature (except for STIPN1M50-H and STIPN2M50-H that do not have an internal NTC feature). Therefore, Figure 15. Re-enabling time constant (with NTC), τ_B shows the behavior of τ_B ($\overline{SD}$ re-enabling time constant) as a function of the C_{SD} capacitor and parameterized with NTC temperature. The suggested range of the C_{SD} value is defined to have τ_A ($\overline{SD}$ activation time constant) no higher than 500 ns for effective protection.

For an effective design of the shutdown circuit, please refer to Application note AN4966.

Figure 15. **Re-enabling time constant (with NTC), τ_B**



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2.2.8 Current sensing shunt resistor selection

As previously discussed, the shunt resistors, R_{SHUNT}, externally connected between the N pin and ground (see Figure 7. High-voltage gate driver block diagram) are used to implement the overcurrent detection. When the output current exceeds the short-circuit reference level (I_{SC}), the CIN signal overtakes the V_{REF} value and the short-circuit protection is active. For reliable and stable operation, the current sensing resistor should be of a high-quality, low-tolerance, non-inductive type. In fact, stray inductance in the circuit, which includes the layout, the RC filter and also the shunt resistor, must be minimized in order to avoid undesired short-circuit detection. For these reasons, the shunt resistor and filtering components must be placed as close as possible to the SLLIMM-nano pins (for additional suggestions, refer to Section 5.2 Layout suggestions). The value of the current sense resistor can be calculated by following different guidelines, functions of the design specifications, or requirements. A common criterion is presented here based on the following steps:

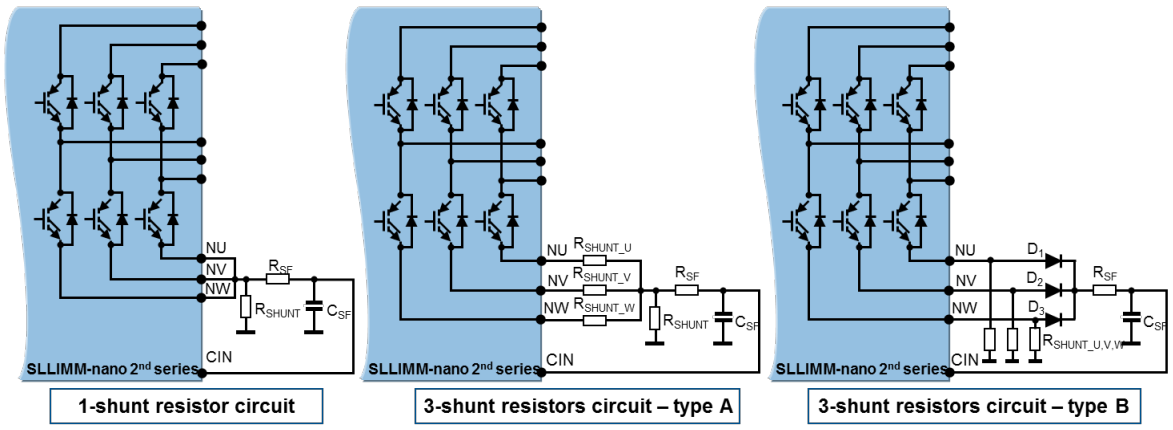
- Defining the overcurrent threshold value (I_{SC}).For example, it can be fixed considering the MOSFET typical working current in the application and adding 20-30% as overcurrent.
- Calculation of the shunt resistor value according to the conditioning network. An example of the conditioning network is shown in Figure 16.
- Selection of the closest shunt resistor commercial value.

$$P_{SHUNT}(T) = \frac{R_{SHUNT} \cdot I_{RMS}^2}{\Delta P(T)\%} \quad (3)$$

2.2.9 RC filter network selection

Two options for the shunt (1- or 3-shunt) resistor circuit can be adopted in order to implement different control and short-circuit protection techniques. For 3-shunt resistor configurations, the figure below shows two simple overcurrent protection variants: type A, using an additional shunt resistor (R_{SHUNT}) and type B, using a diode OR gate circuit.

Figure 16. Examples of SC protection circuit



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An RC filter network is required to prevent undesired short-circuit operation due to the noise on the shunt resistor. All of the solutions allow detection of the total current in all the three phases of the inverter. The filter is based on the R_{SF} and C_{SF} network and its time constant is given by:

$$\tau_{SF} = R_{SF} \cdot C_{SF} \quad (4)$$

The total comparator triggering time t_{SF} is recommended to be set no higher than 1 µs.

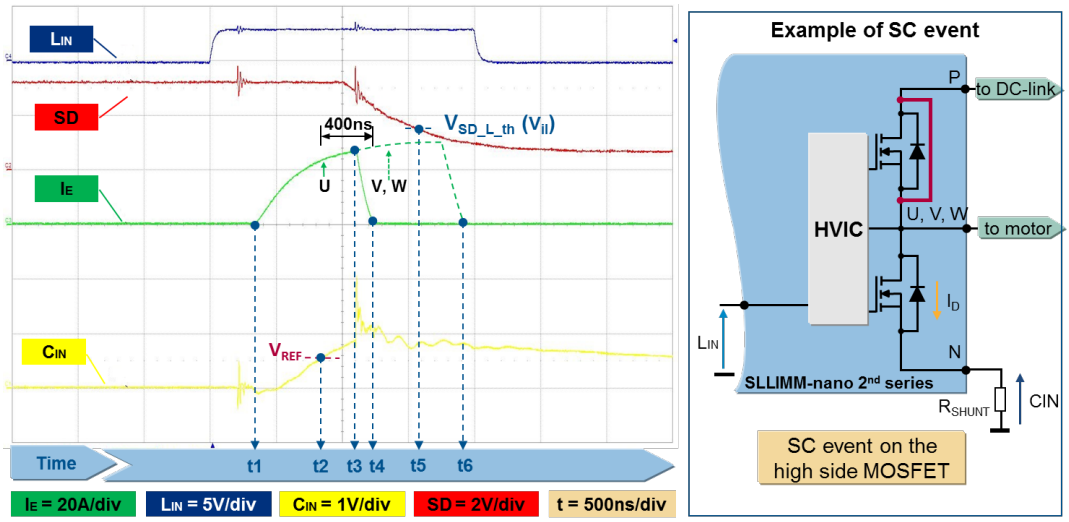
In the case of a 3-shunt resistor circuit, a specific control technique can be implemented by using the three shunt resistors (R_{SHUNT_U}, R_{SHUNT_V} and R_{SHUNT_W}) able to monitor each phase of current.

An example of a short-circuit event is shown in Figure 17. Example of an SC event below. The main steps are:

- t1: collector current IC starts to rise. SC event is not detected yet due to the RC network on the CIN pin.
- t2: voltage on VCIN reaches the V_{REF}. An SC event is detected and the shutdown sends the off signal to the U IC gate driver.
- t3: the U MOSFET starts the fall time.
- t4: the U MOSFET is definitively turned off in 400 ns (turn-off propagation delay time of the driver plus delay off time and fall time.
- t5: the $\overline{SD}$ is activated and even the off signals on the V and W IC drivers are sent.
- t6: all the MOSFETs are definitively turned off.

Finally, the total disable time is t6-t1.

Figure 17. **Example of an SC event**



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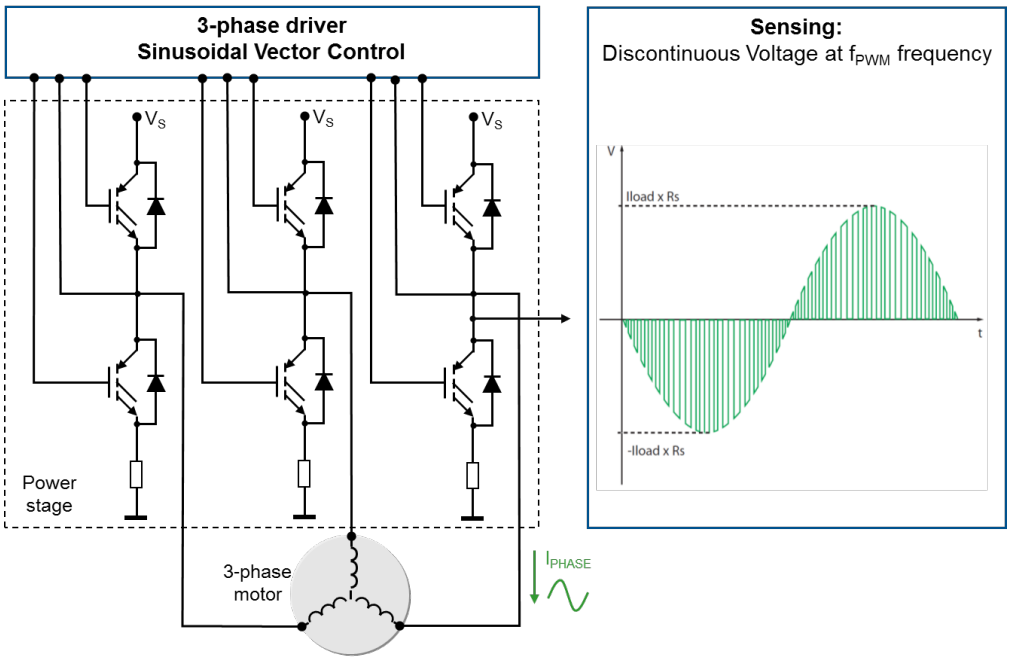
2.2.10 Op-amp for advanced current sensing

The SLLIMM-nano also integrates one operational amplifier optimized for field oriented control (FOC) applications. In a typical FOC application the currents in the three half bridges are sensed using a shunt resistor. The analog current information is transformed into a discontinuous sense voltage signal, having the same frequency as the PWM signal driving the bridge. The sense voltage is a bipolar analog signal, the sign of which depends on the direction of the current (see the following figure):

Figure 18. **3-phase system**



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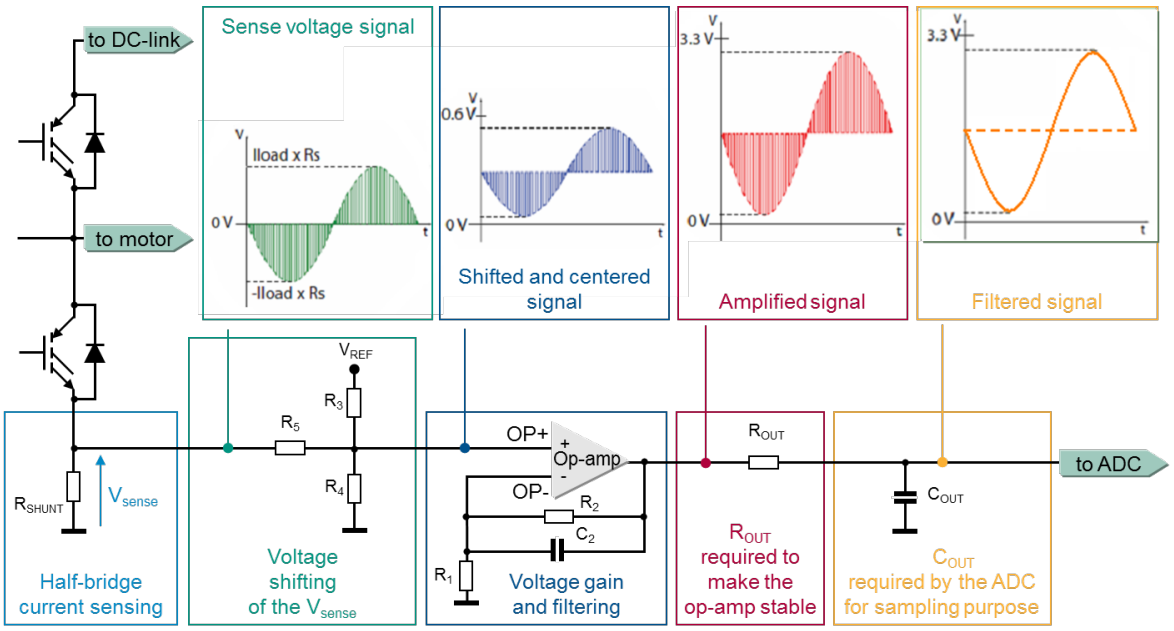
The sense voltage signals must be provided to an A/D converter. They are usually shifted and amplified by dedicated op-amps in order to exploit the full range of the A/D converter. The typical scheme and principle waveforms are shown in the following figure:

Figure 19. General advanced current sense scheme and waveforms



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ADCs used in vector control applications have a typical full scale range (FSR) of about 3.3 V. The sense signals must be shifted and centered on FSR/2 voltage (about 1.65 V) and amplified with a gain which provides matching between the maximum value of the sensed signal and the FSR of the ADC.

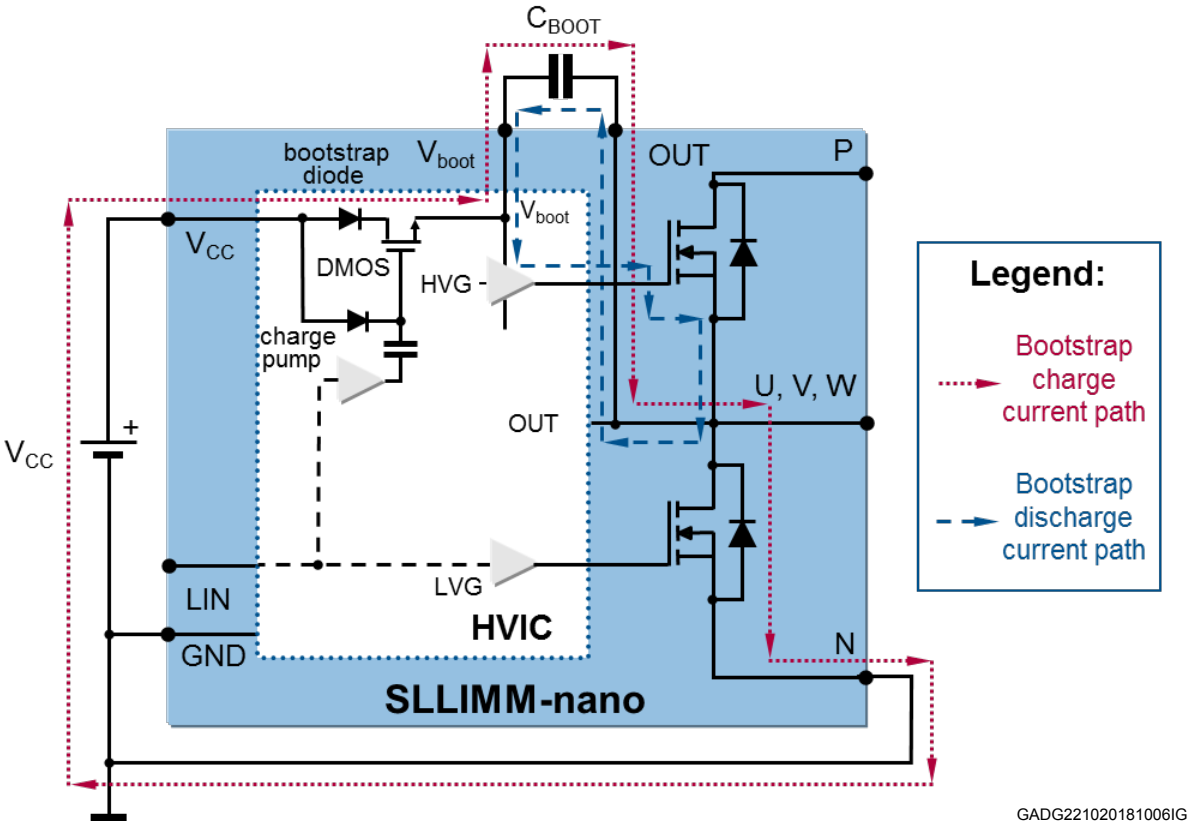
2.2.11 Bootstrap circuit

In the 3-phase inverter the sources of the low-side MOSFETs are connected to the negative DC bus (V_{DC-}) as common reference ground, which allows all low side gate drivers to share the same power supply, while the source of high-side MOSFETs is alternately connected to the positive (V_{DC+}) and negative (V_{DC-}) DC bus during running conditions.

A bootstrap method is a simple and cheap solution to supply the high-voltage section. This function is normally accomplished by a high-voltage fast-recovery diode. The SLLIMM-nano family includes a patented integrated structure that replaces the external diode. It is realized with a high-voltage DMOS driven synchronously with the low-side driver (LVG) and a diode in series. An internal charge pump provides the DMOS driving voltage.

The operation of the bootstrap circuit is shown in the figure below.The floating supply capacitor C_{BOOT} is charged from the V_{CC} supply when the V_{OUT} voltage is lower than the V_{CC} voltage, through the bootstrap diode and the DMOS path with reference to the “bootstrap charge current path”. During the high-side MOSFET on-phase, the bootstrap circuit will provide the right gate voltage to properly drive the MOSFET (see *“Bootstrap discharge current path”* in the figure below). This circuit is iterated for all of the three half bridges.

Figure 20. **Bootstrap circuit**



The value of the C_{BOOT} capacitor should be calculated according to the application conditions and must take the following into account:

- The voltage across C_{BOOT} must be maintained at a value higher than the undervoltage lockout level for the IC driver. This will enable the high-side MOSFET to work with a correct gate voltage (lower dissipation and better overall performance). Please consider that if a voltage value below the UVLO threshold is applied on the bootstrap channel, the IC disables itself (no output) without any fault signal.
- The voltage across C_{BOOT} is affected by different components such as the drop across the integrated bootstrap structure, the drop across the low-side MOSFET, and other ones.
- When the high-side MOSFET is on, the C_{BOOT} capacitor discharges mainly to provide the right MOSFET gate charge but other phenomena must be considered such as leakage currents, quiescent current, etc.

2.2.12 Bootstrap capacitor selection

A simple method to properly size the bootstrap capacitor considers only the amount of charge that is needed when the high-voltage side of the driver is floating and the MOSFET gate is driven once. This approach does not take into account either the duty cycle of the PWM or the fundamental frequency of the current. Observations on PWM duty cycle, type of modulation (six-step, 12-step and sine-wave) must be considered with their own peculiarities to achieve optimal bootstrap circuit sizing. During the bootstrap capacitor charging phase, the low-side MOSFET is on and the voltage across C_{BOOT} (V_{CBOOT}) can be calculated as follows:

$$V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{DS(on)max} \quad (5)$$

where:

V_{CC}: supply voltage of gate driver

V_F: bootstrap diode forward voltage drop

$V_{DS(on)max}$: maximum drain source voltage drop of the low-side MOSFET

$V_{RDS(on)}$: DMOS voltage drop

The dimension of the bootstrap capacitance C_{BOOT} value is based on the minimum voltage drop (ΔV_{CBOOT}) to guarantee when the high-side MOSFET is on, and it must be:

$$\Delta V_{CBOOT} = V_{CC} - V_F - V_{RDS(on)} - V_{GS(min)} - V_{DS(on)max} \quad (6)$$

under the condition:

$$V_{CBOOT}(\min) > V_{BS\_th(on)} \quad (7)$$

where:

$V_{GS(min)}$: minimum gate-source voltage of high side MOSFET

$V_{BS\_th(on)}$: bootstrap turn-on undervoltage threshold (maximum value, refer to the related datasheet)

Considering the factors contributing to a decrease in V_{CBOOT}, the total charge supplied by the bootstrap capacitor (during the high-side on phase) is:

$$Q_{TOT} = Q_{GATE} + \left(I_{LKGS} + I_{QBO} + I_{LK} + I_{LKDiode} + I_{LKCap}\right) \cdot t_{Hon} + Q_{LS} \quad (8)$$

where:

Q_{GATE}: total MOSFET gate charge

I_{LKGS}: MOSFET gate source leakage current

I_{QBO}: bootstrap circuit quiescent

I_{LK}: bootstrap circuit leakage current

$I_{LKDiode}$: bootstrap diode leakage current

I_{LKCap}: bootstrap capacitor leakage current (relevant when using an electrolytic capacitor, but can be ignored if other types of capacitors are used)

t_{Hon}: high-side on time

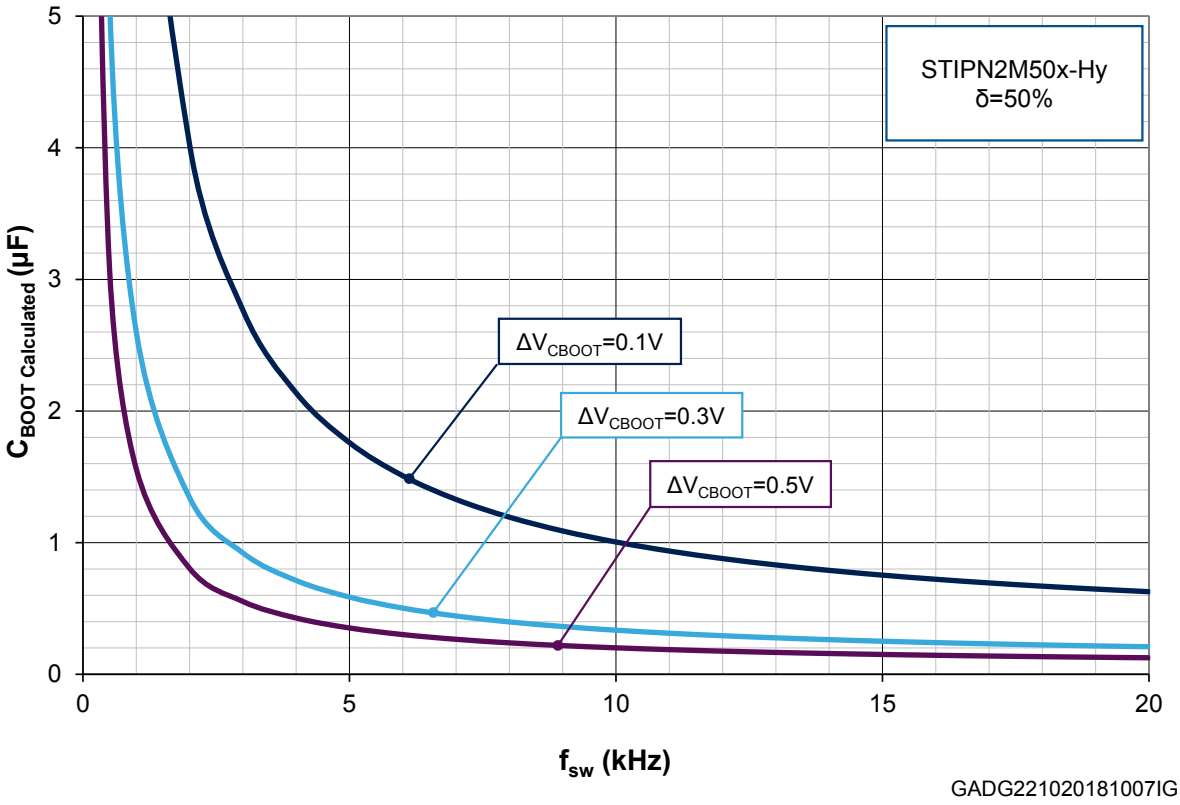
Q_{LS}: charge required by the internal level shifters

Finally, the minimum size of the bootstrap capacitor is:

$$C_{BOOT} = \frac{Q_{TOT}}{\Delta V_{CBOOT}} \quad (9)$$

For an easier selection of the bootstrap capacitor, the following figure shows the behavior of C_{BOOT} (calculated) versus the switching frequency (f_{sw}), with different values of ΔV_{CBOOT}, corresponding to Eq. (9) for continuous sinusoidal modulation and for STIPN2M50x-Hy (worst case) and a duty cycle of δ = 50 %. For all the other devices, the bootstrap capacitor can be calculated using the same curve.

Figure 21. **Bootstrap capacitor vs switching frequency**



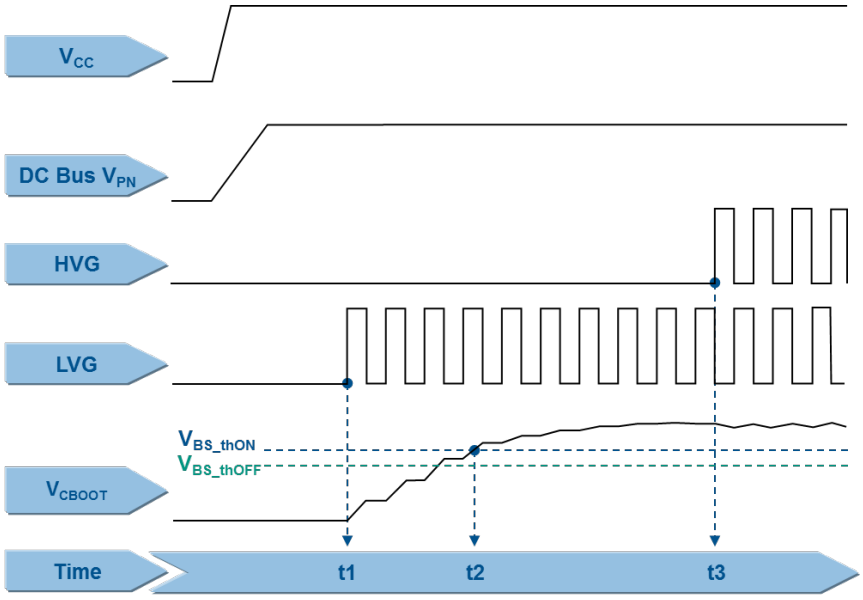
Considering the limit cases during the PWM control and further leakages and dispersions in the board layout, the capacitance value to use in the bootstrap circuit must be two or three times higher than the C_{BOOT} calculated in the graph of Figure 21. Bootstrap capacitor vs switching frequency above.The bootstrap capacitor should have a low ESR value for good local decoupling, therefore, if an electrolytic capacitor is used, one parallel ceramic capacitor placed directly on the SLLIMM-nano pins is highly recommended.

2.2.13 Initial bootstrap capacitor charging

During the startup phase, the bootstrap capacitor must be charged for a suitable time to complete the initial charging time (t_{CHARGE}) which is, at least, the time V_{CBOOT} needs to exceed the turn-on undervoltage threshold $V_{BS\_th(on)}$, as previously stated in Eq. (7). For normal operation, the voltage across the bootstrap capacitor must never drop down to the turn-off undervoltage threshold $V_{BS\_th(off)}$ throughout the working conditions. For the startup period, only the low-side MOSFET is switched on and just after this phase the PWM is run, as described in the following steps shown in the figure below:

- t1: the bootstrap capacitor starts to charge through the low-side MOSFET (LVG)
- t2:the voltage across the bootstrap capacitor (V_{CBOOT}) reaches its turn-on undervoltage threshold $V_{BS\_th(on)}$
- t3: the bootstrap capacitor is fully charged, this enables the high-side MOSFET and the C_{BOOT} capacitor starts to discharge in order to provide the right MOSFET gate charge. The bootstrap capacitor recharges during the on state of low-side MOSFET (LVG).

Figure 22. **Initial bootstrap charging time**



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The initial charging time is given by Eq. (10) and must be, for safety reasons, at least three times longer than the calculated value.

$$t_{CHARGE} \geq \frac{C_{BOOT} \cdot R_{DS(on)}}{\delta} * \ln\left(\frac{V_{CC}}{\Delta V_{CBOOT}}\right) \quad (10)$$

where δ is the duty cycle of the PWM signal and $R_{DS(on)}$ is 120 Ω typical value, as reported in the related datasheet.

A practical example can be done by considering a motor drive application where the PWM switching frequency is 16 kHz, with a duty cycle of 50%, and ΔV_{CBOOT} = 0.1 V (this means a gate driver supply voltage of V_{CC} = 16.9 V). From the graph in Figure 21. Bootstrap capacitor vs switching frequency the bootstrap capacitance is 0.85 µF, therefore the C_{BOOT} can be selected by using a value between 2.2 and 3.3 µF. According to the commercial value, the bootstrap capacitor can be 2.2 µF, while based to Eq. (10), the initial charging time is:

$$t_{CHARGE} \geq \frac{2.2 \cdot 10^{-6} \cdot 120}{0.5} \cdot \ln\left(\frac{16.9}{0.1}\right) = 2.7ms \quad (11)$$

For safety reasons, the initial charging time must be at least 8.1 ms.

3 Package

The NDIP and N2DIP is a dual-in-line transfer mold package available in a 26-lead version (NDIP-26L and N2DIP-26L) capable of meeting the demanding cost and size requirements of consumer appliance inverters. Both consist of a copper lead frame with power stage and control stage soldered on it and housed using the transfer molding process. The excellent thermal properties of the copper allows good heat distribution and heat transfer.

The N2DIP provides improved thermal resistance from reduced thickness and optimized layout of the lead frame. Furthermore, the package is designed to allow a better and more easily screwed-on heatsink thanks to the dedicated slots for screws placed on the short side of the package. This characteristic allows the N2DIP to be used in higher power level applications than the NDIP package. NDIP and N2DIP are offered in two lead options: zig-zag and in-line leads.

The zig-zag leads option is pin-to-pin compatible for both NDIP and N2DIP version for a natural extension targeting higher power-level sockets.

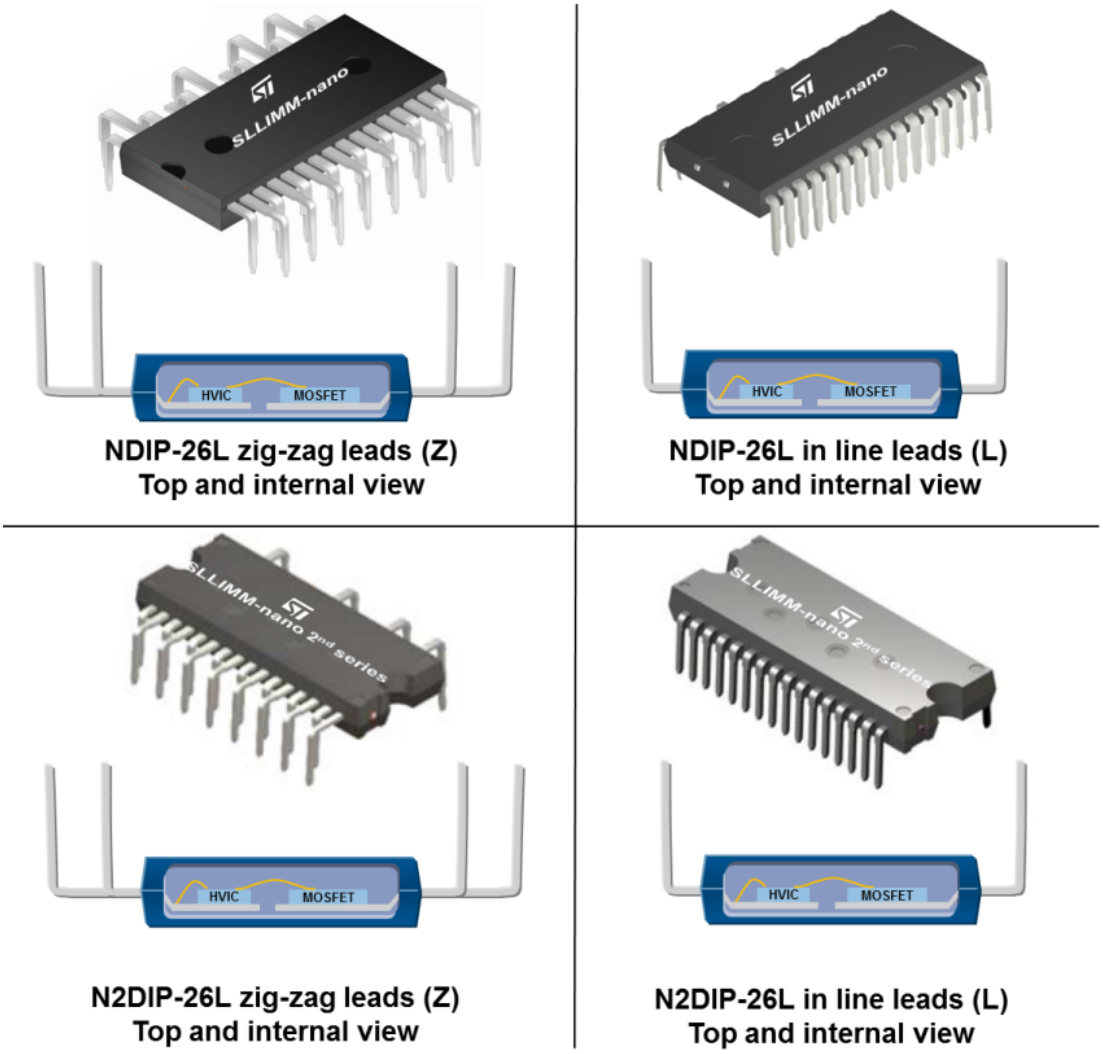
The in-line leads option offers further compactness thanks to the aligned leads and satisfies the needs of applications with space constraint requirements.

Both lead options have been designed to maximize the distance between the high voltage and low voltage pins, by placing the relevant pins on the opposite side of the package. This is mainly useful to keep a safe distance between high voltage and low voltage pins and for easy PCB layout.

3.1 Package structure

The following figure shows the silhouettes and the internal structures of both NDIP and N2DIP packages.

Figure 23. Silhouettes and internal views of NDIP and N2DIP packages



Packages outlines and dimensions of the NDIP and N2DIP alternatives and related lead options are detailed in the datasheet of the relevant product, in section “Package information”.

3.2 Input and output pin description

This section defines the input and output pins of the SLLIMM-nano. For a more accurate description and layout suggestions, please consult the relevant sections.

Table 9. Input and output pins

Pin#	Name	Description
1	GND	Ground
2(1)	T/$\overline{SD}$/OD	NTC thermistor/shutdown logic input (active low)/open drain (comparator output)
3	V_{CC} W	Low-voltage power supply W phase
4	HIN W	High-side logic input for W phase
5	LIN W	Low-side logic input for W phase (active high)
6	OP+	Op-amp non inverting input
7	OP_{OUT}	Op-amp output
8	OP-	Op-amp inverting input
9	V_{CC} V	Low-voltage power supply V phase
10	HIN V	High-side logic input for V phase
11	LIN V	Low-side logic input for V phase (active high)
12	CIN	Comparator input
13	V_{CC} U	Low-voltage power supply U phase
14	HIN U	High-side logic input for U phase
15(1)	T/$\overline{SD}$/OD	NTC thermistor/shutdown logic input (active low)/open drain (comparator output)
16	LIN U	Low-side logic input for U phase (active high)
17	V_{boot} U	Bootstrap voltage for U phase
18	P	Positive DC input
19	U, OUT U	Uphase output
20	N U	Negative DC input for U phase
21	V_{boot} V	Bootstrap voltage for V phase
22	V, OUT V	V phase output
23	NV	Negative DC input for V phase
24	V_{boot} W	Bootstrap voltage for W phase
25	W, OUT W	W phase output
26	N W	Negative DC input for W phase

1. *SD/$\overline{OD}$ for STIPN1M50-H and STIPN2M50-H, without internal NTC feature*

High-side bias voltage pins/high-side bias voltage reference

Pins: V_{bootU}-U, V_{bootV}-V, V_{bootW}-W

- The bootstrap section is designed to realize a simple and efficient floating power supply, in order to provide the gate voltage signal to the high-side MOSFETs.
- The SLLIMM-nano family integrates the bootstrap diodes. This helps customers to reduce cost, board space and number of components.
- The advantage of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side MOSFETs.

- Each bootstrap capacitor is charged from the V_{CC} supply during the on-state of the corresponding low-side MOSFET.
- To prevent malfunctions caused by noise and ripple in supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.
- The value of bootstrap capacitors is strictly related to the application conditions.

Please consult Section 2.2.11 Bootstrap circuit for more information.

Gate driver bias voltage

Pins: V_{CCU}, V_{CCV}, V_{CCW}

- Control supply pins for the built-in ICs.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitors should be mounted close to these pins.

Gate drive supply ground

Pin: GND

- Ground reference pin for the built-in ICs.
- To avoid noise influences, the main power circuit current should not be allowed to flow through this pin (see Section 5.2 Layout suggestions).

Signal input

Pins: HIN_U, HIN_V , HIN_W, LIN_U, LIN_V, LIN_W

- These pins control the operation of the built-in MOSFETs.
- The signal logic of HINx and LINx pins is active high. The MOSFET associated with each of these pins is turned on when a sufficient logic (higher than a specific threshold) voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the device against noise influences. RC coupling circuits should be adopted for the prevention of input signal oscillation. Suggested values are R = 100 Ω and C = 1 nF.

Internal non-inverting comparator

Pin: CIN

- The current sensing shunt resistor, connected on each phase leg, could be used by the internal comparator (pin CIN) to detect short-circuit current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application.
- An RC filter (typically ~1 us) should be connected to the CIN pin to eliminate noise.
- The connection length between the shunt resistor and CIN pin should be minimized.
- If a voltage signal, higher than the specified V_{REF} (see related datasheet), is applied to this pin, the SLLIMM-nano automatically shuts down and the T/$\overline{SD}$/OD pin is pulled down (to inform the microcontroller).

NTC thermistor/shutdown/open drain

Pins: T/$\overline{SD}$/OD

- There are two available pins of T/$\overline{SD}$/OD which are exactly the same. They are placed on the opposite ends of the package in order to offer higher flexibility to the PCB layout. It is sufficient to use only one of two pins for the proper functioning of the device.
- The T/$\overline{SD}$/OD pins work as enable/disable pins.
- The signal logic of T/$\overline{SD}$/OD pins is active low. The SLLIMM-nano shuts down if a voltage lower than a specific threshold is applied to these pins, leading each half bridge in tri-state.
- The T/$\overline{SD}$/OD status is connected also to the internal comparator status (Section 2.2.6 Short-circuit protection and shutdown function). When the comparator triggers, the T/$\overline{SD}$/OD pin is pulled down acting as a FAULT pin.
- The T/$\overline{SD}$/OD, when pulled down by the comparator, are open drain configured.
- The T/$\overline{SD}$/OD voltage should be pulled up to the 3.3 V or 5 V logic power supply through a pull-up resistor.
- The T/$\overline{SD}$/OD pin can be used for temperature monitoring as well, thanks to the co-packaged NTC thermistor (optional). A resistor RSD of 1 kΩ or 2.2 kΩ for the 3.3 V or 5 V MCU power supplies respectively, is required to avoid undesired shutdown, along with a capacitor C_{SD} for a constant time no higher than 500

ns for effective protection. For further details, refer to Section 2.2.7 Timing chart of short-circuit protection and shutdown function.

Integrated operational amplifier

Pins: OP+, OP-, OP_{OUT}

- The op-amp is completely uncommitted.
- The op-amp performances are optimized for advanced control technique (FOC).
- Thanks to the integrated op-amp it is possible to realize compact and efficient board layout, minimizing the required BOM list.

Positive DC-link

Pin: P

- This is a DC-link positive power supply pin of the inverter and it is internally connected to the collectors of the high-side MOSFETs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a snubber capacitor close to this pin (typically, high-voltage metal film capacitors of about 0.1 or 0.22 µF).

Negative DC-link

Pins: N_U, N_V, N_W

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side MOSFET drains of each phase.
- The power ground of the application should be separated from the logic ground of the system and they should be reconnected at one specific point (star connection).

Inverter power output

Pins: U, V, W

- Inverter output pins for connecting to the inverter load (e.g. motor).

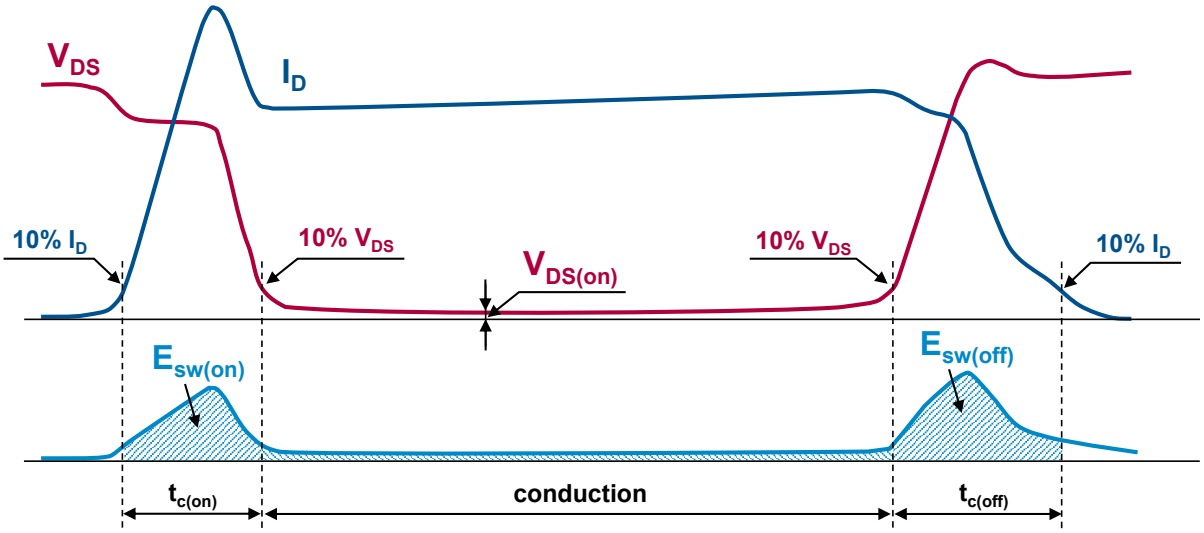
4 Power loss and dissipation

The total power loss in an inverter is comprised of conduction loss, switching loss and off-state loss, and it is essentially generated by the power devices of the inverter stage, such as the MOSFETs. The conduction loss (P_{cond}) is the on-state loss during the conduction phase. The switching loss (P_{sw}) is the dynamic loss encountered during the turn-on and the turn-off. The off-state loss, due to the blocking voltage and leakage current, can be neglected. Finally, the total power loss is given by:

$$P_{tot} \approx P_{cond} + P_{sw} \quad (12)$$

The following figure shows a typical waveform of an inductive hard switching application such as a motor drive, where the major sources of power loss are specified.

Figure 24. Typical MOSFET power loss



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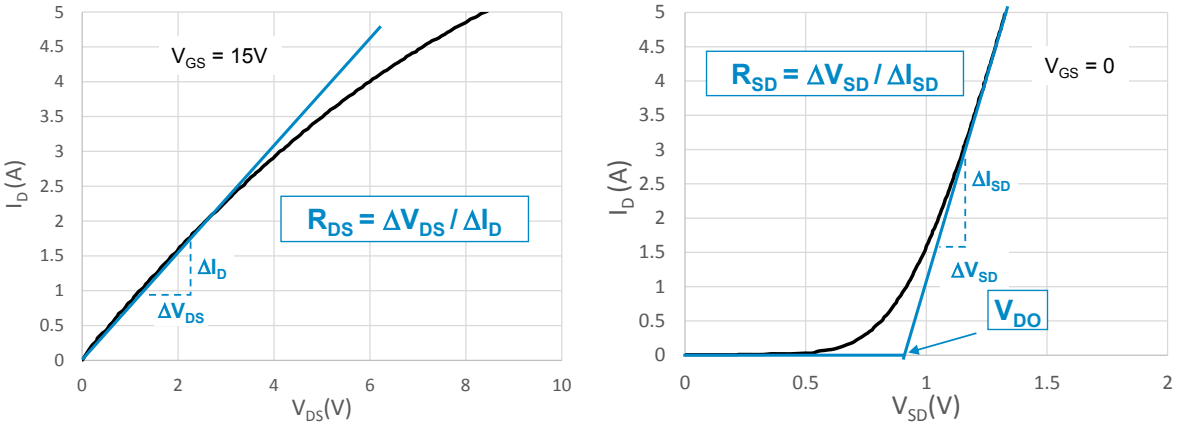
4.1 Conduction power loss

The conduction loss is caused by the MOSFET's and the body diode's voltage drop at rated current. It can be calculated using a linear approximation of the output characteristics for both the MOSFET and the body diode, having a drain-source on-state resistance (R_{DS}) for the first and a series connection of DC voltage source, representing the threshold voltage (V_{DO}) plus a source-drain resistance (R_{SD}) for the latter, as shown in the following figure as a reference.

Figure 25. Examples of MOSFET and body diode approximation of the output



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Both forward characteristics are temperature-dependent, and thus they must be considered under a specified temperature. The linear approximations can be translated for the MOSFET in the following equation:

$$v_{ds}(i_d) = R_{DS} \cdot i_d \quad (13)$$

while for the drain-source body diode:

$$v_{sd}(i_d) = V_{DO} + R_{SD} \cdot i_d \quad (14)$$

The conduction loss of the the MOSFET and the body diode can be derived as the time integral of the product of conduction current and voltage across the devices, as follows:

$$P_{cond\_MOSFET} = \frac{1}{T}\int_0^T v_{ds} \cdot i_d(t)dt = \frac{1}{T}\int_0^T R_{DS} \cdot {i_d}^2(t)dt \quad (15)$$

$$P_{cond\_Diode} = \frac{1}{T}\int_0^T v_{sd} \cdot i_d(t)dt = \frac{1}{T}\int_0^T \left(V_{DO} \cdot i_d(t) + R_{SD} \cdot {i_d}^2(t)\right)dt \quad (@\ V_{GS} = 0) \quad (16)$$

where T is the fundamental period. The different utilization modes of the SLLIMM-nano, modulation technique, and working conditions make the power loss very difficult to estimate; it is therefore necessary to establish some starting points.

Assuming that:

- The application is a variable voltage variable frequency (VVVF) inverter based on sinusoidal PWM technique;
- The switching frequency is high and therefore the output currents are sinusoidal;
- The load is ideal inductive;

under these conditions, the output inverter current is given by:

$$i = \hat{I}\cos(\theta - \emptyset) \quad (17)$$

where Î is the current peak, θ stands for ωt and ϕ is the phase angle between output voltage and current.

The conduction power loss can be obtained as:

$$P_{cond\_MOSFET} = \frac{R_{DS} \cdot \hat{I}^2}{2\pi} \int_{-\frac{\pi}{2}+\emptyset}^{\frac{\pi}{2}+\emptyset} \xi cos^2(\theta - \emptyset) d\theta \quad (18)$$

$$P_{cond\_Diode} = \frac{V_{DO} \cdot \hat{I}^2}{2\pi} \int_{-\frac{\pi}{2}+\emptyset}^{\frac{\pi}{2}+\emptyset} \xi cos^2(\theta - \emptyset) d\theta + \frac{R_{SD} \cdot \hat{I}^2}{2\pi} \int_{-\frac{\pi}{2}+\emptyset}^{\frac{\pi}{2}+\emptyset} \xi cos^2(\theta - \emptyset) d\theta \quad (19)$$

where ξ is the duty cycle for this PWM technique and is given by:

$$\xi = \frac{1 + m_a \cdot cos\theta}{2} \quad (20)$$

and m_a is the PWM amplitude modulation index. Finally, solving Eq. (18) and Eq. (19), we have:

$$P_{cond\_MOSFET} = R_{DS} \cdot \hat{I}^2 \left(\frac{1}{8} + \frac{ma \cdot cos\emptyset}{3\pi}\right) \quad (21)$$

$$P_{cond\_Diode} = V_{DO} \cdot \hat{I} \left(\frac{1}{2\pi} - \frac{ma \cdot cos\emptyset}{8}\right) + R_{SD} \cdot \hat{I}^2 \left(\frac{1}{8} - \frac{ma \cdot cos\emptyset}{3\pi}\right) \quad (@\ V_{GS} = 0) \quad (22)$$

and therefore, the conduction power loss of one device (MOSFET and body diode) is:

$$P_{cond} = P_{cond\_MOSFET} + P_{cond\_Diode} \quad (23)$$

Of course, the total conduction loss per inverter is six times this value.

4.2 Switching power loss

The switching loss is the power consumption during the turn-on and turn-off transients. As shown in Figure 24. Typical MOSFET power loss, it is given by the pulse of the power dissipated during the turn-on (t_{on}) and turn-off (t_{off}).Experimentally, it can be calculated by the time integral of the product of the drain current and drain source voltage for the switching period. In any case, the dynamic performances are strictly related to many parameters such as voltage, current and temperature, so it is necessary to use the same conduction power loss assumptions (Section 4.1 Conduction power loss) to simplify the calculations.

Under these conditions, the switching energy loss is given by:

$$E_{on}(\theta) = \hat{E}_{on} \cos(\theta - \emptyset) \quad (24)$$

$$E_{off}(\theta) = \hat{E}_{off} \cos(\theta - \emptyset) \quad (25)$$

where $\hat{E}_{on}$ and $\hat{E}_{off}$ are the maximum values taken at T_{jmax} and $\hat{I}_c$, θ stands for ωt and ϕ is the phase angle between output voltage and current.

Finally, the switching power loss per device depends on the switching frequency (f_{sw}) and is calculated as follows:

$$P_{sw} = \frac{1}{2\pi} \int_{-\frac{\pi}{2}+\emptyset}^{\frac{\pi}{2}+\emptyset} (E_{MOSFET} + E_{Diode}) \cdot f_{sw} d\theta = \frac{(E_{MOSFET} + E_{Diode}) \cdot f_{sw}}{\pi} \quad (26)$$

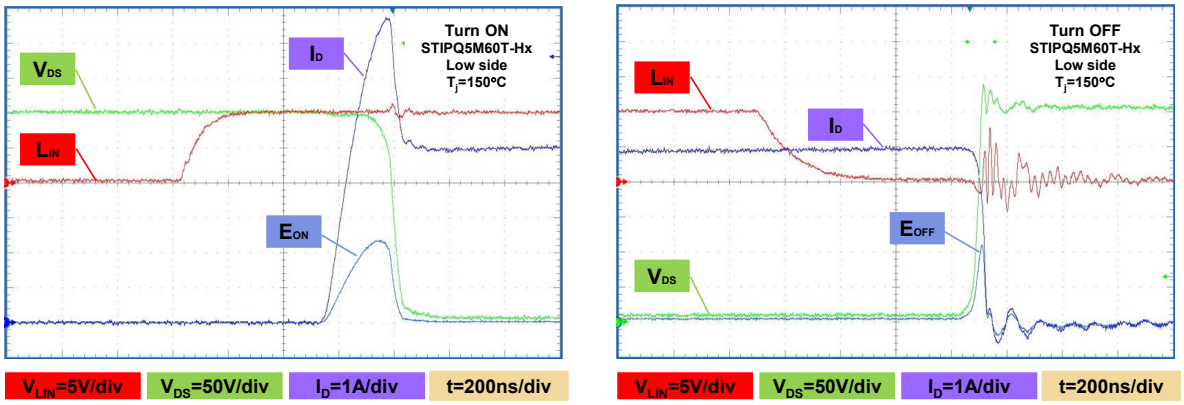
where E_{MOSFET} and E_{Diode} is the total switching energy for the MOSFET and the body diode, respectively. Also in this case, the total switching loss per inverter is six times this value.

Figure 26. Typical switching waveforms of the STIPQ5M60T-Hx shows the real turn-on and turn-off waveforms of STIPQ5M60T-Hx under the following conditions:

- V_{PN} = 300 V, I_D = 5 A, T_j = 150 °C with inductive load on full-bridge topology, taken on the low-side MOSFET.

The blue plots represent instantaneous power as a result of I_{DS} (in purple) and V_{DS} (in green) waveform multiplication, during the switching transitions. The areas under these plots are the switching energies computed by graphic integration, thanks to the digital oscilloscope.

Figure 26. **Typical switching waveforms of the STIPQ5M60T-Hx**



(*) E_{on} and E_{off} are the areas under the blue plots $E = \int (V_{DS} \cdot I_D)\, dt$

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4.3 Thermal impedance overview

During operation, power loss generates heat which elevates the temperature in the internal semiconductor junctions, limiting its performance and lifetime. To ensure a safe and reliable operation, the junction temperature of power devices must be kept below the limits defined in the datasheet, therefore, the generated heat must be conducted away from the power chips and into the environment using an adequate cooling system.

The most common schemes are based on one heatsink designed for free conventional air flow or, in some cases, for forced air circulation. Free conventional air flow systems require larger heatsinks (about 50% bigger) than a forced air-based heatsink, for a given thermal resistance. Therefore, the choice of the cooling system becomes the starting point for the application designer and the thermal aspect of the system is one of the key factors in designing high-efficiency and high-reliability equipment. In this respect, the package and its thermal resistance plays a fundamental role.

Thermal resistance quantifies the ability of a given thermal path to transfer heat in the steady-state and is generally expressed as the ratio between the temperature increase above the reference and the relevant power flow:

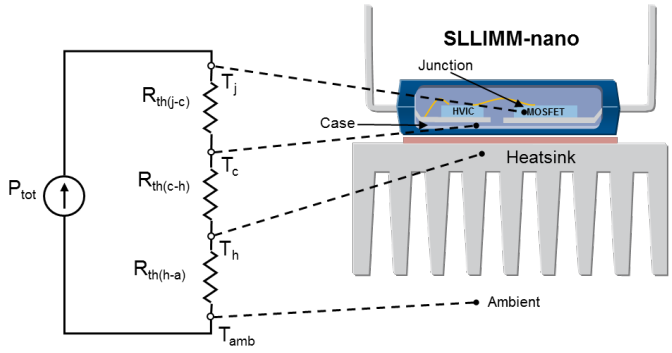
$$R_{th} = \frac{\Delta T}{\Delta P} \tag{27}$$

The thermal resistance specified in the datasheet is the junction-case $R_{th(j\text{-}c)}$, defined as the temperature difference between the junction and case reference divided by the power dissipation per device:

$$R_{th(j-c)} = \frac{T_j - T_c}{P_D} \tag{28}$$

The full-molded package is used as the cooling interface to the heatsink. Thermal grease or some other thermal interface material between the backside and the heatsink is used to reduce the thermal resistance of the interface ($R_{th(c\text{-}h)}$) and, of course, depends on the material and its thickness. Basically, the sum of the three thermal resistance components above gives the thermal resistance between junction and ambient $R_{th(j\text{-}a)}$, as shown in the following figure.

Figure 27. Equivalent thermal circuit with heatsink single MOSFET



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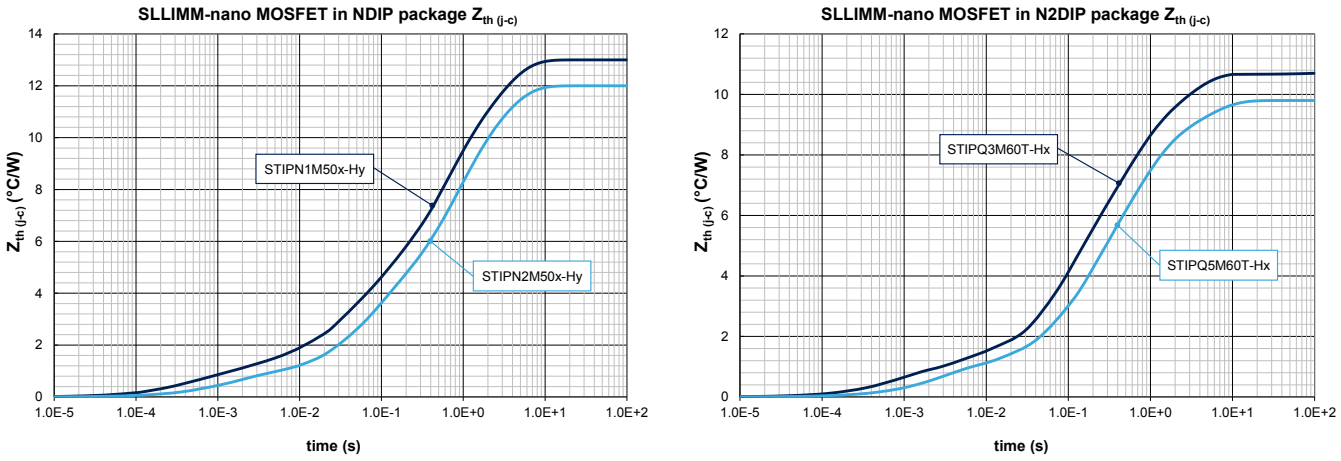
As the power loss P_{tot} is cyclic, the transient thermal impedance must also be considered. It is defined as the ratio between the time dependent temperature increase above the reference, $\Delta T(t)$, and the relevant heat flow:

$$Z_{th}(t) = \frac{\Delta T(t)}{\Delta P} \tag{29}$$

Contrary to what we have already seen regarding the thermal resistance, the thermal impedance is typically represented by an RC equivalent circuit. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature and therefore the advantage of this behavior is the short-term overload capability of the SLLIMM-nano.

For example, the following figure shows the thermal impedance from junction-to-case curves for a single MOSFET of the SLLIMM-nano family.

Figure 28. Thermal impedance $Z_{th(j-c)}$ curves for a single MOSFET



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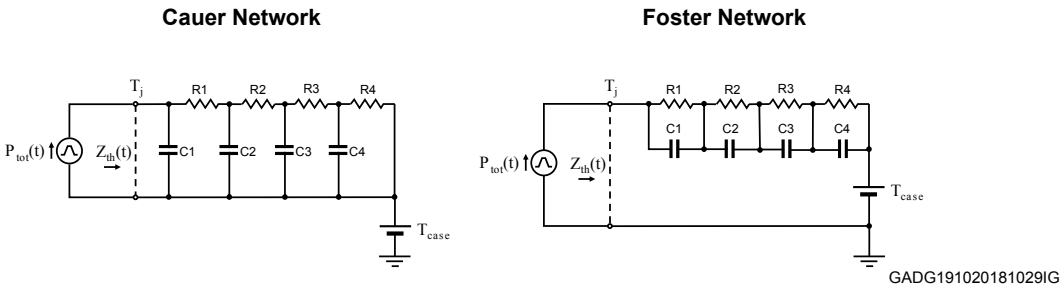
More generally, in the case of the device, power is time-dependent, too. The device temperature can be calculated by using the convolution integral method applied to Eq. (29), as follows:

$$\Delta T(t) = \int_0^t Z_{th}(t-\tau) \cdot P(\tau) d\tau \tag{30}$$

An alternative method, very useful for the simulator tools, is the transient thermal impedance model, which provides a simple method to estimate the junction temperature rise under a transient condition.

By using the thermo-electrical analogy, the transient thermal impedance $Z_{th(t)}$ can be transformed into an electrical equivalent RC network. The number of RC sections increases the model detail, therefore a fourth order model based on the Cauer or Foster network has been adopted to improve the accuracy of the model, as shown in the following figure.

Figure 29. **Cauer and Foster RC equivalent circuits**



Temperatures inside the electrical RC network represent voltages, power flows represent currents, electrical resistances and capacitances represent thermal resistances and capacitances respectively. The case temperature is represented with a DC voltage source and it can be interpreted as the initial junction temperature.

Transient thermal impedance models are derived by curve fitting an equation to the measured data. Values for the individual resistors and capacitors are the variables from that equation and are defined in the following tables for both Cauer and Foster thermal networks.

Table 10. **Cauer RC thermal network elements for SLLIMM-nano MOSFETs**

Element	STIPN1M50x-Hy	STIPN2M50x-Hy	STIPQ3M60T-Hx	STIPQ5M60T-Hx
R1 (°C/W)	1.26	0.89	1.12	1.05
R2 (°C/W)	3.49	3.57	4.90	4.62
R3 (°C/W)	5.53	5.46	3.19	2.86
R4 (°C/W)	2.72	2.07	1.48	1.27
C1 (W·s/°C)	5.76E-04	1.65E-03	1.07E-03	2.77E-03
C2 (W·s/°C)	1.24E-02	1.89E-02	2.06E-02	3.53E-02
C3 (W·s/°C)	8.25E-02	1.14E-01	1.31E-01	1.97E-01
C4 (W·s/°C)	7.28E-01	9.74E-01	1.37	2.84

Table 11. **Foster RC thermal network elements for SLLIMM-nano MOSFETs**

Element	STIPN1M50x-Hy	STIPN2M50x-Hy	STIPQ3M60T-Hx	STIPQ5M60T-Hx
R1 (°C/W)	4.70	0.75	2.53	4.30
R2 (°C/W)	1.14	2.55	3.27	2.80
R3 (°C/W)	4.56	4.25	1.01	1.80
R4 (°C/W)	2.60	4.45	3.88	0.90
C1 (W·s/°C)	9.73E-02	1.80E-03	9.14E-01	1.50E-01
C2 (W·s/°C)	6.03E-04	2.40E-02	2.68E-02	5.00E-02
C3 (W·s/°C)	5.09E-01	5.70E-01	1.13E-03	2.20
C4 (W·s/°C)	1.49E-02	1.40E-01	1.14E-01	3.00E-03

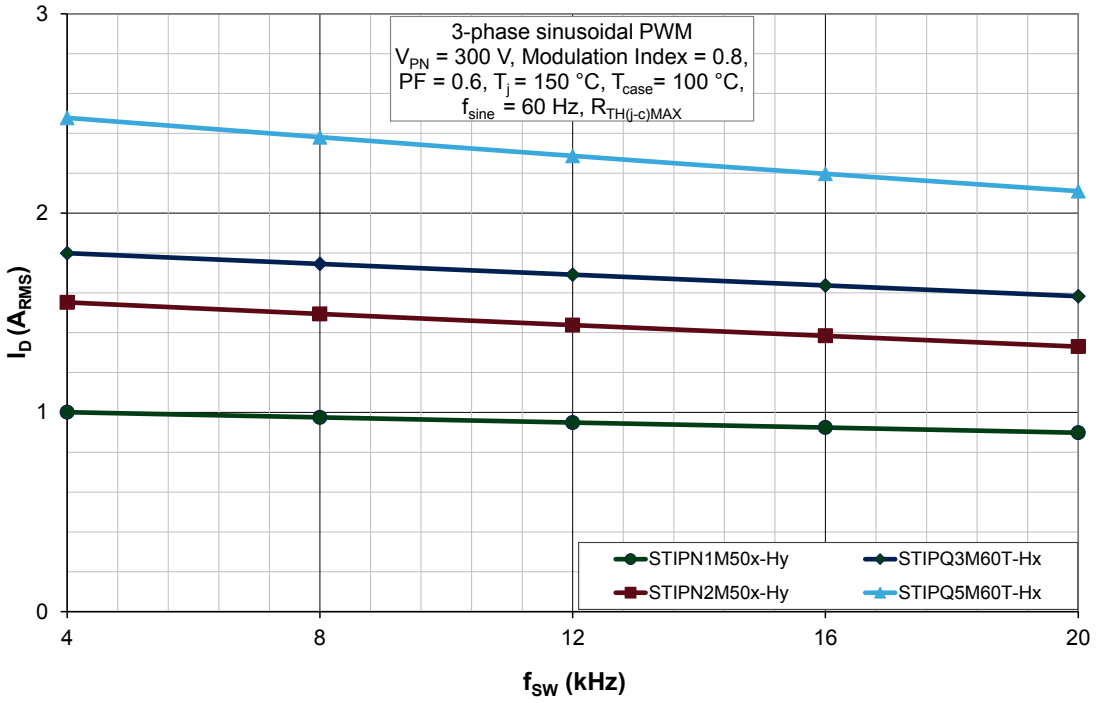
4.4 Power loss calculation example

As a result of the power loss calculation and thermal aspects discussed in the previous sections, we are able to simulate the maximum $I_{D(RMS)}$ current versus switching frequency curves for a VVVF inverter using a 3-phase sinusoidal PWM to synthesize sinusoidal output currents.

The curves graphed in Figure 30. Maximum $I_{D(RMS)}$ current vs f_{sw} simulated curves below represent the maximum current managed by the SLLIMM- nano MOSFET in safety conditions, when the junction temperature rises to the maximum junction temperature of 150 °C and the case temperature is 100 °C, which is a typical operating condition to guarantee the reliability of the system. These curves, which are functions of the motor drive typology and control scheme, are simulated under the following conditions:

V_{PN} = 300 V, MI = 0.8, PF = 0.6, T_j =150 °C, T_{case} = 100 °C, f_{sine} = 60 Hz, maximum value of $R_{th(j-c)}$, typical $V_{DS(ON)}$ and E_{tot} values.

Figure 30. Maximum $I_{D(RMS)}$ current vs f_{sw} simulated curves



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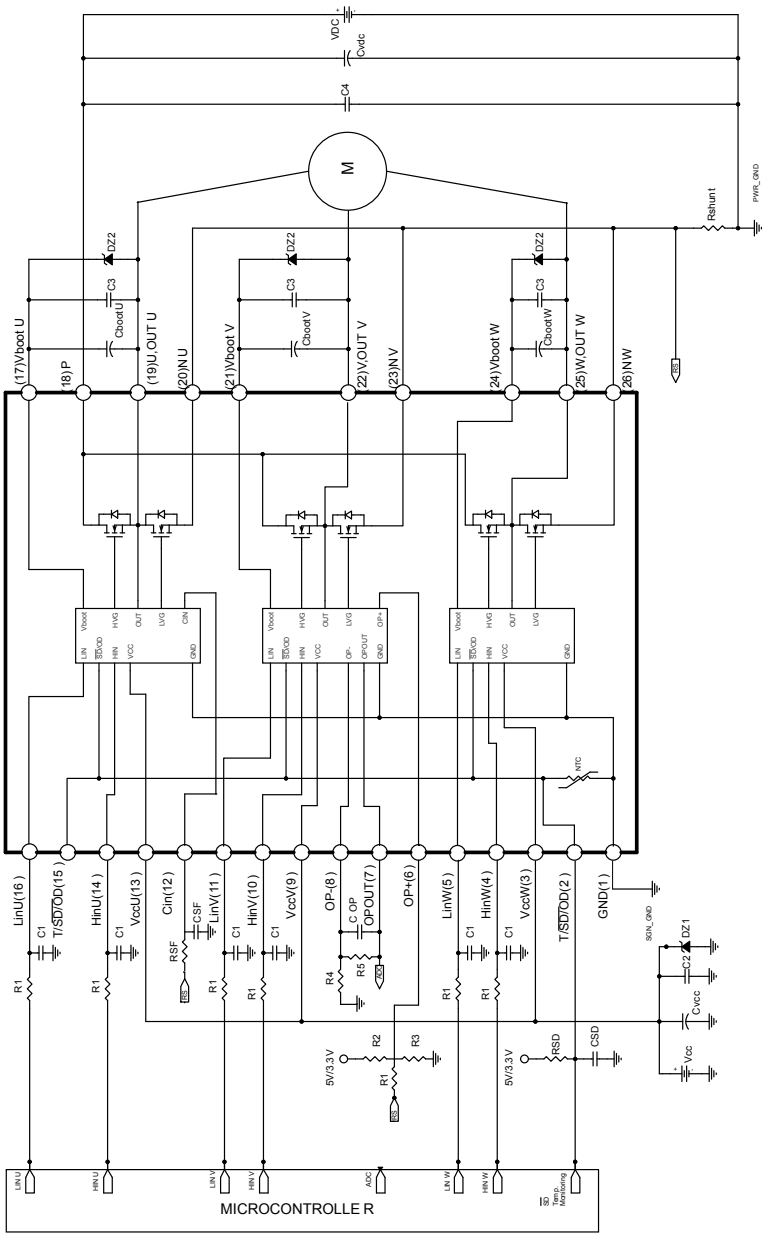
5 Design guidelines

This section provides the main layout suggestions for an optimized design and the major recommendations to appropriately handle and assemble the SLLIMM-nano family.

5.1 Typical application circuit and recommendations

The following figure shows a typical application circuit using the SLLIMM-nano family, including signal interfaces with the MCU.

Figure 31. Typical application circuit



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Here are some hardware and PCB layout recommendations:

- Input signals HIN, LIN are active-high logic. A 375 kΩ (typ.) pull-down resistor is built-in for each input. To prevent the input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R_1, C_1) on each input signal is suggested. The filters should be with a time constant of about 100 ns and placed as close as possible to the IPM input pins.

- The use of a bypass capacitor C_{VCC} (aluminum or tantalum) can help to reduce the transient circuit demand on the power supply. Besides, to reduce any high-frequency switching noise distributed on the power lines, a decoupling capacitor C_2 (100 to 220 nF, with low ESR and low ESL) should be placed as close as possible to the V_{cc} pin and in parallel with the bypass capacitor.
- The use of an RC filter (R_{SF}, C_{SF}) can prevent protection circuit malfunction. The time constant (R_{SF} x C_{SF}) should be set to 1 µs and the filter must be placed as close as possible to CIN pin.
- The $\overline{SD}$ is an input/output pin (open-drain type if used as output). A built-in thermistor NTC is internally connected between the $\overline{SD}$ pin and GND. The voltage VSD-GND decreases as the temperature increases, due to RSD pull-up resistor . In order to be sure that the voltage is always higher than the high level logic threshold, the pull-up resistor should be set to 1 kΩ or 2.2 kΩ for 3.3 V or 5 V MCU power supply, respectively. The CSD capacitor of the filter on $\overline{SD}$ should not be higher than 3.3 nF in order to assure the $\overline{SD}$ activation time $T_1 \leq$ 500 ns; the filter should be placed as close as possible to the $\overline{SD}$ pin.
- The decoupling capacitor C_3 (from 100 to 220 nF, ceramic with low ESR and low ESL), in parallel with each C_{boot}, filters the high-frequency disturbance. Both C_{boot} and C_3 (if present) should be placed as close as possible to the U, V, W and V_{boot} pins. Bootstrap negative electrodes should be connected to U, V, W terminals directly and separated from the main output wires.
- To prevent the overvoltage on V_{cc} pin, a Zener diode (Dz1) can be used. Similarly on the V_{boot} pin, a Zener diode (Dz2) can be placed in parallel with each C_{boot}.
- The use of the decoupling capacitor C_4 (100 to 220 nF, with low ESR and low ESL), in parallel with the electrolytic capacitor C_{vdc}, prevents surge destruction. Both capacitors C_4 and C_{vdc} should be placed as close as possible to the IPM (C_4 has priority over C_{vdc}).
- By integrating an application-specific type HVIC inside the module, direct coupling to the MCU terminals without an optocoupler is possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- In order to avoid malfunctions, the wiring on N pins, the shunt resistor and PWR_GND should be as short as possible.
- The connection of SGN_GND to PWR_GND on one point only (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.

5.2 Layout suggestions

PCB layout optimization for high-voltage, high-current and high switching frequency applications is a critical factor. PCB layout is a complex matter involving several aspects such as track length and width and circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application function properly and achieve expected performance. On the other hand, PCBs without a careful layout can generate EMI issues (both induced and perceived by the application), can create overvoltage spikes due to parasitic inductances along the PCB traces, and can produce higher power loss and even malfunction in the control and sensing stages.

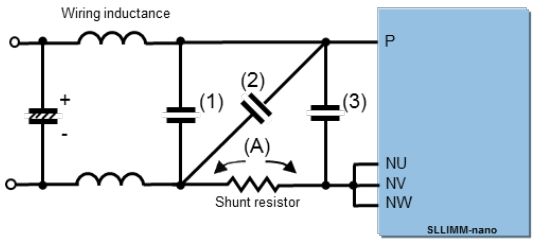
The compactness of the SLLIMM-nano solution, which offers an optimized gate driving network and reduced parasitic elements, allows designers to concentrate on other issues such as the ground or noise filter. In any case, to avoid the aforementioned conditions, the following general PCB layout guidelines and suggestions should be followed for 3-phase applications.

For more information please refer to application note AN4694.

5.2.1 General suggestions

- PCB traces should be designed as short as possible, and the area of the circuit (power or signal) should be minimized to reduce the sensitivity of such structures to surrounding noise.
- Ensure a good distance between the switching lines with high-voltage transitions and the signal lines sensitive to electrical noise. Specifically, the tracks of each OUT phase carrying significant currents and voltages should be separated from logic lines and analog op-amp and comparator sensing circuits.
- Place the R_{SENSE} resistors as close as possible to the low-side pins of the SLLIMM- nano (N U, N V and N W). Parasitic inductance can be minimized by connecting the ground line (also called driver ground) of the SLLIMM-nano directly to the cold terminal of sense resistors. Use a low inductance type resistor, such as an SMD resistor instead of long lead type resistors, to help further decrease parasitic inductance.
- Avoid any ground loop. Only a single path must connect two different ground nodes.
- Place each RC filter as close as possible to the SLLIMM-nano pins in order to increase their effectiveness.
- Fixed voltage tracks such as GND or HV lines can be used to shield the logic and analog lines from electrical noise produced by the switching lines (e.g., OUT U, OUT V and OUT W).
- Generally, it is recommended to connect each half bridge ground in a star configuration and the three R_{SENSE} very close to each other and to the power ground.
- In order to prevent surge destruction, the wiring between the snubber capacitor and the P N pins should be as short as possible. The use of a high-frequency, high-voltage non-inductive capacitor of about 0.1 or 0.22 µF is recommended. In order to effectively suppress the surge voltage, the snubber capacitor has to be placed in position (2) in Figure 32. Recommended snubber capacitor position below .The position (1) is incorrect for effective surge voltage suppression. If the capacitor is placed on the position (3), the charging and discharging currents generated by wiring inductance and the snubber capacitor will appear on the shunt resistor with possible undesired protection activation, even if the surge suppression effect is the greatest. Finally, position (2) is the right compromise. The parasitic inductance on the A tracks (including that of the shunt resistor) should be as small as possible in order to suppress the surge voltage.

Figure 32. Recommended snubber capacitor position



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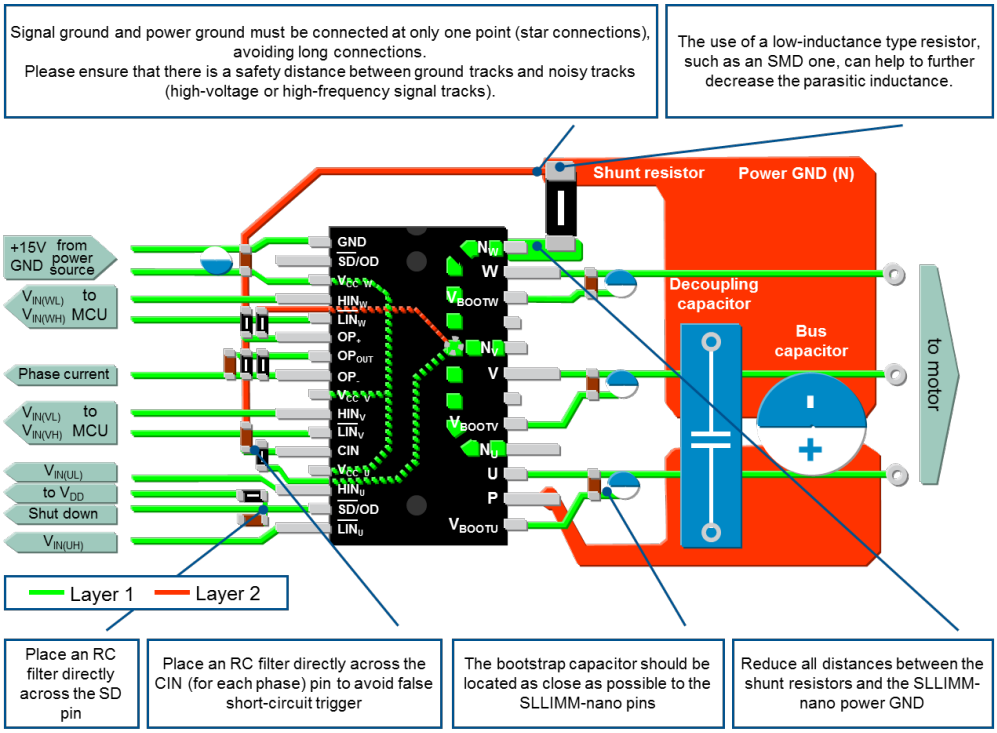
The following figure summarizes some general suggestions for all SLLIMM-nano products.

Figure 33. General suggestions



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6 Mounting and handling instructions

Some basic assembly rules must be followed in order to limit thermal and mechanical stress and optimize the thermal conduction and electrical isolation for the NDIP/N2DIP package when mounting a heatsink.

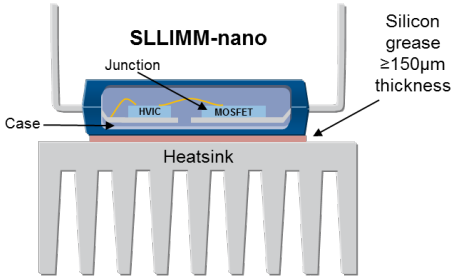
Moreover, semiconductors are normally electrostatic discharge sensitive devices (ESDS) requiring specific precautionary measures regarding handling and processing. Static discharges caused by human touch or by processing tools may cause high-current and/or high-voltage pulses which may damage or even destroy sensitive semiconductor structures. Integrated circuits (ICs) may also be charged by static during processing. If discharging takes place too quickly (“hard” discharge), it may cause peak loads and consequent damage.

Make careful choices regarding workspaces, personal equipment and processing and assembly equipment.

6.1 Heatsink mounting

- When attaching a heatsink to a SLLIMM-nano, do not apply excessive force to the device for assembly. Drill holes for screws in the heatsink exactly as specified. Smooth the surface by removing burrs and protrusions. Do not touch the heatsink when the SLLIMM-nano is operational to avoid burn injury.
- To get the most effective heat dissipation, enlarge the contact area as much as possible to minimize the contact thermal resistance. The proper application of thermal-conductive grease over the contact surface between modules and heatsinks is also useful for preventing contact surfaces from corrosion. Apply a minimum 150 µm layer of thermal grease to the module base plate or to the heatsink, as shown in the figure below. Use a torque screwdriver to fasten to the maximum specified torque rating. Exceeding the maximum torque may lead to module damage or degradation.
- Remove any dirt from the contact surface.
- Ensure the grease quality remains constant over time and is able to perform long-term over a wide operating temperature range.

Figure 34. Recommended silicon grease thickness and positioning



6.1.1 Mounting torque

Mounting torque, heatsink flatness, screw fastening sequence and many other precautions regarding handling and contamination, ESD, storage and transportation are available in the Technical note TN1037 *"SLLIMM™-nano mounting instructions and heatsink"* and TN1221 *"Mounting instruction for SLLIMM™ -nano 2nd series (N2DIP-26L)"*.

7 References

- STIPN1M50x-Hy datasheet
- STIPN2M50x-Hy datasheet
- STIPQ3M60T-Hx datasheet
- STIPQ5M60T-Hx datasheet
- AN4043 – *“SLLIMM™-nano”*
- AN4840 – *“SLLIMM™-nano 2nd series”*
- AN4694 – *“EMC design guides for motor control applications"*
- AN4966 – *“Design guidelines for the shutdown function in the SLLIMM-nano series”*
- TN1037 – *“Mounting instruction for SLLIMM™-nano”*
- TN1221 – *“Mounting instruction for SLLIMM™-nano 2nd series”*

Revision history

Table 12. **Document revision history**

Date	Version	Changes
20-Nov-2018	1	First release.

Contents

List of tables

List of figures