AN5312
Application note

Migration from RevY to RevV for STM32H743/753 and STM32H750 Value line microcontrollers

Introduction

The major limitations identified on silicon revision Y (RevY) of STM32H743/753xx and STM32H750 Value line MCUs have been fixed on revision V (RevV).

The detailed list of limitations is available in the errata sheet document. In addition to fixed limitations, some peripheral updates have been carried out.

This application note shows the differences to take in consideration when migrating from one revision to another.

For STM32H750 Value line MCUs all listed updates are available, unless those related to the Flash memory features, restricted to STM32H743/753xx.

RevV is software compatible with revision X (RevX), there is no functional difference between them.

Regarding electrical characteristics, there is no difference in between RevX and RevV, except for the USB pull-up enhancement.

RM0433 “STM32H743/753 and STM32H750 advanced ARM®-based 32-bit MCUs”, available on *www.st.com*, is the reference document.

Contents

List of tables

List of figures

1 Modified peripherals

The STM32H7 Series microcontrollers are based on Arm®(a) Cortex® processor(s).

The following peripherals have been modified passing from RevY to RevV:

- *FLASH*
- *PWR*
- *RCC*
- *CRS*
- *GPIO* (alternate functions only)
- *SYSCFG*
- *ADC*
- *CRYP*
- *USB*
- *TIM*

1.1 FLASH

1.1.1 Write sequence

On RevV the behavior of BSY1/2 has changed compared to RevY. This bit indicates that an effective write, erase or option byte change operation is ongoing in the non-volatile memory. The bit can toggle during the write operation.

The recommended write sequence is updated as follows:

1. unlock the FLASH_CR1/2 register (only if register is not already unlocked)
2. enable write operations by setting the PG1/2 bits in the FLASH_CR1/2 registers
3. check the protection of the targeted memory areas
4. write one Flash memory word (corresponding to 32-byte) data starting at a 32-byte aligned address
5. check that QW1/QW2 (respectively for FLASH_CR1/2) has been set high and wait until it is reset to 0.

This change has an impact on custom Flash memory loader/write sequence.

arm

a. Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1.2 Dynamic swap bank

On RevV the swap bank feature is available, with a minor change compared to RevY. The swap bank bit (highlighted cells in *Figure 1*) in FLASH_OPTCR is read-only.

Figure 1. Change in FLASH_OPTCR register

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x018	FLASH_OPTCR	**SWAP_BANK**	OPTCHANGEERRIE	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	MER	Res.	Res.	OPTSTART	OPTLOCK
	0x00000001	0	0																											0			0	1

Since FLASH_OPTCR is read-only, it is not possible to swap banks on the fly.

1.1.3 Flash memory CRC

Flash memory CRC calculation is available on RevV, with new control bits compared to RevY.

The concerned bits are CRCRDERRIE, CRCRDERR and CLR_CRCRDERR (for both bank 1 and bank 2), highlighted in gray in *Figure 2*. ALL_BANK bit (highlighted in light gray in *Figure 2*) has been added to run CRC on the full Flash memory bank.

Figure 2. Changes in FLASH registers

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x00C	FLASH_CR1	Res.	Res.	Res.	**CRCRDERRIE1**	CRCENDIE1	DBECCERRIE1	SNECCERRIE1	RDSERRIE1	RDPERRIE1	OPERRIE1	INCERRIE1	Res.	STRBERRIE1	PGSERRIE1	WRPERRIE1	EOPIE1	CRC_EN	Res.	Res.	Res.	Res.	SNB1			START1	FW1	PSIZE1		BER1	SER1	PG1	LOCK1
	0x00000031				0	0	0	0	0	0	0	0		0	0	0	0	0					0	0	0	0	0	1	1	0	0	0	1
0x010	FLASH_SR1	Res.	Res.	Res.	**CRCRDERR1**	CRCEND1	DBECCERR1	SNECCERR1	RDSERR1	RDPERR1	OPERRIE1	INCERR1	Res.	STRBERR1	PGSERR1	WRPERR1	EOP1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	CRC_BUSY1	QW1	WBNE1	BSY1
	0x00000000				0	0	0	0	0	0	0	0		0	0	0	0													0	0	0	0
0x014	FLASH_CCR1	Res.	Res.	Res.	**CLR_CRCRDERR1**	CLR_CRCEND1	CLR_DBECCERR1	CLR_SNECCERR1	CLR_RDSERR1	CLR_RDPERR1	CLR_OPERRIE1	CLR_INCERR1	Res.	CLR_STRBERR1	CLR_PGSERR1	CLR_WRPERR1	CLR_EOP1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
	0x00000000				0	0	0	0	0	0	0	0		0	0	0	0																
0x050	FLASH_CRCCR1	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	**ALL_BANK**	CRC_BURST		Res.	Res.	CLEAN_CRC	START_CRC	Res.	Res.	Res.	Res.	Res.	CLEAN_SECT	ADD_SECT	CRC_BY_SECT	Res.	Res.	Res.	Res.	Res.	Res.	CRC_SECT	
	0x001C0000										0	0	1			0	0						0	0	0						0	0	0

1.2 PWR

1.2.1 Voltage scaling

In addition to voltage scales available on RevY, RevV introduces a new V_{core} level (VOS0) that boosts the device performance (maximum frequency). VOS0 is activated via a dedicated sequence and a bit in the SYSCFG controller.

Table 1. VOS0 overview

VOS0	RevY	RevV
Typical range	Not available	1.36 V
Flash memory wait states		4

1.2.2 Monitoring low-power modes

RevV introduces low-power state monitoring pins, to monitor the CPU and domain state transition to low-power modes. The GPIO pin corresponding to each monitoring signal has to be programmed in alternate function mode.

This feature is not available in system Standby mode since these I/O pins are switched to high impedance.

Table 2. Low-power modes monitoring pin overview

Power state monitoring pins	Description
CSLEEP	Sleeping state
CDSLEEP	Deep sleep CPU state
DxPWREN	Domain (Dx, x= 1 or 2) power enabled

The values of the monitoring pins reflect the state of the CPU(s) and domain(s). Refer to *Table 3* for the GPIO state depending on CPU and domain state.

Table 3. GPIO state according to CPU and domain state

Domain DxPWREN	CPU		Power state	
	CSLEEP	CDSLEEP	CPU	Domain x
1	0	0	Run mode	DRun mode
1	1	0	Sleep mode	
1	0	1	Run mode	
1	1	1	Deep sleep mode	DStop mode
0	-	-	-	DStandby mode

1.3 RCC

1.3.1 HSI / CSI trimming bits extension

Register RCC_ICSCR in RevY is replaced in RevV by the two registers RCC_HSICFGR and RCC_CSICFGR. As shown in *Figure 3*:

- HSITRIM and HSICAL (cells in gray) are moved to RCC_HSICFGR register and HSITRIM bit field is extended from 6 to 7 bits
- CSITRIM and CSICAL (cells in light gray) are moved to the RCC_CSICFGR register, CSITRIM bit field is extended from 5 to 6 bits and CSICAL bit field is extended from 8 to 10 bits.

The bit field offsets are changed compared to RevY.

Figure 3. Changes in RCC registers

Rev Y

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x004	RCC_ICSCR	Res.	CSITRIM[4:0]					CSICAL[7:0]								HSITRIM[5:0]						HSICAL[11:0]											
	Reset value		1	0	0	0	0	-	-	-	-	-	-	-	-	1	0	0	0	0	0	-	-	-	-	-	-	-	-	-	-	-	-

RevV

		31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x004	RCC_HSICFGR	Res.	HSITRIM[6:0]							Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	HSICAL[11:0]											
	Reset value		1	0	0	0	0	0	0													X	X	X	X	X	X	X	X	X	X	X	X
0x00C	RCC_CSICFGR	Res.	Res.	CSITRIM[5:0]						Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	CSICAL[9:0]									
	Reset value			1	0	0	0	0	0															X	X	X	X	X	X	X	X	X	X

1.3.2 Kernel clocks

On RevV the ADC requires an input clock two times faster than the sampling clock. The maximum allowed ADC input clock frequency is 100 MHz instead of 36 MHz.

1.3.3 LSE drive change on the fly

The LSE also offers a programmable driving capability (LSEDRV[1:0]) that can be used to modulate the amplifier driving capability. On RevV the driving capability cannot be changed when the LSE oscillator is ON.

1.4 CRS

To allow the user application to tune HSI48 oscillator using an external source, the SYNC signal source in RevV authorizes to select an external pin (via the SYNCSRC bit field of the CRS_CFGR register).

Table 4. External pin selection

SYNCSRC	RevV	RevY
0	CRS_SYNC pin (external) is the SYNC signal	OTG HS2 SOF is the SYNC signal
1	LSE is the SYNC signal	
2	OTG HS1 SOF is the SYNC signal	
3	OTG HS2 SOF is the SYNC signal	Reserved

Binary codes using OTG HS2 SOF as SYNC signal on RevY are not compatible with RevV.

1.5 GPIO

For more flexibility, new alternate functions are added on RevV.

Table 5. New alternate functions

Number	Name
PB3: AF10	CRS_SYNC
PG11: AF01	LPTIM1_IN2
PC2: AF0	CDSLEEP
PC3: AF0	CSLEEP
PA4: AF0	D1PWREN
PA5: AF0	D2PWREN

There is no impact on applications designed with RevY.

1.6 SYSCFG

1.6.1 Boost V_{DD} selection

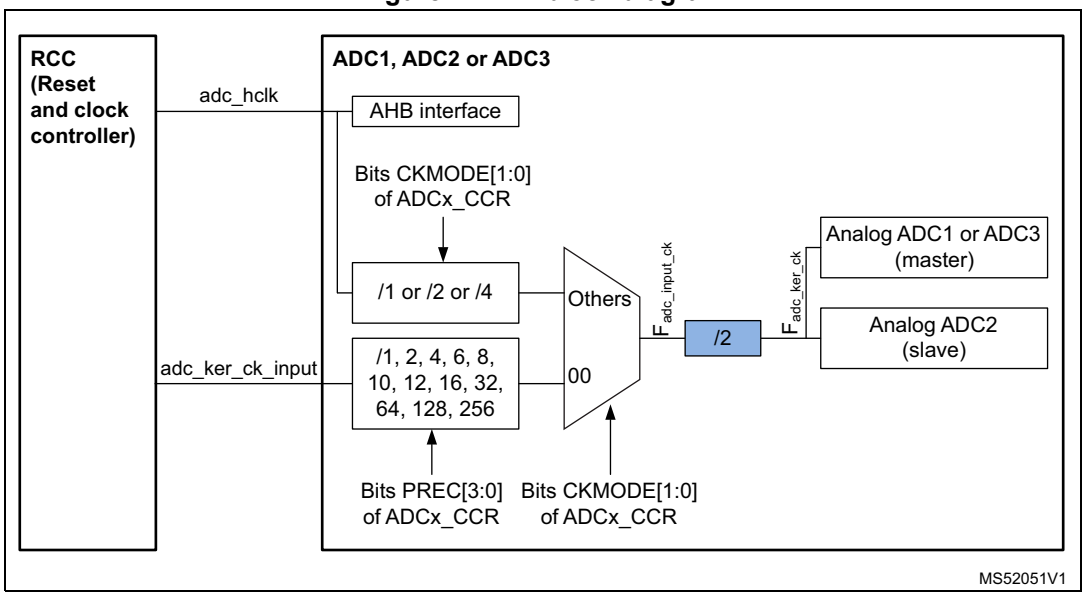
BOOSTVDDSEL bit is added to the SYSCFG_PMCR register to select the analog switch supply voltage.

1.7 ADC

1.7.1 ADC clocks

One of the major changes on the ADC interface is the clock scheme. With the addition of a divider by 2 (highlighted in *Figure 4*) Fadc_ker_ck for analog block is half the ADC input clock frequency.

Figure 4. ADC block diagram



On RevV the ADC kernel clock must be twice the frequency needed for the sampling (as an example, if a 25 MHz clock is needed, ADC kernel clock must be set to 50 MHz).

1.7.2 ADC boost

On RevV Boost mode control bit of ADC_CR register is modified, the BOOST configuration bit is extended from a single bit to two bits. The possible configurations are defined in *Table 6*.

Table 6. ADC clock frequency

BOOST[9:8]	RevV	RevY
00	f ≤ 6.25 MHz	f < 20 MHz
01	6.25 MHz < f ≤ 12.5 MHz	f > 20 MHz
10	12.5 MHz < f ≤ 25 MHz	Not available
11	25 MHz < f ≤ 50 MHz	

1.7.3 ADC resolution

On RevV the data resolution bitfield (bits 4:2 RES[2:0] bits of ADC_CFGR register) is modified as shown in *Table 7*.

Table 7. ADC resolution

RES[2:0]	RevV	RevY
000	16-bit	
001	14-bit	
010	12-bit	
011	10-bit	
100	Reserved	8-bit
111	8-bit	Reserved

1.8 CRYP

RevV supports hardware management for GCM encryption or CCM decryption with the last block of payload size inferior to 128 bits. This is possible thanks to the addition of the NPBLB bit field (the highlighted cells in *Figure 5*) in the CRYP_CR register.

Figure 5. Changes in CRYP_CR register

RevY

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ALGO MODE3	Res.	GCM_CCMPH [1:0]	
												rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPEN	FFLUSH	Res.	Res.	Res.	Res.	KEYSIZE[1:0]		DATATYPE[1:0]		ALGOMODE[2:0]			ALGODIR	Res.	Res.
rw	w					rw	rw	rw	rw	rw	rw	rw	rw		

RevV

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	**NPBLB[3:0]**				ALGO MODE3	Res.	GCM_CCMPH [1:0]	
								rw	rw	rw	rw	rw		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRYPEN	FFLUSH	Res.	Res.	Res.	Res.	KEYSIZE[1:0]		DATATYPE[1:0]		ALGOMODE[2:0]			ALGODIR	Res.	Res.
rw	w					rw	rw	rw	rw	rw	rw	rw	rw		

1.9 USB

The USB controller on RevV is updated to support descriptor-based scatter / gather DMA controller for Device and Host mode, improving performance for Device mode isochronous endpoints. Software needs to be modified to support scatter / gather feature.

Table 8. Updated OTG_HS registers

Register	RevV	RevY	Comments
OTG_HCFG	– Bit 26 PERSSCHEDENA: Enable periodic scheduling – Bits 25:24 FRLSTEN[1:0]: Frame list entries – Bit 23 DESCDMA: Enable scatter / gather DMA mode	– Bit [26:23] Reserved	Applicable in host scatter / gather DMA mode only
OTG_HFLBADDR	– HFLBADDR[31:0]: The starting address of the frame list (scatter/gather mode).	-	
OTG_HCCHARx	– Bit 29: Reserved	– Bit 29: ODDFRM: Odd frame	ODDFRM bit reserved in RevV
OTG_HCINTx	– Bit 13 DESCLSTROLL: Descriptor rollover interrupt. – Bit 12 XCSXACTERR: Excessive transaction error. – Bit 11 BNA: Buffer not available interrupt.	– Bit [13:11]: Reserved	Applicable in host scatter / gather DMA mode only
OTG_HCINTMSKx	– Bit 13 DESCLSTROLLMSK: Descriptor rollover interrupt mask register. – Bit 11 BNAMSK: Buffer not available interrupt mask register. – Bit 2 AHBERRM: AHB error. In scatter/gather DMA mode for host, interrupts will not be generated due to the corresponding bits set in OTG_HCINTx.	– Bit 2: AHBERRM: AHB error	
OTG_HSIZESGx	New register	-	Applicable in host scatter / gather DMA mode only
OTG_HCDMASGx		-	
OTG_HCDMABx		-	
OTG_DIEPMSK	– Bit 9: BNAM: BNA interrupt mask	-	Applicable in Device mode
OTG_DOEPMSK		-	
OTG_HS_DIEPEACHMSK1		-	
OTG_HS_DOEPEACHMSK1		-	
OTG_DIEPINTx	– Bit 9 BNA: Buffer not available interrupt	-	
OTG_DOEPINTx		-	

1.10 TIM

The spdifrx_frame_sync is no longer mapped on TIM 17, but is linked to TIM12 on RevV.

Table 9. Alternate functions

Domain	Bus	Peripheral	Signal	RevY	RevV	Trigger input
D2	APB1	SPDIFRX	spdifrx_frame_sync	TIM17	TIM12	TI1_1

2 Conclusion

Although there is a large compatibility between RevV and RevY, migrating from one silicon revision to another requires a few adjustments, detailed in this document. For more details refer to RM0433, available on *www.st.com*.

3 Revision history

Table 10. Document revision history

Date	Revision	Changes
04-Apr-2019	1	Initial release.