Migrating from STM32L4 and STM32L4+ to STM32U5 MCUs

Introduction

The designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another one from the same product family or products from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os.
- To meet cost reduction constraints that require to switch to smaller components and shrink the PCB area.

This document details the steps to migrate from an existing design based on the STM32L4 and STM32L4+ MCUs to an application based on one of the STM32U5 MCUs.

This document provides the full set of features available for STM32L4 and STM32L4+ MCUs, and the equivalent features of STM32U5 MCUs. This document also provides guidelines on both hardware and peripheral migration.

To better understand the information inside this application note, the user must be familiar with the STM32 microcontroller family.

This application note is a complement to the STM32L4, STM32L4+, and STM32U5 datasheets and reference manuals.

For additional information, refer to the product datasheets and reference manuals available on www.st.com

Table 1. Reference documents

Document number	Title
[1]	STM32L41xxx/42xxx/43xxx/44xxx/45xxx/46xxx Arm®-based 32-bit MCUs reference manual (RM0394).
[2]	STM32L47xxx, STM32L48xxx, STM32L49xxx, and STM32L4Axxx Arm®-based 32-bit MCUs reference manual (RM0351).
[3]	STM32L4+ series Arm®-based 32-bit MCUs reference manual (RM0432).
[4]	STM32U5 series Arm®-based 32-bit MCU's reference manual (RM0456).
[5]	STM32 microcontroller system memory boot mode application note (AN2606).

1 General information

This document applies to Arm®-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 STM32U5 series overview

Compared to the STM32L4 and STM32L4+ series, the STM32U5 series use a newer technology to achieve excellence in ultralow power, increased security, with enhanced efficiency, performance, and memory size such as:

- Up to 4 Mbytes of flash memory.
- Up to 3 Mbytes of RAM.
- Ultra-low-power Arm®Cortex®-M33 32-bit core, with TrustZone® for Armv8-M.
- ST instruction cache (ICACHE), supporting both internal and external memories.
- A dedicated data cache (DCACHE1) for external memories.
- In terms of graphic features, STM32U5x7/5x9 lines benefit of advanced peripherals offering best-in-class processing, like the NeoChrom graphic processor with its dedicated DCACHE2, the Chrom-GRC, or a JPEG codex on STM32U5Fx/STM32U5Gx.

2.1 Main features

The STM32U5 MCUs include a larger set of peripherals and advanced features, compared to the STM32L4 and STM32L4+ MCUs, such as the ones listed below:

- **Security**
  - Arm®TrustZone® and securable I/Os, memories, and peripherals
  - RDP and password protected debug, active tamper, secure firmware upgrade support, secure firmware installation, secure hide protection
  - Up to eight configurable SAU regions
  - Additional encryption accelerator engine (available only on STM3U585xx devices)
    - HASH hardware accelerator
    - Two advanced encryption hardware accelerators (AES) including one with DPA resistance
    - Public key accelerator (PKA), DPA resistant
    - On-the-fly decryption engine of OCTOSPI (OTFDEC)
- **Power consumption**
  - Embedded regulator (LDO)
  - SMPS step-down converter
    - Regulators are placed in parallel. Thus, it is possible to switch from one to another on the fly.
    - Both regulators can provide four different voltages (voltage scaling) and can operate in Stop modes.
  - Optimized RTC consumption
- **Performance**
  - Frequency up to 160 MHz
  - Direct access to Flash interface through ICACHE (without passing by AHB bus)
  - ICACHE for internal and external memories
  - DCACHE for external memories
- **Graphic**
  - NeoChrom graphic processor (GPU2D) supporting HW Vector Graphic
  - Chrom-GRC (GFXMMU)
  - Chrom-ART (DMA2D)
  - Dedicated Data CACHE (DCACHE2)
  - JPEG compressor/decompressor
  - MIPI DSI Host Controller

- **New peripherals**
  - Advanced 14-bit ADC and ultralow power 12-bit ADC
  - Mathematics accelerators: FMAC and CORDIC
  - Digital filters: MDF and ADF
  - Hexadeca-SPI interface (HSPI)

Note: This document only compares the differences between the common features in the STM32L4 and STM32L4+ MCUs against the STM32U5 MCUs. The new features of series, mainly linked to the TrustZone® support, are not covered. The detailed list of available features and packages for each product is available in the respective product datasheet.

2.2 System architecture

The STM32U5 series embed high-speed memories (up to 4-Mbyte flash memory and up to 3-Mbyte SRAM), a flexible external memory controller (FSMC) for static memories (available on high-pin-count packages: 100 pins and more), up to two octo-SPI interface (available on all packages), and an extensive range of enhanced I/Os and peripherals connected to a 32-bit multi-AHB bus matrix, three AHB buses and three APB buses.

The following table illustrates the bus matrix differences between STM32L4, STM32L4+, and STM32U5 series.

Table 2. Bus matrix on STM32L4, STM32L4+ and STM32U5 series

Bus type	STM32L4	STM32L4+	STM32U5
AHB bus matrix masters	5 masters: CPU, AHB system, D-Code, I-Code, DMA1 and DMA2(1)	Up to 9 masters: CPU, AHB system, D-Code, I-Code, DMA1 and DMA2, DMA2D, LCD-TFT controller DMA, SDMMC1, SDMMC2, GFXMMU(2)	Up to 11 masters: Fast C-bus, Slow C-bus, CPU S-bus for internal memories, CPU S-bus for external memories, GPDMA1, DMA2D, SDMMC1, SDMMC2, OTG_HS, LTDC, GPU2D M0 and M1 ports, and GFXMMU.
AHB bus matrix slaves	Up to 8 slaves: internal flash memory (on I-Code and D-Code bus), SRAM1, SRAM2, AHB1 (including APB1 and APB2), AHB2, FMC, and QUADSPI.	Up to 11 slaves: internal flash memory (on I-Code and D-Code bus), SRAM1, SRAM2, SRAM3, GFXMMU, AHB1 (including APB1 and APB2), AHB2, OCTOSPI1, OCTOSPI2, and FSMC.	Up to 10 slaves: internal flash memory, SRAM1, SRAM2, SRAM3, AHB1, AHB2, and AHB3 peripherals (including APB1, APB2, and APB3) and backup RAM, AHB2 peripherals, FSMC, OCTOSPI1, OCTOSPI2, SmartRun domain (SRD) peripherals and SRAM4, SRAM5, SRAM6, HSPI1, and GFXMMU.

1. *Up to six masters with DMA2D only for STM32L496/4A6xx.*
2. *SDMMC2 and GFXMMU only available for STM32L4P5/L4Q5xx.*

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

The system architectures of STM32L4, STM32L4+, and STM32U575/585 are shown in the figures below.

Figure 1. STM32L4 series system architecture

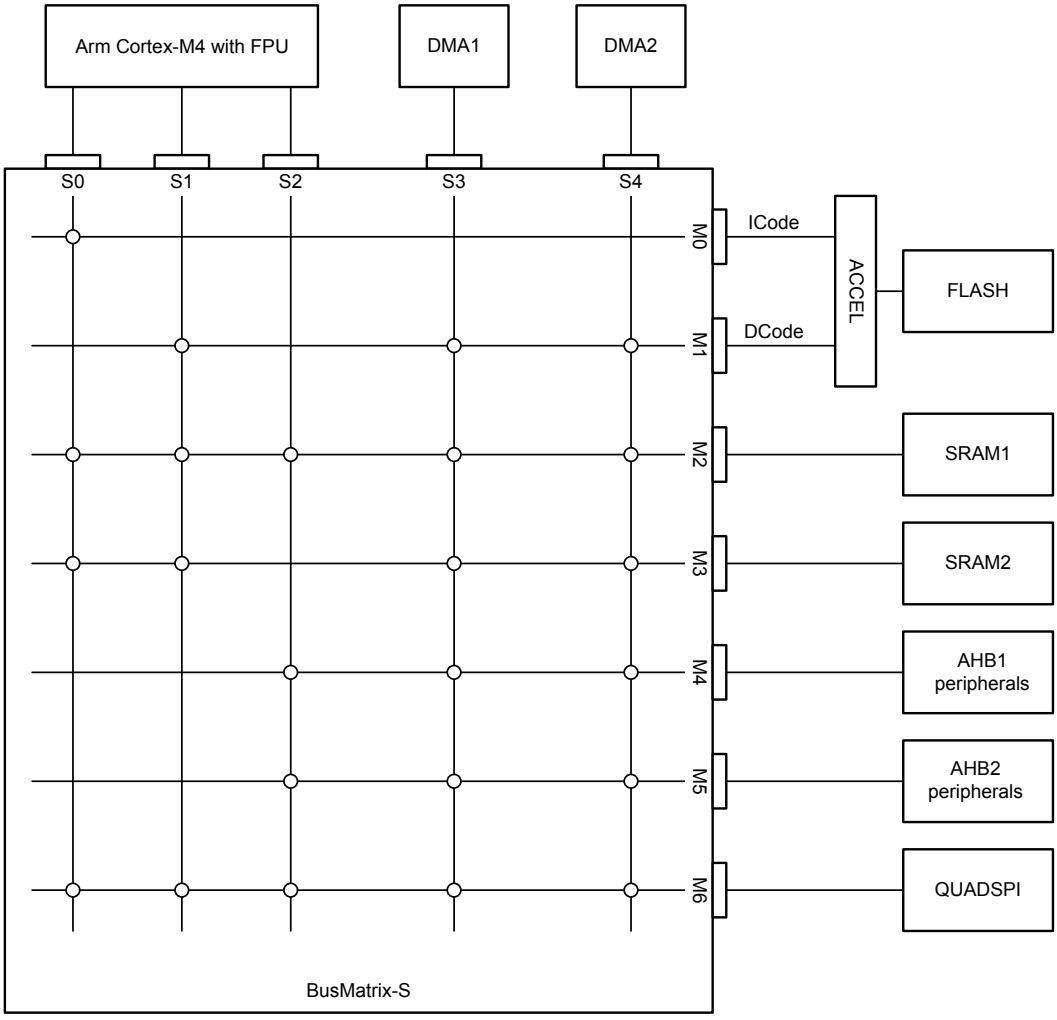


Figure 2. **STM32L4+ series system architecture**

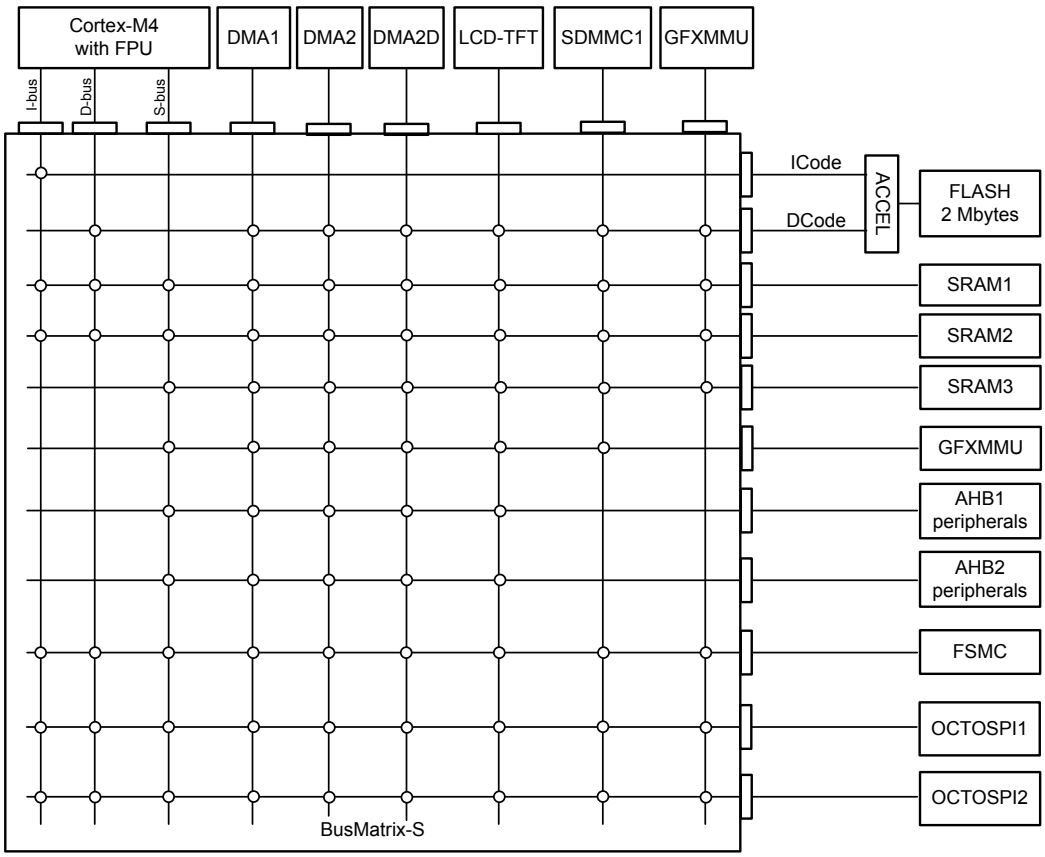
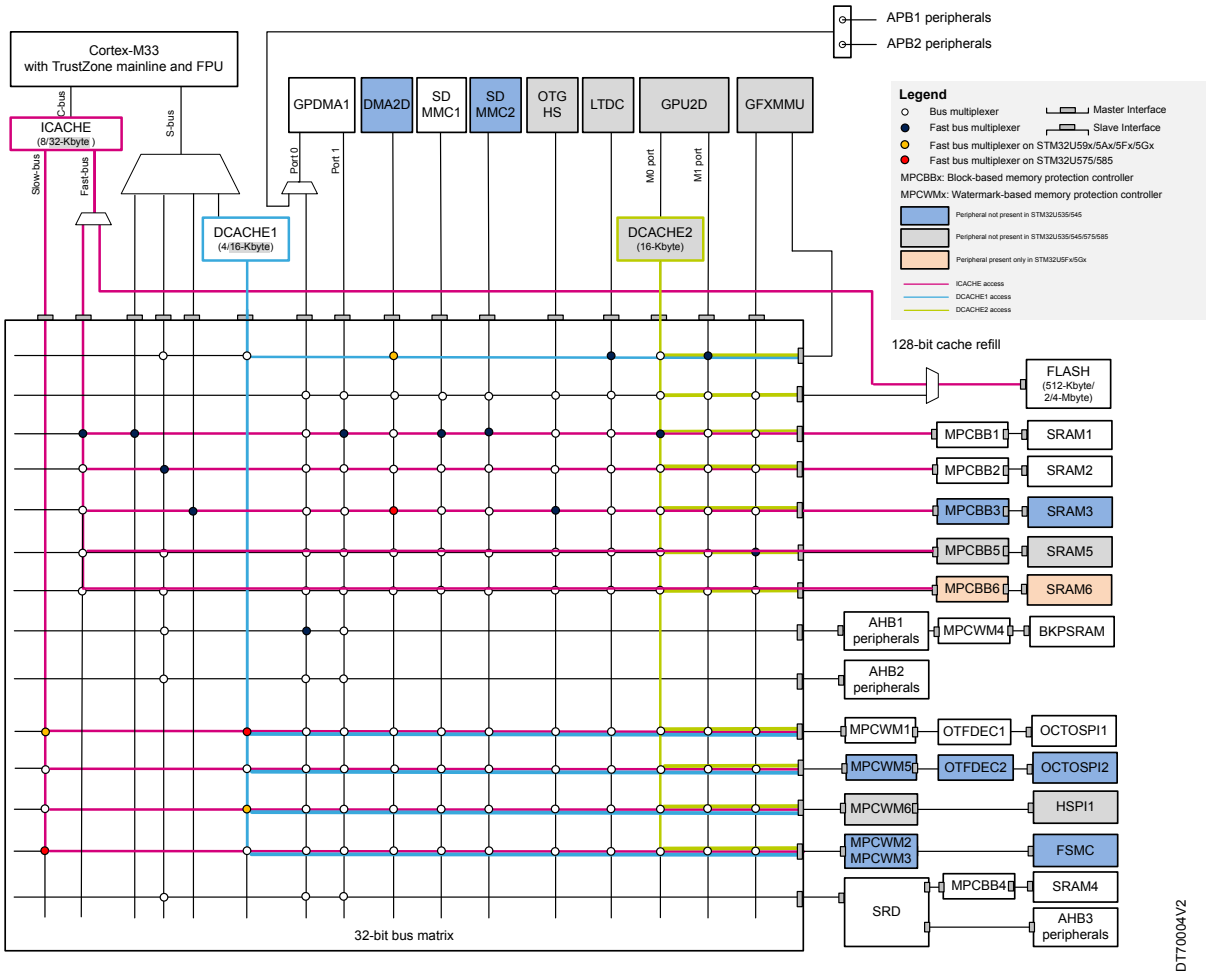


Figure 3. **STM32U5 series system architecture**



2.3 Memory availability

The table below summarizes the memory availability for STM32L4, STM32L4+, and STM32U5 MCUs.

Table 3. **Memory availability for STM32L4, STM32L4+, and STM32U5 MCUs**

Product	Flash memory		RAM size (Kbytes)							Comment
	Size	Bank	SRAM1	SRAM2	SRAM3	SRAM4 (SRD)	SRAM5	SRAM6	BKPSRAM	
STM32U535	512 Kbytes	Dual	192	64	-	16	-	-	2	Without hardware crypto
STM32U545										With hardware crypto
STM32U575	1 to 2 Mbytes				512					Without hardware crypto
STM32U585	2 Mbytes									With hardware crypto

Product	Flash memory		RAM size (Kbytes)							Comment
	Size	Bank	SRAM1	SRAM2	SRAM3	SRAM4 (SRD)	SRAM5	SRAM6	BKPSRAM	
STM32U59x	4 Mbytes	Dual	768	64	832	16	832	-	2	Without hardware crypto
STM32U5Ax										With hardware crypto
STM32U5Fx								512		Without hardware crypto
STM32U5Gx										With hardware crypto
STM32L552xx	Up to 256 Kbytes	Single/ dual	192		-					Without hardware crypto
STM32L562xx	512 Kbytes									With hardware crypto
STM32L41x/42x	128 Kbytes	-	32 Kbytes	8 Kbytes	-					-
STM32L43x/44x	256 Kbytes	-	48 Kbytes	16 Kbytes	-					-
STM32L45x/46x	512 Kbytes	-	128 Kbytes	32 Kbytes	-					-
STM32L47x/48x	1 MB	-	96 Kbytes	32 Kbytes	-					-
STM32L49x/ L4Ax	1 MB	-	256 Kbytes	64 Kbytes	-					-
STM32L4P5x/ L4Q5	1 MB	-	128 Kbytes	64 Kbytes	128 Kbytes	-				-
STM32L4Rx/ L4Sx	2 MB	-	192 Kbytes	64 Kbytes	384 Kbytes	-				-

1. *SmartRun domain*

3 Hardware migration

The STM32U5 MCUs offer eight packages from 48 to 216 pins, and two pinout versions:

- without internal SMPS: most packages are compatible with STM32L4 and STM32L4+ MCUs.
- with internal SMPS: fully new packages that are not compatible with STM32L4 and STM32L4+ MCUs. For this pinout version, the SMPS step-down converter and the LDO are embedded in parallel to provide the V_{CORE} supply.

For more details on the pinout, refer to the product datasheets.

The table below lists the available packages on the STM32U5 MCUs compared to STM32L4 and STM32L4+ MCUs, as well as their compatibility. Only packages common in both series are present. WLCSPxxx and packages not present in the STM32L4 and STM32L4+ MCUs, like TFBGA216, are not listed.

Table 4. Packages on STM32U5 MCUs compared to STM32L4 and STM32L4+ MCUs

Package(1) (Size in mm x mm)	STM32L4		STM32U5		
	STM32L4	STM32L4+	STM32U575/585	STM32U575/585 without SMPS compared to STM32L4/L4+	STM32U575/585 with SMPS compared to STM32L4/L4+
LQFP 144 (20 x 20)	X(2)(3)	X	X	Compatible(4)	New pinout/ballout(5)
LQFP 100 (14 x 14)	X(6)	X	X		
LQFP 64 (10 x 10)	X	N/A	X		
UFBGA169 (7 x 7)	X(7)	X	X	Incompatible	
UFBGA132 (7 x 7)	X(3)	X	X		
LQFP 48 (7 x 7)	X(8)	N/A	X	Compatible(4)	
UFQFPN48 (7 x 7)	X(9)	N/A	X		

1. *For more details about the available packages for STM32L4 and STM32L4+ , refer to product datasheet.*
2. *X = available, N/A = not available*
3. *Available only for STM32L47/48/49/4Axxx.*
4. *Compatible except PB11 pin in STM32L4/L4+ that becomes VCAP on STM32U575/585.*
5. *Eight new packages introduced for STM3U575/585 with SMPS step-down converter option.*
6. *Not available for STM32L41/42xxx.*
7. *Available only for STM32L49/4Axxx.*
8. *Not available for STM32L45/46/47/48/49/4Axxx devices.*
9. *Not available for STM32L47/48/49/4Axxx devices.*

When SMPS is supported, new dedicated pinout supporting the SMPS step-down converter are available for STM32U5 series.

When SMPS is not supported, the STM32U5 series are pin to pin compatible with the STM32L4 and STM32L4+ except:

- UFBGA132 and UFBGA169 packages: incompatible pinouts (refer to the product datasheet for the full pinout tables)
- for other packages, the only incompatibility is in PB11 pin in STM32L4 and STM32L4+, that is replaced by VCAP pin on STM32U5.

Table 5. PB11/VCAP pin position

Package	Only different pin	STM32L4 and STM32L4+	STM32U5
LQFP 144 (20 x 20)	70	PB11	VCAP
LQFP 100 (14 x 14)	48		
LQFP 64 (10 x 10)	30		
LQFP 48 (7 x 7)	22		
UFQFPN48 (7 x 7)	22		

In addition, dedicated pinout featuring the MIPI DSI HOST controller is available on both series. Those are not pin to pin compatible between these series.

4 Boot mode compatibility

4.1 Boot mode selection

For the STM32U5, the BOOT0 input pin may come from the PH3-BOOT0 pin or from an option bit, depending on the value of a user option bit to free the GPIO pad if needed.

The tables below present the STM32U5 boot modes, when TrustZone® is disabled or enabled.

Table 6. Boot modes for STM32U5xx when TrustZone® is disabled (TZEN = 0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000

Table 7. Boot modes for STM32U5xx when TrustZone® is enabled (TZEN = 1)

BOOT _LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot address option-bytes selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000
	-	1	1	0	N/A	RSS: 0x0FF8 0000	
	1	-	0	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000
	0	-	0	0	N/A	RSS: 0x0FF8 0000	
	-	-	-	≠0			
1	-	-	-	-	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000

In STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx, the boot mode is selected with the nBOOT1 option bit and the BOOT0 pin, or nBOOT0 option bit, depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register (see the table below).

Table 8. Boot modes for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx

nBOOT1 FLASH_ OPTR[23]	nBOOT0 FLASH_ OPTR [27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR [26]	Main Flash empty	Boot memory space alias
X	X	0	1	0	Main Flash memory selected as boot area
X	X	0	1	1	System memory selected as boot area
X	1	X	0	X	Main Flash memory selected as boot area
0	X	1	1	X	Embedded SRAM1 selected as boot area
0	0	X	0	X	Embedded SRAM1 selected as boot area
1	X	1	1	X	System memory selected as boot area
1	0	X	0	X	System memory selected as boot area

1. *X = equivalent to 0 or 1.*
2. *For STM32L41/42/43/44/45/46xxx, a Flash memory empty check mechanism is implemented to force the boot from system Flash memory, if the first Flash memory location is not programmed (0xFFFF FFFF), and if the boot selection was configured to boot from the main Flash memory.*

In the other STM32L4 devices (STM32L47/48xxx), the boot mode is selected with one BOOT0 pin and the nBOOT1 option bit located in the user option bytes, at memory address 0x1FFF 7800 (see the table below).

Table 9. Boot modes for STM32L47/48xxx

Selected boot area	BOOT1(1)	BOOT0
Main Flash memory	X(2)	0
System Flash memory	0	1
Embedded SRAM1	1	1

1. *The BOOT1 value is the opposite of the nBOOT1 option bit.*
2. *X = equivalent to 0 or 1.*

4.2 Embedded bootloader

The embedded bootloader is located in the system memory and programmed by STMicroelectronics during production. It allows the flash memory to be reprogrammed, using the serial interfaces listed in the table below.

Table 10. Bootloader interface on STM32L4, STM32L4+, and STM32U5 MCUs

Peripheral	Pin	STM32L4 and STM32L4+	STM32U5
DFU	USB_DM (PA11)	X	X
	USB_DP (PA12)	X	X
USART1	USART1_TX (PA9)	X	X
	USART1_RX (PA10)	X	X
USART2	USART2_TX (PA2)	X	X
	USART2_RX (PA3)	X	X
USART3	USART3_TX (PC10)	X	X
	USART3_RX (PC11)	X	X
I2C1	I2C1_SCL (PB6)	X	X

Peripheral	Pin	STM32L4 and STM32L4+	STM32U5
I2C1	I2C1_SDA (PB7)	X	X
I2C2	I2C2_SCL (PB10)	X	X
	I2C2_SDA (PB11)	X	X
I2C3	I2C3_SCL (PC0)	X	X
	I2C3_SDA (PC1)	X	X
I2C4	I2C4_SCL (PD12)	X(1)	NA
	I2C4_SDA (PD13)	X(1)	NA
SPI1	SPI1_NSS (PA4)	X	X
	SPI1_SCK (PA5)	X	X
	SPI1_MISO (PA6)	X	X
	SPI1_MOSI (PA7)	X	X
SPI2	SPI2_NSS (PB12)	X	X
	SPI2_SCK (PB13)	X	X
	SPI2_MISO (PB14)	X	X
	SPI2_MOSI (PB15)	X	X
SPI3	SPI3_NSS (PG12)	NA	X
	SPI3_SCK (PG9)	NA	X
	SPI3_MISO (PG10)	NA	X
	SPI3_MOSI (PB5)	NA	X
CAN1	CAN1_RX (PB8)	X(2)	X(3)
	CAN1_TX (PB9)	X(2)	X(3)
CAN2	CAN2_RX (PB5)	X(4)	NA
	CAN2_TX (PB6)	X(4)	NA

1. *Only for STM32L45/46/49/4Axxx.*
2. *Not available on STM32L41/42xxx.*
3. *FDCAN1 is available for STM32U5 series.*
4. *Only for STM32L49/4Axxx.*

For more details on the bootloader, refer to the application note *STM32 microcontroller system memory boot mode* (AN2606).

5 Peripheral migration

5.1 STM32 products cross-compatibility

The STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- **Group1**: peripherals by definition common to all products
  Those peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- **Group2**: peripherals shared by all products but with only minor differences. In general, they support new features.
  The migration from one product to another is very easy and does not need any significant new development effort.
- **Group3**: peripherals that have considerable changes from one product to another (new architecture or new features, for example).
  For this group of peripherals, the migration requires a new development at application level.

Each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, DCACHE, or small part of flash memory or SRAM can be configured as trusted or untrusted on the STM32U5 MCUs.

The following table summarizes the available peripherals in the STM32L4, STM32L4+, and STM32U5 MCUs, as well as their compatibility.

Table 11. STM32 peripheral compatibility between STM32L4, STM32L4+ and STM32U5 MCUs

<table>
<tr><th colspan="2" rowspan="2">Peripheral</th><th colspan="2">STM32L4</th><th colspan="4">STM32U5</th></tr>
<tr><th>STM32L4</th><th>STM32L4+</th><th>STM32U535/ 545xx</th><th>STM32U575/ 585xx</th><th>STM32U59/ 5Axxx</th><th>STM32U5F/ 5Gxxx</th></tr>
<tr><td colspan="2">Core</td><td colspan="2">Cortex-M4</td><td colspan="4">Cortex-M33</td></tr>
<tr><td colspan="2">Maximum CPU frequency</td><td>Up to 80 MHz</td><td>120 MHz</td><td colspan="4">160 MHz</td></tr>
<tr><td rowspan="3">Cache</td><td>ICACHE</td><td colspan="2">N/A</td><td colspan="4">1x ICACHE</td></tr>
<tr><td>DCACHE1</td><td colspan="2">N/A</td><td colspan="4">1</td></tr>
<tr><td>DCACHE2</td><td colspan="2">N/A</td><td colspan="2">-</td><td colspan="2">1</td></tr>
<tr><td rowspan="4">PWR/regulators</td><td>Power supply</td><td colspan="6">1.71V to 3.6V</td></tr>
<tr><td>LDO</td><td colspan="6">Available on all products</td></tr>
<tr><td>LDO + internal DC-DC</td><td colspan="2">N/A</td><td colspan="4">STM32U5xxxxQ products
+ DC-DC/LDO on-the-fly selection
Advanced features</td></tr>
<tr><td>LDO + external DC-DC</td><td colspan="2">Possible through VDD12 supply</td><td colspan="4">N/A (no regulator bypass option)</td></tr>
<tr><td rowspan="2">Flash memory</td><td>Size</td><td>1 Mbyte</td><td>2 Mbytes</td><td>512 Kbytes + advanced features</td><td>2 Mbytes + advanced features</td><td colspan="2">4 Mbytes + advanced features</td></tr>
<tr><td>Bank</td><td colspan="2">Dual bank</td><td colspan="4">Dual bank with TrustZone®Specific direct bus to Fast C-Bus</td></tr>
<tr><td rowspan="5">SRAMs</td><td>SRAM1</td><td>Up to 256 Kbytes</td><td>192 Kbytes</td><td colspan="2">192 Kbytes</td><td colspan="2">768 Kbytes</td></tr>
<tr><td>SRAM2</td><td>Up to 64 Kbytes</td><td>64 Kbytes</td><td colspan="4">64 Kbytes with optional ECC</td></tr>
<tr><td>SRAM3</td><td>N/A</td><td>384 Kbytes</td><td>N/A</td><td>512 Kbytes with optional ECC</td><td colspan="2">832 Kbytes with optional ECC</td></tr>
<tr><td>SRAM4</td><td colspan="2">N/A</td><td colspan="4">16 Kbytes in SRD</td></tr>
<tr><td>SRAM5</td><td colspan="2">N/A</td><td colspan="2">N/A</td><td colspan="2">832 Kbytes</td></tr>
</table>

Peripheral		STM32L4		STM32U5			
		STM32L4	STM32L4+	STM32U535/ 545xx	STM32U575/ 585xx	STM32U59/ 5Axxx	STM32U5F/ 5Gxxx
SRAMs	SRAM6	N/A		N/A			512 Kbytes
	Backup SRAM	N/A		BKPSRAM (2Kbytes)			
DMA (not compatible)		DMA request line is connected directly to peripherals.	DMA request line is connected to peripherals through DMAMUX.	GPDMA (16 channels) + **advanced features**			
				LPDMA (4 channels) in SRD			
			DMA2D	N/A	DMA2D: Chrom-ART Accelerator		
PLL		PLL PLL SAI1 PLL SAI2		PLL1 PLL2 PLL3 dedicated PLLs for DSI PHY and USB_HS PHY			
GTZC (global TrustZone® controller)		N/A		3 independent 32-bit AHB interface for TZSC, TZIC, and MPCBB. TZIC accessible only with secure transactions. Secure and non-secure access supported for the privileged and unprivileged part of TZSC. Set of registers to define product security settings. **Privilege mode extended to internal/external memories and internal backup SRAM**			
Anti-tamper detection		Up to 3		Eight tamper input/output pins 128-byte backup registers **+ new advanced features**			
CRC		1x CRC					
FSMC (external memory controller for static memory/ LCD)		1x FSMC(1)					
High-Speed Low-Voltage mode (HSLV)		N/A		Some I/Os have the capability to increase their speed at low voltage by configuring them in HSLV mode			
LPGPIOs		N/A		• **16 I/Os controlled by LPDMA down-to Stop 2 mode** • **LPGPIO designed to be used with GPIO**			
Timers	Advanced control	2 (16-bit)					
	General purpose	5 (16-bit) 2 (32-bit)		4 (32-bit) + 3 (16-bit)			
	Basic	2 (16-bit)					
	Low-power	2 (16-bit)		4 (16-bit) **Autonomous mode**			
	Watchdogs	1x WWDG and 1x IWDG		1x WWDG and 1x IWDG + early interrupt feature			
	RTC	1x RTC **+ binary mode selection**n					
	SysTick	1	1	2			
	GFXTIMER	N/A		Yes			
Communication interfaces	SPI	3(2)		3x SPI **Advanced features**			

Peripheral		STM32L4		STM32U5			
		STM32L4	STM32L4+	STM32U535/ 545xx	STM32U575/ 585xx	STM32U59/ 5Axxx	STM32U5F/ 5Gxxx
Communication interfaces				**Registers not compatible**			
	I²C	3[3]	4	4x I²C + **autonomous mode**		6x I²C +**autonomous mode**	
	USART	USART1/2/3		USART1/3 **+ autonomous mode**	USART1/2/3 **+ autonomous mode**	USART 1/2/3/6 **+ autonomous mode**	
	UART	UART4/5		UART4/5 **+ autonomous mode**			
	LPUART	1x LPUART		1x LPUART + **autonomous mode**			
	SAI (audio interface)	2x SAI		1x SAI	2x SAI1/2		
	FDCAN	1 bxCAN		1x FDCAN			
	USB	OTG_FS without clock recovery [4].	OTG_FS with clock recovery	1x USB full-speed host and device	1x USB **OTG full-speed**	1x USB **OTG high-speed with embedded PHY**	
	UCPD	N/A	N/A	N/A	1x UCPD (USB Type-C® and Power Delivery interface)		
	SDMMC	1x SDMMC [5]		1x SDMMC	**2x** SDMMC		
	Camera interfaces	N/A	1x DCMI and **1x PSSI**				
	OCTOSPI	N/A	2x OCTOSPI + I/O manager multiplexer	1x OCTOSPI	2x OCTOSPI + I/O manager multiplexer		
	OCTOSPIM	N/A	1	N/A	1		
	HSPI	N/A		N/A		1	
Analog peripherals	ADC	12-bit ADC		1x 14-bit ADC1 (2.5 Msps) 1x 12-bit ADC4 (2.5 Msps) **+ new features + autonomous mode**		2x 14-bits ADC1/2 (2.5 Msps) 1x 12-bits ADC4 (2.5 Msps) **+ new features + autonomous mode**	
	DAC	2x 12-bit DAC		2x 12-bit DAC **+autonomous mode**			
	COMP	2x comparators		1x comparator Registers not compatible	2x comparators Registers not compatible		
	OPAMP	2x operational amplifiers [6]		1x operational amplifier **New slew rate configuration**	2x operational amplifiers **New slew rate configuration**		
	Voltage reference buffer	yes		VREFBUF0/1/2/3			
Cryptographic peripherals [7]	AES	1x AES (not available for STM32L476/486xx)					
	SAES (secure AES)	N/A		**1x SAES Advanced features**			
	OTFDEC (on-the-fly decryption)	N/A		1x OTFDEC	2x OTFDEC		

Peripheral		STM32L4		STM32U5			
		STM32L4	STM32L4+	STM32U535/ 545xx	STM32U575/ 585xx	STM32U59/ 5Axxx	STM32U5F/ 5Gxxx
Cryptographic peripherals [7]	PKA (private key accelerator)	N/A	Only available on STM32L4P5/ Q5xx	1x PKA **Advanced features**			
	HASH (SHA-256)	Only available on STM32L496/ 4A6xx	1x HASH	1x HASH			
	RNG (true random number generator)	1x RNG **Transparent usage by SAES and PKA, for DPA resistance**					
Signal-processing coprocessors accelerators	Digital filters	Yes		**1x MDF**[8], multifunction digital filter (six filters) **1x ADF**, audio digital filter (one filter) **Advanced features**			
	GPU2D Neochrom graphic processor	N/A		1[9]			
	JPEG codec	N/A		1[9]			
	CORDIC coprocessor	N/A		1x CORDIC[9]			
	FMAC (filter mathematical accelerator)	N/A		1x FMAC			
	TSC (touch sensing control)	24 channels [10]					
	LTDC (LCD-TFT display controller)	N/A	1	N/A		1	
	DSI	N/A	1	N/A		1	

1. *FSMC is not available on STM32U535/545.*
2. *Only 2 on STM32L41/42xx*
3. *4 on STM32L452/462/496/4A6xx*
4. *Only on STM32L41/42/43/44/45/46xxx*
5. *Not available on STM32L41x/42x/432/442xx.*
6. *Only available on STM32L41/42/43/44/45/46xxx*
7. *These features are available on STM32U545/585/5Ax/5Gx devices, except for RNG and HASH, which are available on all STM32U5 MCUs.*
8. *Only two filters in STM32U535/545 devices*
9. *Not available on STM32U535/545 and STM32U575/585.*
10. *Up to 24 channels for all series except ST32U535/545 devices.*

5.2 Memory mapping

As shown in the table below, the peripheral address mapping has been changed in the STM32U5 MCUs, compared to the STM32L4 and STM32L4+ MCUs. The secure boundary address is not disclosed in this table, as they cannot be compared to the STM32L4/L4+ products. For further information, refer to the product reference manual.

Table 12. Peripheral address mapping of STM32L4, STM32L4+, and STM32U5 MCUs

Peripheral	STM32L4/L4+	STM32U5
	Boundary address(1)	Nonsecure boundary address
HASH	0x5006 0400- 0x5006 07FF	0x420C 0400 - 0x420C 07FF
AES	0x5006 0000- 0x5006 03FF	0x420C 0000 - 0x420C 03FF
DCMI	0x5005 0000- 0x5005 03FF	0x4202 C000 - 0x4202 C3FF
GPIOI	0x4800 2000- 0x4800 23FF	0x4202 8000 - 0x4202 83FF
OCTOSPIM	0x5006 1C00- 0x5006 1FFF	0x420C 4000 - 0x420C 43FF
DMA2D	0x4002 B000- 0x4002 BBFF	0x4002 B000 - 0x4002 BBFF (2)
GFXMMU	0x4002 C000- 0x4002 EFFF (3)	0x4002 C000 - 0x4002 EFFF (4)
DMAMUX1	0x4002 0800- 0x4002 0BFF	N/A
I2C4	0x4000 8400- 0x4000 87FF	0x4000 8400 - 0x4000 87FF
OCTOSPI2	0xA000 1400- 0xA000 17FF	0x420D 2400 - 0x420D 27FF (5)
OCTOSPI1	0xA000 1000- 0xA000 13FF	0x420D 1400 - 0x420D 17FF
FSMC	0xA000 0000- 0xA000 03FF	0x420D 0400 - 0x420D 07FF(5)
DSI	0x4001 6C00- 0x4001 73FF	0x4001 6C00 - 0x4001 7BFF(4)
LTDC	0x4001 6800- 0x4001 6BFF	0x4001 6800 - 0x4001 6BFF(4)
UCPD1	N/A	0x4000 DC00 - 0x4000 DFFF(2)
USB_FS SRAM	0x4000 6C00- 0x4000 6FFF	0x4001 6400 - 0x4001 6BFF(6)
USB_FS	0x4000 6800- 0x4000 6BFF	0x4001 6000 - 0x4001 63FF(6)
OTG_FS	0x5000 0000- 0x5003 FFFF	0x4204 0000 - 0x420B FFFF (7)
SDMMC1	• 0x4001 2800- 0x4001 2BFF (APB2) on STM32L4 • 0x5006 2400- 0x5006 27FF (AHB2) on STM32L4+	0x420C 8000 - 0x420C 83FF
SDMMC2	0x5006 2800- 0x5006 2BFF(3)	0x420C 8C00 - 0x520C 8FFF(2)
OTFDEC1	N/A	0x420C 5000 - 0x420C 53FF
OTFDEC2		0x420C 5400 - 0x420C 57FF(2)
PKA	0x5005 E000- 0x5005 FFFF(3)	0x420C 2000 - 0x420C 3FFF
PSSI	0x5005 0400- 0x5005 07FF(3)	0x4202 C400 - 0x4202 C7FF
RNG	0x5006 0800- 0x5006 0BFF	0x420C 0800 - 0x420C 0BFF
ADC1(8)	0x5004 0000- 0x5004 03FF	0x4202 8000 - 0x4202 83FF
ADC2 (9)		
GPIOJ	N/A	0x4202 2400 - 0x4202 27FF(4)
GPIOI		0x4202 2000 - 0x4202 23FF(4)
GPIOH		0x4202 1C00- 0x4202 1FFF
GPIOG	0x4800 1800- 0x4800 1BFF	0x4202 1800 - 0x4202 1BFF
GPIOF	0x4800 1400- 0x4800 17FF	0x4202 1400 - 0x4202 17FF(2)
GPIOE	0x4800 1000- 0x4800 13FF	0x4202 1000 - 0x4202 13FF
GPIOD	0x4800 0C00- 0x4800 0FFF	0x4202 0C00 - 0x4202 0FFF
GPIOC	0x4800 0800- 0x4800 0BFF	0x4202 0800 - 0x4202 0BFF
GPIOB	0x4800 0400- 0x4800 07FF	0x4202 0400 - 0x4202 07FF
GPIOA	0x4800 0000- 0x4800 03FF	0x4202 0000 - 0x4202 03FF

Peripheral	STM32L4/L4+	STM32U5
	Boundary address(1)	Nonsecure boundary address
GTZC1_ TZSC	N/A	0x4003 2400 - 0x4003 27FF
GTZC1_ TZIC		0x4003 2800 - 0x4003 2BFF
GTZC1_ MPCBB1		0x4003 2C00 - 0x4003 2FFF
GTZC1_ MPCBB2		0x4003 3000 - 0x4003 33FF
GTZC1_ MPCBB3		0x4003 3400 - 0x4003 37FF(2)
TSC	0x4002 4000- 0x4002 43FF	0x4002 4000 - 0x4002 43FF
CRC	0x4002 3000- 0x4002 33FF	0x4002 3000 - 0x4002 33FF
Flash registers	0x4002 2000- 0x4002 23FF	0x4002 2000 - 0x4002 23FF
RCC	0x4002 1000- 0x4002 13FF	0x4602 0C00 - 0x4602 0FFF
DMA1	0x4002 0000- 0x4002 03FF	N/A
DMA2	0x4002 0400- 0x4002 07FF	N/A
GPDMA1	N/A	0X4002 0000 - 0x4002 0FFF
LPDMA1		0x4602 5000 - 0x4602 5FFF
FIREWALL	0x4001 1C00- 0x4001 1FFF	N/A
EXTI	0x4001 0400- 0x4001 07FF	0x4602 2000 - 0x4602 23FF
DFSDM1	0x4001 6000- 0x4001 67FF	N/A
SAI2	0x4001 5800- 0x4001 5BFF	0x4001 5800 - 0x4001 5BFF(2)
SAI1	0x4001 5400- 0x4001 57FF	0x4001 5400 - 0x4001 57FF
TIM17	0x4001 4800- 0x4001 4BFF	0x4001 4800 - 0x4001 4BFF
TIM16	0x4001 4400- 0x4001 47FF	0x4001 4400 - 0x4001 47FF
TIM15	0x4001 4000- 0x4001 43FF	0x4001 4000 - 0x4001 43FF
USART1	0x4001 3800- 0x4001 3BFF	0x4001 3800 - 0x4001 3BFF
TIM8	0x4001 3400- 0x4001 37FF	0x4001 3400 - 0x4001 37FF
SPI1	0x4001 3000 - 0x4001 33FF	0x4001 3000 - 0x4001 33FF
TIM1	0x4001 2C00- 0x4001 2FFF	0x4001 2C00 - 0x4001 2FFF
COMP	0x4001 0200- 0x4001 03FF	0x4600 5400 - 0x4600 57FF
VREFBUF	0x4001 0030- 0x4001 01FF	0x4600 7400 - 0x4600 77FF
SYSCFG	0x4001 0000 - 0x4001 002F	0x4600 0400 - 0x4600 07FF
FDCAN1 RAM	N/A	0x4000 AC00 - 0x4000 AFFF
LPTIM3		0x4600 4800 - 0x4600 4BFF
CAN1/FDCAN1(11)	0x4000 6400- 0x4000 67FF	0x4000 A400 - 0x4000 A7FF
LPTIM2	0x4000 9400- 0x4000 97FF	0x4000 9400 - 0x4000 97FF
LPUART1	0x4000 8000- 0x4000 83FF	0x4600 2400 - 0x4600 27FF
LPTIM1	0x4000 7C00- 0x4000 7FFF	0x4600 4400 - 0x4600 47FF
OPAMP	0x4000 7800- 0x4000 7BFF	0x4600 5000 - 0x4600 53FF
DAC(12)	0x4000 7400- 0x4000 77FF	0x4602 1800 - 0x4602 1BFF
PWR	0x4000 7000- 0x4000 73FF	0x4602 0800 - 0x4602 0BFF
CRS	0x4000 6000- 0x4000 63FF	0x4000 6000 - 0x4000 63FF
I2C3	0x4000 5C00- 0x4000 5FFF	0x4600 2800 - 0x4600 2BFF

Peripheral	STM32L4/L4+	STM32U5
	Boundary address(1)	Nonsecure boundary address
I2C2	0x4000 5800- 0x4000 5BFF	0x4000 5800 - 0x4000 5BFF
I2C1	0x4000 5400- 0x4000 57FF	0x4000 5400 - 0x4000 57FF
UART5	0x4000 5000- 0x4000 53FF	0x4000 5000 - 0x4000 53FF
UART4	0x4000 4C00- 0x4000 4FFF	0x4000 4C00 - 0x4000 4FFF
USART3	0x4000 4800- 0x4000 4BFF	0x4000 4800 - 0x4000 4BFF
USART2	0x4000 4400- 0x4000 47FF	0x4000 4400 - 0x4000 47FF(4)
SPI3	0x4000 3C00- 0x4000 3FFF	0x4600 2000 - 0x4600 23FF
SPI2	0x4000 3800- 0x4000 3BFF	0x4000 3800 - 0x4000 3BFF
TAMPER and BKP registers(13)	0x4000 3400- 0x4000 37FF(14)	0x4600 7C00 - 0x4600 7FFF
IWDG	0x4000 3000- 0x4000 33FF	0x4000 3000 - 0x4000 33FF
WWDG	0x4000 2C00- 0x4000 2FFF	0x4000 2C00 - 0x4000 2FFF
RTC	0x4000 2800- 0x4000 2BFF	0x4600 7800 - 0x4600 7BFF
TIM7	0x4000 1400- 0x4000 17FF	0x4000 1400 - 0x4000 17FF
TIM6	0x4000 1000- 0x4000 13FF	0x4000 1000 - 0x4000 13FF
TIM5	0x4000 0C00- 0x4000 0FFF	0x4000 0C00 - 0x4000 0FFF
TIM4	0x4000 0800- 0x4000 0BFF	0x4000 0800 - 0x4000 0BFF
TIM3	0x4000 0400- 0x4000 07FF	0x4000 0400 - 0x4000 07FF
TIM2	0x4000 0000- 0x4000 03FF	0x4000 0000 - 0x4000 03FF
ADF1	N/A	0x4602 4000 - 0x4602 4FFF
LPGPIO1		0x4602 0000 - 0x4602 03FF
LPTIM4		0x4600 4C00 - 0x4600 4FFF
DLYBOS1		0x420C F400 - 0x420C F3FF
DLYBOS2		0x420C F400 - 0x420C F7FF
DLYBSD1		0x420C 8400 - 0x420C 87FF
DLYBSD2		0x420C 8800 - 0x420C 8BFF
SAES		0x420C 0C00 - 0x420C 0FFF
BKPSRAM		0x4003 6400 - 0x4003 6BFF
DCACHE1		0x4003 1400 - 0x4003 17FF
DCACHE2		0x4003 1800 - 0x4003 1BFF(4)
ICACHE		0x4003 0400 - 0x4003 07FF
RAMCFG		0x4002 6000 -0x4002 6FFF
MDF1		0x4002 5000 - 0x4002 5FFF
FMAC		0X4002 1400 - 0x4002 17FF
CORDIC		0X4002 1400 - 0x4002 13FF
GTZC2_ MPCBB4		0x4602 3800 - 0x4602 3BFF
GTZC2_ TZIC		0x4602 3400 - 0x4602 37FF
GTZC2_ TZSC		0x4602 3000 - 0x4602 33FF
LPGPIO1		0x4602 0000 - 0x4602 03FF

Peripheral	STM32L4/L4+	STM32U5
	Boundary address(1)	Nonsecure boundary address
HSPI1	N/A	0x420D 3400 - 0x420D 37FF
PKA		0x420C 2000 - 0x420C 3FFF
OTG_HS		0x4204 0000 - 0x4205 FFFF(4)
GTZC1_ MPCBB6		0x4003 3C00 - 0x4003 3FFF
GTZC1_ MPCBB5		0x4003 3800 - 0x4003 3BFF
GTZC1_ MPCBB3		0x4003 3400 - 0x4003 37FF
GTZC1_ MPCBB2		0x4003 3000 - 0x4003 33FF
GTZC1_ MPCBB1		0x4003 2C00 - 0x4003 2FFF
GTZC1_ TZIC		0x4003 2800 - 0x4003 2BFF
GTZC1_ TZSC		0x4003 2400 - 0x4003 27FF
GPU2D		0x4002 F000 - 0x4002 FFFF(4)
JPEG		0x4002 A000 - 0x4002 AFFF(4)
GFXTIM		0x4001 6400 - 0x4001 67FF(4)
UCPD1		0x4000 DC00 - 0x4000 DFFF(2)

1. *If no boundary address, it means the peripheral is not available on all STM32L4/L4+.*
2. *Not available on STM32U535/545*
3. *Only available on STM32L4P5/4Q5xx.*
4. *Not available on STM32U535/545 and STM32U575/585*
5. *Not available on STM32U535/545*
6. *Not available for STM32U575/585, STM32U59x/5Ax, and STM32U5Fx/5Gx*
7. *Only available on STM32U575/585*
8. *ADC1 for STM32U575/585. ADC1 and ADC2 for STM32L4P/4Q5xx.*
9. *Named ADC4 for STM32U575/585.*
10. *Only one COMP on STM32U535/545*
11. *FDCAN1 for STM32U575/585.*
12. *DAC1 for STM32L4+ and STM32U575/585.*
13. *TAMP for STM32U575/585.*
14. *Only on STM32L4+.*
15. *GPU2D supports HW vector graphic only in STM32U5Fx/5Gx*

6 Migration of system peripherals

6.1 System configuration controller (SYSCFG)

Table 13. SYSCFG features in STM32L4, STM32L4+ and STM32U5 MCUs

STM32L4/L4+	STM32U5
• Remapping memory areas • Managing the external interrupt line connection to the GPIOs • Managing robustness feature • Setting SRAM2 write protection and software erase • Configuring FPU interrupts • Enabling the firewall • Enabling/disabling the I2C Fast-mode plus driving capability on some I/Os	• Managing robustness feature • Setting SRAM write protection and software erase: this feature is not ensured by SYSCFG peripheral but using RAMCFG peripheral. • Configuring FPU interrupts • Enabling/disabling the I2C fast-mode plus driving capability on some I/Os and voltage booster for I/Os analog switches • Configuring TrustZone security register access • Tracking the PVT conditions to control the current slew-rate and output impedance in I/O buffer through compensations cells on VDD, VDDIO2 and HSPI GPIOs. • Configuring the OTG_HS PHY • Adjust the HSPI supply capacitance • Disable internal SRAMs cacheability by DCACHE2

6.2 Embedded flash memory (FLASH)

Table 14. Flash memory features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4/L4+	STM32U5
Page size	• 0x0800 0000 to up to 0x080F FFFF • 0x0810 0000 to up to 0x081F FFFF (only for STM32L4+)	• Bank1: 0x0800 0000 to 0x081F FFFF • Bank2: 0x0810 0000 to 0x083F FFFF
Main/program memory	For **STM32L4+**: • up to 2 Mbytes • split in two banks • when dual bank is enabled: – each bank = 256 pages of 4 Kbytes – each page = 8 rows of 512 bytes • when dual bank is disabled: – memory block contains 256 pages of 8 Kbytes – each page = 8 rows of 1024 bytes For **STM32L47/48/49/4Axxx**: • up to 1 Mbyte • split in two banks: – each bank = 256 pages of 2 Kbytes – each page = 8 rows of 256 bytes For **STM32L45/46xxx**: • up to 512 Kbytes • one bank – each bank = 256 pages of 2 Kbytes – each page = 8 rows of 256 bytes For **STM32L43/44xxx**: • up to 256 Kbytes • one bank – each bank = 128 pages of 2 Kbytes – each page = 8 rows of 256 bytes	For **STM32U535/545**: • up to 512 Mbytes: – dual-bank architecture – 256 Kbyte per bank for main memory – 8 Kbytes page size • system memory: 32 Kbytes • 32 Kbytes immutable secure area containing the root security services For **STM32U575/585**: • up to 2 Mbytes: – dual-bank architecture – 1 Mbyte per bank for main memory – 8 Kbytes page size • system memory: 32 Kbytes • 32 Kbytes immutable secure area containing the root security services For **STM32U59x/5Ax/5Fx/5Gx**: • up to 4 Mbytes: – dual-bank architecture – 2 Mbyte per bank for main memory – 8 Kbytes page size • system memory: 32 Kbytes • 32 Kbytes immutable secure area containing the root security services

Feature		STM32L4/L4+	STM32U5
		For **STM32L41/42xxx**: • up to 128 Kbytes • one bank = 64 pages of 2 Kbytes	
Specific features		• RWW (read-while-write) • dual-bank boot (only for STM32L4+ and STM32L47/48/49/4Axxx)	• RWW (read-while-write) • dual-bank boot
ECC (single-error correction and double-error detection)		Programming and read granularity: 72 bits (including 8 ECC bits)	128 effective bits plus 9 ECC bits
Read access		Read access of 64 bits	128-bit wide data read
Wait states (WS)		Up to 4 WS (depending on the supply voltage and the frequency)	The number of WS depends on LPM value: • Up to 4 WS when LPM = 0 (depending on the supply voltage and the frequency) • Up to 16 WS when LPM = 1 (depending on the supply voltage and the frequency)
One time programmable (OTP)		1-Kbyte OTP bytes (bank1)	512-byte OTP for user data
Read protection (RDP)	Level 0 (RDP = 0xAA)	No protection: No debug restriction	Device open • No debug restriction (secure and nonsecure) • Boot @ must target a secure area. • Boot on secure SRAM, flash memory and system flash memory (RSS) possible
	Level 0.5 (RDP = 0x55)	N/A	Device partially closed (only when TrustZone® is enabled) • Nonsecure debug only • NS-Flash access allowed (with debug connection) • Boot @ must target secure user flash memory. • Boot on SRAM not permitted • Regression from Level 1 to level 0.5 can be blocked by OEM2 key.
	Level 1 (RDP ≠ {0xAA, 0xCC})	Memory readout protection	Device memories protected: Flash, backup registers, SRAM2, and backup RAM totally inaccessible: • Nonsecure debug only • Flash access not allowed (with debug connection) • Boot @ must target secure user flash memory. • Regression from Level 1 to level 0 can be blocked by OEM1 key.
	Level 2 (RDP = 0xCC)	Full protection: No debug(1)	• Closed device (no JTAG) • No option byte change: – No debug (JTAG fuse) – Boot @ in secure user flash memory • RDP level 2 cannot be changed, unless OEM2 unlocking key is activated.
Write protection (WRP)		Two write protection area per bank: 2-Kbyte granularity For **STM32L4+** MCUs: dual bank with 2 areas per bank or single bank with 4 areas	Two write protection area per bank: 8-Kbyte granularity
User option bytes	RDP option bytes	• 0xAA: Level 0 • 0xCC: Level 2 • Others: Level 1	• 0xAA: Level 0 • 0x55: Level 0.5 • 0xCC: Level 2 • Others: Level 1

Feature		STM32L4/L4+	STM32U5
User option bytes	Reset option bytes	• BOR_LEV[2:0] • nRST_STOP • nRST_STDBY • nRST_SHDW • SRAM_RST (only on STM32U5 series) • SRAM2_RST	
	Watchdog option bytes	• IDWG_SW • IWDG_STOP • IWDG_STDBY • WWDG_SW	
	FLASH banking option bytes	BFB2 (except for STM32L41/42/43/44/45/46xxx)	SWAP_BANK
		• Dual bank (except for STM32L4+ and STM32L41/42/43/44/45/46xxx MCUs) • DB1M (for STM32L4+ MCUs) • DBANK (for STM32L4+ MCUs)	DUALBANK
	RAM and ECC enable option bits	N/A (parity check option bit only)	• BKPRAM_ECC • SRAM3_ECC • SRAM2_ECC
		SRAM2_PE	Removed, replaced by ECC options bits
	Secure and nonsecure boot option bytes	nSWBOOT0 (only for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx)	nSWBOOT0
		nBOOT0 (only for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx)	nBOOT0
		N/A	• NSBOOTADD0[24:0] • NSBOOTADD1[24:0] • SECBOOTADD0[24:0]
	IO speed and pull-up selection option bits		• PA15_PUPEN • IO_VDD_HSLV • IO_VDDIO2_HSLV
	Global TrustZone® activation option bit		TZEN
	FLASH secure watermark option bytes	For **STM32L4** MCUs: • PCROPx_STRT[15:0] • PCROPx_END[15:0] For **STM32L4+** MCUs: • PCROPx_STRT[16:0] • PCROPx_END[16:0]	• SECWM1_PSTRT[6:0] • ECWM1_PEND[6:0] • HDP1_PEND[6:0] • HDP1EN • SECWM2_PSTRT[6:0] • SECWM2_PEND[6:0] • HDP2_PEND[6:0] • HDP2EN
	FLASH write protection (WRP) area option bytes	N/A	• WRP1A_PSTRT[6:0] • WRP1A_PEND[6:0] • WRP1B_PSTRT[6:0] • WRP1B_PEND[6:0] • WRP2A_PSTRT[6:0] • WRP2A_PEND[6:0] • WRP2B_PSTRT[6:0] • WRP2B_PEND[6:0] • UNLOCK
	FLASH locking keys for level regression option bytes		• OEM1KEY[31:0] • OEM1KEY[63:32] • OEM2KEY[31:0] • OEM2KEY[63:32]
Protections		• Write protection: 2 areas per bank	• 4 write protection areas: 2 per bank • Configurable protection against unprivileged accesses with Flash page granularity

Feature	STM32L4/L4+	STM32U5
	• PCROP protection: one PCROP area per bank	
Security	N/A	• TrustZone® • 2 secure areas (1 per bank) • 2 secure HDP (hide protection) areas part of the secure areas (1 per bank)

1. *Memory read protection Level 2 is an irreversible operation. When Level 2 is activated, the level of protection cannot be decreased to Level 0 or Level 1.*

6.3 SRAMs

In STM32L4 and STM32L4+ MCUs, the control of SRAM1 and SRAM2 is integrated within the SYSCFG.

In STM32U5 MCUs, the new peripheral RAMCFG controller is dedicated to control SRAM1, SRAM2, SRAM3, SRAM4, and BKPSRAM.

Refer to section 'RAMs configuration controller' in the product reference manual for more details.

Table 15. SRAM features in STM32L4, STM32L4+ and STM32U575/585 MCUs

Feature	STM32L4		STM32U5			
	STM32L4	STM32L4+	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
Size	• 196 Kbytes for STM32L41/42/43/44/45/46xxx devices: – SRAM 1 = up to 128 Kbytes – SRAM 2 = up to 32 Kbytes • 128 Kbytes for STM32L4x1/47x/48xxx devices: – SRAM 1 = up to 128 Kbytes – SRAM 2 = up to 32 Kbytes	• 640 Kbytes for STM32L4R/4Sxxx devices: – SRAM 1 = 192 Kbytes – SRAM 2 = 64 Kbytes – SRAM 3 = 384 Kbytes • 320 Kbytes for STM32L4P5/Q5xx devices: – SRAM 1 = 128 Kbytes – SRAM 2 = 64 Kbytes – SRAM 3 = 128 Kbytes	274: SRAM1 = 192 SRAM2 = 64 SRAM4 = 16 BKPSRAM = 2	786: SRAM1 = 192 SRAM2 = 64 SRAM3 = 512 SRAM4 = 16 BKPSRAM = 2	2514: SRAM1 = 768 SRAM2 = 64 SRAM3 = 832 SRAM4 = 16 SRAM5 = 832 BKPSRAM = 2	3026: SRAM1 = 768 SRAM2 = 64 SRAM3 = 832 SRAM4 = 16 SRAM5 = 832 SRAM6 = 512 BKPSRAM = 2

Feature		STM32L4		STM32U5			
		STM32L4	STM32L4+	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
		• 320 Kbytes for STM32L49/4Axxx devices: – SRAM 1 = 256 Kbytes – SRAM 2 = 64 Kbytes					
Access by DMA and CPU		Bytes, half-words (16 bits) or full words (32 bits) possible access					
CPU access bus	System bus	SRAM1	SRAM1, SRAM2, SRAM3	SRAM1, SRAM2, SRAM4, and BKPSRAM	SRAM1, SRAM2, SRAM3, SRAM4 and BKPSRAM	SRAM1, SRAM2, SRAM3, SRAM4, SRAM5 and BKPSRAM	SRAM1, SRAM2, SRAM3, SRAM4, SRAM5, SRAM6 and BKPSRAM
	Other bus access	SRAM1, SRAM2 (I-bus/D-bus)		SRAM1 and SRAM2	SRAM1, SRAM2 and SRAM3	SRAM1, SRAM2, SRAM3 and SRAM5	SRAM1, SRAM2, SRAM3, SRAM5 and SRAM6
Retention		SRAM1, SRAM2, and all registers content are retained in Stop 0, Stop 1 and Stop 2 modes.		Either 8, 56, or 64 Kbytes of SRAM2 can be retained in Standby mode.			
		N/A		BKPSRAM • Retention in Standby mode • Optional retention in V_{BAT} mode			
Security		N/A		When the TrustZone security is enabled, all SRAMs are secure after reset. The SRAMs can be programmed as nonsecure using the MPCBB with a block granularity of 512 bytes.			
Hardware erase conditions		N/A		All SRAMs are erased by hardware in case of RDP level regression to L0.5 or L0. SRAM2 and optionally BKPSRAM are protected by the tamper detection circuit and are erased by hardware in case of tamper detection. SRAM2 and BKPSRAM are erased by hardware in case of Backup domain reset.			
Software erase conditions		The SRAM2 erase can also be requested by software by setting SRAM2ER in SYSCFG_SCSR.		All SRAMs erase can be requested by executing a specific software sequence, detailed in section ‘RAMCFG’ of the product reference manuals.			
System reset erase		The SRAM2 can be erased with a system reset using the option bit SRAM2_RST in the flash memory user option bytes.					
		N/A		SRAM1, SRAM3, SRAM4 and SRAM5 are erased when a system reset occurs if SRAM_RST option is selected in flash memory user option bytes.			
WRP		SRAM2 can be write-protected with a page granularity of 1 Kbyte.					
		The write protection can be enabled in SYSCFG SRAM2 write protection register (SYSCFG_SWPR).		Each 1-Kbyte page can be write-protected by setting its corresponding PxWP (x = to 63) bit in RAMCFG registers.			
Error detection and correction		Single-error correction and double-error detection					
		Parity check: 4 bits added per 32 bits (1 bit per byte)		ECC: 7 bits added per 32 bits			
		Parity checks supported by the SRAM2 only		ECC supported by SRAM2, SRAM3 and BKPSRAM			

Feature	STM32L4		STM32U5			
	STM32L4	STM32L4+	STM32U535/545	STM32U575/585	STM32U59x/5Ax	STM32U5Fx/5Gx
Error detection and correction	If one parity bit fails, an NMI is generated. Event can be linked to the BRK_IN break input of TIM1, TIM8, TIM15, TIM16, or TIM17.		Interrupts are generated when single and/or double ECC errors are detected: • 2 ECC RAMCFG interrupts • 1 ECC NMI interrupt • Interrupts allow the device to exit Sleep, Stop 0 or Stop 1 mode, but not Standby mode.			
Read access latency	N/A		3-bit programmable wait-states depending on AHB clock frequency (HCLK) and voltage scaling range (for all SRAMs).			

6.4 Instruction and data caches (ICACHE/DCACHE)

The STM32U5 MCUs embed an ICACHE and DCACHEs (DCACHE1 and DCACHE2) that allows more efficient use of the external memory through the OCTOSPI and FSMC ports.

The STM32L4 and STM32L4+ MCUs do not embed these caches.

Table 16. Embedded caches on STM32U5 devices

Feature		STM32L4 and STM32L4+	STM32U5		
			STM32U535/545	STM32U575/585	STM32U59x/5Ax/5Fx/5Gx
CACHEs (Kbytes)	ICACHE	N/A	8		32
	DCACHE1		4		16
	DCACHE2		N/A		

6.5 Direct memory access controller (DMA)

The STM32L4, STM32L4+ and STM32U5 MCUs have different DMA architecture and features.

All devices embed two DMA controllers:

- DMA1 (7 channels) and DMA2 (7 channels) for STM32L4 and STM32L4+ MCUs
- GPDMA1 (16 channels) and LPDMA1 (4 channels) for STM32U5 MCUs

STM32U5 and STM32L4+ embed also a Chrom-ART Accelerator (DMA2D) that is a specialized DMA dedicated to image manipulation. DMA2D peripheral is not present in STM32L4.

The following table illustrates the main differences between DMA requests in STM32L4, STM32L4+ and STM32U5 MCUs.

Table 17. DMA features of STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4/L4+		STM32U5	
	DMA1	DMA2	GPDMA1	LPDMA1
Architecture	Each instance of DMA controllers can access memory and peripherals.			
Number of instances	1	1	1	1
Number of masters	1 single bidirectional AHB master per instance		Dual bidirectional AHB master	Single bidirectional AHB master
Number of channels	7	7	16	4
Linked-List	N/A		• Separately programmed source and destination transfers • Programmable data handling between source and destination • Block-level (programmable number of data bytes) • Linear source and destination addressing: programmable signed address offsets between successive burst transfers	
Linked-List 2D addressing	N/A		• 2D source and destination addressing	N/A

Feature	STM32L4/L4+		STM32U5	
	DMA1	DMA2	GPDMA1	LPDMA1
			• Scatter-gather (multi-buffer transfers), data interleaving and de-interleaving via 2D addressing	
Autonomous data transfer in Sleep and Stop modes	N/A		Autonomous data transfers and wakeup during Sleep and Stop low power modes	
	N/A		Sleep, Stop 0 and Stop 1 modes	Sleep, Stop 0, Stop 1 and Stop 2 modes
TrustZone security	N/A		Yes	
Privileged/unprivileged DMA	N/A		Yes	

6.6 Reset and clock control (RCC)

The STM32U5 MCUs implement the same RCC features as the STM32L4 and STM32L4+ MCUs, with some specification updates.

Table 18. RCC features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4/L4+	STM32U5
MSI	• MSI is a low-power oscillator with programmable frequency up to 48 MHz. • It can replace PPLs as system clock (faster wake-up, lower consumption). • It can be used as USB device clock (no need for an external high speed crystal oscillator). • 12 frequency ranges are available: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz, and 48 MHz. • Auto-calibration from LSE	• MSI is made of four internal RC oscillators. Two output clocks are generated from these divided oscillators: MSIS and MSIK. • MSIS can replace PPLs as system clock (faster wake-up, lower consumption). • MSIK can be selected by some peripherals as kernel clock. • MSI can be used as USB device clock (no need for external high-speed crystal oscillator). • 16 frequency ranges are available (from 100 kHz to 48 MHz). Refer to “MSIS and MSIK ranges per internal MSIRCs” table on the reference manual for more information. • Default value for MSIS and MSIK frequencies is 4 MHz. • Auto-calibration from LSE
HSI16	16 MHz RC factory and user trimmed	
LSI	• 32 kHz RC • Lower consumption, higher accuracy (refer to the electrical characteristics section of the datasheet) • On STM32U5 MCUs, the LSI is available under Backup Domain (VBAT).	
HSE	4 to 48 MHz	4 to 50 MHz
LSE	• 32.768 kHz • Configurable drive/consumption • Available in Backup domain (VBAT)	
HSI48	• 48 MHz RC (only for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx) • Can drive USB FS, SDMMC, and RNG	• 48 MHz RC • Can drive USB FS, SDMMC, and RNG
SHSI	N/A	Internal securable RC oscillator dedicated to clock the SAES
PLL	• Main PLL for system: – x2 PLLs for SAI1/2, ADC, RNG, SDMMC and OTG_FS clock (for STM32L4+ and STM32L47/48/49/4Axxx) – x1 PLL for SAI1, ADC, RNG, SDMMC, USB FS clock (for STM32L43/44/45/46xxx)	• Three PLLs: – Main PLL(PLL1) provides clock for CPU and some peripherals. – PLL2 and PLL3 generate the kernel clocks for peripherals. • Each PLL offers three independent outputs with post-dividers.

Feature	STM32L4/L4+	STM32U5
	• Each PLL provides up to three independent outputs. • The PLL sources are MSI, HSI16, HSE.	• The internal PLLs can be used to multiply the HSI16, HSE, or MSIS output clock frequency. • Capability to work in integer or fractional mode
System clock frequency	• Up to 80 MHz (or 120 for STM32L4+) • 4 MHz after reset using MSI	• Maximum frequency is 160 MHz. • 4 MHz after reset using MSI
AHB, APB1, APB2 frequency	Up to 80 MHz (or 120 for STM32L4+)	Up to 160 MHz
RTC clock source	LSI, LSE or HSE/32	
MCO clock source	• MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, • LSI or HSI48 (for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx) • With configurable prescaler 1, 2, 4, 8 or 16 for each output	One of nine clock signals can be selected as MCO clock: LSI, LSE, SYSCLK, HSI16, HSI48, HSE, PLLCLK, MSIS, or MSIK.
Clock security system (CSS)	CSS on HSE or CSS on LSE	
Internal oscillator measurement/calibration	• LSE connected to TIM15 or TIM16 CH1: can measure HSI16 or MSI with respect to LSE clock high precision. • LSI connected to TIM16 CH1: can measure LSI with respect to HSI16 or HSE clock precision. • HSE/32 connected to TIM17 CH1: can measure HSE with respect to LSE/HSI16 clock. • MSI connected to TIM17 CH1: can measure MSI with respect to HSI16/HSE clock. • On STM32L41/42/43/44/45/46xxx, the HSE/32 and MSI are connected to TIM16 CH1.	• The frequency of all on-board clock sources can be indirectly measured by means of the TIM15, TIM16, or TIM17 channel 1 input capture and LPTIM1 or LPTIM2 channel 2 input capture. • Calibration using LSE: HSI16 and MSI calibration using LSE and TIM15/TIM16/TIM17 and LPTIM2. • Calibration using HSE: – HSI16 and MSI calibration using HSE, TIM16/TIM17 and LPTIM2 – LSI calibration using HSE, TIM16/TIM17 and LPTIM1
Interrupt	• CSS (linked to NMI IRQ) • LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, PLLSAI1RDY, PLLSAI2RDY (only on STM32L4+ and STM32L47/48/49/4Axxx) (linked to RCC global IRQ)	• CSS (linked to NMI IRQ for HSE and Tamper for LSE) • HSECSS, HSERDY, LSERDY, HSIRDY, SHSIRDY, HSI48RDY, LSIRDY, MSISRDY, MSIKRDY, PLL1RDY, PLL2RDY, PLL3RDY, ITAMP3
Autonomous mode	N/A	• Peripherals supporting autonomous mode are able to generate a kernel clock and AHB/APB bus clock requests when needed even in Stop mode. • Either MSI or HSI16 are woken up for this purpose.

6.6.1 Performance versus VCORE ranges

In the STM32U5 series, the maximum CPU clock frequency and the number of flash memory wait states depend on the selected voltage range V_{CORE}. The tables below present the different clock source frequencies depending on different product voltage range for STM32L4, STM32L4+ and STM32U5 series.

Table 19. RCC registers of STM32L4 and STM32L4+ series

CPU performance	Power performance (1)	V_{CORE} range	Typical value (V)	Max frequency (MHz)(2)					
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS
STM32L4 series									
High	Medium	1	1.2	-	80	64	48	32	16
Medium	High	2	1.0	-	26	26	18	12	6
STM32L4+ series									
High	Medium	1 (boost mode)	1.28	120	100	80	60	40	20
		1 (normal mode)	1.2	-	-	80	60	40	20
Medium	High	2	1.0	-	-	-	26	16	8

1. *When power performance increases, power consumption per MHz decreases.*
2. *WS = wait states.*

Table 20. RCC registers of STM32U5 series

CPU performance	Power performance	V_{CORE} range	Typical value (V)	Max frequency (MHz)											
				LPM = 0						LPM = 1					
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS	5 WS	4 WS	3 WS	2 WS	1 WS	0 WS
High	Low	1	1.2	-	160	128	96	64	32	Up to 16 WS may be needed to obtain max clock source when LPM = 1 for ranges 1,2 and 3. For more information, refer to FLASH section, table "Number of wait states according to CPU clock (HCLK) frequency (LPM = 1)" in the reference manual.					
Medium-high	Medium-low	2	1.1	-	-	110	75	50	25						
Medium-low	Medium-high	3	1.0	-	-	55	37.5	25	12.5						
Low	High	4	0.9	-	-	-	24	16	8	-	-	-	24	16	8

6.6.2 Peripheral access configuration

Since the address mapping of some peripherals has been changed in the STM32U5 MCUs, compared to STM32L4 and STM32L4+ MCUs, different registers must be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from Reset mode]. In addition, the STM32U5 MCUs need to [enable/disable] the autonomous mode for SmartRun domain (SRD). The table below shows the RCC registers used for peripheral access configuration in STM32L4, STM32L4+ and STM32U5 MCUs.

Table 21. RCC registers for peripheral access configuration of STM32L4, STM32L4+ and STM32U5 MCUs

Bus	STM32L4/L4+	STM32U5	Comments
AHB	• RCC_AHB1RSTR (AHB1) • RCC_AHB2RSTR (AHB2)	• RCC_AHB1RSTR (AHB1) • RCC_AHB2RSTR (AHB2) • RCC_AHB3RSTR (AHB3) • RCC_ AHB4RSTR (AHB4)	Used to [enter/exit] the AHB peripheral from reset
APB1	• RCC_AHB1ENR (AHB1) • RCC_AHB2ENR (AHB2)	• RCC_AHB1ENR (AHB1) • RCC_AHB2ENR (AHB2) • RCC_AHB3ENR (AHB3) • RCC_ AHB4ENR (AHB4)	Used to [enable/disable] the AHB peripheral clock
APB2	• RCC_AHB1SMENR (AHB1) • RCC_AHB2SMENR (AHB2) • RCC_AHB3SMENR (AHB3)	• RCC_AHB1SMENR (AHB1) • RCC_AHB2SMENR (AHB2) • RCC_AHB3SMENR (AHB3) • RCC_AHB4SMENR (AHB4)	Used to [enable/disable] the AHB peripheral clock in Sleep mode
APB3	N/A	RCC_ APB3RSTR	Used to [enter/exit] the APB3 peripheral from reset
		RCC_ APB3ENR	Used to [enable/disable] the APB1 peripheral clock
		RCC_ APB3SMENR	Used to [enable/disable] the APB1 peripheral clock in Sleep mode
SRD (SmartRun domain)		RCC_ SRDAMR	Used to [enable/disable] the peripheral in autonomous mode in Stop 0,1,2 modes

6.6.3 Peripheral clock configuration

The peripherals presented below have a dedicated clock source (independent from the system clock), that is used to generate the clock required for their operation. This section presents the difference between STM32L4, STM32L4+ and STM32U575/585, for the peripherals with different clock sources.

SAI

- In STM32L4+ and STM32L47/48/49/4Axxx devices, the SAI clocks are derived from one of the following sources:
  - An external clock mapped on SAI1_EXTCLK or SAI2_EXTCLK
  - PLLSAI1 VCO (PLLSAI1CLK)
  - PLLSAI2 VCO (PLLSAI2CLK)
  - Main PLL VCO (PLLSAI3CLK)
  - HSI16 clock
- In STM32L43/44/45/46xxx devices, the SAI clocks are derived from one of the following sources:
  - An external clock mapped on SAI1_EXTCLK for SAI1
  - PLLSAI1 (P) divider output (PLLSAI1CLK)
  - Main PLL (P) divider output (PLLSAI2CLK)
  - HSI16 clock
- In STM32U5 devices, the SAI1 and SAI2 clocks are derived from one of the following sources (selected by software):
  - An external clock mapped on AUDIOCLK for SAI1 and SAI2
  - PLL1_p clock
  - PLL2_p clock
  - PLL3_p clock
  - HSI16 clock

DFSDM/ADF/MDF

- In STM32L4 and STM32L4+ devices, the DFSDM clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK)
  - APB2 clock (PCLK2)
- In STM32U5 devices, the MDF and ADF audio clocks are derived from one of the following sources (selected by software):
  - PLL1 _p clock
  - PLL3_q clock
  - MSIK clock

OCTOSPI

- STM32L4 devices do not support the OCTOSPI peripheral.
- In STM32L4+ devices, the OCTOSPI clock is derived from one of the following sources (selected by software):
  - System clock
  - PLL48M1CLK
  - MSI clock
- In STM32U5 devices, the OCTOSPI clock is derived from one of the following sources (selected by software):
  - System clock
  - PLL1_q clock
  - MSIK clock
  - PLL2_q clock

FDCAN

In STM32U5 devices, the FDCAN clock is derived from one of the following sources (selected by software):

- PLL1_q clock
- PLL2_p clock
- HSE clock

Note: FDCAN is not available on STM32L4 and STM32L4+ devices.

USB

- In STM32L4 and STM32L4+ devices, the OTG_FS clock is derived from one of the following sources (selected by software):
  - Main PLL VCO (PLL48M1CLK)
  - PLLSAI1 VCO (PLL48M2CLK)
  - MSI clock (only when autotrimmed with the LSE)
  - HSI48 internal oscillator (not available on STM32L4x1/475/476/486xx)
- In STM32U5 devices, the OTG_FS or USB_FS clock is derived from one of the following sources (selected by software):
  - PLL1_q clock
  - PLL2_q clock
  - HSI48 clock
  - MSIK clock
- The OTG_HS clock is derived from one of the following sources (selected by software):
  - HSE clock
  - PLL1_q clock
  - HSE/2 selected
  - PLL1_p clock divided by 2

SDMMC

- In STM32L4 and STM32L4+ devices, the SDMMC clock is derived from one of the following sources (selected by software):
  - PLL1_p clock
  - PLLSAI1 VCO (PLL48M2CLK)
  - MSI clock (only when autotrimmed with the LSE)
  - HSI48 internal oscillator (not available on STM32L4x1/475/476/486xx)
- In STM32U5 devices, the SDMMC clock is derived from one of the following sources (selected by software):
  - PLL1_p clock
  - CLK48 (48 MHz)

RNG

- In STM32L4 and STM32L4+ devices, the RNG clock is derived from one of the following sources (selected by software):
  - PLL1_p clock
  - PLLSAI1 VCO (PLL48M2CLK)
  - MSI clock (only when autotrimmed with the LSE)
  - HSI48 internal oscillator (not available on STM32L4x1/475/476/486xx)
- In STM32U5 devices, the RNG clock is derived from one of the following sources (selected by software):
  - PLL1_p clock
  - HSI48 internal oscillator

ADC/DAC

- In STM32L4 and STM32L4+ devices, the ADC clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK)
  - PLLSAI1 VCO (PLLADC1CLK): not available on STM3L41/42xxx
  - PLLSAI2 VCO (PLLADC2CLK): not available on STM32L4+ and STM32L41/42/43/44/45/46xxx
- STM32L4 and STM32L4+ devices do not have a dedicated clock for DAC, independent from the system clock.
- In STM32U5 devices, the ADC and DAC clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK)
  - HCLK
  - pll2_r_ck
  - HSE
  - HSI16
  - MSIK
  - LSI and LSE: only as DAC1 clock source

U(S)ART

- In STM32L4 and STM32L4+ devices, the U(S)ARTs clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK)
  - HSI16 clock
  - LSE clock
  - APB1 or APB2 clock (PCLK1 or PCLK2 depending on which APB is mapped to the U(S)ART)
- In STM32U5 devices, the U(S)ARTs clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK)
  - PCLK2
  - LSE
  - HSI16

LPTIM

- In STM32L4 and STM32L4+ devices, the LPTIMx clock is derived from one of the following sources (selected by software):
  - LSI clock
  - LSE clock
  - HSI16 clock
  - APB1 clock (PCLK1)
  - External clock mapped on LPTIMx_IN1
- In STM32U5 devices, the LPTIMx clock is derived from one of the following sources (selected by software):
  - APB1 clock (PCLK1)
  - LSI
  - LSE
  - HSI16

LPUART

- In STM32L4 and STM32L4+ devices, the LPUART1 clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK)
  - APB1 clock (PCLK1)
  - LSE
  - HSI16 clock (only for STM32L4+ and STM32L41/42/43/44/45/46xxx)
  - HSI clock (only for STM32L4x1/4x5/4x6xx).
- In STM32U5 devices, the LPUART1 clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK)
  - MSIK
  - LSE
  - HSI16

SPI

- STM32L4 and STM32L4+ devices do not have a dedicated clock for SPI.
- In STM32U5 devices, the SPI clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK)
  - APBx clock (PCLKx)
  - MSIK
  - HSI16

HSPI

- STM32L4 and STM32L4+ devices do not support the OCTOSPI peripheral.
- In STM32U5 devices, the HSPI clock is derived from one of the following sources (selected by software):
  - System clock
  - PLL1_q clock (
  - PLL2_q clock
  - PLL3_r clock

DSI

- STM32L4 devices do not support the DSI peripheral.
- In STM32L4+ devices, the DSI clock is derived from one of the following sources (selected by software):
  - DSI-PHY is selected as DSI byte lane clock source (usual case)
  - PLLDSICLK is selected as DSI byte lane clock source, used in case DSI PLL and DSIPHY are off (low-power mode).
- In STM32U5 devices, the DSI clock is derived from one of the following sources (selected by software):
  - PLL3_p clock
  - DSI PHY PLL output selected

LTDC

- STM32L4 devices do not support the LTDC peripheral.
- In STM32L4+ devices, the LTDC clock is derived from one of the following sources (selected by software):
  - PLL3_r clock
  - PLL2_r clock
- In STM32U5 devices, the LTDC clock is derived from one of the following sources (selected by software):
  - PLL3_r clock
  - PLL2_r clock

(S)AES

In STM32U5 devices, the (S)AES clock is derived from the SHSI RC oscillator.

Note: (S)AES is not available on STM32L4 and STM32L4+.

6.7 Power controller (PWR)

The STM32U5 MCUs implement the same PWR features as the STM32L4 and STM32L4+ MCUs, with some specification updates and enhancements.

In STM32L4, STM32L4+ and STM32U5 MCUs, several peripherals are supplied through independent power domains: VDDA, VDDIO2, and VDDUSB. These supplies must not be provided without a valid operating supply on the VDD pin.

STM32L412/433/452/4x6xx and STM32L4Rx allow an external SMPS (DC-DC) power converter to be connected.

Moreover, the STM32U5 MCUs integrate an SMPS(DC-DC) power-converter function in parallel to the LDO, with on-the-fly selection, for optimum power consumption and noise filtering.

In STM32U5 MCUs, the SMPS power supply pins are available only on specific packages embedding an SMPS step-down converter. If the selected package features the SMPS step-down converter option but this converter is never used by the application, it is recommended to set the SMPS power supply pins as follows:

- VDDSMPS and VLXSMPS connected to VSS.
- VDD11 pins connected to VSS through two 2.2 µF capacitors as in normal mode.

Table 22. PWR features of STM32L4, STM32L4+ and STM32U5 MCUs

Features	STM32L4 and STM32L4+	STM32U5
Power supplies	• V_{DD} = 1.71 to 3.6V: external power supply for I/Os, flash memory and internal regulator • It is provided externally through VDD pins.	• V_{DD} = 1.71 to 3.6 V: external power supply for I/Os, the internal regulator, and the system analog such as reset, power management and internal clocks • It is provided externally through VDD pins.
	• V_{CORE} = 1.0 to 1.28 V: power supply for digital peripherals, SRAM, and flash memory • It is generated by an internal voltage regulator. • Two V_{CORE} ranges can be selected by software depending on target frequency.	• V_{CORE} = 0.9 to 1.2 V: power supply for digital peripherals, SRAM, and flash memory • It is generated by an internal voltage regulator. • Four V_{CORE} power ranges (1, 2, 3, 4) can be programmed by software depending on target frequency.
	V_{BAT} = 1.55 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present	V_{BAT} = 1.55 to 3.6 V: when V_{DD} is not present, V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator, backup registers and optionally backup SRAM.
	Independent power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}) allow a reduction of the power consumption by running MCU at lower supply voltage than analog and USB.	
	• V_{SSA}, V_{DDA} = 1.62 to 3.6 V (ADCs/COMPs) / 1.8 to 3.6 V (DAC/OPAMPs) / 2.4 V to 3.6 V (VREFBUF) • V_{DDA} is the external analog power supply for ADCs and DACs, voltage reference buffer, operational amplifiers, and comparators. • The VDDA voltage level is independent from the VDD voltage.	• V_{SSA}, V_{DDA} = 1.62 to 3.6 V (ADCs, COMPs, DACs, OPAMPs) / 1.8 to 3.6 V (VREFBUF) • V_{DDA} is the external analog power supply for ADCs and DACs, voltage reference buffer, operational amplifiers, and comparators. • The V_{DDA} voltage level is independent from the V_{DD} voltage.
	• V_{DDUSB} = 3.0 to 3.6 V: external independent power supply for USB transceivers • The V_{DDUSB} voltage level is independent from the V_{DD} voltage. • An additional digital supply is required. $V_{DD11USB}$ for HS interface (only available on STM32U59x/5Ax/5Fx/5Gx).	
	• V_{DDIO2} = 1.08 V to 3.6 V: external power supply for 14 I/Os (Port G[15:2]) • V_{DDIO2} voltage level is independent from the V_{DD} voltage (not applicable for STM32L41/42/43/44/45/46xxx)	

Features	STM32L4 and STM32L4+	STM32U5
Power supplies	N/A	• V_{DDSMPS} = 1.71 V to 3.6 V: external power supply for the SMPS step-down converter. It is provided externally through VDDSMPS supply pin, and must be connected to the same supply as VDD pin. • V_{LXSMPS} is the switched SMPS step-down converter output. • An external coil with typical value of 2.2 µH to be connected between the dedicated VLXSMPS pin to VSSSMPS, via a capacitor of 4.7 µF.
	V_{LCD} = 2.5 to 3.6 VN/A	
	Available only on SM32L4R9/4S9xx: • V_{DDDSI} is an independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY. • It must be connected to VDD.	• V_{DDDSI} is an independent DSI power supply dedicated for the DSI regulator and the MIPI D-PHY. • It must be connected to VDD.
	Available only on SM32L4R9/4S9xx: V_{CAPDSI} is the output of the DSI regulator (1.2 V), that must be connected externally to VDD12DSI.	V_{CAPDSI} is the output of the DSI regulator (1.2 V), that must be connected externally to VDD12DSI.
	Available only on SM32L4R9/4S9xx: • $V_{DD12DSI}$ is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. • An external capacitor of 2.2 µF must be connected on the VDD12DSI pin.	• $V_{DD12DSI}$ is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. • An external capacitor of 2.2 µF must be connected on the VDD12DSI pin.
Battery backup domain	• RTC with backup registers (128 bytes) • LSE • PC13 to PC15 I/Os	
Power supply supervisor	• Integrated POR/PDR circuitry • Programmable voltage detector (PVD)	
	• Brownout reset (BOR) • BOR is always enabled, except in Shutdown mode.	
	Four peripheral voltage monitorings (PVM): • PVM1 for V_{DDUSB} (~1.2 V) • PVM2 for V_{DDIO2} (~0.9 V) • PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V)	Four peripheral voltage monitorings (PVM): • UVM for V_{DDUSB} (~1.2V) • IO2VM for VDDIO2 (~0.9V) • AVM1/AVM2 for V_{DDA} (~1.6 V/~1.8V)
Low-power modes	Sleep mode	
	Low-power run mode (up to 2 MHz)	Range 4 in voltage scaling (24 MHz)
	• Low-power sleep mode (up to 2 MHz) • System clock is limited to 2 MHz. • I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz. • Consumption is reduced at lower frequency thanks to the low-power regulator.	
	Stop 0 and Stop 1 modes(1)	
	• Stop 2 mode for STM32L4 • Stop 2 mode for STM32L4+: SRAM3 enabled (RRSTP = 1) and disabled (RRSTP = 0) within PWR_CR1 register	Stop 2 mode(1)
	N/A	Stop 3 mode(1): Functional peripherals and sources of wake-up reduced to the same ones as in Standby mode.
	• Standby mode (VCORE domain powered off) • Optional SRAM2 retention • Optional I/O pull-up or pull-down configuration	• Standby mode (VCORE domain powered off) • Full SRAM2 content or 8 Kbytes or 56 Kbytes can be retained

Features	STM32L4 and STM32L4+	STM32U5
Low-power modes		• Optional I/O pull-up or pull-down configuration
	Shutdown mode (VCORE domain powered off and power monitoring off)	
External SMPS	• Support for external SMPS for high-power efficiency • Refer to the application note *Design recommendations for STM32L4xxxx with external SMPS, for ultra-low-power applications with high performance* (AN4978) for STM32L4 series.	N/A
Wake-up sources	Sleep mode: any peripheral interrupt/wakeup event	
	Stop 0, Stop 1 and Stop 2 modes: • any EXTI line event/interrupt • BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD	Stop 0, Stop 1 and Stop 2 modes: • any EXTI line event/interrupt
	Standby mode: • 5 WKUP pins configurable rising or falling edge • RTC event • external reset in NRST pin • IWDG reset	Standby mode: • 24 WKUP pins configurable rising or falling edge • RTC event • external reset in NRST pin • IWDG reset • Tamper detection
System clock after wake-up	Wake-up from Sleep (Sleep-now or Sleep-on-exit): same as before entering Sleep mode.	
	Wake-up from Stop: HSI16 (16 MHz) or MSI (all ranges up to 48 MHz) allowing 5 µs wake-up at high speed, without waiting for PLL startup time.	Wake-up from Stop: MSIS up to 24 MHz or HSI16, depending on software configuration.
	Wake-up from Standby: MSI (from 1 to 8 MHz)	Wake-up from Standby: MSIS (from 1 to 4 MHz)
	Wake-up from Shutdown: MSI (4 MHz)	Wake-up from Shutdown: MSIS (4 MHz)

1. *For STM32U5 MCUs, some peripherals are autonomous and can operate in Stop mode by requesting their kernel clock and their bus (APB or AHB) when needed.*

The following figures present the power supply for STM32L4, STM32L4+ and STM32U5 MCUs.

Figure 4. STM32L4 power supply overview

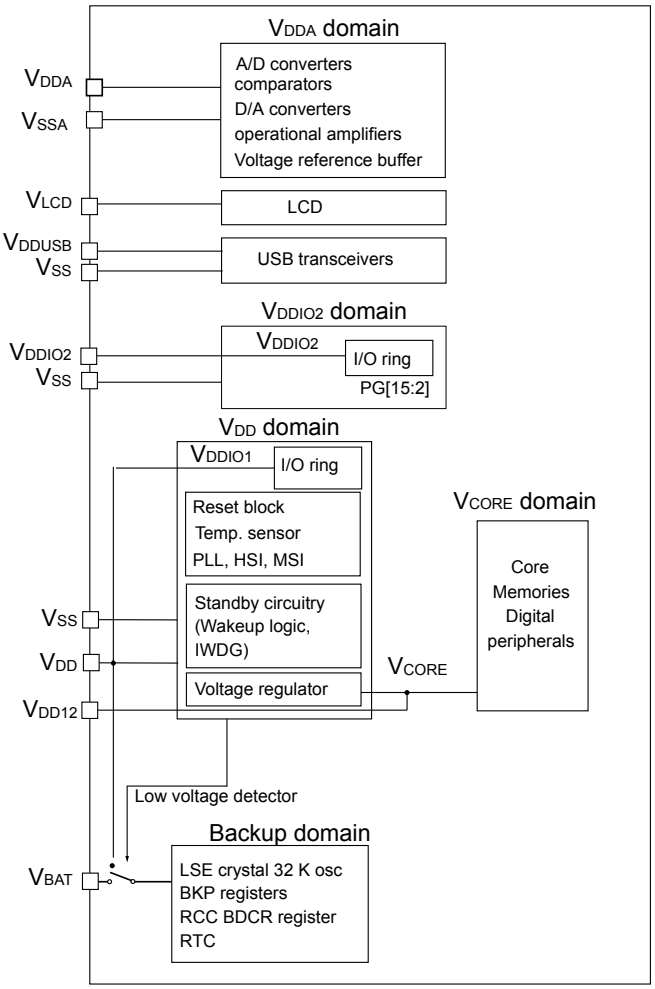


Figure 5. STM32L4P5/4Q5/4S5/4R5/4S7/4R7xx power supply overview

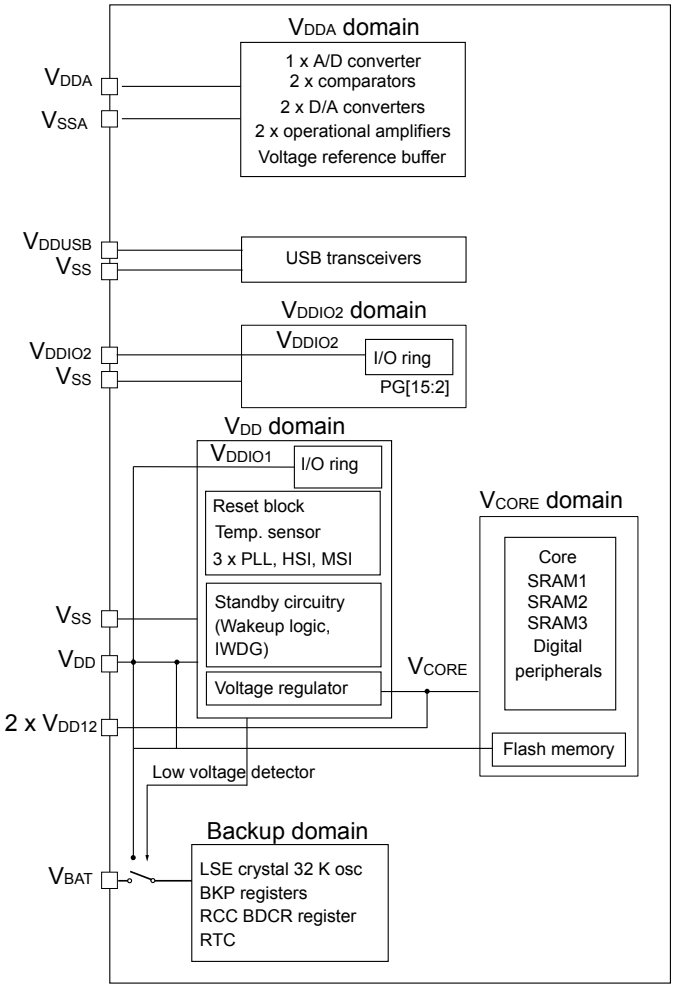


Figure 6. STM32L4R9/4S9xx power supply overview

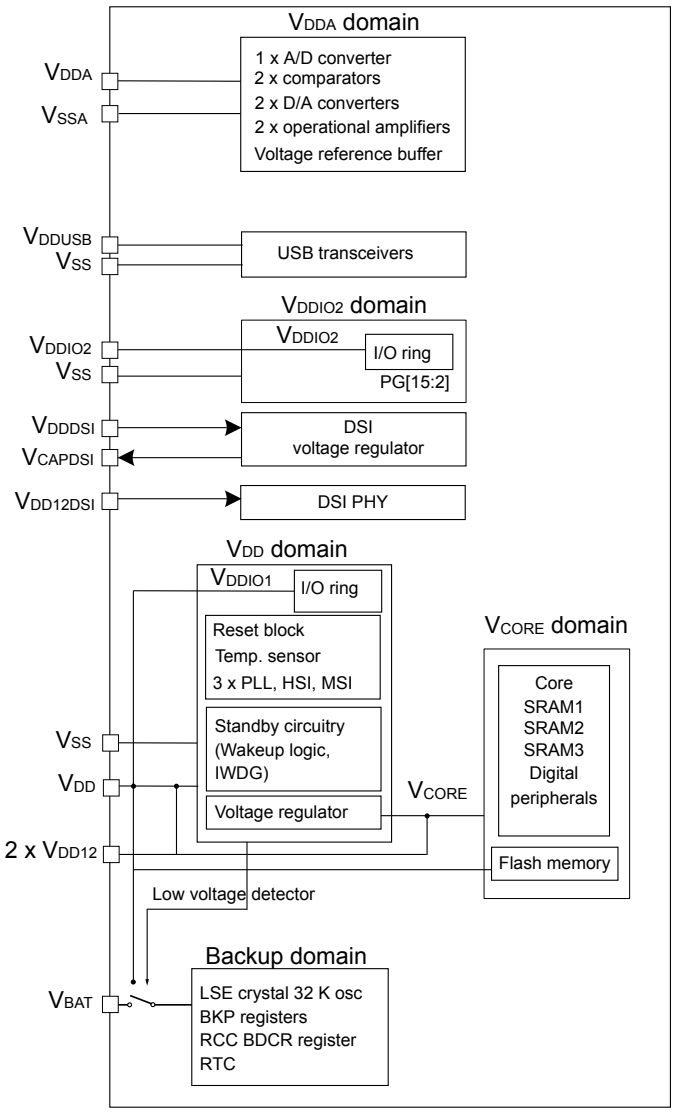
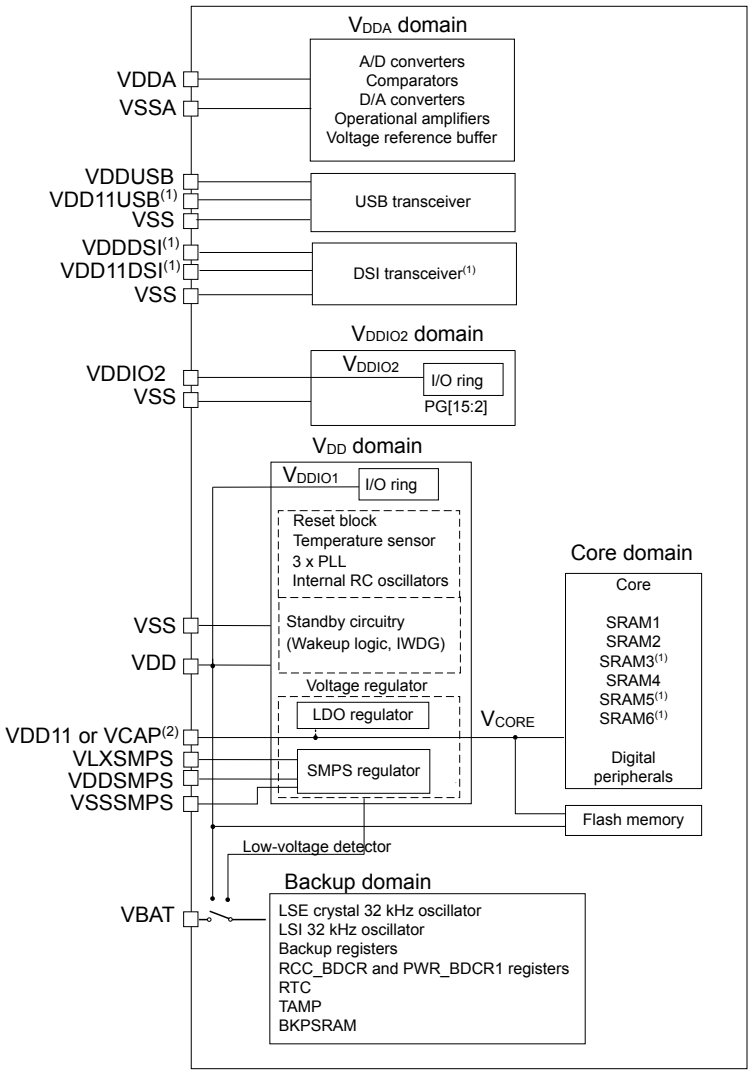


Figure 7. STM32U5 series power supply overview



1. This feature is only available on some devices in the STM32U5 series. Refer to the device datasheet for availability of its associated peripheral.
2. VDD11 supplies only on SMPS packages, otherwise VCAP pin(s).

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6.8 Autonomous peripherals and low-power background autonomous mode (LPBAM)

This mode is a key feature of STM32U5 series in order to reduce power consumption. Several peripherals support the autonomous mode which allows it to be functional and perform DMA transfers in Stop 0, Stop 1, and Stop 2 modes. The low-power background autonomous mode (LPBAM) is supported for Stop 2 mode, allowing to build more complex use cases with autonomous peripherals, without any CPU wake-up as a result of DMA transfers.

The autonomous peripherals request their kernel clock and their bus (APB or AHB) when needed in order to transfer data with DMA. The assigned DMA can be LPDMA1 or GPDMA1 as specified in the table below. For more details about this mode, refer to product reference manual.

Table 23. STM32U5 autonomous peripherals to DMA assignment in autonomous mode

Mode	DMA and memory transfers	Autonomous peripherals
Stop 0 and Stop 1 modes	GPDMA1 and SRAM1 to SRAM6	• LPTIM2 • USARTx (x = 1 to 6) • SPI1, SPI2 • I2C1, I2C2, I2C4, I2C5, I2C6 • MDF1
Stop 0, Stop 1 and Stop 2 modes	LPDMA1 and SRAM4	• ADC4 • DAC1 • LPTIM1, LPTIM3 • LPUART1 • SPI3 • I2C3 • ADF1

1. *The autonomous peripherals are the peripherals supporting DMA requests in Stop mode. All other peripherals that are functional in Stop mode can be accessed by DMA in Stop mode, using memory to memory mode. Refer to RM0456 for more details.*

6.9 General-purpose I/Os (GPIO)

The STM32U5 devices implement the same GPIO features than STM32L4 and STM32L4+, but with additionalTrustZone® security support.

For STM32U5 devices, each GPIO port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR) and a 32-bit set/reset register (GPIOx_BSRR).

In addition, all GPIOs in STM32U5 series have a 32-bit locking register (GPIOx_LCKR) and two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL), a secure configuration register (GPIOx_SECCFGR) and a high-speed low-voltage register (GPIOx_HSLVR).

Each general-purpose I/O pin of GPIO port in STM32U5 series can be individually configured as secure/non-secure in the GPIOx_SECCFGR register. After reset, all general-purpose I/O of GPIO ports are secure.

All GPIO registers can be read and written by privileged and unprivileged accesses, whatever the security state secure or non-secure.

In addition to the GPIO peripheral, the STM32U5 series embed a low-power general-purpose input/output (LPGPIO) that is designed to be used in conjunction with the GPIO interface and allows the I/O control in Stop mode (down to Stop 2 mode), using DMA in memory-to-memory transfer mode.

For more information about TrustZone security and GPIO and LPGPIO programming and usage for the STM32U5 devices, refer to the “General-purpose I/Os (GPIO)” and “Low-power general-purpose I/Os (LPGPIO)” sections of the reference manual and to the product datasheet for detailed description of the pinout and alternate function mapping.

6.10 Extended interrupt and event controller (EXTI)

The STM32U5 MCUs implement almost the same EXTI features than STM32L4 and STM32L4+ MCUs, with two exceptions: STM32U5 devices feature TrustZone® security support and privileged/unprivileged mode selection and do not feature direct event inputs.

Table 24. EXTI features of STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4/L4+	STM32U5
Number of event/interrupt lines	Up to 41 lines: • 12 direct, 26 configurable on STM324R/4Sxxx • 15 direct, 26 configurable on STM32L49/4Axxx • 14 direct, 26 configurable on STM32L47/48xxx • 12 direct, 25 configurable on STM32L41/42/43/44xxx	23 lines: all lines are configurable.

EXTI security protection

When security is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a secure access. A non-secure write access is discarded and a read returns 0.

EXTI privilege protection

When privilege is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a privileged access. An unprivileged write access is discarded and a read returns 0.

The table below presents the EXTI line differences between STM32L4, STM32L4+ and STM32U5 series.

Table 25. EXTI lines of STM32L4, STM32L4+ and STM32U5 MCUs

Line	STM32L4	STM32L4+	STM32U5
17	OTG_FS wake-up event (OTG_FS_WKUP)(1)(2)		COMP1 output
18	RTC alarms		COMP2 output
19	RTC tamper or timestamp or CSS_LSE		VDDUSB voltage monitor
20	RTC wake-up timer		VDDIO2 voltage monitor
21	COMP1 output		VDDA voltage monitor 1
22	COMP2 output		VDDA voltage monitor 2
30	UART5 wake-up(2)	N/A	N/A
34	Reserved	SWPMI1 wake-up(2)(3)	
36	PVM2 wake-up	N/A	
39	Reserved	LCD wake-up(4)	
40	I2C4 wake-up	I2C4 wake-up(5)	

1. *Not available for STM32L431xx.*
2. *This line source cannot wake up from Stop 2 mode.*
3. *Not available on STM32L41/42/45/46xxx.*
4. *Only available on STM32L4x3/4x5/4x6xx.*
5. *Not available on STM32L41/42/43/44xxx.*

6.11 Cyclic redundancy check calculation unit (CRC)

The CRC architecture is the same in STM32U5, STM32L4, and STM32L4+ series, supporting the same features, with a minor difference in CRC_IDR, that is extended from an 8-bit register in STM32L4 series to a 32-bit register in STM32L4+ and STM32U5 series.

7 Migration of security peripherals

7.1 Tamper and backup registers (TAMP)

The STM32U5 devices anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 backup registers, each of 32-bit size, are retained in all low-power modes and also in V_{BAT} mode.

The table below compares the tamper pins and internal events and lists the main differences between STM32U5, STM32L4+ and STM32L4 MCUs.

Table 26. Tamper pins and events of STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4/L4+	STM32U5
Tamper pins (not compatible)	3 tamper pins: • PC13(RTC_TAMP1) • PA0(RTC_TAMP2) • PE6(RTC_TAMP3)	8 inputs/outputs TAMP pins for 8 external tamper detection events: • PC13(TAMP_IN1/TAMP_OUT2) • PA0 (TAMP_IN2/TAMP_OUT1) • PE6(TAMP_IN3/TAMP_OUT6) • PC5 (TAMP_IN4/TAMP_OUT5) • PA1 (TAMP_IN5/TAMP_OUT4) • PE3 (TAMP_IN6/TAMP_OUT3) • PE4 (TAMP_IN7/TAMP_OUT8) • PE5 (TAMP_IN8/TAMP_OUT7)
TAMP internal events to protect against transient or environmental perturbation attacks	N/A	11 internal tamper events: • tamp_itamp1: supply voltage monitoring • tamp_itamp2: temperature monitoring • tamp_itamp3: LSE monitoring • tamp_itamp5: RTC calendar overflow • tamp_itamp6: JTAG/SWD access when RDP > 0 • tamp_itamp7: voltage monitoring through ADC analog watchdog 1 • tamp_itamp8: monotonic counter overflow • tamp_itamp9: cryptographic peripheral fault (SAES, AES, PKA, or RNG) • tamp_itamp11: IDWG reset when tamper flag is set • tamp_itamp12: voltage monitoring through ADC analog watchdog 2 • tamp_itamp13: voltage monitoring through ADC analog watchdog 3
TAMP pins functionality over V_{DD} mode	All tamper pins are functional in all low-power modes when the external V_{DD} power supply is present.	
TAMP pins functionality over V_{BAT} mode	All tampers are functional in V_{BAT} mode.	
Active tamper detection mode	N/A	X
Potential tamper detection mode		X
Boot hardware key		• Stored in the first backup registers • Programmed during boot for secure AES
Tamper protected assets	Backup registers	• Backup registers • SRAM2 • ICACHE/DCACHE content • OTFDEC keys and CRC registers • SAES, AES, HASH peripherals • PKA SRAM • RHUK in system flash memory

7.2 Hash processor (HASH)

The STM32U5, STM32L4+ and STM32L49/4Axxx devices embed a HASH hardware accelerator with same features.

Both hash processors provide an interface to connect to the DMA controller. The STM32U5 HASH peripheral supports both single- and fixed-DMA burst transfers of four words. However, the HASH in STM32L4+ and STM32L49/4Axxx devices only support single-DMA transfers.

HASH registers are compatible, except a minor difference on HASH_CR:

- ALGO[0] in bit 7 for STM32L4+ and STM32L49/4Axxx devices
- ALGO[0] in bit 17 for STM32U5 devices.

7.3 On-the-fly decryption engine (OTFDEC)

The OTFDEC decrypts in real-time the encrypted content stored in the external OCTOSPI memories used in Memory-mapped mode. The OTFDEC uses the AES-128 algorithm in counter mode (CTR).

The STM32U5 embed two OTFDEC peripherals. While in STM32L4 and STM32L4+, this peripheral is not supported.

7.4 True random number generator (RNG)

The STM32U5, STM32L4, and STM32L4R/4Sxxx devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit, with the same features except the minor differences detailed in the table below.

Table 27. RNG features of STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4	STM32L4R/4Sxxx (in STM32L4+ series)	STM32U5
True random number generator	X		
Can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)			
Tested using German BSI statistical tests of AIS-31 (T0 to T8)	N/A	X	
Embeds start-up and NIST SP800-90B approved continuous health tests			
Can be disabled to reduce power consumption	X		
Can be enabled with an automatic low-power mode (default configuration).	N/A	X	
AHB slave peripheral, accessible through 32-bit word single accesses only	X		
RNG internal tamper event signal to TAMP	N/A	X	
Transparent use by SAES and PKA for DPA resistance			

In STM32U5 MCUs, the RNG is transparently used by SAES and PKA for DPA resistance. When an unexpected error is found by the RNG, an internal tamper event is triggered in TAMP peripheral, and the RNG stops delivering random data.

When this event occurs, a secure application needs to reset the RNG, either using the central reset management, or the global SoC reset. Then a proper initialization of the RNG is required, again.

7.5 Public key accelerator (PKA)

The STM32U5 and STM32L4P5/Q5xx devices embed one PKA peripheral intended for the computation of cryptographic public key primitives within the Montgomery domain. All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The STM32U5 and STM32L4P5/Q5xx devices share almost the same PKA features. The STM32U5 devices embed two new features and three new computation operators. Registers are compatible, except new bits added in STM32U5 to map the new features.

The STM32L4 devices do not support a PKA peripheral.

Table 28. PKA features of STM32L4+ and STM32U5 MCUs

Feature	STM32L4P5/Q5xx (in STM32L4+ series)	STM32U5
RSA modular exponentiation, RSA Chinese remainder theorem (CRT) exponentiation	X	
ECC scalar multiplication, point on curve check		
ECC complete addition	N/A	X
ECC double-base ladder		
ECC projective to affine		
ECDSA signature generation and verification	X	
Size of RSA/DH operands (in bits)	3136	4160
Size of ECC operands (in bits)	640	
Arithmetic and modular operations (such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication)	X	
Built-in Montgomery domain inward and outward transformations		
Protection against differential power analysis (DPA) and related side-channel attacks	N/A	X

7.6 AES and SAES hardware accelerators

The STM32U5 embed two AES accelerators: one secure AES (SAES) and a faster AES. This is a new feature in STM32U5, that is not available in STM32L4 and STM32L4+ devices.

In STM32U5 series, the SAES with hardware unique key embeds protection against differential power analysis (DPA) and related side channel attacks. When an unexpected hardware fault occurs, an output tamper event is triggered, and the AES automatically clears key registers. A reset is required for the AES to be usable again.

The AES can use the SAES as security coprocessor. In this case, the secure application prepares the key in robust SAES then, when ready, the AES can load this key through a dedicated hardware key bus. Recommended sequences are described in sections 'AES shared key usage' and 'SAES operations with shared keys' of the product reference manual.

7.7 Global TrustZone controller (GTZC)

The security architecture of the STM32U5 MCUs is based on Arm®TrustZone®with the Armv8-M mainline extension. Each GPIO or peripheral, DMA channel, clock configuration register, DCACHE/ICACHE, or small part of flash memory or SRAM can be configured as trusted or untrusted.

The GTZC embedded in the STM32U5 is used to configure secure-TrustZone and privileged attributes within the full system. All details about GTZC are described in the product reference manual.

This controller is a new feature of the STM32U5 MCUs and is not embedded in STM32L4 or STM32L4+ MCUs.

8 Migration of timer peripherals

The STM32U5, STM32L4+ and STM32L4 devices include two advanced-control timers, up to seven general-purpose timers, two basic timers, up to four low-power timers (two for STM32L4 and STM32L4+), two watchdog timers and two SysTick timers.

This section compares the features of the above listed timers and RTC in STM32L4, STM32L4+ and STM32U575/585 devices.

8.1 Advanced-control timers (TIM1/8)

The STM32U5, STM32L4+ and STM32L4 include two advanced-control timers, TIM1 and TIM8, with identical features detailed in the table below (only TIM1 for STM32L41/42/43/44/45/46xxx devices).

Table 29. Advanced-control timer (TIM1/8) features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4, STM32L4+ and STM32U5
Counter resolution and type	16-bit up, down, up/down auto-reload counter
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536
Channels	Up to six independent channels for: • Input capture (but channels 5 and 6) • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output
Complementary outputs	Complementary outputs with programmable dead-time
Synchronization with external signals and general-purpose timers	Synchronization circuit to control the timer with external signals and to interconnect several timers together. The advanced-control (TIM1/TIM8) and general-purpose (TIMx) timers are completely independent, and do not share any resources.
Repetition counter	Repetition counter to update the timer registers only after a given number of counter cycles
Break inputs	Two break inputs to put the timer output signals in a safe user selectable configuration
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare
Encoders and sensors	Support incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes
Trigger input	Trigger input for external clock or cycle-by-cycle current management
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)

8.2 GP timers with up, down, up-down auto-reload counter (TIM2/3/4/5)

The GP (general-purpose) timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler. The STM32U5, STM32L4+ and STM32L4 devices include GP timers with up, down or up-down auto-reload counter (TIM2, TIM3, TIM4 and TIM5), with identical features (TIM4/5 only available on STM32L4x1/47x/48x/49x/4Axxx, TIM3 only available on STM32L4x1/451/452/462/47x/48x/49x/4Axxx).

Table 30. GP timer (TIM2/3/4/5) features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4/L4+	STM32U5
32-bit resolution	TIM2/TIM5	TIM2/TIM3/TIM4/TIM5
16-bit resolution	TIM3/TIM4	-
Counter resolution and type	16- or 32-bit up, down, up/down auto-reload counter	
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536	
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output	
Synchronization with external circuits and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers	
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare	
Encoders and sensors	Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes	
Trigger input	Trigger input for external clock or cycle-by-cycle current management	
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)	

8.3 GP timers with auto-reload up-counter (TIM15/16/17)

The STM32U5, STM32L4+ and STM32L4 MCUs include three 16-bit resolution GP timers with a 16-bit auto-reload up-counter (TIM15, TIM16, and TIM17) with identical features (no TIM17 on STM32L41/42/43/44/45/46xxx).

Table 31. GP timer (TIM15/16/17) features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4, STM32L4+ and STM32U5
Counter resolution and type	16-bit auto-reload up-counter
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536
Channels	Up to two independent channels for: • Input capture • Output compare • PWM generation (edge mode) • One-pulse mode output
Complementary outputs	Complementary outputs with programmable dead-time (for channel 1 only)

Feature	STM32L4, STM32L4+ and STM32U5
Synchronization with external circuits and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers
Repetition counter	Repetition counter to update the timer registers only after a given number of counter cycles
Break inputs	One break input to put the timer output signals in the reset state or a known state
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization, or count by internal/external trigger) • Input capture • Output compare • Break input (interrupt request)
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)

8.4 Basic timers (TIM6/7)

The basic timers TIM6 and TIM7 consist in a 16-bit auto-reload counter driven by a programmable prescaler. These timers are completely independent, and do not share any resources.

The STM32U5, STM32L4 and STM32L4+ devices have the same basic timers features.

Table 32. Basic timer (TIM6/7) features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4, STM32L4+ and STM32U5
Counter resolution and type	16-bit auto-reload up-counter
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536
Synchronization signals	Synchronization circuit to trigger the DAC
Interrupt/DMA generation	Interrupt/DMA generation on the update event, counter overflow
Application examples	• Time-base generation • Driving the DAC

8.5 Low-power timers (LPTIM1/2/3/4)

The LPTIMx is a 16-bit timer that benefits from the ultimate developments in power-consumption reduction. The STM32U5 devices include four LPTIMs versus two in the STM32L4 and STM32L4+ devices. LPTIMs share the same features in these series, but new features are added in STM32U5 series, such as:

- Two independent channels per LPTIM
- Input capture channel
- DMA requests
- Autonomous function in Stop modes

Table 33. LP timer (LPTIMx) features of STM32L4, STM32L4+ and STM32U5 series

Feature	STM32L4 series	STM32L4+ series	STM32U5 series
LPTIMx	LPTIM1 and LPTIM2		LPTIM1, LPTIM2, LPTIM3, and LPTIM4
Counter resolution and type	16-bit up-counter		
Prescaler factor	3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64 or 128)		
Selectable clock	• Internal clock sources: LSE, LSI, HSI or APB clock • External clock source over LPTIMx input (working with no low-power oscillator running, used by pulse counter application)		

Feature	STM32L4 series	STM32L4+ series	STM32U5 series
Auto-reload	16-bit ARR auto-reload register		
Capture/compare	16 bit compare register		16-bit capture/compare register
Continuous mode	Continuous/one-shot mode		
Trigger mode	Selectable software/hardware input trigger		
Glitch filter	Programmable digital glitch filter		
Configurable output	Configurable output: pulse, PWM		
Polarity	Configurable I/O polarity		
Encoder mode	X		
Repetition counter	X(1)	X(2)	X
Input capture, PWM, and one-pulse channels	N/A		Up to two independent channels for: • Input capture • PWM generation (edge aligned mode) • One-pulse mode output
DMA requests			DMA request generation on the following events: • Update event • Input capture

1. *Only available on STM32L41/42xxx devices.*
2. *Only available on STM32L4P5/4Q5xx devices.*

Some of the above features are not similarly implemented on LPTIMx instances, as described in the table below.

Table 34. Implementation of LPTIMx features on various instances

Feature	STM32L4/L4+ series		STM32U5 series			
	LPTIM1	LPTIM2	LPTIM1	LPTIM2	LPTIM3	LPTIM4
Encoder mode	X	-	X	X	-	-
PWM mode	-	-	X	X	X	X
Input capture	-	-	X	X	X	-
Number of DMA requests	-	-	3	3	3	-
Autonomous mode	-	-	X	X	X	-

8.6 Watchdogs (WWDG/IWDG)

The STM32U5, STM32L4+ and STM32L4 MCUs embed two watchdogs:

- a system window watchdog (WWDG) with same features
- an independent watchdog (IWDG) with same features, except the STM32U5 IWDG capability to generate an early wakeup interrupt

Table 35. IDWG features of STM32L4, STM32L4+ and STM32U5 series

Feature	STM32L4/L4+	STM32U5
LSI used as IWDG kernel clock	X	
Window function		
Early wakeup interrupt generation	-	X

Feature	STM32L4/L4+	STM32U5
Reset generation (refer to the RCC section of the product reference manual for more details)	X	
Capability to work in system Stop		
Capability to work in system Standby	-	X
Capability to generate an interrupt in system Stop		

8.7 Real-time clock (RTC)

The STM32U5 MCUs implement similar RTC features as STM32L4 and STM32L4+, adding some specification updates and enhancements. The main differences are stated in the table below.

Table 36. RTC features of STM32L4, STM32L4+ and STM32U5 MCUs

Features	STM32L4/L4+	STM32U5
Binary mode with 32-bit free-running counter	N/A	X
RTC TrustZone support		

8.8 SysTick timer

The SysTick timer is dedicated to real-time operating systems but can also be used as a standard down-counter.

The STM32U5 Cortex®-M33 with TrustZone® embeds two SysTick timers. When TrustZone® is activated, the two SysTick timers are available. But, when TrustZone® is disabled, only one SysTick timer is available.

STM32L4 and STML32L4+ embed a Cortex®-M4 with just one SysTick timer.

9 Migration of communication peripherals

9.1 Serial peripheral interface (SPI)

This section highlights the SPI features implemented on STM32L4, STM32L4+ and STM32U5 MCUs.

Table 37. SPI features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4/L4+	STM32U5
SPI peripherals	SPI1, SPI2, and SPI3 (same features in the three instances)	• SPI1, SPI2 (full feature set instances) • SPI3 (limited feature set instance)
Full-duplex synchronous transfer on three lines	X	X
Half-duplex synchronous transfer on two lines (with bidirectional data line)	X	X
Simplex synchronous transfer on two lines (with unidirectional data line)	X	X
Data size	4- to 16-bit data size selection	4- to 32-bit data size selection on SPI1, SPI2
	N/A	Fixed to 8- and 16-bit only on SPI3
Multimaster or multislave mode capability	X	X
Clock inputs	One input: PCLK is the unique SPI clock source.	Two independent clock inputs: peripheral kernel clock (spi_ker_ck) is independent of PCLK.
Baudrate prescalers	Master/slave mode baudrate prescalers up to f_{PCLK} / 2	Baudrate prescaler up to kernel frequency / 2
	N/A	spi_ker_ck prescaler can be bypassed from RCC in master mode.
Protection of configuration and settings	N/A	X
Slave select (SS) management	NSS management by hardware or software for both master and slave: dynamic change of master/slave operations	Hardware or software management of SS for both master and slave
Adjustable minimum delays between data and between SS and data flow	N/A (fixed)	X
Configurable SS signal polarity and timing	N/A	Configurable SS signal polarity and timing, MISO x MOSI swap capability
Programmable clock polarity and phase	X	X
Programmable data order with MSB-first or LSB-first shifting	X	X
Programmable transaction data	N/A	Programmable number of data within a transaction to control SS and CRC
Dedicated transmission and reception flags with interrupt capability	X	X
SPI Motorola and Texas Instrument formats support	X	X
Hardware CRC feature can secure communication at the end of transaction by: • adding CRC value in Tx mode • automatic CRC error checking for Rx mode	CRC fixed to 8- or 16-bit for all SPIs	• SPI1 and SPI2: CRC polynomial length configurable from 9 to 17 bits • SPI3: CRC polynomial length configurable from 9 to 17 bits

Feature	STM32L4/L4+	STM32U5
Interrupt events and error detection with interrupt capability	Interrupts: • Transmit TXFIFO ready to be loaded • Data received in receive RXFIFO • Master mode fault • Overrun error • TI frame format error • CRC protocol error	Interrupts: • TxFIFO ready to be loaded • Data received in RxFIFO • Both TXP and RXP active • Transmission Transfer Filled • Overrun error • Underrun error • TI frame format Error • CRC error • Mode fault • End of transfer • Master mode suspended • TxFIFO transmission complete
	N/A	All the interrupt events can wake up the system from Sleep mode at each instance
FIFO size	Two 32-bit embedded Rx and Tx FIFOs with DMA capability	Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability
Number of transferred data	Number defined by the counter for the SPI transmission DMA channel	Programmable number of data in transaction: • SPI1 and SPI2: unlimited, expandable • SPI3: up to 1024 (no data counter)
FIFO thresholds	Fixed threshold to 1/2 FIFO or 1/4 FIFO level	Configurable FIFO thresholds (data packing)
Configurable behavior at slave underrun condition	N/A	X (support of cascaded circular buffers)
Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wake-up from Stop capability	N/A	• SPI 1/2: Stop 0 and Stop 1 modes with wake-up • SPI3: Stop 0, Stop 1 and Stop 2 modes
RDY status pin	N/A	Optional status pin RDY signalizing the slave device ready to handle the data flow

SPI autonomous mode

The three SPI peripherals in the STM32U5 series support autonomous operation (SPI1 and SPI2 support autonomous operation down to Stop 1 mode and SPI3 down to Stop 2 mode), with the following main feature:

The SPI can handle and initialize transactions autonomously, requiring no specific system execution interaction until the ongoing transaction ends.

9.2 Inter-integrated circuit (I2C)

The I2C peripherals share the same features in the STM32U5, STM32L4+ and STM32L4 MCUs. Differences are shown in the table below.

In addition, the STM32U5 MCUs embed the autonomous mode of I2C peripherals, allowing the I2C to be functional in Stop mode. The autonomous mode can also be used in Run, Sleep or Stop mode.

Table 38. I2C features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4/L4+	STM32U5
Instances	I2C1, I2C2, I2C3, and I2C4	I2C1, I2C2, I2C3, I2C4, I2C5(1), I2C6(1)
7- and 10-bit addressing mode	Same feature on all the instances	
Standard-mode (up to 100 Kbit/s)		
Fast-mode (up to 400 Kbit/s)		
Fast-mode Plus with 20 mA output drive I/Os (up to 1 Mbit/s)		
Independent clock		
SMBus/PMBus		
Wake-up from Stop 0 and Stop 1 modes		
Wakeup from Stop 2 mode	Same feature on I2C3	
Autonomous mode	N/A	• I2C1, I2C2, I2C4, I2C5(1) and I2C6(1) in CD (CPU domain) • I2C3 in SRD (SmartRun domain)

1. *I2C5 and I2C6 are only available for STM32U59x/5Fx/5Gx devices.*

9.3 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32U5 MCUs implement the same U(S)ART features as the STM32L4 and STM32L4+ MCUs, with some specification updates and enhancements. The main differences are stated in the table below.

Table 39. U(S)ART features of STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4 and STM32L4+	STM32U5
Instances	• 3 USARTs • 2 UARTs for STM32L4+ and STM32L47/48/49/4Axxx • 1 UART for STM32L45/46xxx • 1 LPUART	• up to 4 USARTs • 2 UARTs • 1 LPUART
Baud rate	Up to 10 Mbit/s (when the clock frequency is 80 MHz and oversampling is by 8)	Depends on the frequency (oversampling by 16 or by 8)(1)
Clock	Dual-clock domain allowing: • UART functionality and wake-up from Stop mode • Convenient baud rate programming independent from the PCLK reprogramming	Dual-clock domain and wake-up from low-power mode
Data	• Word length: programmable (7, 8 or 9 bits) • Programmable data order with MSB-first or LSB-first shifting	
Interrupt	• 14 interrupt sources with flags for STM32L4 • 23 interrupt sources with flags for STM32L4+	23 interrupt sources with flags
Autonomous mode	N/A	Autonomous functionality in Stop mode with wake-up from Stop capability.
Other features	• RS232 hardware flow control (CTS/RTS) • Continuous communication using DMA • Multiprocessor communication • Single-wire half-duplex communication • IrDA SIR ENDEC block • LIN mode • SPI master	• RS232 hardware flow control and RS485 • Continuous communication using USART and DMA • Multiprocessor communication • Single-wire half-duplex communication • IrDA SIR ENDEC block • LIN mode
	• Wakeup from Stop mode (start bit, received byte, address match) • Support for ModBus communication: timeout feature CR/LF character recognition • Two internal FIFOs to transmit and receive data (for STM32L4+) • SPI slave (for STM32L4+) • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable TX/RX pin configuration *Note: LPUART does not support Synchronous mode (SPI master), Smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt and auto baud rate detection.*	• Wake-up from Stop mode (start bit, received byte, address match) • ModBus communication: timeout feature CR/LF character recognition • Two internal FIFOs to transmit and receive data • SPI slave • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable TX/RX pin configuration *Note: LPUART does not support Synchronous mode (SPI master), Smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt and auto baud rate detection.*
	• Smartcard mode (T = 0, T = 1) are supported. • Features are added to support T = 1 (such as receiver timeout, block length, end of block detection and binary data inversion) • Number of stop bits: 1, 1.5, 2	

1. *Refer to the USART section in the reference manual.*

9.4 Serial audio interface (SAI)

The SAI offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted (such as I^2S standards, LSB- or MSB-justified, PCM/DSP, TDM, and AC'97 protocols). The SPDIF output is offered when the audio block is configured as a transmitter.

Table 40. SAI features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4	STM32L4+	STM32U5
Instances	SAI1 and SAI2(1)		
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	Same feature on all available instances		
Mute mode			
Stereo/Mono audio frame capability			
16 slots with configurable size			
Configurable data size: 8-, 10-, 16-, 20-, 24-, 32-bit			
SPDIF			
FIFO size	8 words		
PDM	N/A	Available on SAI1 only	

1. *No SAI in STM32L41/42xxx and STM32U35/545 devices. Only SAI1 on STM32L43/44/45/46xxx devices.*

9.5 Controller area network (CAN)

The main differences related to CAN between STM32L4, STM32L4+ and STM32U5 MCUs are presented in the table below.

Table 41. CAN features in STM32L4, STM32L4+ and STM32U5 MCUs

CAN	STM32L4 and STM32L4+	STM32U5
Instances	• x1 on STM32L4+ and STM32L43/44/45/46/47/48xxx • x2 on STM32L49/4Axxx • Not available on STM32L41/42xxx	x1 FDCAN
Features	• Supports CAN protocol version 2.0 A, B active • Bit rates up to 1 Mbit/s • Supports the time triggered communication option • Tx: 3 transmit mailboxes, configurable priority, time stamp on SOF transmission • Rx: 2 receive FIFOs with 3 stages, scalable filter banks, identifier list, configurable FIFO overrun, time stamp on SOF reception • Time-triggered communication option: Disable automatic retransmission mode 16-bit free running timer Time Stamp sent in last two data bytes • Management – Maskable interrupts – Software-efficient mailbox mapping at a unique address space	• Conform with CAN protocol version 2.0 part A, B, and ISO 11898-1: 2015, -4 • CAN FD with maximum 64 data bytes supported • CAN error logging • AUTOSAR and J1939 support • Improved acceptance filtering • Rx: 2 receive FIFOs of 3 payloads each (up to 64 bytes per payload) • Separate signaling on reception of high-priority messages • Configurable transmit FIFO/queue of 3 payloads (up to 64 bytes per payload) • Transmit event FIFO • Programmable loop-back test mode • Maskable module interrupts • 2 clock domains: APB bus interface and CAN core kernel clock • Power down support • Dual-interrupt lines

9.6 Secure digital input/output MultiMediaCard interface (SDMMC)

The STM32U5 MCUs embed up to two SDMMC instances, and implement the same SDMMC features as the STM32L4 and STM32L4+ MCUs, but with some specification updates.

Note: SDMMC is not available on STM32L41/42xxx and STM32L432/442xx.

Table 42. SDMMC features of STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4	STM32L4+	STM32U5
Bus	APB2		
Clock source	• MSI clock • PLL/Q • PLLSAI1/Q	• MSI clock • PLL/Q • PLLSAI1/Q • HSI48(1)	• Main PLL VCO (PLL48M1CLK) • PLLSAI1 VCO (PLL48M2CLK) • MSI clock • HSI48
Other features	Full compliance with MultiMediaCard system specification version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit	Full compliance with MultiMediaCard system specification version 4.51. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit	Full Compliance with embedded MultiMediaCard system specification version 5.1. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit. HS200 SDMMC_CK speed limited to maximum allowed I/O speed. HS400 not supported
	Full compliance with SD memory card specification version 2.0	Full compliance with SD memory card specification version 4.1	Full compliance with SD memory card specification version 6.0
	Full compliance with SD I/O card specification version 2.0 Card support for two different databus modes: 1-bit (default) and 4-bit	Full compliance with SDIO card specification version 4.0. Card support for two different databus modes: 1-bit (default) and 4-bit	Full compliance with SDIO card specification version 4.0. Card support for two different databus modes: 1-bit (default) and 4-bit
	Data transfer up to 50 MHz for the 8-bit mode	Data transfer up to 104 Mbyte/s for the 8-bit mode	Data transfer up to 208 Mbyte/s for the 8-bit mode
	N/A	DMA is used to provide high-speed transfer between the SDMMC FIFO and the memory. The SDMMC internal DMA (IDMA) provides one channel to be used either for transmit or receive.	
		N/A	IDMA linked list support

1. *Only on STM32L4+ and STM32L43/44/45/46/49/4Axxx.*

9.7 Digital camera interface (DCMI) and parallel synchronous slave interface (PSSI)

The DCMI is available on STM32L49/4Axx, STM32L4+ and STM32U5 MCUs. The PSSI is only available on STM32L4P5/Q5xx and STM32U5 MCUs.

DCMI and PSSI use the same circuitry and then, when they are both implemented on a device, they cannot be used at the same time: when using the PSSI, DCMI registers cannot be accessed, and vice-versa. In addition, PSSI, and DCMI share the same alternate functions and interrupt vector.

The DCMI main features are the following:

- 8-, 10-, 12-, or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature

- Data formats supported:
  - 8-, 10-, 12-, and 14-bit progressive video (either monochrome or raw Bayer)
  - YCbCr 4:2:2 progressive video
  - RGB 565 progressive video
  - Compressed data JPEG

The PSSI peripheral main features are listed below:

- Slave mode operation
- 8- or 16-bit parallel data input or output
- 8-word (32-byte)
- Data enable (PSSI_DE) alternate function input and ready (PSSI_RDY) alternate function output

9.8 Universal serial-bus interface (USB)

The STM32L4, STM32L4+ and STM32U5 MCUs have different USB peripherals:

- USB OTG FS implemented in STM32U575/585, STM32L4+ and STM32L47/48/49/4Axx MCUs.
- USB FS implemented in STM32U535/545 and STM32L41/42/43/44/45/46xxx.
- USB OTG HS implemented in STM32U59x/5Ax/5Fx/5Gx.

On STM32U5, STM32L4+ and STM32L41/42/43/44/45/46/49/4Axx MCUs, an included CRS (clock recovery system) provides a precise clock to the USB peripheral:

- When using USB device mode, the CRS allows crystal-less USB operation.
- When using USB host mode, the CRS allows low frequency crystal (32.768 kHz) USB operation.

Most OTG_FS features supported by the STM32L4 and STM32L4+ MCUs are also supported by the STM32U5 MCUs.

Table 43. USB features in STM32L4, STM32L4+ and STM32U5 MCUs

Features	STM32L4/L4+	STM32U5
General	• Full support for the USB OTG_FS without clock recovery (for STM32L476/486xx) • Full support for the USB OTG_FS) with clock recovery (only on STM32L4+ and STM32L47/48/49/4Axxx) • USB FS device (only on STM32L41/42/43/44/45/46xxx)	For STM32U59x/5Ax/5Fx/5Gx series: Full support for the USB OTG_HS without clock recovery For STM32U575/585 series: Full support for the USB OTG_FS with clock recovery. For STM32U535/545 series: USB FS device.
	FS mode: • For STM32L4+ and STM32L47/48/49/4Axxx: – 1 bidirectional control endpoint – 5 IN endpoints (bulk, interrupt, isochronous) – 5 OUT endpoints (bulk, interrupt, isochronous) • For STM32L43/44/45/46xxx: – 1 bidirectional control endpoint – 7 IN endpoints (bulk, interrupt, isochronous) – 7 OUT endpoints (bulk, interrupt, isochronous)	12 configurable endpoints: • 1 bidirectional control endpoint • 5 IN endpoints (bulk, interrupt or isochronous) • 5 OUT endpoints (bulk, interrupt or isochronous)
	• Attach detection protocol (ADP) (only on STM32L4+ and STM32L47/48/49/4Axxx) • Battery charging detection (BCD)	• Attach detection protocol (ADP) • Battery charging detection (BCD)
	Independent V_{DDUSB} power supply allowing lower V_{DDCORE} while using USB	
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D+ (USB_DP) line	N/A
Mapping	• APB1 for STM32L4+ and STM32L47/48/49/4Axxx • AHB2 for STM32L14/42/43/44/45/46xxx	AHB2

Features	STM32L4/L4+	STM32U5
Buffer memory	• 1.25-Kbyte data FIFOs management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO (for STM32L4+ and STM32L47/48/49/4Axxx) • 1024 bytes of dedicated packet buffer memory SRAM (for STM32L41/42/43/44/45/46xxx)	1.25-Kbyte data FIFOs management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO
Low-power modes	• USB suspend and resume • USB revision 2.0 including link power management (LPM) support	• System stop during USB suspend • Switch-off of clock domains internal to the digital core • PHY and DFIFO power management • USB revision 2.0 including link power management (LPM) support

10 Migration of analog peripherals

10.1 Analog-to-digital converter (ADC)

The STM32U5, STM32L4 and STM32L4+ MCUs embed successive approximation ADC, which can be tightly coupled on some devices, and can operate in dual mode (ADC1 is master). Further information is available on the below table.

Table 44. ADC features of STM32L4, STM32L4+ and STM32U5 MCUs

Feature		STM32L4x1/47x/48x/49x/4Axxx		STM32L41/42/43/44/45/46xx x and STM32L4+	STM32U5	
		ADC1, ADC2	ADC3	ADC1, ADC2	ADC1, ADC2[1]	ADC4
Resolution		12 bits			14 bits	12 bits
Configurable resolution		12, 10, 8 or 6 bits			14, 12, 10, or 8 bits	12, 10, 8 or 6 bits
Single-ended inputs		X				
Differential inputs		X				N/A
Injected channel conversion						
Dual mode		Up to two ADCs can operate in dual mode: • ADC1 connected to 16 external channels and 3 internal channels • ADC2 connected to 16 external channels + 2 internal channels.	ADC3 connected to 12 external channels and 4 internal channels	Two ADCs can operate in dual mode[2]: • ADC1 connected to 16 external channels and 3 internal channels • ADC2 connected to 16 external channels + 2 internal channels.		
Oversampling	Ratio	Up to 256x			Up to 1024	Up to 256x
	Data register	16 bits			32 bits	16 bits
	Programmable data shift	Up to 8 bits shift			Right and left shift	Up to 8 bits shift
DMA support		X				
Autonomous mode		N/A				X
Number of analog watchdogs		3				

1. *Only present in STM32U59x/5Ax/5Fx/5Gx lines*
2. *Only available on STM32L4P5/Q5xx for STM32L4+ series and STM32U59x/5Ax/5Fx/5Gx for STM32U5 series.*

10.2 Digital-to-analog converter (DAC)

DAC peripherals in STM32L4, STM32L4+ and STM32U5 MCUs have identical electrical parameters and configuration options, with two differences in the new autonomous mode and double-data DMA capability for STM32U5 series:

- Autonomous mode to reduce the power consumption for the system
  The autonomous mode can be used to update the DAC output voltage in Stop mode. This allows DMA transfers to be performed when the device operates in Run, Sleep or Stop mode. The autonomous mode is supported only when the DAC is in sample-and-hold mode.
- Double-data DMA capability to reduce the bus activity
  When the DMA controller is used in normal mode, only 12-bit (or 8-bit) data are transferred by a DMA request. As the AHB width is 32 bits, two 12-bit data may be transferred simultaneously.

Table 45. DAC features in STM32L4, STM32L4+ and STM32U5 MCUs

Feature	STM32L4 (1)	STM32L4+	STM32U5
Number of instances	1(2)	1	1
Resolution	12 bits		
Dual channel	X(3)		
Output buffer	X		
I/O connection	DAC1_OUT1 on PA4 and DAC1_OUT2 on PA5(3)		
Maximum sampling time	1 Msps		
Autonomous mode	N/A		X
Double-data DMA			

1. *No DAC in the STM32L41/42xxx devices.*
2. *Two instances in STM32L4x1xx devices (one output channel each).*
3. *Only single channel on STM32L451/452/462xx devices (DAC1_OUT1 on PA4 as I/O connection).*

10.3 Comparator (COMP)

Each STM32L4, STM32L4+ and STM32U5 MCU embeds two ultra-low-power comparators, COMP1 and COMP2, with identical electrical parameters.

Comparators for STM32L4 and STM32L4+ MCUs have the same configuration options that are different from the STM32U5 MCUs: COMP1_CSR and COMP2_CSR registers are not compatible. Differences are listed in the table below.

Table 46. COMPx_CSR registers in STM32L4, STM32L4+ and STM32U5 MCUs

COMPx_CSR bit	STM32L4/L4+	STM32U5
Bit 0	EN: COMPx(1) enable	
Bits 3:2	PWRMODE[1:0]: Power mode of the comparator x	
Bits 6:4	INMSEL: Comparator x input minus selection bits	INMSEL[3:0]: COMPx signal selector for inverting input INM
Bit 7	INPSEL: Comparator x input plus selection bit	
Bits 9:8	Reserved: for COMP1_CSR Bit 9: WINMODE: Windows mode selection bit for COMP2_CSR (Bit 8: reserved)	INPSEL[1:0]: COMPx signal selector for non-inverting input
Bit 11	Reserved	WINMODE: COMPx non-inverting input selector for Window mode
Bit 14	Reserved	WINOUT: COMPx output selector
Bit 15	POLARITY: COMPx polarity selector	
Bits 17:16	HYST[1:0]: COMPx hysteresis selector	
Bits 19:18	BLANKING[2:0]: Comparator x blanking source selection bits	PWRMODE[1:0]: COMPx power mode selector
Bit 20		Bits 24:20 BLANKSEL[4:0]: COMPx blanking source selector
Bit 21	Reserved	
Bit 22	BRGEN: Scaler bridge enable	
Bit 23	SCALEN: voltage scaler enable bit	
Bit 24	Reserved	
Bit 30	VALUE: COMPx output status	
Bit 31	LOCK: COMPx_CSR register lock	

1. *x corresponds to the number of COMP instance used (1 or 2).*

There is also one difference in the new blanking sources for STM32U5 series:

- TIM3 OC3 is added as blanking source in COMP1.
- TIM3 OC4, TIM8 OC5 and TIM15 OC1 are added as blanking sources in COMP2.

10.4 Voltage reference buffer (VREFBUF)

The internal VREFBUF is an operational amplifier, with programmable gain. The amplifier input is connected to the internal voltage reference VREFINT.

The STM32U5, STM32L4, and STM32L4+ MCUs embed one VREFBUF that can be used as voltage reference for ADCs and DACs. VREFBUF can also be used as voltage reference for external components through the VREF+ pin.

The STM32U5 VREFBUF supports four voltages, when the STM32L4 and STM32L4+ MCUs support only two voltages.

Table 47. VREFBUF features in STM32L4, STM32L4+ and STM32U5 MCUs

STM32L4/L4+ (1)		STM32U5	
Symbol	Voltage (V)	Symbol	Voltage (V)
N/A		VREFUBUF0	1.5
		VREFUBUF1	1.8
VREF_OUT1	2.048	VREFUBUF2	2.048
VREF_OUT2	2.5	VREFUBUF3	2.5

1. *No VREFBUF in STM32L41/42xxx devices.*

10.5 Operational amplifier (OPAMP)

The two OPAMP1 and OPAM2 (two inputs and one output each) in STM32U5, STM32L4 and STM32L4+ devices have identical features. The three I/Os can be connected to the external pins to enable any type of external interconnections.

Each OPAMP can be configured internally as a follower or as an amplifier with a non-inverting gain ranging from 2 to 16. The positive input can be connected to the internal DAC. The output can be connected to the internal ADC.

The only difference is that the STM32U5 OPAMPs support the high-speed mode and achieves a better slew rate.

11 Migration of signal/image processing accelerators

11.1 Digital filters

The STM32U5 devices embed two hardware digital filters, MDF and ADF, while STM32L4 and STM32L4+ devices include one DFSDM filter. Differences between the embedded filters are listed in the table below.

Table 48. Digital filters in STM32L4, STM32L4+ and STM32U5 MCUs

Features	STM32L4/L4+	STM32U5	
Digital filter type	DFSDM	ADF	MDF
Number of filters	Up to 8	1	6(1)
Input from internal ADC	X(2)	N/A	X
Supported trigger sources	11/12(3)	2	14(4)
Pulses skipper	X(2)	N/A	
Autonomous in Stop mode	N/A	X(5)	X(6)

1. *Only 2 filters available for STM32U535/545*
2. *Not available for STM32L476/486xx.*
3. *LPTIM1 is the new trigger source for STM32L4+.*
4. *For available trigger sources, refer to the 'MDF/ADF trigger connections' tables in the reference manual.*
5. *Only Stop 0, Stop 1 and Stop 2 modes.*
6. *Only Stop 0 and Stop 1 modes.*

11.2 CORDIC co-processor (CORDIC)

The CORDIC co-processor is a new peripheral embedded only in STM32U5 MCUs. It provides hardware acceleration of certain mathematical functions (mainly trigonometric ones) commonly used in motor control, metering, signal processing and many other applications.

The CORDIC speeds up the calculation of these functions compared to a software implementation, making possible the use of a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

The cording main features are the following:

- 24-bit CORDIC rotation engine.
- Circular and Hyperbolic modes.
- Rotation and Vectoring modes.
- Functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm.
- Programmable precision.
- Low-latency AHB slave interface.
- Results readable as soon as ready, without polling or interrupt.
- DMA read and write channels.
- Multiple register read/write by DMA.

11.3 Filter math accelerator (FMAC)

The FMAC is only implemented on STM32U5 MCUs. This peripheral performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic that allows FMAC to index vector elements held in local memory.

The FMAC main features are the following:

- 16 x 16-bit multiplier.
- 24 + 2-bit accumulator with addition and subtraction.
- 16-bit input and output data.
- 256 x 16-bit local memory.
- Up to 3 areas in memory for data buffers (two inputs, one output) can be defined by programmable base address pointers and associated size registers.
- Circular input and output buffer.
- Filter functions: FIR, IIR (direct form 1).
- Vector functions: dot product, convolution, correlation.
- AHB slave interface.
- DMA read and write data channels.

11.4 Tough sensing controller (TSC)

The STM32U5, STM32L4, and STM32L4+ MCUs embed a touch sensing controller (TSC) with the same features. The TSC provides a simple solution to add capacitive-sensing functionality to any application. A capacitive-sensing technology can detect a finger presence near an electrode that is protected from direct touch by a dielectric (such as glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. Refer to the product reference manual for more details on TSC features.

The number of capacitive-sensing channels is dependent on the size of the package and subject to I/O availability. The TSC input/output signals and their pins mapping are partially compatible between STM32L4, STM32L4+ and STM32U5 MCUs.

12 Migration of external memory interface peripherals

12.1 Octo-SPI interface (OCTOSPI)

The OCTOSPI peripheral provides a serial interface that enables communication with external serial memories such as flash memory, PSRAM, HyperRAM™, HyperFlash™ and some specific ICs like FPGA or ASICs.

The OCTOSPI specialized communication interface targets single-, dual-, quad- or octal-SPI memories, and can be configured in three modes: Indirect, Status-polling, and Memory-mapped.

The OCTOSPI I/O manager (OCTOSPIM) is a hardware peripheral that implements a low-level interface that enables:

- an efficient OCTOSPI pin assignment with a full I/O matrix (before alternate function map), and
- a multiplex of single-, dual-, quad- and octal-SPI interfaces over the same bus.

The OCTOSPI peripheral is available on STM32L4+ and STM32U5 MCUs, with several additional features.

Note: The STM32L4 MCUs feature a QUADSPI peripheral, not an OCTOSPI. The OCTOSPI supports the same features as the QUADSPI, and additionally supports Octo-SPI memories.

Table 49. OCTOSPI features in STM32L4+ and STM32U5 MCUs

Features	STM32L4+	STM32U5
Number of OCTOSPI instances	2(1)	
Octo-SPI I/O manager (OCTOSPIM)	Yes(2)	
Single-ended clock for 3.0 V HyperBus™ mode		
Inverted clock for 1.8 V HyperBus mode	N/A	Yes
Zero wait states like performance execution		
Support of AP Memory quad-SPI and Octal-SPI PSRAMs		
CS boundary and refresh		
Full support for HyperRAM memories	Yes	
OTFDEC protecting Flash code	N/A	
TrustZone security		

1. *Single instance in STM32U535/545.*
2. *Manager is not available in STM32U535/U545.*

In addition, STM32U59x/5Ax/5Fx/5Gx features an Hexadeca-SPI interface with HW transceiver to access 16 bit memories at maximum system frequency.

12.2 Flexible static memory controller (FSMC)

The following table presents the FSMC interface differences between of STM32L4, STM32L4+, and STM32U5 MCUs.

Note: STM32L41/42/43/44/45/46xxx and STM32U535/U545xx does not support FSMC.

Table 50. FSMC features in STM32L4, STM32L4+, and STM32U5 MCUs

Features	STM32L4	STM32L4+	STM32U5
External memory interfaces	• SRAM • NOR/NAND memories • PSRAM • NAND flash memory with ECC hardware	• SRAM • NOR/NAND memories • PSRAM • NAND flash memory with ECC hardware • FRAM (ferroelectric RAM)	• SRAM • NOR flash memory/one NAND flash memory • PSRAM • NAND flash memory with ECC hardware • FRAM (ferroelectric RAM)
Data bus width	8 or 16 bits		
New timing	N/A	• NBL setup timing • Data hold timing • Clock divider ratio 1	New PSRAM counter timing

For STM32U5 MCUs, FSMC registers can be configured as secure through the TZSC controller.
Refer to the reference manual for more details.

13 Software migration

13.1 Reference documents

- Definitive guide to Cortex-M33 and Cortex-M4 processors
- *STM32 Cortex-M4 MCUs and MPUs programming manual* (PM0214)
- Cortex-M4 processor Technical Reference Manual
- Cortex-M33 processor Technical Reference Manual

13.2 Cortex-M4 and Cortex-M33 overview

13.2.1 STM32 Cortex-M4 processor and core peripherals

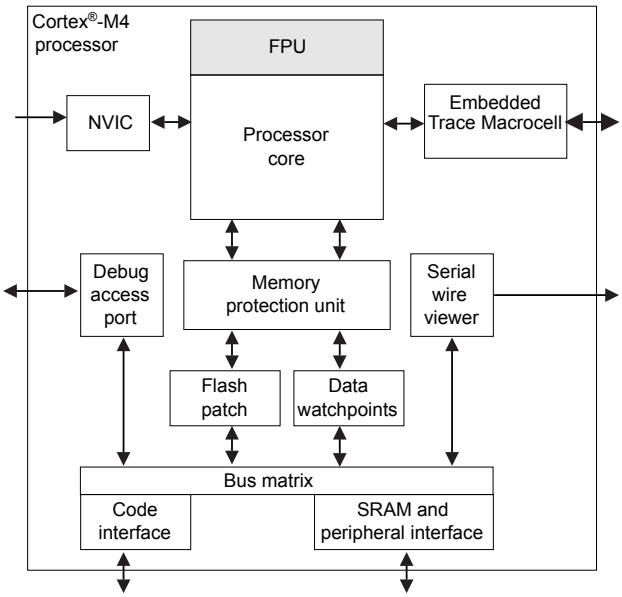
The Cortex-M4 processor is a high-performance 32-bit processor designed for the microcontroller market. It offers significant benefits to the developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system and memories
- Ultra-low power consumption with integrated sleep modes
- Platform security robustness, with integrated memory protection unit (MPU)

The Cortex-M4 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers an exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754- compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, a saturating arithmetic and dedicated hardware division.

The STM32 Cortex-M4 implementation is illustrated in the figure below.

Figure 8. STM32 Cortex-M4 implementation



Cortex-M4 key features

- Architecture 32 bits RISC Armv7E-M
- 3-stage pipeline with branch speculation
- Instruction set:
  - Thumb, Thumb-2
  - Hardware multiply, hardware divide, saturated arithmetic
  - DSP extensions:
    - Single-cycle 16/32-bit MAC
    - Single-cycle dual 16-bit MAC
    - 8/16-bit SIMD arithmetic
- FPU (VFPv4-SP)

13.2.2 STM32 Cortex-M33 processor and core peripherals

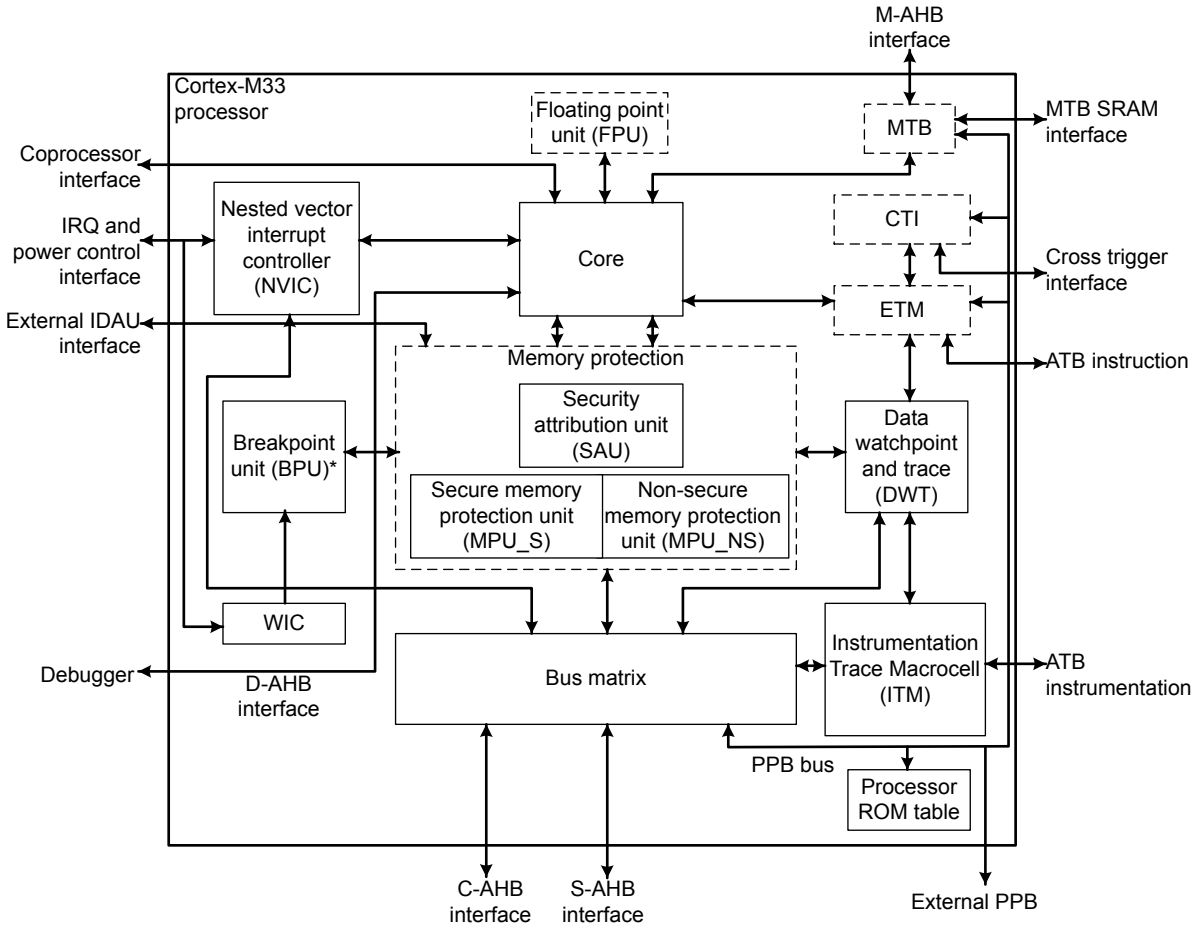
The Cortex-M33 processor is excellence in ultra-low-power, performance and security.

This processor is based on the Armv8-M architecture for use in environments requiring more security implementation. The Cortex-M33 core implements a full set of DSP (digital signal processing) instructions, TrustZone-aware support and a memory protection unit (MPU) that enhances the application security.

The Cortex-M33 core also features a single-precision floating-point unit (FPU), that supports all the Arm single precision data-processing instructions and all the data types.

STM32 Cortex-M33 implementation is illustrated in the figure below.

Figure 9. STM32 Cortex-M33 implementation



* Flash patching is not supported in the Cortex-M33 processor.

Cortex-M33 key features are listed below:

- Arm-v8M architecture with 2/3 stage pipeline, Harvard, 1,4 DMIPS/MHz
- Single-cycle branch, no branch prediction
- Hardware divide instruction
- Debug (CoreSight compliant)
- Memory exclusive instructions
- NVIC without interrupts increased up to 480 max (256 priority levels)
- Enhanced MPU, more flexible (32 bytes) up to 16 regions (for each one of the secure and non-secure states)
- New AMBA® 5 AHB interface, support of security state extension to the system
- Support of external implementation defined attribution unit
- Fully compatible with TrustZone system

The differences between Cortex-M4 and Cortex-M33 are presented in the table below.

Table 51. Cortex-M4 versus Cortex-M33

Feature	Cortex-M4	Cortex-M33
Instruction set architecture	Armv7-M	Armv8-M mainline
	Thumb, Thumb-2	
Pipeline	Three-stages	
Performance efficiency (CoreMark/MHz)	3.40	3.86
DMIPS/MHz	1.25	1.50
Memory protection	Yes	
Maximum MPU regions	8	8 secure and 8 non-secure
Trace (ETM or MTB)	ETMv3	MTB and/or ETMv4
DSP	Yes	
Floating point hardware		
Bus protocol	AHB Lite, APB	AHB5
Max. number of external interrupts	240	480
CMSIS support	Yes	
TrustZone for Armv8-M	No	Yes
Coprocessor interface		

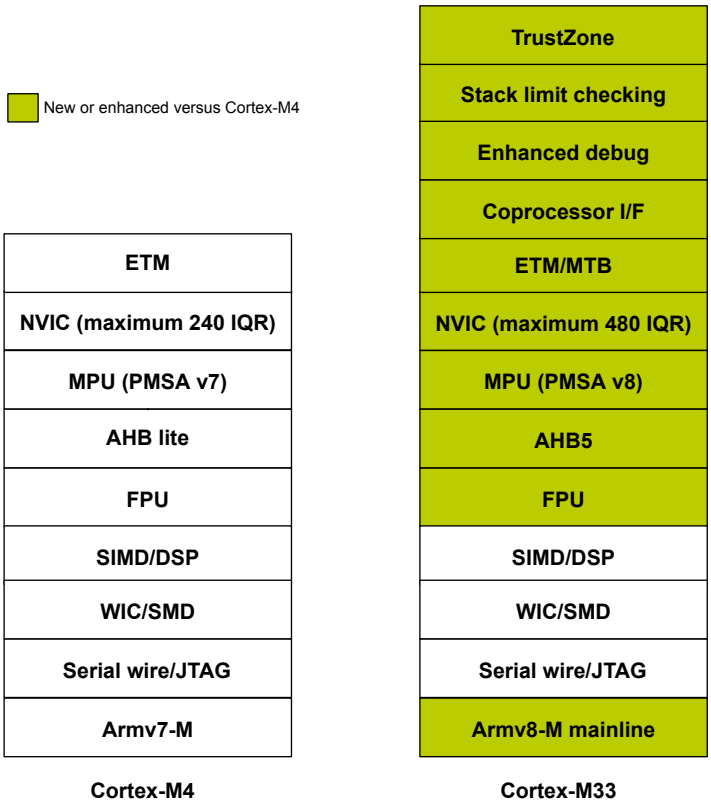
13.2.3 Software point of view

The Cortex-M33 has the same features than the Cortex-M4, but includes also the following ones:

- Implementing Armv8-M architecture
- Implementing the latest floating point unit FPU specification (based on Arm FPv5 architecture) that adds more instructions than the Cortex-M4 has
- AHB5 specification used for the system and memory interface, to extend security across the whole system
- Latest version of the memory protection unit (MPU) specification used to simply the setup of regions
- Extended number of maximum interrupts to 480
- Optional execution trace using MTB or ETM
- Enhanced debug components to make simplify usage
- Coprocessor interface supporting up to 8 coprocessors units
- Hardware stack limit checking
- TrustZone security features adding efficient security features

The Cortex-M33 enhancements compared to Cortex-M4 are illustrated in the figure below.

Figure 10. Cortex-M33 enhancements versus Cortex-M4



13.3 Cortex mapping overview

The mapping is different on the Cortex®-M4 and the Cortex®-M33, as shown in the table below.

Table 52. Cortex mapping for STM32L4, STM32L4+ and STM32U5 MCUs

Feature		STM32L4 and STM32L4+	STM32U5
Core	Architecture	Cortex®-M4	Cortex®-M33
	NVIC	Maskable interrupt channel: • 95 (STM32L4+) • 91 (STM32L49/4Axxx) • 82 (STM32L47/48xxx) • 67 (STM32L41/42/43/44/45/46xxx)	125 maskable interrupt channels (not including the 16 Cortex-M33 with FPU interrupt lines)
	EXTI	• Up to 41 events/interrupts (STM32L4+ and STM32L49/4Axxx) • Up to 40 events/interrupts (STM32L47/48xxx) • Up to 37 events/interrupts (STM32L41/42/43/44/45/46xxx)	23 events/interrupts
Mapping	System timer	0xE000 E010 to 0xE000 E01F	0xE000 E010 to 0xE000 E0FF
	NVIC	0xE000 E100 to 0xE000 E4EF	0xE000 E100 to 0xE000 ECFF
	Floating point unit	0xE000 EF30 to 0xE000 EF44	0xE000 EF30 to 0xE000 EF44
	MPU (memory protection unit)	0xE000 ED90 to 0xE000 EDB8	0xE000 ED90 to 0xE000 EDB8

Revision history

Table 53. **Document revision history**

Date	Version	Changes
20-Apr-2021	1	Initial release.
11-May-2023	2	Updated: • the document title. • Section Introduction • Section 2 STM32U5 series overview • Section 2.1 Main features • Section 2.2 System architecture • Section 3 Hardware migration • Section 5.1 STM32 products cross-compatibility • Section 5.2 Memory mapping • Section 6.1 System configuration controller (SYSCFG) • Section 6.2 Embedded flash memory (FLASH) • Section 6.3 SRAMs • Section 6.6 Reset and clock control (RCC) • Section 6.6.1 Performance versus VCORE ranges • Section 6.7 Power controller (PWR) • Section 9.3 Universal synchronous/asynchronous receiver transmitter (USART) • Section 9.8 Universal serial-bus interface (USB) • Section 10.1 Analog-to-digital converter (ADC) • Section 12.1 Octo-SPI interface (OCTOSPI) • Section 12.2 Flexible static memory controller (FSMC) • Section 13.3 Cortex mapping overview • Section 6.4 Instruction and data caches (ICACHE/DCACHE) • Section 6.6.3 Peripheral clock configuration • Section 11.1 Digital filters • Section 9.6 Secure digital input/output MultiMediaCard interface (SDMMC) Added the following sections to this document: • Section 1 General information • Section 2.3 Memory availability Added the STM32U5 series. Applied minor changes to the whole document. Removed the conclusion section.

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