Guidelines for PCB design on BlueNRG-LP/BlueNRG-LPS/STM32WB0 MCUs

Introduction

The BlueNRG-LP, BlueNRG-LPS, STM32WB0 series are ultra-low power Bluetooth® Low Energy (Bluetooth LE) 2.4 GHz RF transceivers with a Cortex-M0+ microcontroller compliant with Bluetooth specification v5.4. These devices are suitable to implement applications compliant with Bluetooth Low Energy SIG specifications.

Bluetooth Low Energy technology operates in the same spectrum range (2400 - 2483.5 MHz, ISM band) as classical Bluetooth technology, but uses a different set of channels. Bluetooth Low Energy technology has 40 channels (37 data channels + 3 advertising channels) of 2 MHz band. Two modulation schemes are defined. The mandatory modulation scheme (1 Msym/s) uses a shaped, binary FM to minimize the transceiver complexity. The symbol rate is 1 Msym/s. An optional modulation scheme (2 Msym/s) is similar but uses a symbol rate of 2 Msym/s. The maximum transmit power is 10 mW (10 dBm).

Further details are given in volume 6 part A of the Bluetooth Core specification v5.1 or later.

The BlueNRG-LP/STM32WB07xC/STM32WB06xC devices are provided in three different packages:

1. VFQFPN48
2. WLCSP49
3. VFQFPN32

The BlueNRG-LPS/STM32WB05xZ/STM32WB09xE devices are provided in two different packages:

1. VFQFPN32
2. WLCSP36

ST provides all necessary source files (reference designs) for users that want to speed up their development.

This application note aims to accompany the reference designs of the application boards and provide detailed information regarding the design decisions adopted within STMicroelectronics designs. In addition, it details the design guidelines to develop a generic radio frequency application using these devices.

The RF performance and the critical maximum peak voltage, spurious and harmonic emission, receiver matching strongly depend on the PCB layout as well as the selection of the matching network components.

For the optimal performance, STMicroelectronics recommends the use of the PCB layout design hints described in the following sections. Furthermore, STMicroelectronics strongly suggests to use the BOM defined in the reference design, BOM that guarantees, with a good PCB design, the correct RF performance.

For further information, visit the STMicroelectronics web site www.st.com.

1 General information

The STM32WB0 are Arm® Cortex® core-based microcontrollers.

For more information on Bluetooth®, refer to http://www.bluetooth.com.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

References

[1] BlueNRG-LP Datasheet (DS13282)
[2] BlueNRG-LPS Datasheet (DS13819)
[3] STM32WB05xZ Datasheet (DS14591)
[4] STM32WB07xC, STM32WB06xC datasheet (DS14676)
[5] STM32WB09xE datasheet (DS14210)

2 Two or more layers application board

Different approaches can be taken when an application board is designed:

1. Two layers solution
2. More layers solution

2.1 Two layers solution

When it is possible to route all the tracks on two layers and a cheaper solution is requested, a two layers application board can be designed.

Figure 1. Two layers application board stack-up

The suggested thickness of the board is 600 µm or lower. Design of a two layer board should not exceed 800 µm thickness.

The two layers board has to be distributed as follows:

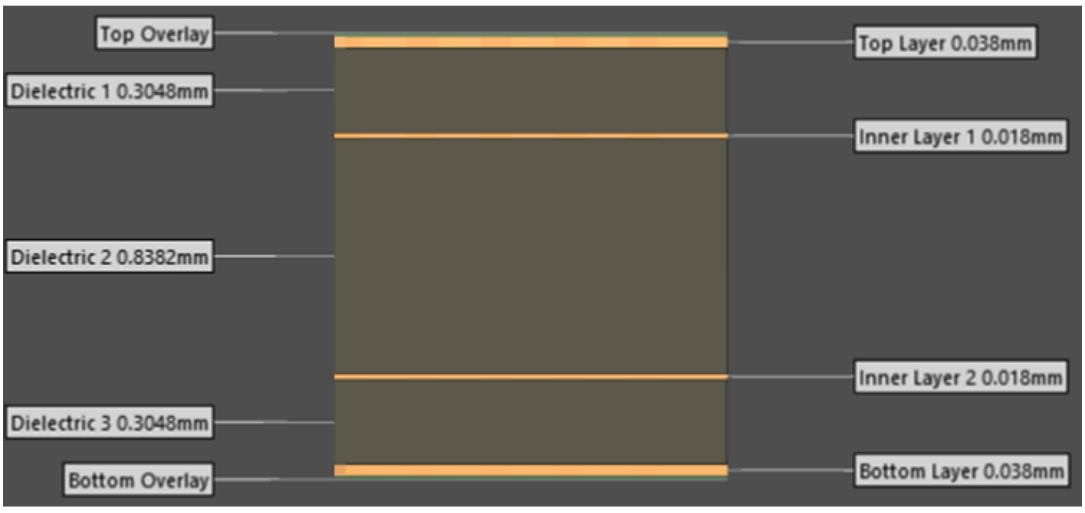
1. TOP layer: used for RF signal and routing
2. BOTTOM layer: used for grounding under the RF zones and for routing in the other part

The two layers solution is indicated for the QFPN package.

2.2 More layers solution

When it is not possible to route all the tracks on two layers and/or a cheaper solution is not requested, a more layers application board can be designed. This is the case, for example, for the WLCSP package where a four or more layers solution is suggested. See Figure 2. Four layers application board stack-up.

Figure 2. Four layers application board stack-up



Four layers usually address thicker boards (1.6 mm). Depending on the technology selected, like in WLCSP package, thinner boards are required.

The four/more layers board has to be distributed as follows:

1. TOP layer: used mainly for RF signal and routing
2. GROUND layer: used for grounding under the RF zones
3. INNER and BOTTOM layers: used to route the low frequency tracks

3 Matching network

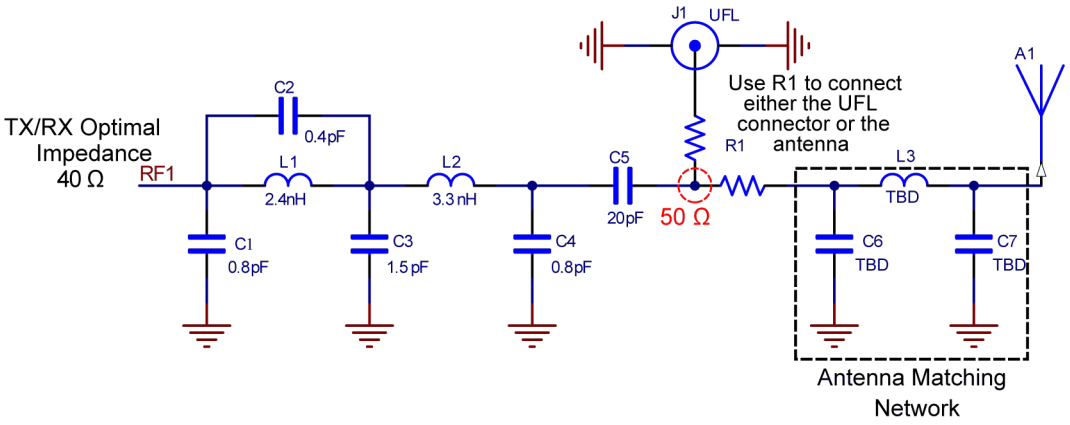
The schematic below reports the suggested matching network. It presents the optimal impedance for TX and RX performances and guarantees the harmonics filtering for TX power up to the maximum level achievable by BlueNRG-LP, BlueNRG-LPS, STM32WB0 devices. It is composed of two cascaded pi networks with a notch filter for 2nd harmonic suppression that can be tuned adjusting the value of C2. The capacitor C5, placed at the end, is mandatory and cuts any DC current.

The optimal impedance to be presented to the BlueNRG-LP, BlueNRG-LPS, STM32WB0 devices is 40 Ω and represents the right trade-off for Tx and Rx performance. The matching network transforms this optimal impedance into 50 Ω.

Two resistor footprints with overlapping pads can be used to realize a selector for either the antenna or a coaxial connector placed on the board, avoiding stubs that de-tune the network.

A pi-network for antenna matching is usually foreseen and can be used to compensate de-tuning factors like the surrounding materials.

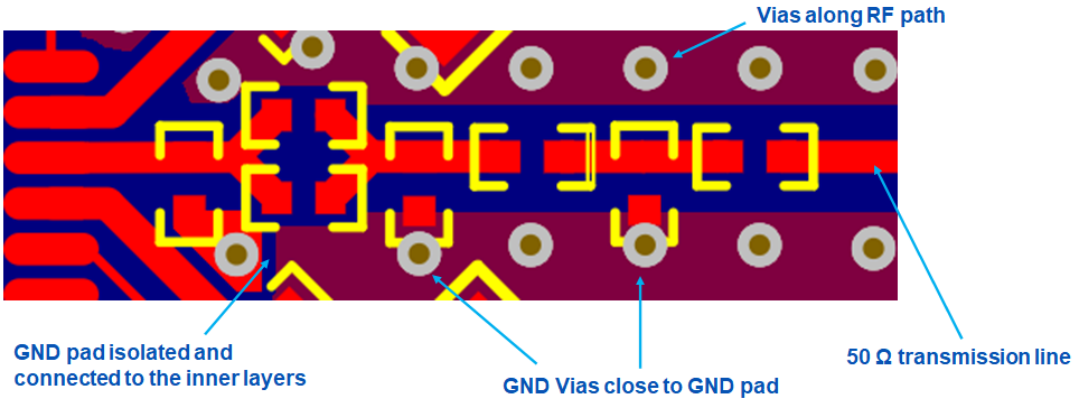
Figure 3. Matching network schematic



The reference matching network layout is shown below and some placement suggestions are also reported:

- Use a coplanar waveguide structure.
- It is highly recommended to place the first shunt capacitor as close as possible to the RF pin and isolate the GND pad from the top layer ground. Connect it to the inner layers to improve harmonic rejection.
- When necessary, taper the track from the RF pin to the first shunt capacitor to minimize discontinuities in the track width.
- Place at least one GND via close to each capacitor ground pad. Put vias along the RF path.
- Use 0201 or 0402 SMD components.
- Ensure 50 Ω transmission line after the matching network.

Figure 4. **Matching network layout**

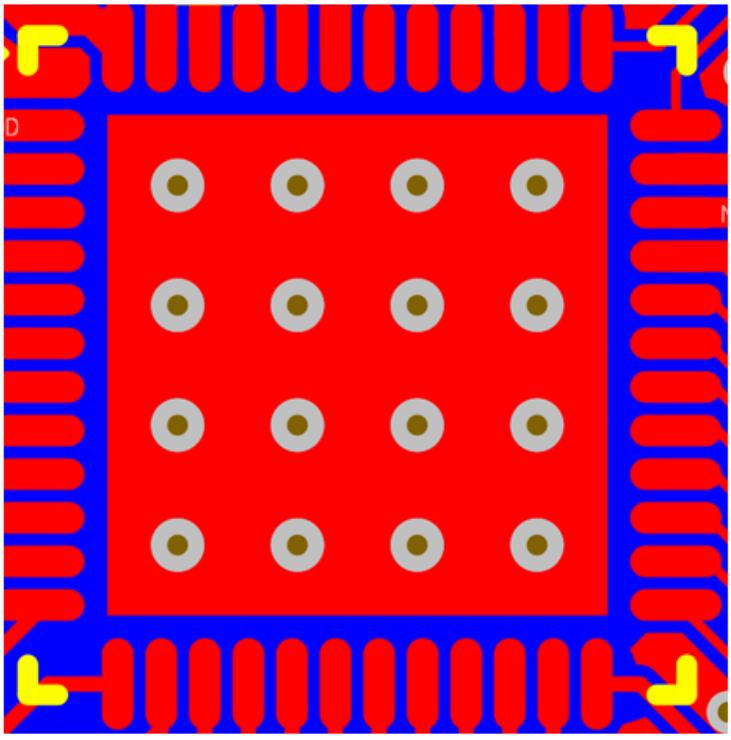


4 Layout recommendations

The layout recommendations to follow during the development of a product based on the BlueNRG-LP, BlueNRG-LPS, STM32WB0 devices are reported below:

- Put power supply decoupling capacitors as close as possible to VDD pins in order to reduce parasitic effects. Always put the smallest capacitor first. Where possible, put more than one via close to the ground pad of the decoupling capacitor
- Ensure an uninterrupted ground area under the RF part and the decoupling capacitors in order to guarantee the shortest return path for high frequency currents
- When the SMPS is used, care must be taken in the layout of the external components in order to minimize the noise and unwanted couplings with the RF line (see Section 5.4: SMPS layout examples for layout suggestions)
- Minimize series parasitic inductance between ground pours of different layers putting as many stitching vias as possible
- Create a ring of stitching vias along the edges of the board to reduce radiation due to fringing fields
- Ensure optimum connection of the exposed pad of the QFPN48 and QFPN32 to the other ground layers. Use at least a 4x4 matrix of ground vias (see Figure 5. BlueNRG-LP/STM32WB07CC/STM32WB06CC VFQFPN48 exposed pad)
- The high-speed external crystal should be placed as close as possible to the OSCIN and OSCOUT pins to minimize wire parasitic capacitances and frequency shift
- Avoid any routing under the high-speed crystal and close to OSCIN and OSCOUT pins
- No high-speed crystal external load capacitors are necessary. The frequency tuning is performed exploiting the internal tuning network made by a fixed capacitor + 6 binary weighted switchable ones. The effective range of loading capacitors are programmable through an internal register. The programmable register and the capacitor range are reported in the BlueNRG-LP, BlueNRG-LPS, STM32WB0 devices datasheets.
- When possible, reserve the inner layers for most of the routing.

Figure 5. BlueNRG-LP/STM32WB07CC/STM32WB06CC VFQFPN48 exposed pad



5 Layout examples

The layout of different packages of the BlueNRG-LP, BlueNRG-LPS, STM32WB0 devices with the external components are presented. The proposed layouts cover two and four layer boards.

Figure 6. BlueNRG-LP/STM32WB07CC/STM32WB06CC VFQFPN48 - 2 layers

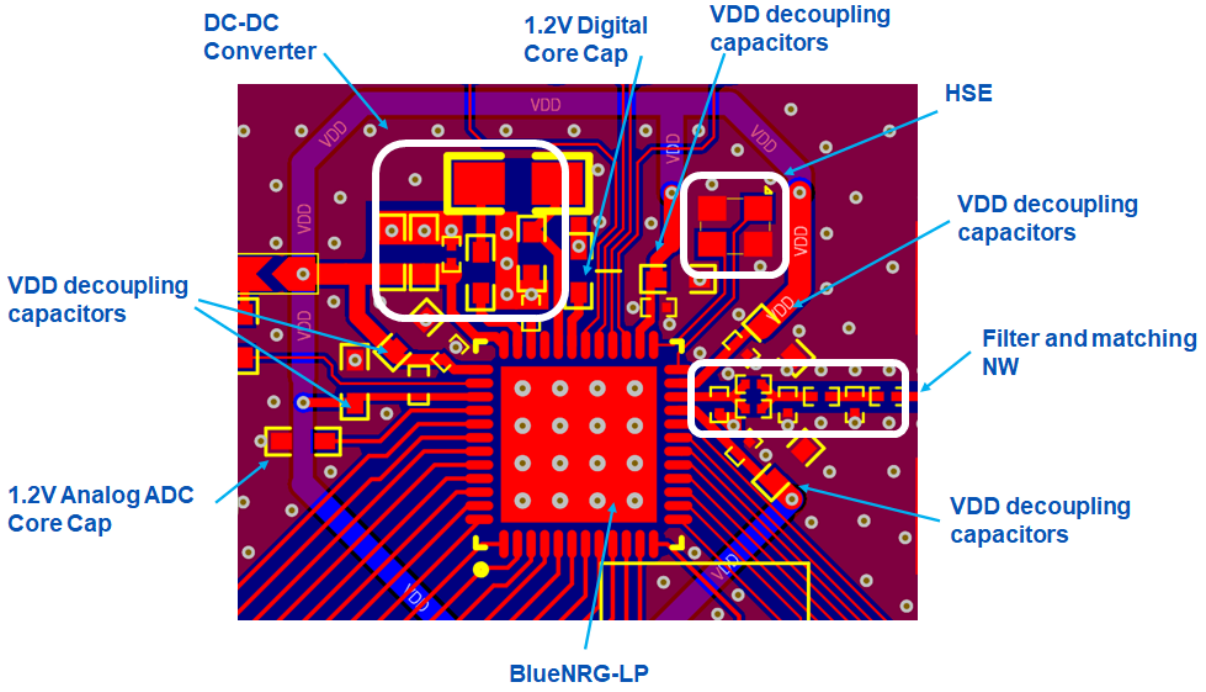


Figure 7. BlueNRG-LPS/STM32WB05KZ and STM32WB09KE VFQFPN32 - 4 layers

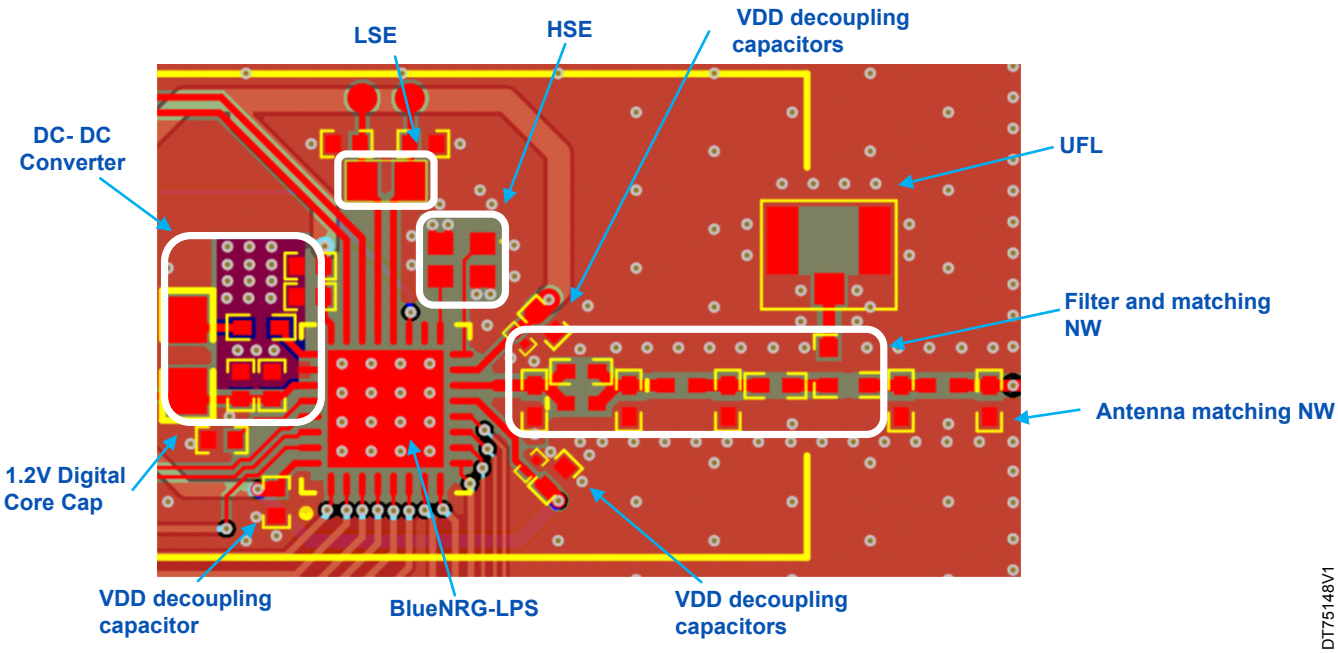
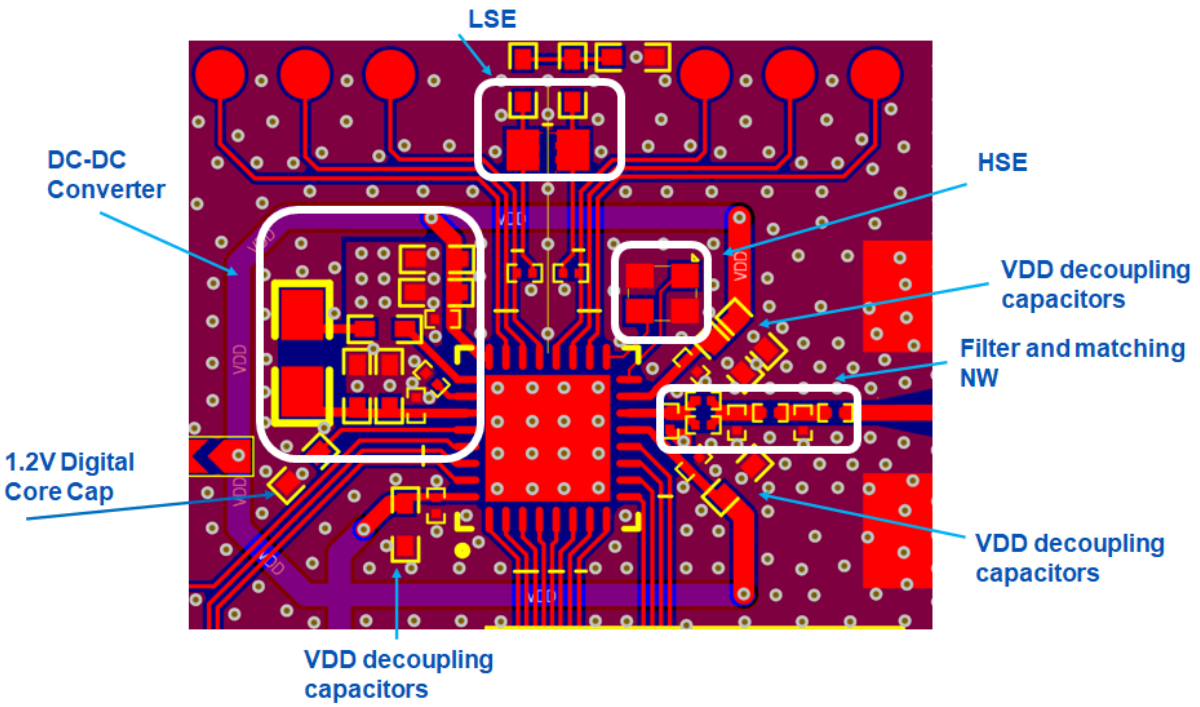


Figure 8. **BlueNRG-LPS/STM32WB05KZ and STM32WB09KE VFQFPN32 - 2 layers**



5.1 BlueNRG-LP/STM32WB07CC/STM32WB06CC WLCSP49 routing

The layout of the BlueNRG-LP/STM32WB07CC/STM32WB06CC WLCSP49 is more complex than QFPN. The BlueNRG-LP/STM32WB07CC/STM32WB06CC devices need four layers to route out all the signals. More layers, different technologies, and PCB classes can be used according to manufacturing capabilities and the cost.

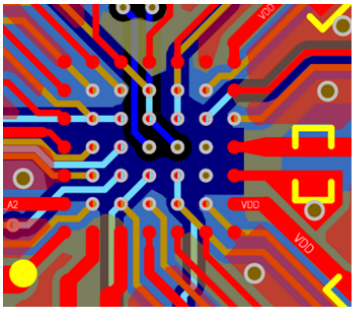
A solution is presented below by using in pad stacked micro vias.

Maximum micro via aspect ratio is 1:1. Considering a via hole size of 100 um, a board 400um thick allows building stacked vias as represented below.

A thicker board needs more advanced HDI technology.

When the application does not requires all the signals, one level of micro via could be enough, reducing the cost of the board.

Figure 9. **BlueNRG-LP/STM32WB07CC/STM32WB06CC WLCSP49 balls routing and stackup**



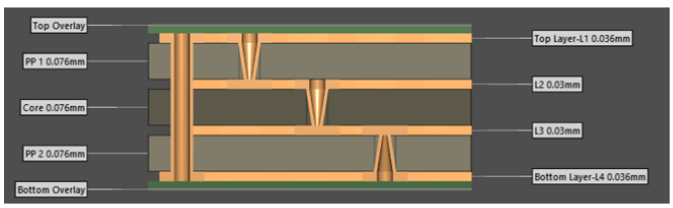
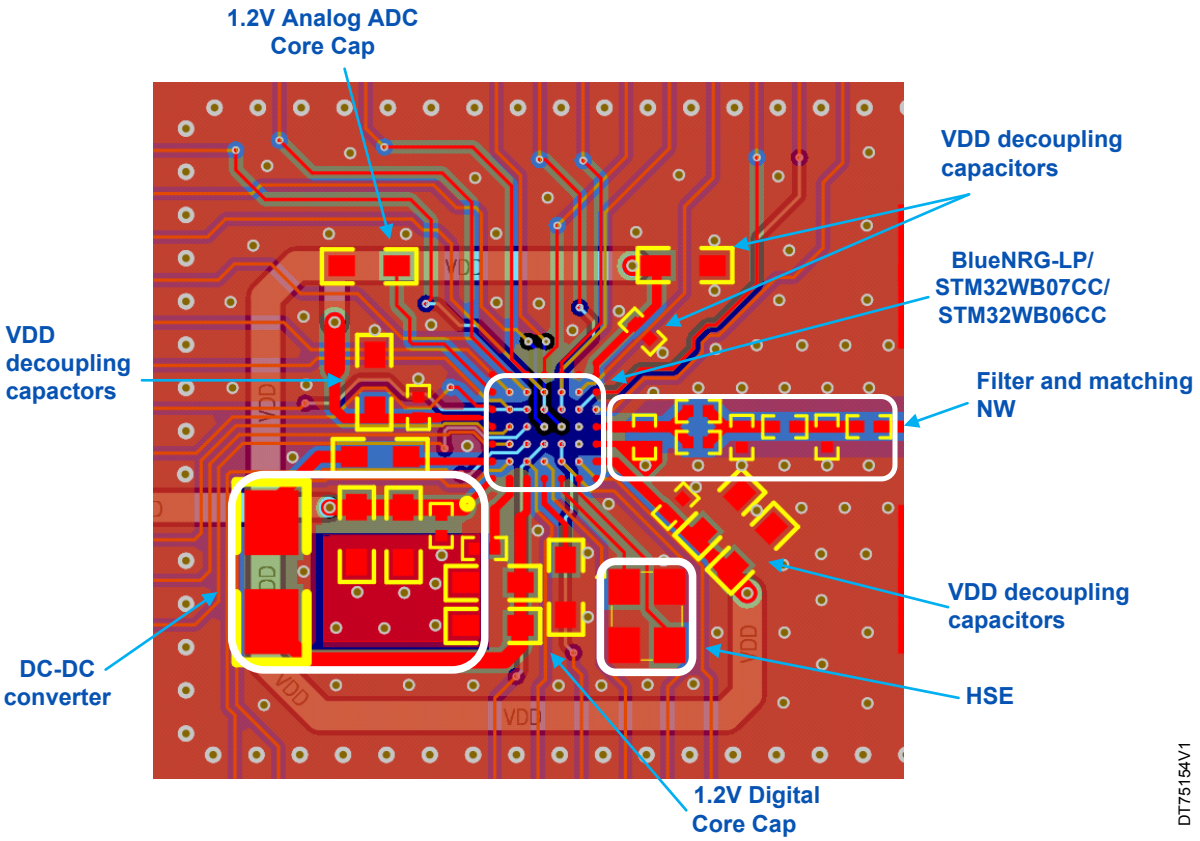
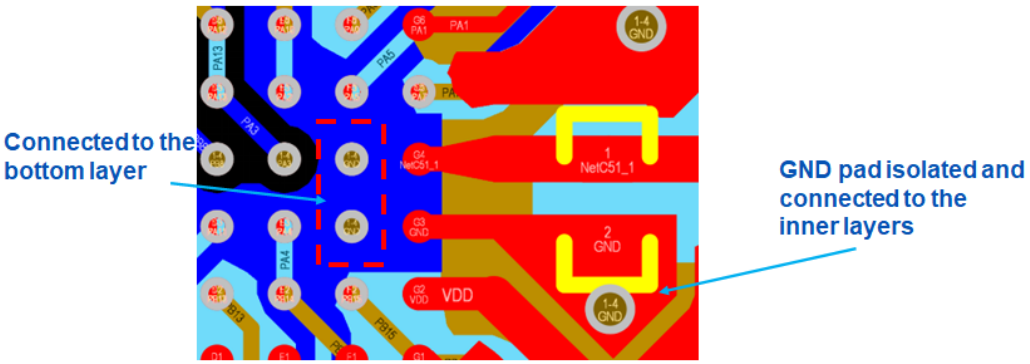


Figure 10. **BlueNRG-LP/STM32WB07CC/STM32WB06CC WLCSP49 4 layers**



It is suggested that VSSRF and VSSIFADC are directly linked to the bottom layer and not to the top layer ground pour.

Figure 11. **BlueNRG-LP/STM32WB07CC/STM32WB06CC VSSRF and VSSIFADC connection**



5.2 BlueNRG-LPS/STM32WB05TZ WLCSP36 routing

Figure 12. **BlueNRG-LPS/STM32WB05TZ WLCSP36 – 4 layers**

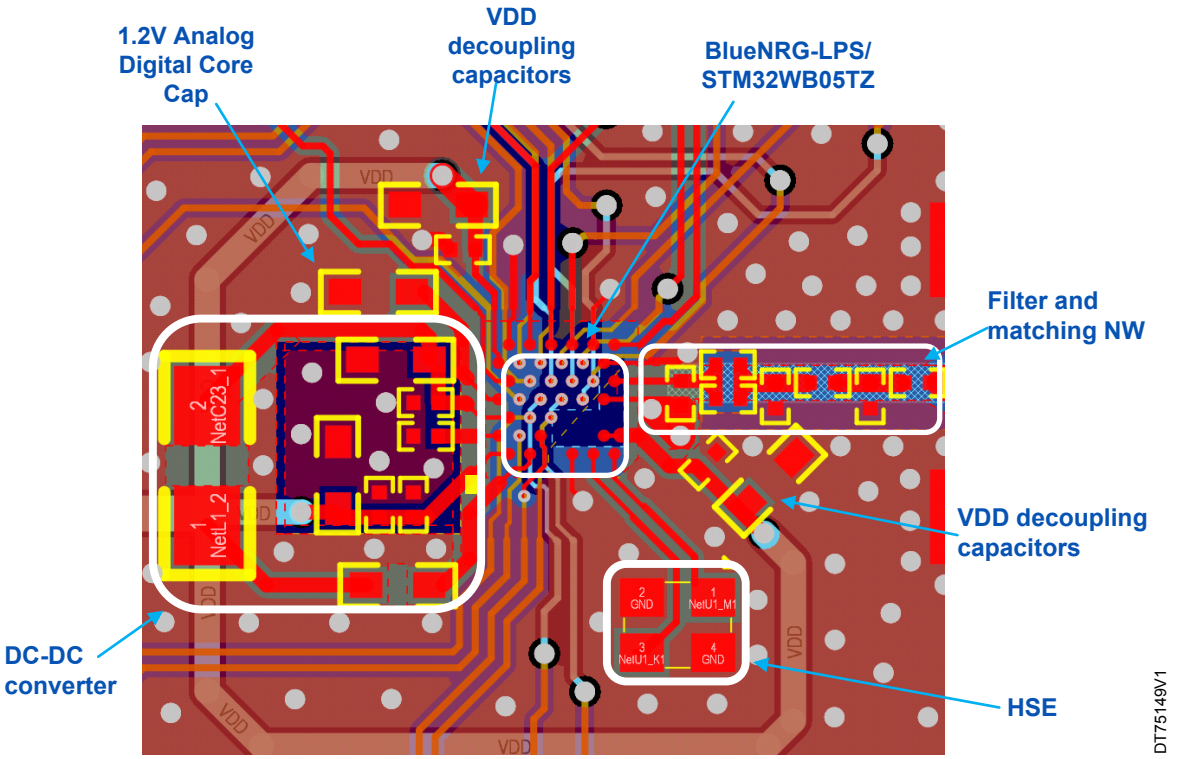
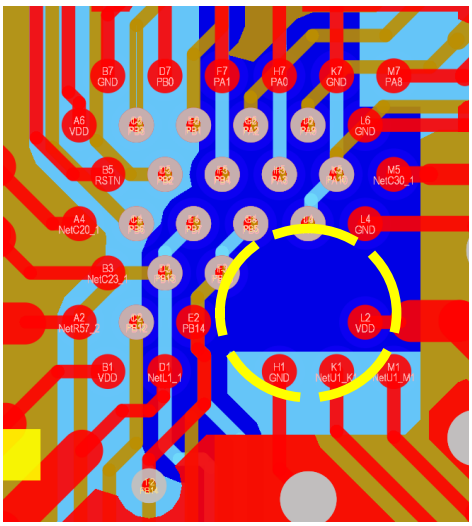


Figure 13. **BlueNRG-LPS/STM32WB05TZ WLCSP36 balls routing**



The area bounded by the yellow circle needs to be kept free to minimize the coupling with internal RF components and avoid unwanted leakage of electromagnetic radiation.

It means that routing is not allowed in this area and it is suggested to remove copper from Top, Mid1 and Mid2 layers

5.3 STM32WB09TE WLCSP36 routing

Figure 14. **STM32WB09TE WLCSP36 – 4 layers**

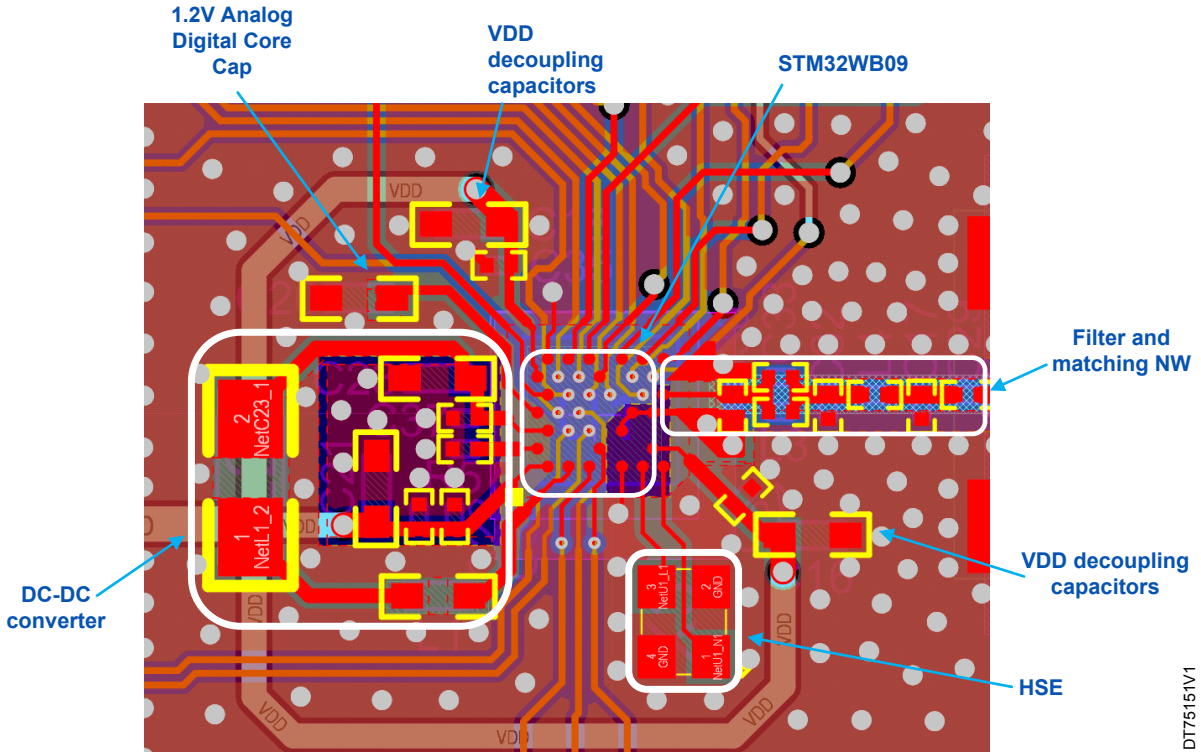
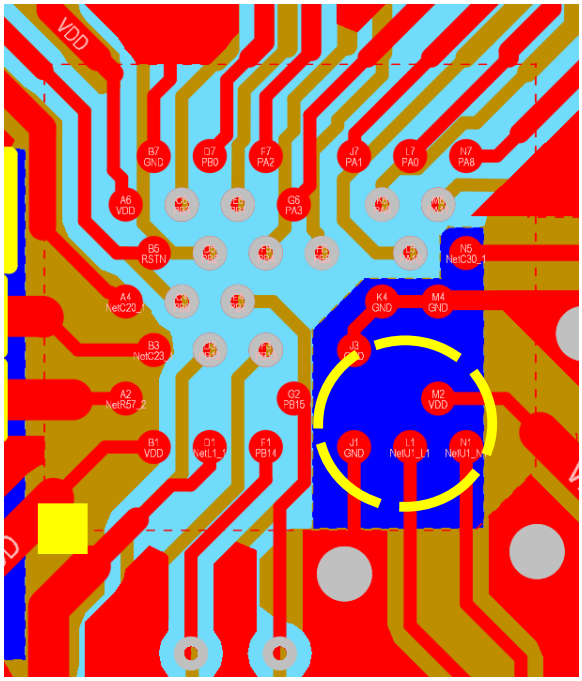


Figure 15. **STM32WB09TE WLCSP36 balls routing**



The balls arrangement enables routing every signal using only one level of microvias. The area bounded by the yellow circle needs to be kept free to minimize the coupling with internal RF components and avoid unwanted leakage of electromagnetic radiation. It means that routing is not allowed in this area and it is suggested to remove copper from Top, Mid1 and Mid2 layers. J3, K4, and M4 are connected to the top layer.

5.4 SMPS layout examples

The DC-DC converter area is very sensitive and it is necessary to pay attention to the layout of this part. This is because the DC-DC converter generates noise that can get coupled on a surrounding ground. Moreover, the high frequency components can couple onto the RF part reducing the sensitivity.

The general strategy is to make the switching current loop small and isolate the nodes carrying the noisy current. Most of the switching current is drained by the DC-DC converter input capacitor.

To ensure a correct layout, it is necessary to:

1. Provide efficient filtering by placing capacitors as close as possible to the BlueNRG-LP, BlueNRG-LPS, STM32WB0 devices.
2. Reduce parasitic inductance ensuring wide and short connections to the BlueNRG-LP, BlueNRG-LPS, STM32WB0 devices.
3. Use a smaller inductor (L1) in series to the power inductor (L2) (see Figure 16. SMPS schematic) to improve noise filtering. In particular, L1 filters the high frequency components generated by the SMPS that fall inside the Bluetooth LE band. If possible, put the two inductors orthogonal to each other to reduce the mutual coupling.

Figure 16. SMPS schematic

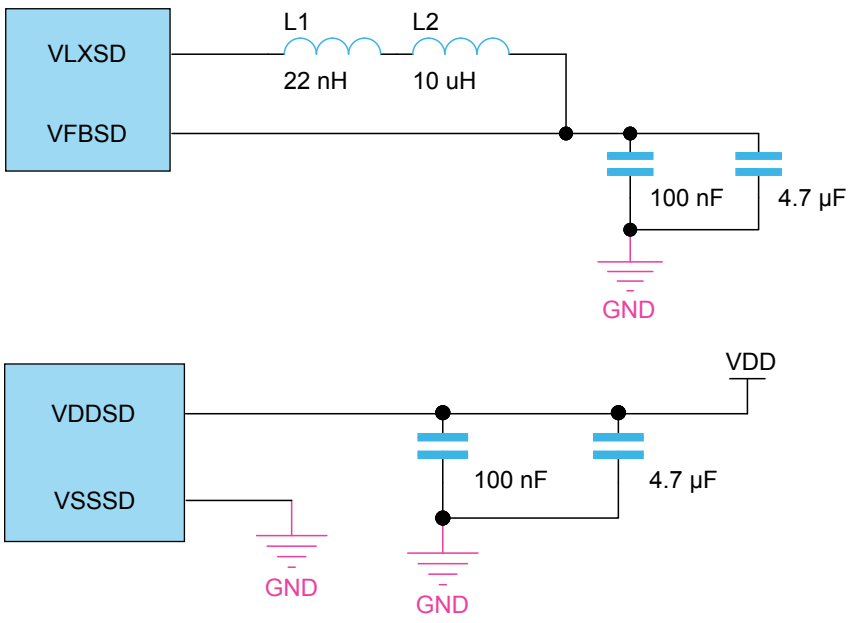


Figure 17. **BlueNRG-LPSTM32WB07CC/STM32WB06CC VFQFPN48 SMPS layout**

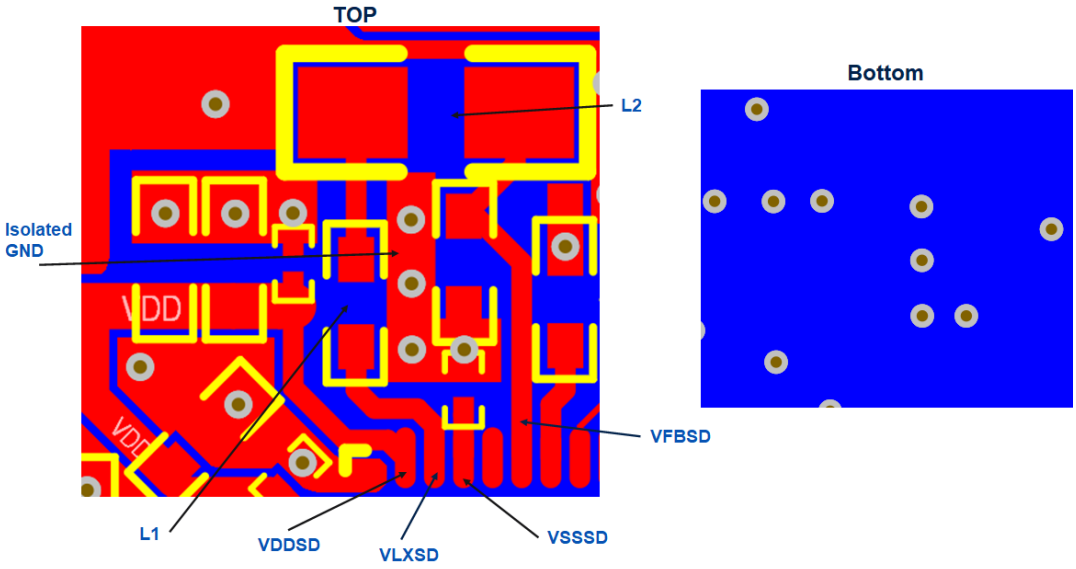


Figure 18. **BlueNRG-LP STM32WB07CC/STM32WB06CC WLCSP49 SMPS layout**

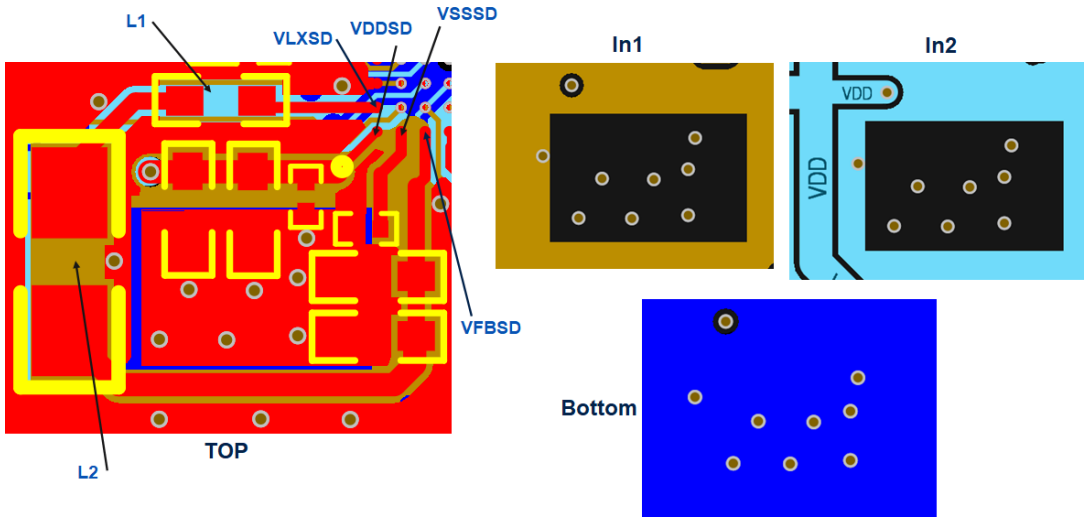
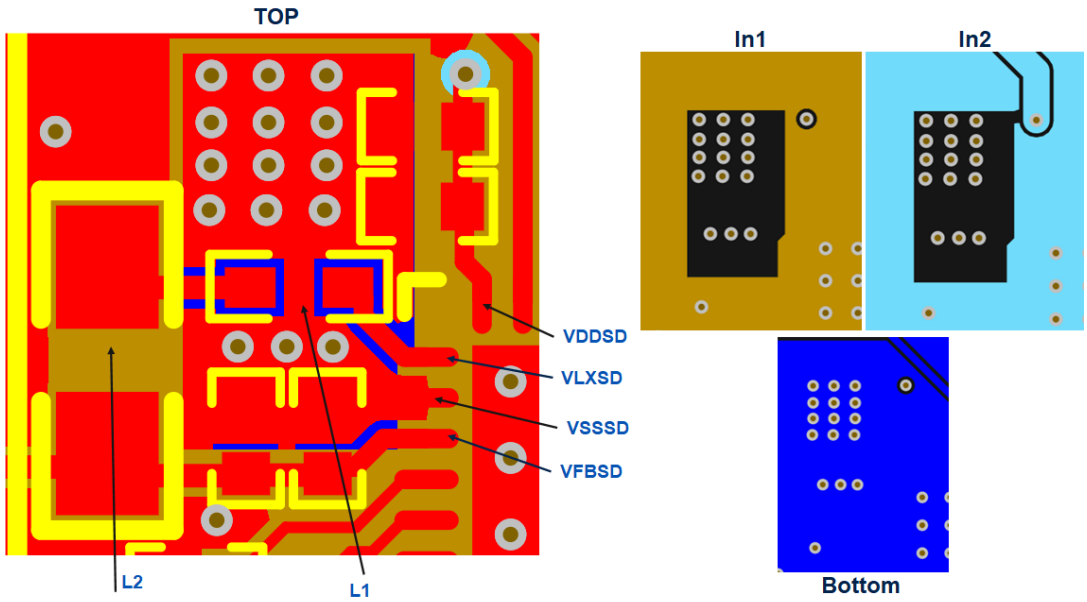


Figure 19. **BlueNRG-LPS/STM32WB05KZ and STM32WB09KE VFQFPN32 SMPS layout**



Revision history

Table 1. **Document revision history**

Date	Version	Changes
24-Jul-2020	1	Initial release.
15-Sep-2020	2	Updated Section Introduction.
13-Jun-2022	3	Added references to the BlueNRG-LPS and related PCB design guidelines. Updated Figure 1. BlueNRG-LP QFN48 application board schematic, Figure 2. BlueNRG-LP WLCSP49 application board schematic, Figure 4. Two layer application board stack-up, Figure 5. Four layer application board stackup. Added Section 3 Matching network, Section 4 Layout recommendations, Section 5 Layout examples, Section 5.1 BlueNRG-LP WLCSP routing, Section 5.2 SMPS layout examples.
18-Jun-2024	4	Added the STM32WB0 series reference throughout the document.

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