SLLIMM high power 650 V, 50 A for industrial application

Introduction

The STPOWER SLLIMM (small low-loss intelligent molded module) high power is the new family of compact, high efficiency, dual-in-line intelligent power modules, with optional extra features, offering an all-in-one solution that increases efficiency and reliability.

This new family expands the existing SLLIMM product portfolio, approaching higher power level required by applications such as: heating, ventilation and air conditioning (HVAC), general purpose inverter (GPI) and servo motor.

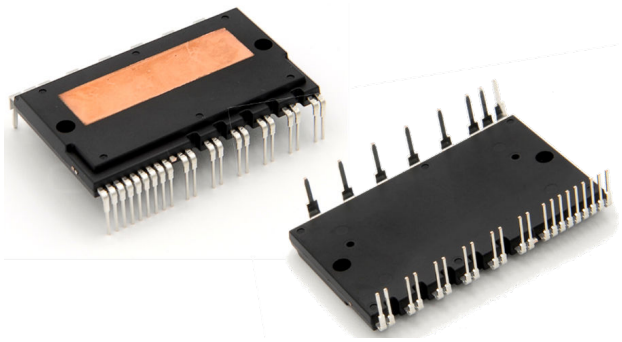
The new IPM family is available in fully isolated direct bonded copper (DBC) substrate based on transfer mold package and includes several features to enhance system reliability, such as temperature sensing, overcurrent protection, fault detection and undervoltage lockout.

Features:

- 650 V, 50 A, 3-phase inverter configuration
- Compact and fully isolated package using DBC substrate for improved thermal behavior
- Isolation voltage rating of 2500 V_{RMS}/min
- Short-circuit rugged IGBTs in trench-gate field stop (TFS) technology for efficiency improvement
- Soft recovery diodes for low EMI
- 175 °C maximum junction temperature of power chips
- Built-in bootstrap diodes
- Built-in NTC thermistor for an accurate temperature monitoring
- Separate open emitter outputs
- Comparator for fault protection against overcurrent and short-circuit
- Shutdown input/fault output
- Undervoltage lockout for power supplies and bootstrap voltage

The aim of this application note is to provide a detailed description of the new product, providing the guidelines to the motor drive designers for an efficient, reliable, and fast design when using the high power SLLIMM family.

Figure 1. SLLIMM high power package



1 Product definition

The SLLIMM high power has been designed to satisfy requirements such as low-power dissipation, high thermal performance, low EMI, high reliability in a minimized package. This has been achieved thanks to new trench-gate field stop (TFS) IGBT and fast recovery diode (FRD) technologies, new IC gate drivers and improved direct bonded copper (DBC) substrate based on transfer mold package.

1.1 Product synopsis

The SLLIMM high power targets a wide variety of industrial applications such as:

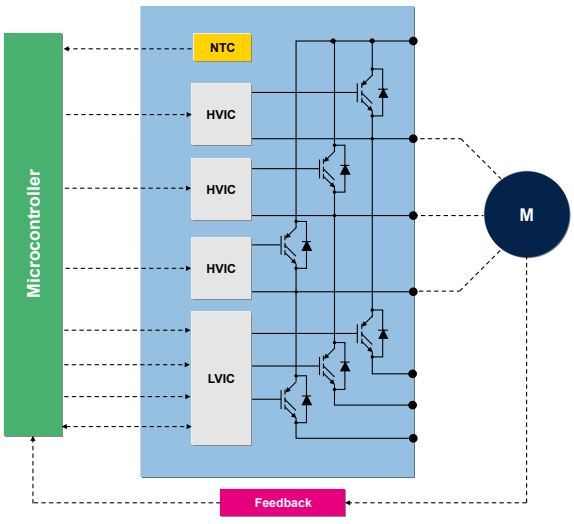
- Heating, ventilation and air conditioning (HVAC)
- General purpose inverter (GPI)
- Servo motor

The main features and integrated functions can be summarized as follows:

- 650 V, 50 A rating
- 3-phase IGBT inverter bridge including:
- – Six short-circuit protected IGBTs
  – Six fast recovery diodes (FRDs)
- Three built-in bootstrap diodes
- Three single HVIC gate drivers for high-side section, including following feature:
  – Undervoltage lockout on V_{CC} and V_{BOOT}
- One triple LVIC gate driver for low-side section with extra features:
  – Shutdown input/fault output
  – Comparator for fault protection against overcurrent and short-circuit
  – Undervoltage lockout on V_{CC}
- NTC thermistor for temperature monitor on the power stage
- Open emitter configuration for individual phase current sensing
- DBC fully isolated package for enhanced thermal behavior
- Isolation voltage rating of 2500 V_{RMS}/min

The Figure 2. SLLIMM high power block diagram shows the block diagram of an inverter solution based on a SLLIMM high power.

Figure 2. SLLIMM high power block diagram



1.2 Product line-up and nomenclature

The Table 1. Synoptic shows the product in production.

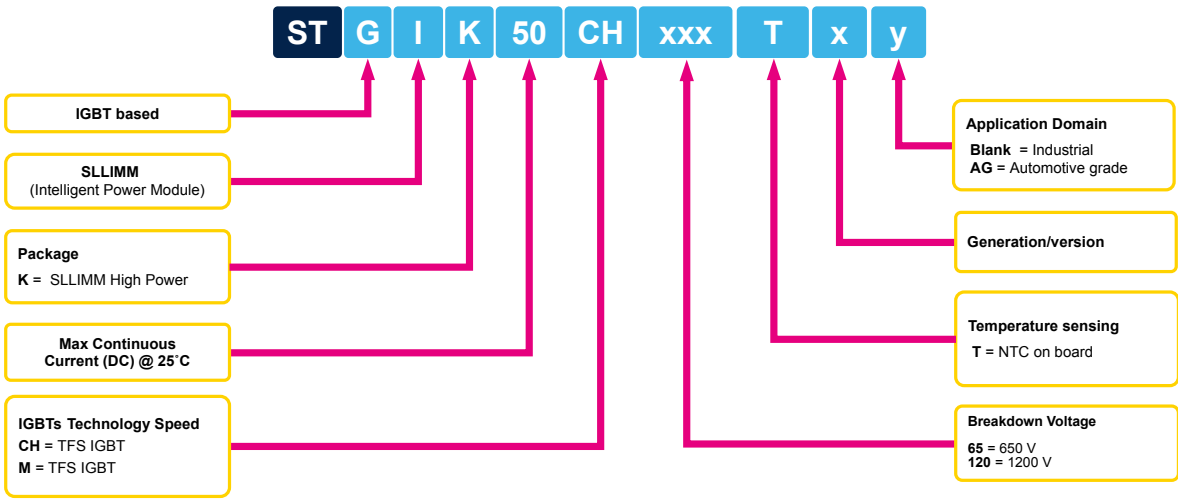
Table 1. Synoptic

Feature	STGIK50CH65T
Collector-emitter voltage each IGBT	650 V
Continuous collector current each IGBT	50 A
Maximum junction temperature	175 °C
Thermal resistance, junction-to-case single IGBT	1 °C/W
Isolation voltage	2500 V_{RMS}/min
Package	SDIPHP-30L
Number of pins	30
Package size X, Y, Z	52.5 x 31.0 x 5.6 mm
Built-in bootstrap diode	Yes
Shutdown input / fault output	Yes
Comparator for fault protection	Yes
Temperature monitoring	NTC
Undervoltage lockout	Yes
Open emitter configuration	Yes
3.3/5 V input interface compatibility	Yes
High and low-side input signal	Active high

Refer to www.st.com for the complete product portfolio.

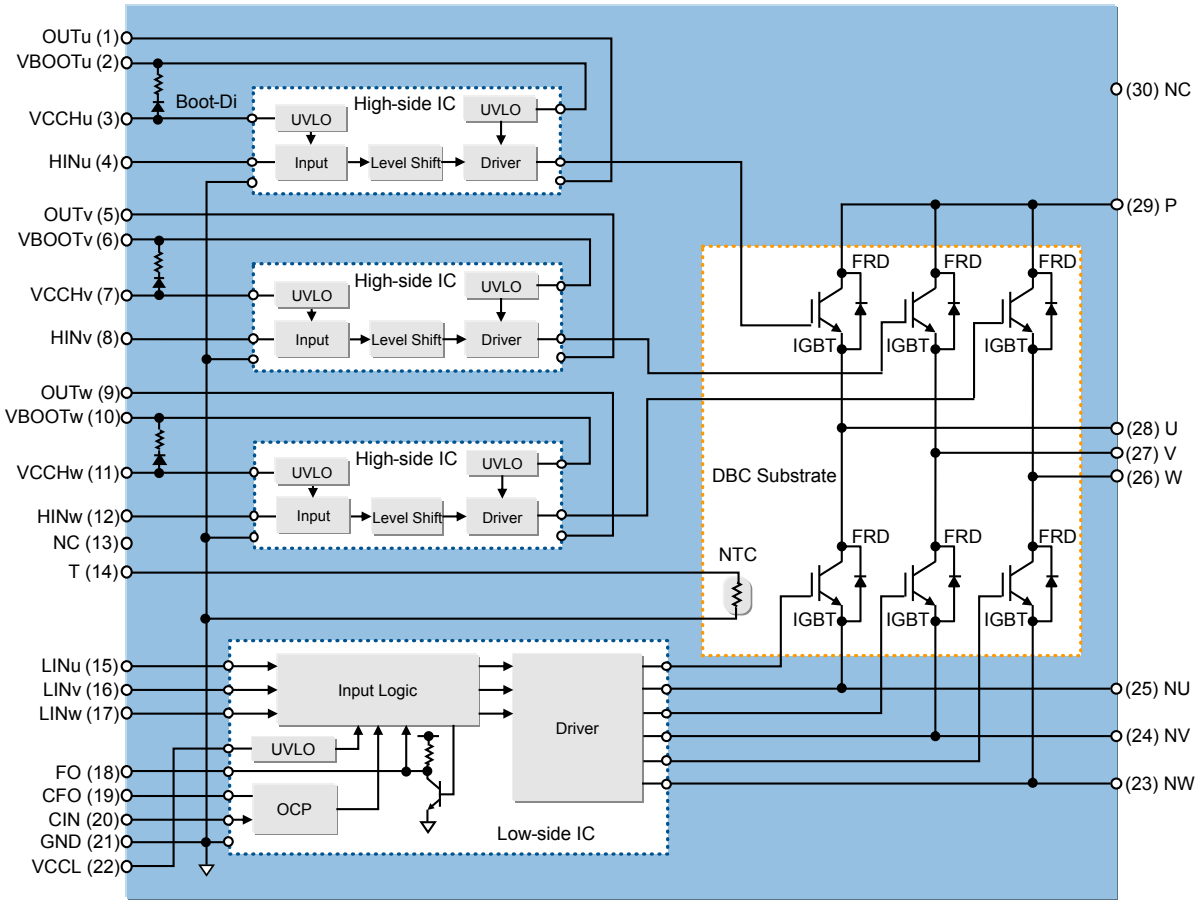
The Figure 3. SLLIMM high power nomenclature describes the SLLIMM high power product family nomenclature.

Figure 3. SLLIMM high power nomenclature



1.3 Internal circuit

Figure 4. **Internal circuit of STGIK50CH65T**



Note: External connections between OUTu, OUTv and OUTw to U, V and W leads respectively, is requested.

1.4 Absolute maximum ratings

The absolute maximum ratings represent the extreme capabilities of the device and can be normally used to set the worst case design limit conditions.

Absolute maximum values are based on specific test parameters such as temperature, frequency, voltage and current. Device performance can change according to the applied condition.

The SLLIMM high power specifications are described in Table 2. Inverter part of STGIK50CH65T with the STGIK50CH65T datasheet example. Refer to the relevant product datasheet for detailed information regarding the other device types.

Table 2. Inverter part of STGIK50CH65T

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - NU, NV, NW	500	V
$V_{PN(surge)}$	Supply voltage surge between P - NU, NV, NW	550	V
V_{CES}	Collector-emitter voltage each IGBT	650	V
I_C	Continuous collector current each IGBT	50	A
I_{CP}	Peak collector current each IGBT (less than 1ms)	100	A
P_{TOT}	Total power dissipation at T_C = 25 °C each IGBT	150	W
$V_{PN(SP)}$	Self-protection supply voltage limit, V_{CC} = 13.5 – 16.5 V, T_J = 150 °C, non-repetitive, less than 2 µs	400	V

The power stage of SLLIMM high power is based on IGBTs (and FRDs) with a 650 V V_{CES} rating. Considering the IPM internal stray inductance during the commutations, which can generate up to 100 V of surge voltage, the maximum surge voltage between P-N ($V_{PN(surge)}$) allowed is 550 V. At the same time, the maximum supply voltage (in steady-state) applied between P-N (V_{PN}) is limited to 500 V because of an additional 50 V surge voltage generated by the stray inductance between the SLLIMM high power and the DC-link capacitor.

I_c is the allowable DC current continuously flowing at the collector electrode of each IGBT.

$V_{PN(SP)}$ is the maximum supply voltage between P-N allowed during short-circuit or overcurrent event for a safe IGBT turn off. If the short-circuit conditions exceed the above specifications, the lifetime of the device is drastically shortened, see Section 1.5 SCSOA.

The internal IPM layout and board layout shown in Figure 5. Stray inductance components of output stage are the two major components of parasitic inductance.

Figure 5. **Stray inductance components of output stage**

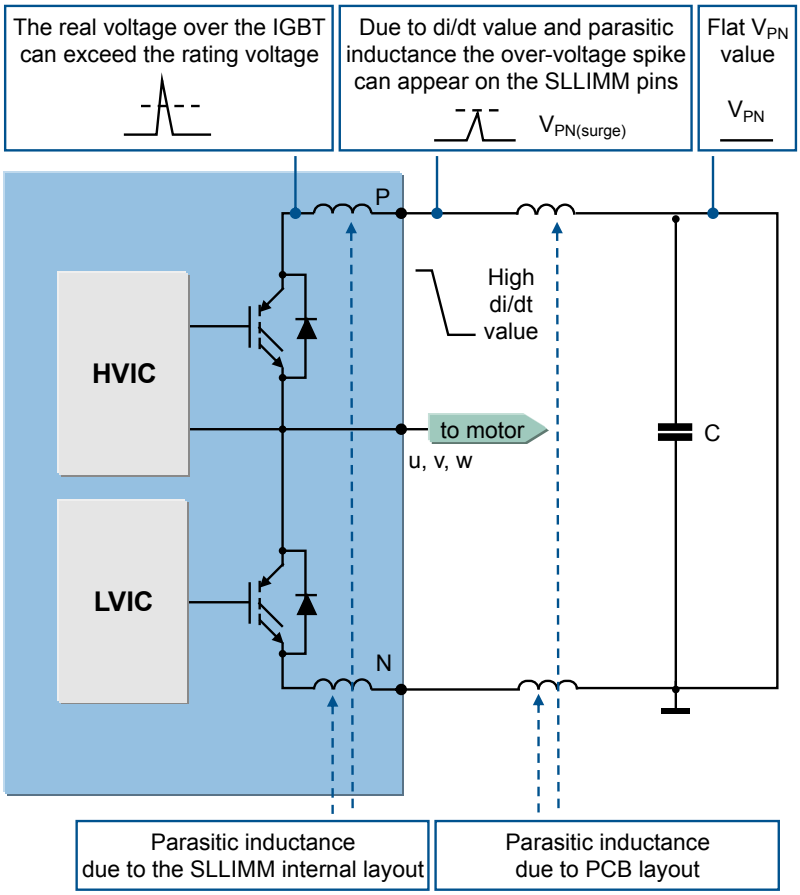


Table 3. **Control part of STGIK50CH65T**

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage between V_{CCHx} - GND, V_{CCL} - GND	-0.5	25	V
V_{BOOT}	Bootstrap voltage	-0.5	25	V
V_{OUT}	Output voltage between U, V, W and GND	-0.5	650	V
V_{CIN}	Comparator input voltage	-0.5	V_{CCL}+0.3	V
V_{INH}	Logic input voltage applied between HINx and GND	-0.5	V_{CCHx}+0.3	V
V_{INL}	Logic input voltage applied between LINx and GND	-0.5	V_{CCL}+0.3	V
V_{FO}	Fault output voltage	-0.5	V_{CCL}+0.3	V
I_{FO}	Fault output sink current	-	1	mA

V_{CC} represents the supply voltage of the control part for high-side gate drivers and low-side one. Local filtering is recommended to enhance the SLLIMM noise immunity. Generally, it is suggested to use one electrolytic capacitor (with a higher value) and a faster and smaller ceramic capacitor (in the order of hundreds of nF, with low ESL and ESR) to provide current.

Refer to the details in the Table 4. Supply voltage and operation behavior to drive the SLLIMM properly.

Table 4. Supply voltage and operation behavior

V_{CC} voltage (typ. value)	Operating behavior
0 ÷ 6.3 V	Logic blocks of IC gate drivers are not properly operating, and no protection function is assured. Normally, IGBT should be OFF, but external noise could change its state.
6.3 V ÷ V_{VCCL_H}, V_{VCCHx_H}, $V_{VBOOTx\text{-}OUTx\_H}$	As the voltage is lower than the UVLO thresholds, therefore even if the input signals are applied the IGBT are in OFF state.
V_{VCCL_H}, V_{VCCHx_H}, ÷ 13.5 V $V_{VBOOTx\text{-}OUTx\ \_H}$ ÷ 13.0 V	IGBTs can function, however conduction and switching losses increase due to low voltage gate signal.
13.5 V ÷ 16.5 V (V_{VCCL}, V_{VCCHx}) 13.0 V ÷ 18.5 V ($V_{BOOTx\text{-}OUTx}$)	Recommended value (see relevant datasheets).
16.5 V ÷ 25.0 V (V_{VCCL}, V_{VCCHx}) 18.5 V ÷ 25.0 V ($V_{VBOOTx\text{-}OUTx}$)	IGBTs can function. Switching speed is faster and saturation current higher, increasing short-circuit broken risk and EMI issues.
> 25 V (V_{VCCL}, V_{VCCHx}, $V_{VBOOTx\text{-}OUTx}$)	Control circuit is destroyed. Absolute max. rating is 25V.

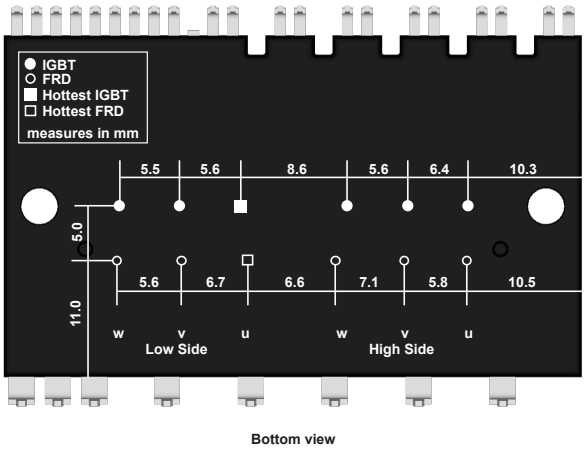
For further information, refer to the STGIK50CH65T datasheet.

Table 5. Total STGIK50CH65T system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s)	2500	V_{RMS}
T_J	IGBT and FRD operating junction temperature range	-40 to 175	°C
	Driver IC and bootstrap diode operating junction temperature range	-40 to 150	°C
T_C	Module case operating temperature range	-40 to 125	°C

The Figure 6. Power chip position and T_C measurement point (for complementary switching scheme) shows the position point of each power chips, where are also highlighted the hottest IGBT and FRD. The case temperature measurement point is intended to be right above the hottest power chip, in case of complementary switching scheme. To obtain accurate temperature information, mount a thermocouple on the heat sink surface at this specific location. For non-complementary switching schemes, the highest T_C point could occur in a different position. In this case, the measurement location is over the point where the highest power chip temperature is generated.

Figure 6. Power chip position and T_C measurement point (for complementary switching scheme)



Bottom view

1.5 SCSOA

Short-circuit safety operating area (SCSOA) defines the permitted voltage and current during non-repetitive turn-off of short-circuit current in the IPM, without endangering its survival.

Figure 7. SCSOA test circuit and Figure 8. SCSOA main parameters show the circuits for obtaining the SCSOA of SLLIMM high power devices and the SCSOA main parameters, respectively.

Figure 7. SCSOA test circuit

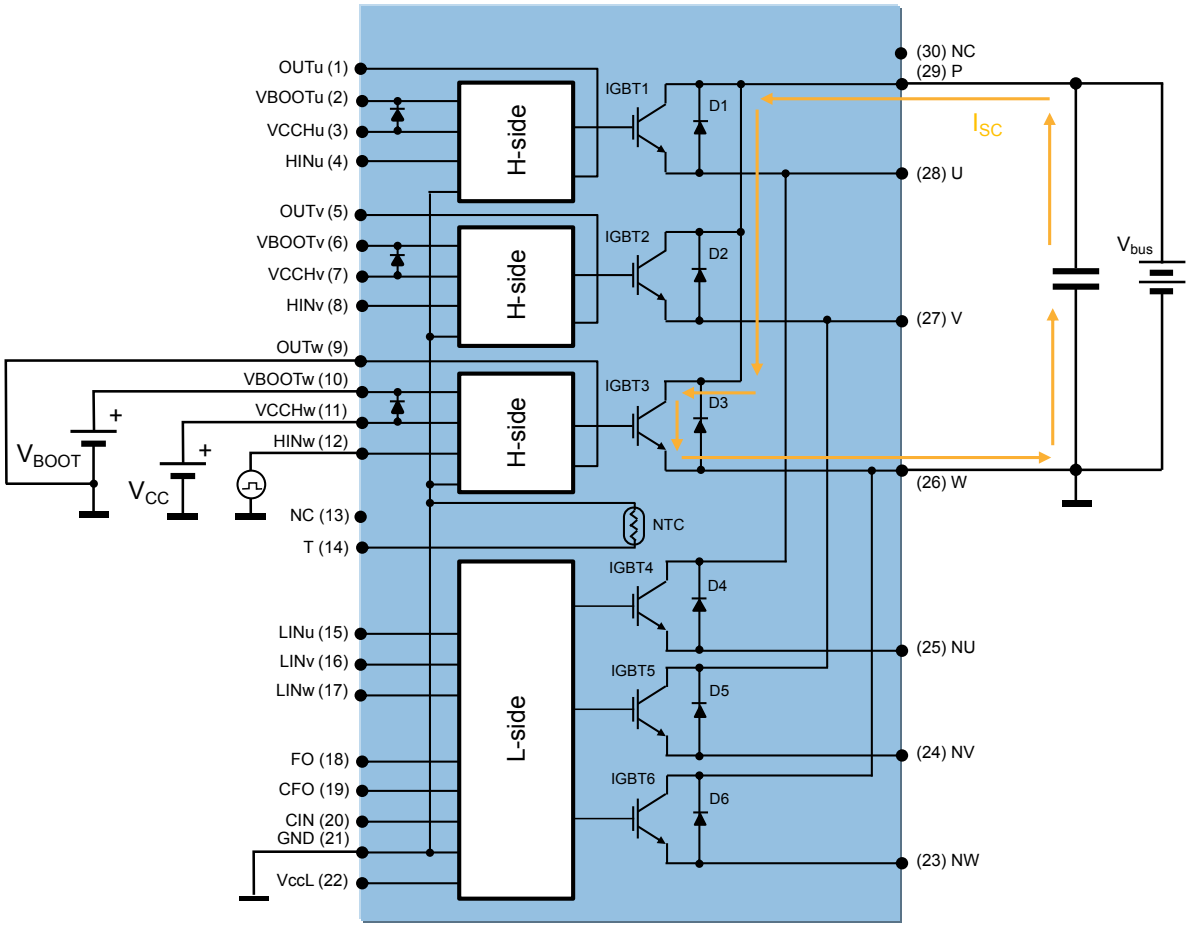
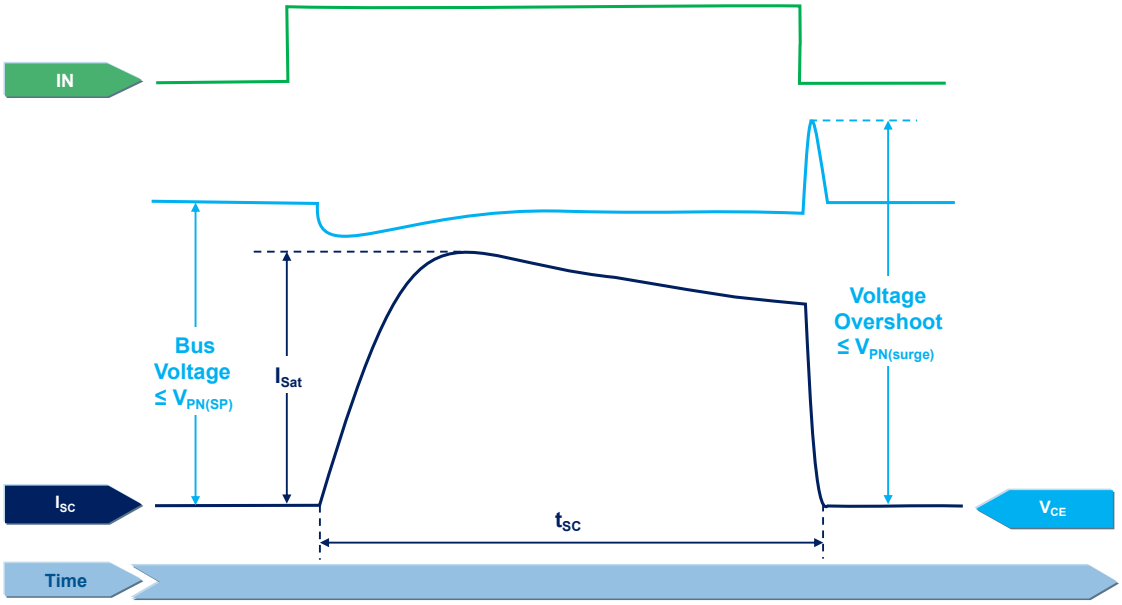


Figure 8. **SCSOA main parameters**

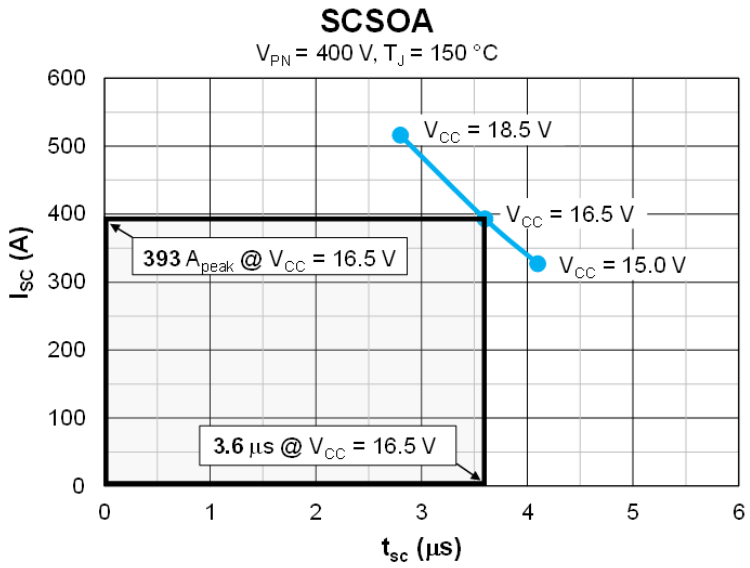


The Figure 9. Typical STGIK50CH65T SCSOA curve shows the typical SCSOA performance curve of the STGIK50CH65T.

The testing conditions are: V_{PN} = 400 V, T_J = 150 °C at initial stage, $V_{PN(surge)}$ ≤ 500 V, V_{IN} = 5 V, non-repetitive.

Since SCSOA is function of several conditions (effective voltage applied to the IGBT, to the V_{CC} and V_{BOOT}) and circuit parameters (stray inductances and resistances), it is suggested to keep the overall short-circuit protection time lower than t_{sc}, with sufficient margin, in the final application.

Figure 9. **Typical STGIK50CH65T SCSOA curve**



2 Electrical characteristics and functions

In this section, the main electrical characteristics of the power stage are discussed, together with a detailed description of the SLLIMM high power functions.

2.1 IGBTs

The high power version of this SLLIMM range embeds a new IGBTs with trench-gate field stop (TFS) technology with high current density and optimized for typical motor control switching frequencies. They offer an excellent tradeoff between voltage drop ($V_{CE(sat)}$) and switching speed (t_{fall}) to therefore minimize the two major sources of energy loss, conduction and switching, thus reducing the environmental impact of daily-use equipment.

Furthermore, this IGBT series is also capable of surviving short-circuits, as required by targeted applications. For further details, refer to Section 1.5 SCSOA.

2.2 Fast recovery diodes

The fast recovery high voltage diodes (FRDs) have been appropriately selected for the SLLIMM high power series and carefully tuned to achieve the best t_{rr}/V_F tradeoff and softness as freewheeling diodes to further improve the total performance of the inverter and significantly reduce electromagnetic interference (EMI) in motor control applications, which are quite sensitive to this phenomenon.

2.3 Gate driver ICs

The new SLLIMM high power family is equipped with three single high voltage gate drivers for each HS IGBTs and a triple low voltage gate driver for LS IGBTs. They are designed to provide all the functions, protections, and the proper current capabilities necessary for IGBT driving.

Figure 10. Single high-side gate driver block diagram

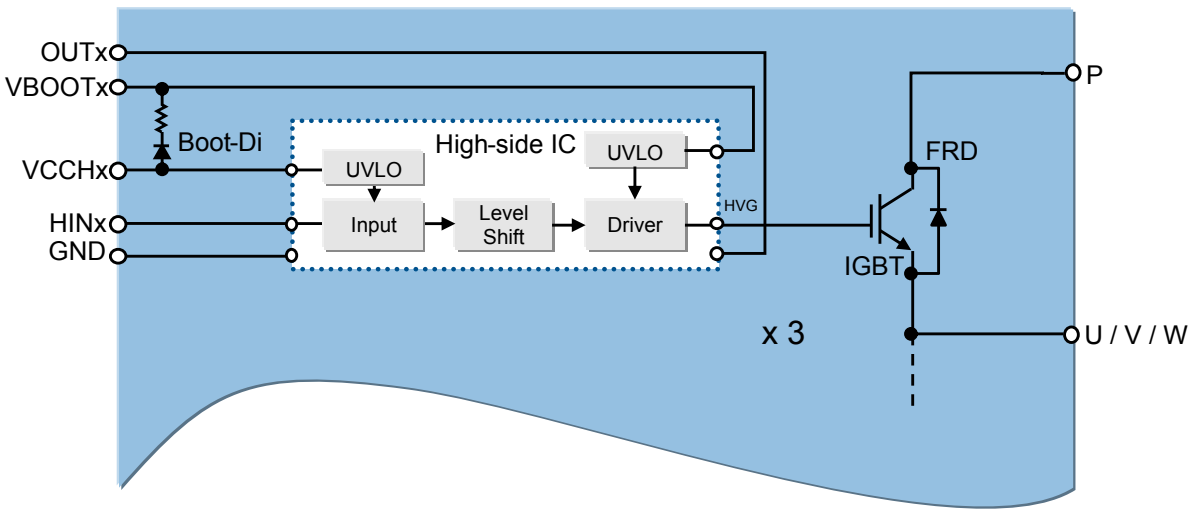
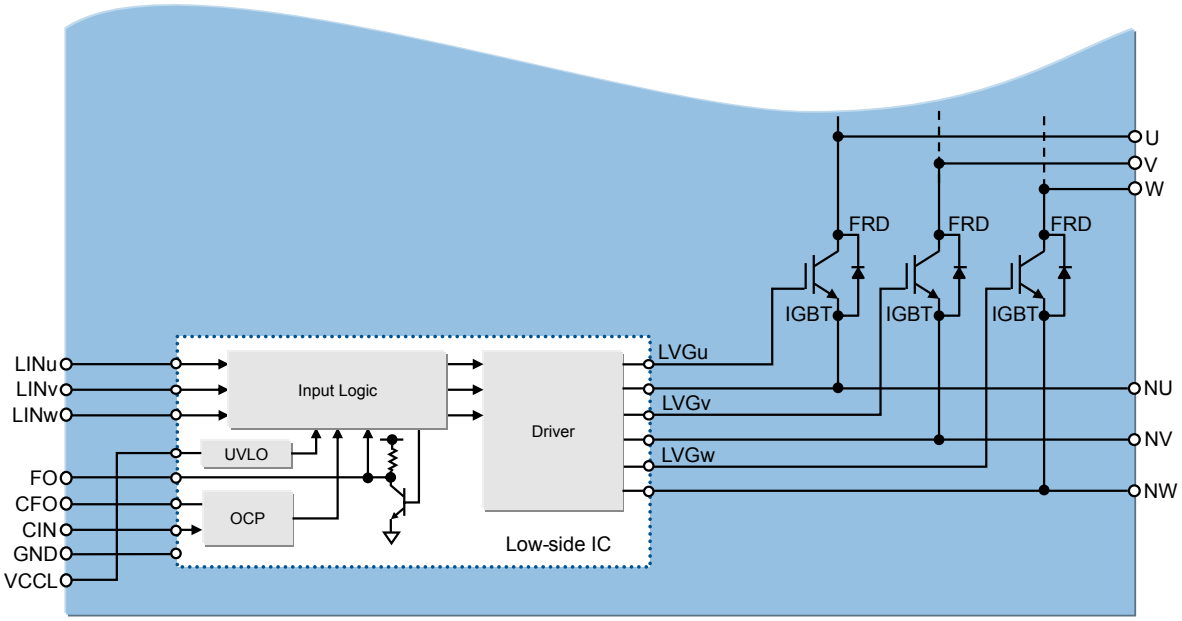


Figure 11. **Triple low-side gate driver block diagram**



For pin descriptions, refer to Section 3.2 Input and output pin descriptions.

2.4 Logic inputs

All the logic inputs include hysteresis for low noise sensitivity and are TTL/CMOS 3.3 V compatible. Thanks to this low voltage interface logic compatibility, the SLLIMM high power can be used with any kind of high performance controller like microcontrollers, DSPs or FPGAs.

Both high-side and low-side gate drivers' logic inputs have internal pull-down resistors in order to set the proper logic level in case of interruption in the logic lines. If logic inputs are left floating, the gate driver output signals (HS and LS) are set to low level. This simplifies the interface circuit by eliminating the six external resistors, therefore saving on cost, board space and number of components.

Table 6. **Integrated pull-down resistor values**

Input pin	Input pin logic	Internal pull-down (typical value)
High-side gate driving HINu, HINv, HINw	active high	20 kΩ
Low-side gate driving LINu, LINv, LINw	active high	20 kΩ

All the IC input pins are protected by ESD events thanks to dedicated structures. All the IC output pins embed protection against below ground voltage. In addition, an effective protection able to improve the emitter below ground robustness is placed between the low-side IGBT emitters and the IC signal ground.

2.5 High voltage level shift

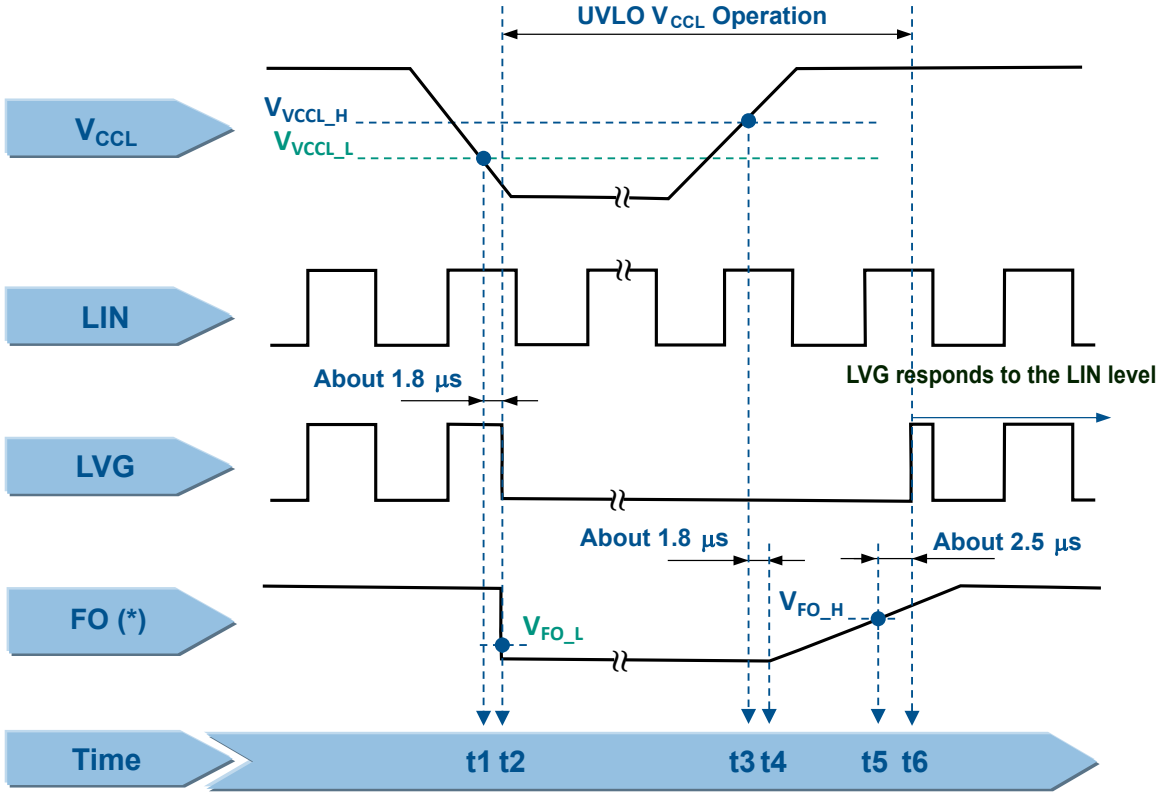
In the HS gate drivers ICs, the built-in high voltage level shift allows direct connection between the low voltage control inputs and the high voltage power half bridge in any power application up to 650 V. It is obtained thanks to a logic circuitry and high voltage DMOS transistors with a breakdown voltage in excess of 650 V. This key feature eliminates the need for external optocouplers, resulting in significant savings, component count and power losses. Other advantages are high-frequency operation and short input-to-output delays.

2.6 Undervoltage lockout

Both HS and LS gate driver ICs supply voltages, V_{CCHx} and V_{CCL} respectively, are continuously monitored by an undervoltage lockout (UVLO) circuit able to turn the high-side and low-side gate driver outputs off when the supply voltage fall below the V_{VCCHx_L} and V_{VCCL_L} thresholds specified on the datasheet, and turns the ICs on when the supply voltages rise above the V_{VCCHx_H} and V_{VCCL_H} thresholds voltage. To prevent noise-inducted malfunctions an internal filter circuit of about 1.8 µs, as well as a hysteresis of 0.5 V (typical value) is provided. In addition, a fault signal on the FO pin is activated if an undervoltage is detected by the LS gate driver IC only and it is pulled low for the whole UVLO duration.

Furthermore, in the HS gate driver ICs, the high voltage floating supply V_{BOOT} is also provided with similar undervoltage lockout circuitry. In case of an UVLO condition on V_{BOOT}, the output signals of the gate drivers are set to low level.

Figure 12. Timing chart of undervoltage lockout function on low-side section



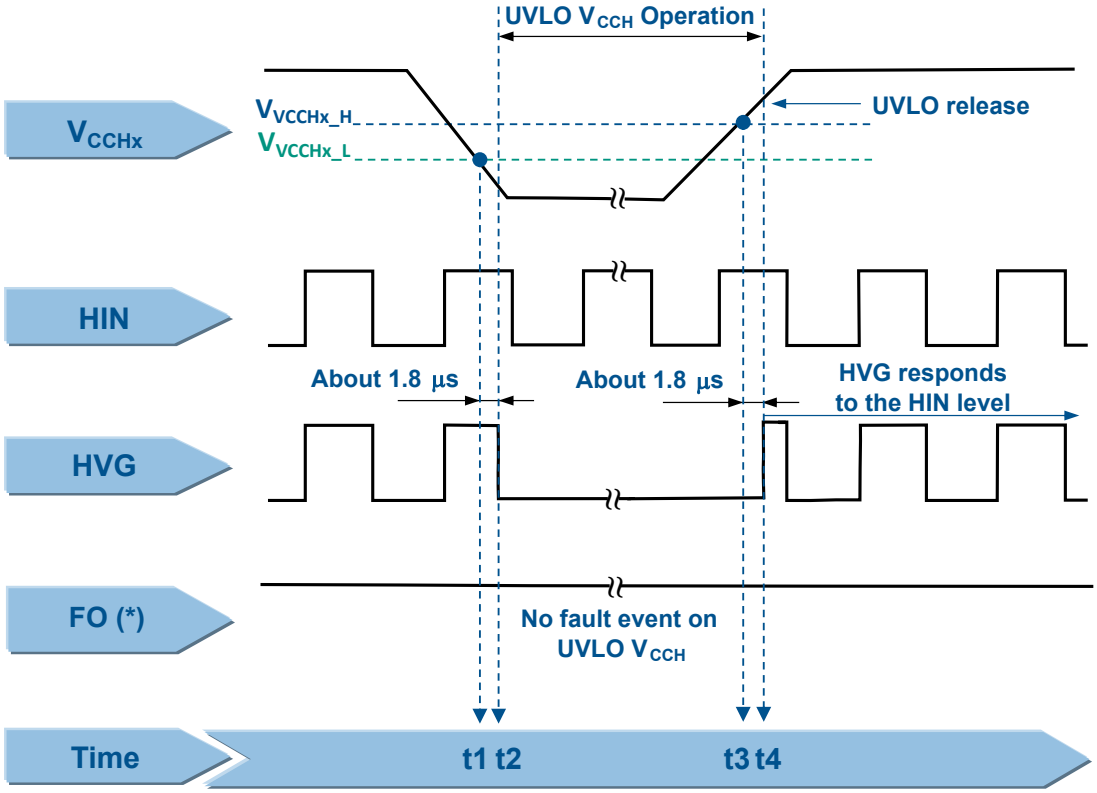
(*) FO fall and rise times are function of the external R_{FF} - C_{FF} filter

Figure 12. Timing chart of undervoltage lockout function on low-side section shows the timing chart of the low-side gate driver for an undervoltage on V_{CCL}. It is based on the following steps:

- t1: when the V_{CCL} supply voltage falls below the V_{VCCL_L} threshold, an UVLO event is detected.
- t2: after a delay time of about 1.8 µs the UVLO function starts to operate. The LS output driver (LVG) is in off state, even if the input signal LIN is still present. The FO signal falls below the V_{FO_L} threshold and fault information is sent to the MCU.
- t3: the V_{CCL} supply voltage rises above the V_{VCCL_H} threshold.
- t4: after a delay time of about 1.8 µs the FO starts to rise.
- t5: the FO signal reaches the V_{FO_H} threshold.
- t6: after a delay time of about 2.5 µs the UVLO function is ended. The LS gate driver output (LVG) operates according with the LIN input signal.

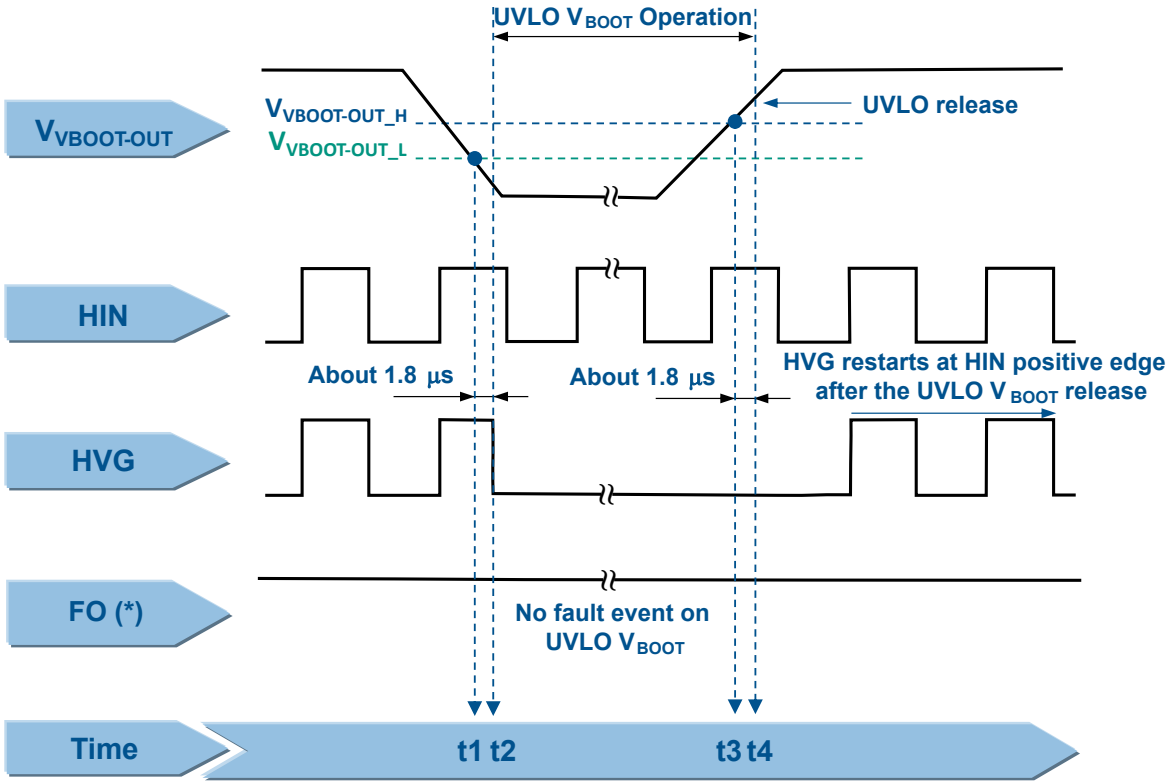
The FO state time duration (t5 – t2) is treated in the Section 2.11 Fault (FO) time setting

Figure 13. Timing chart of undervoltage lockout function on high-side section



(*) embedded on the Low Side Driver

Figure 14. **Timing chart of undervoltage lockout function on bootstrap section**



(*) embedded on the Low Side Driver

The Figure 13. Timing chart of undervoltage lockout function on high-side section and Figure 14. Timing chart of undervoltage lockout function on bootstrap section show the timing charts of the high-side gate driver for an undervoltage on V_{CCH} or V_{BOOT}. It is based on the following steps:

- t1: when the V_{CCHx} (or $V_{VBOOTx-OUTx}$) supply voltage falls above the V_{VCCHx_L} (or $V_{VBOOTx-OUTx\_L}$) threshold(s), an UVLO event is detected.
- t2: after a delay time of about 1.8 µs the UVLO function starts to operate. The HS output driver (HVG) is in off state, even if the input signal HIN is still present.
- t3: the V_{CCHx} (or $V_{VBOOTx-OUTx}$) supply voltage rises above the V_{VCCHx_H} (or $V_{VBOOTx-OUTx\_H}$) threshold(s).
- t4: after a delay time of about 1.8 µs the UVLO is released. The HS output driver (HVG) responds to HIN input signal level, in case of UVLO V_{CCH}, or restarts at HIN positive edge after the UVLO release, in case of UVLO V_{BOOT}.
- The FO signal is not activated on UVLO V_{CCH} (or V_{BOOT}) event.

2.7 Comparator for fault sensing and short-circuit protection function

The SLLIMM high power integrates one comparator intended for advanced fault protection such as overcurrent, overtemperature or any other type of fault measurable via a voltage signal. The comparator has an internal reference voltage on its inverting input, while the non-inverting input is available on the CIN pin, which can be connected to an external shunt resistor to implement a simple overcurrent function. The over current protection is activated when the CIN signal exceeds the V_{CIN_H} (specified in the datasheet) and remains in this condition for, at least, a period set by an internal filter circuit (about 0.3 µs typical) to prevent noise-induced malfunctions.

The output signal of the comparator is fed into an integrated transistor with the open collector available on the FO pin.

When the comparator triggers, the device is set to the shutdown state, all LS IGBTs are turned off and FO pin is put in low state for a fixed over current protection (OCP) hold time (t_{FO}) even if the CIN pin voltage falls below V_{CIN_L}. Then, the output IGBTs operate according to input signals. The OCP hold time, t_{FO}, can be adjusted by the value of the CFO pin capacitor (C_{CFO}). For further details please refer to Section 2.11 Fault (FO) time setting.

An external RC filter network (R_{CF} and C_{CF}), placed as close as possible to the CIN pin, is necessary to prevent erroneous operation of the protection. Its time constant is suggested to be set at the recommended value of 1.0 µs.

In addition, to prevent noise interference, an external RC network (R_{FF} and C_{FF}) is suggested to be connected to the FO pin. The filter should be placed as close as possible to the FO and GND pins and its value of C_{FF} must be set to ≤3300 pF.

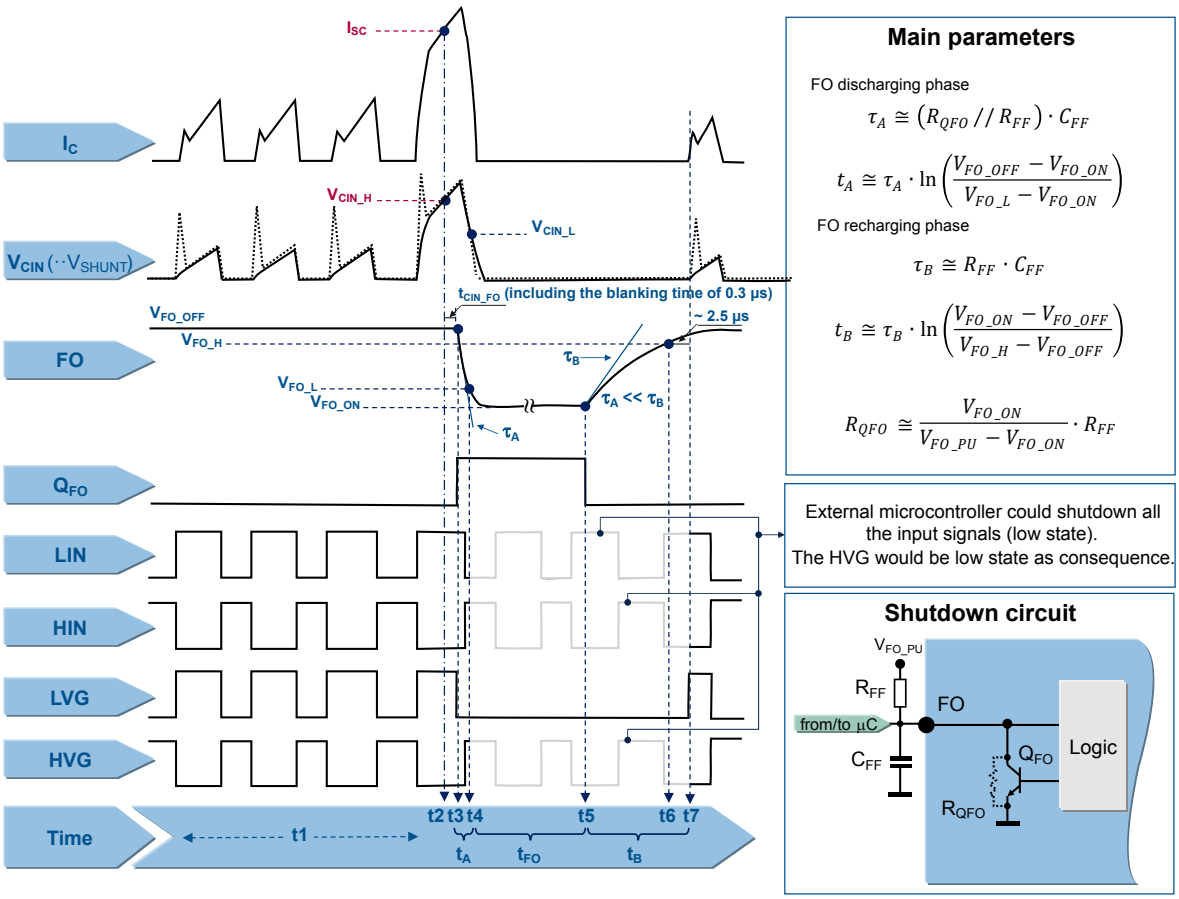
To avoid the repetition of OCP activations, the external microcontroller must shut off any input signals to the IPM within an OCP hold time, t_{FO}, which occurs after the internal transistor (Q_{FO}) turn-on.

Note: Repeated short-circuit operations will stress the device.

2.8 Timing chart of short-circuit protection function

Figure 15. Timing chart of short-circuit protection function shows the timing chart during an overcurrent or short-circuit event.

Figure 15. Timing chart of short-circuit protection function



The timing chart is based on the following steps:

- t1: when the output current is lower than the max. allowed level, the SLLIMM high power functions normally.

- t2: when the output current reaches the max. allowed level (I_{SC}), the overcurrent/short-circuit event is detected and the protection is activated. The voltage across the shunt resistor arises and then the CIN voltage (V_{CIN}) reaches the V_{CIN_H} value. The comparator has an internal blanking time of about 0.3 µs typical value, in order to prevent noise-induced malfunctions. The comparator triggers and after this delay time the shutdown phase begins.
- t3: the internal transistor Q_{FO} is switched on, the FO starts the discharge phase (with a time constant according to Equation 1) and the low-side IGBTs are switched off. As result of this the output current decreases.

Equation 1

$$\tau_A \cong \left(R_{QFO} // R_{FF}\right) \cdot C_{FF} \quad (1)$$

- t4: at this time, the FO signal reaches the low voltage logic level (V_{FO_L}). Even if the overcurrent disappeared and the CIN pin voltage falls below V_{CIN_L}, the IC holds the FO pin in the low state for a fixed OCP hold time (t_{FO}) adjustable by the value of the CFO pin capacitor, (C_{CFO}, see Section 2.11 Fault (FO) time setting). If the external microcontroller is programmed to detect the fault event, it switches the input signals LIN and HIN off (refer to faded area on the figure). The HVG is at low state as consequence. The internal transistor Q_{FO} is remains on.
- t5: when the t_{FO} has elapsed, the FO signal can rise with a time constant given by Equation 2:

Equation 2

$$\tau_B \cong R_{FF} \cdot C_{FF} \quad (2)$$

- t6: the FO signal reaches the upper threshold V_{FO_H} (in the worst case) but the system is not yet re-enabled
- t7: after a delay time of about 2.5 µs the system is re-enabled and the output IGBTs operate according to input signals.

The discharging time t_A and the charging time t_B are the time intervals between t4-t3 and t7-t5, respectively.

2.9 Current sensing shunt resistor selection

As previously discussed, the shunt resistors R_{SHUNT} externally connected between the N pins and ground are used in the overcurrent detection circuitry.

When the output current exceeds the short-circuit reference level (I_{SC}), the CIN signal overtakes the V_{CIN_H} value and the short-circuit protection is activated. For reliable and stable operation, the current sensing resistor should be a high quality, low tolerance non-inductive type. In fact, stray inductance in the circuit due to the layout, the RC filter, and even the shunt resistor, must be minimized in order to avoid undesired short-circuit detection.

For these reasons, the shunt resistor and the filtering components must be placed as close as possible to the SLLIMM high power pins. For further details please refer to Section 5.2 Layout suggestions.

The value of the current shunt resistor can be calculated according to different guidelines, functions of the design specifications, or requirements. Based on a simplified 3-shunt configuration, a common criterion is presented here based on the following steps:

- Setting of the overcurrent threshold value (I_{OC_th}). This value can, for example, be set by considering the IGBT typical working current in the application and adding 20-30% as overcurrent.
- Calculation of the shunt resistor value according to the conditioning network.
- Selection of the closest shunt resistor commercial value.
- Calculation of the power rating of the shunt resistor, taking into account that this parameter is strongly temperature dependent. Therefore, the power derating ratio of the shunt resistor, ΔP(T)%, shown in the manufacturer's datasheet, must be considered, as shown in the formula below:

Equation 3

$$P_{SHUNT}(T) = \frac{1}{2} \frac{R_{SHUNT} \cdot I_{ph(RMS)}^2}{\Delta P(T)\%} \quad (3)$$

Where $I_{ph(RMS)}$ is the RMS motor phase current. For further details please refer to the AN4076.

For proper selection of the shunt resistor, a safety margin of at least 30% is recommended on the calculated power rating.

Below is an example.

The value of shunt resistor is calculated by Equation 4:

Equation 4

$$R_{SHUNT} = \frac{V_{CIN\_H}}{I_{OC}} \quad (4)$$

Where V_{CIN_H} is reference voltage of the internal comparator (CIN) (0.50 V typ.) and I_{OC} is the OC trigger level.

Considering, as example, an inverter working at 25 A_{RMS} (= 35.2 A_{peak}) as maximum operating phase current, the OC protection level can be set at 45.8 A (30% higher than peak current), which is still inside the IPM SOA. The shunt resistor value is:

Equation 5

$$R_{SHUNT} = \frac{V_{CIN\_H}}{I_{OC}} = \frac{0.50}{45.8} = 0.011\Omega \quad (5)$$

For the power rating of the shunt resistor, these parameters must be considered:

- RMS motor phase current (worst case): $I_{ph(RMS)} = 25$ A
- Shunt resistor value at T_C=25°C.
- Power derating ratio of shunt resistor at T_{SHUNT} = 100 °C
- Safety margin.

The power rating is calculated with Equation 6:

Equation 6

$$P_{SHUNT} = \frac{1}{2} \cdot \frac{R_{SHUNT} \cdot I_{ph(RMS)}^2 \cdot margin}{Derating\ ratio} \quad (6)$$

- The R_{SHUNT} commercial value is 0.010 Ω
- power derating ratio of shunt resistor at T_{SHUNT} =100 °C: 80% (from datasheet manufacturer)
- safety margin: 30%

Finally, the shunt power is:

Equation 7

$$P_{SHUNT} = \frac{1}{2} \cdot \frac{0.010 \cdot 25^2 \cdot 1.3}{0.8} \cong 5W \quad (7)$$

and the effective OC protection level is:

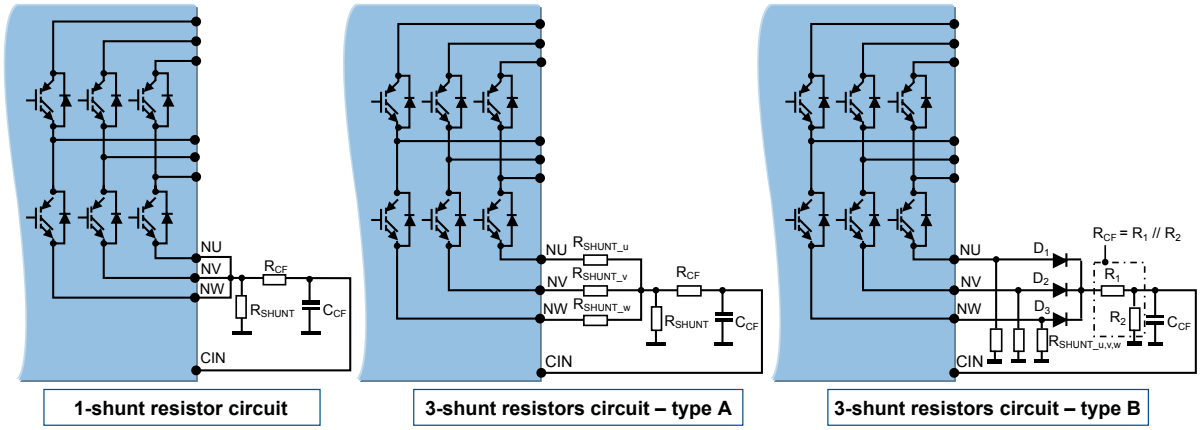
Equation 8

$$I_{OC} = \frac{V_{CIN\_H}}{R_{SHUNT}} = \frac{0.5}{0.010} = 50A \quad (8)$$

2.10 RC filter network selection

Two options of shunt (1- or 3-shunt) resistor circuits can be adopted for different control and short-circuit protection techniques. For 3-shunt resistor configurations, the Figure 16. Examples of SC protection circuits shows two simple overcurrent protection variants: type A, using an additional shunt resistor (R_{SHUNT}) and type B, using a diode OR gate circuit.

Figure 16. Examples of SC protection circuits



An RC filter network is required to prevent undesired short-circuit operation due to noise on the shunt resistor.

All the solutions allow detection of the total current in all the three phases of the inverter. The filter is based on the R_{CF} and C_{CF} network and its time constant is given by:

Equation 9

$$\tau_{CF} = R_{CF} \cdot C_{CF} \tag{9}$$

In addition to the RC filter delay time (2÷3 times t_{CF}), the turn-off propagation delay of the gate driver, and the IGBT turn-off time (in the order of tens of ns), must be considered in the total delay time (t_{Total}), which is the time necessary to completely switch the IGBT off once the short-circuit event is detected. Therefore, t_{Total} is calculated as follows:

Equation 10

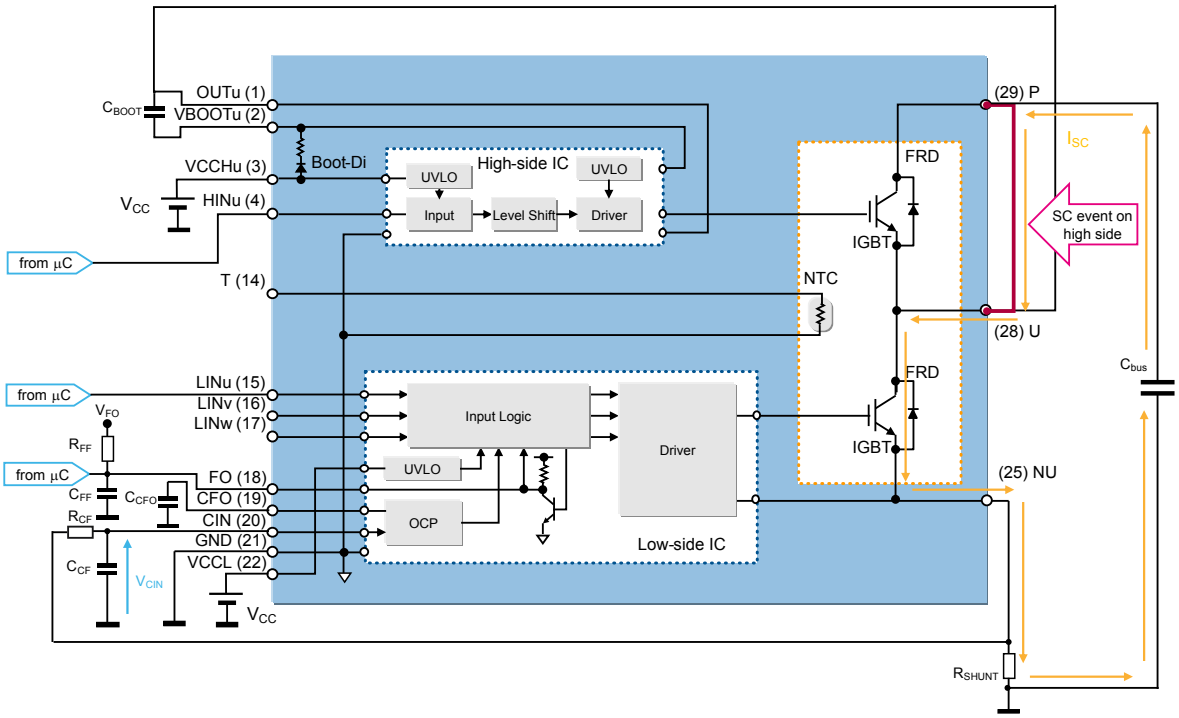
$$t_{Total} = t_{CF} + t_{internal\_propagation\_delay} + t_{IGBT\_off} \tag{10}$$

Therefore, the t_{CF} should be set to 1 µs (max.).

In a 3-shunt resistor circuit, a specific control technique can be implemented by using the three shunt resistors (R_{SHUNT_U}, R_{SHUNT_V} and R_{SHUNT_W}) to monitor each phase current.

An example short-circuit event during normal operation, between P and OUTx when LINx is high, is shown in Figure 17. Example of a short-circuit event.

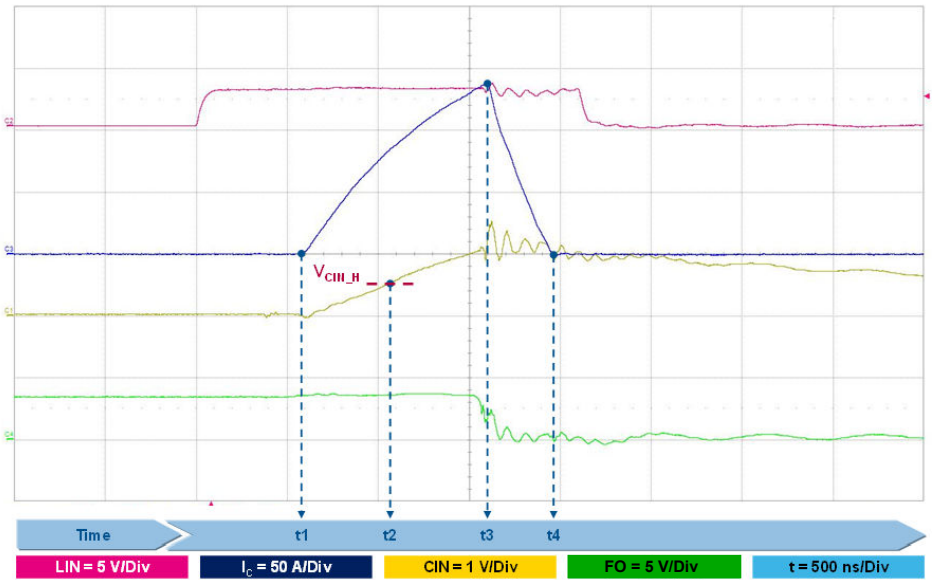
Figure 17. **Example of a short-circuit event**



The main steps are shown in Figure 18. Overcurrent protection waveforms:

- t1: collector current I_C starts to rise. An SC event is not detected yet due to the RC network on the CIN pin.
- t2: voltage on V_{CIN} reaches V_{CIN_H}. An SC event is detected and the shutdown function starts turning off the LS IGBTs. The FO signal is enabled (low state) so the MCU can stop the PWM signals and as consequence of this, even the HS IGBTs are turned off.
- t3: the IGBT starts to turn off in about 500 ns from SC detection.
- t4: the IGBT is definitively turned off about 1.3 µs from the begin of SC event.

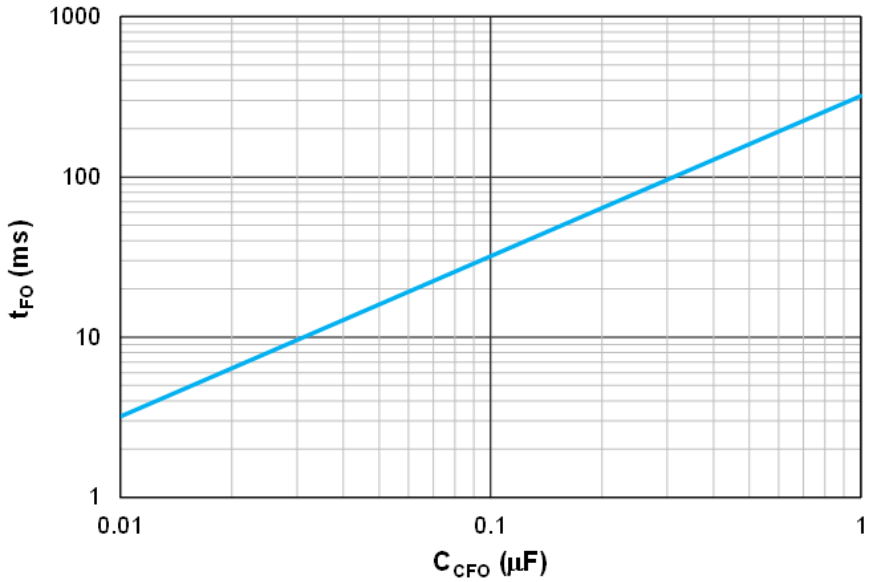
Figure 18. **Overcurrent protection waveforms**



2.11 Fault (FO) time setting

The OCP hold time (t_{FO}), which is the time of fault condition during the overcurrent event can be set by adjusting the capacitor (C_{CFO}) connected to the CFO pin. Figure 19. C_{CFO} - t_{FO} relationship shows the relationship between t_{FO} and C_{CFO}.

Figure 19. C_{CFO} - t_{FO} relationship



In case of UVLO (on the LS driver) the FO signal is enabled as well. Unlike the OCP event, the FO signal doesn't follow a hold time given by the C_{CFO} but it stays low for all the UVLO duration.

Table 7. Fault event summary effect on IGBT and FO summarizes the fault events and the effect on the IGBTs and FO pin.

Table 7. Fault event summary effect on IGBT and FO

Fault event	HS IGBTs	LS IGBTs	FO state	FO time duration
Overcurrent	Operative	OFF	Low (SET)	t_{FO}
UVLO V_{CCH}	OFF	Operative	High (RESET)	-
UVLO V_{CCL}	Operative	OFF	Low (SET)	UVLO duration (1)
UVLO V_{BOOT}	OFF	Operative	High (RESET)	-

1. *R_{FF}-C_{FF} filter (on FO pin) impacts on the total FO time duration. Furthermore, the system needs an additional delay time of about 2.5 µs to be re-enabled.*

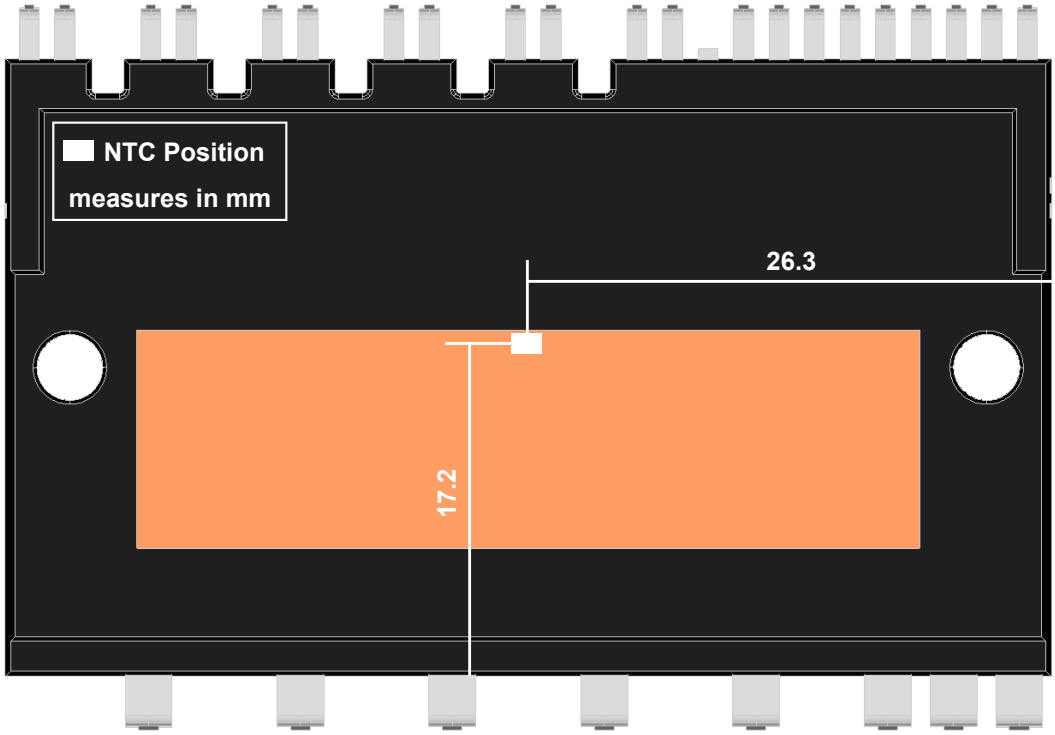
2.12 NTC thermistor

The SLLIMM high power is equipped with a negative temperature coefficient (NTC) thermistor for a real-time temperature monitoring.

Due to the thermal impedance of SLLIMM and its own time constant, the NTC thermistor is not suited to detecting rapid junction temperature rises directly in the power devices. Therefore, it cannot be used for short-circuit or overcurrent protection, but only to monitor gradual changes in temperature.

The NTC thermistor is placed on the DBC structure (see Figure 20. NTC position (top view)) and very close to the power stage for accurate junction temperature monitoring of power chips.

Figure 20. **NTC position (top view)**



The resistance versus temperature characteristic of NTC thermistor is non-linear and it is described by the following expression:

Equation 11

$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)} \quad (11)$$

Where T is the temperature in Kelvin, B is a constant in the IPM operating range and R25 is the resistance at 25 °C; these last two parameters are shown in the Table 8. NTC thermistor information and in the datasheet.

The built-in thermistor (100 kΩ at 25 °C) is inside the IPM and connected between T and GND pins (14, 21).

Table 8. **NTC thermistor information**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{25}	Thermistor Resistance	T_A = 25 °C	-	100	-	kΩ
$B_{25/85}$	B-constant (25/85 °C)			4395		K
T	Operating temperature range		-40		175	°C

Figure 21. **NTC resistance vs temperature**

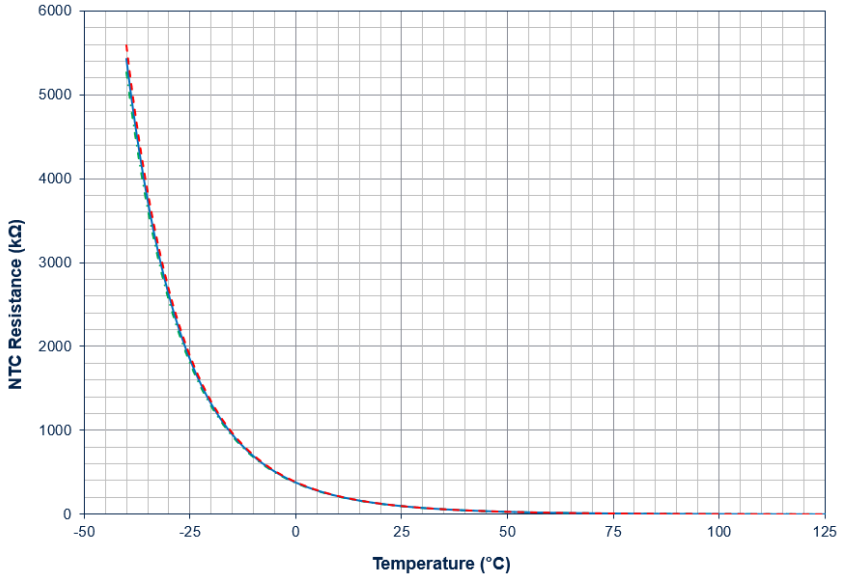
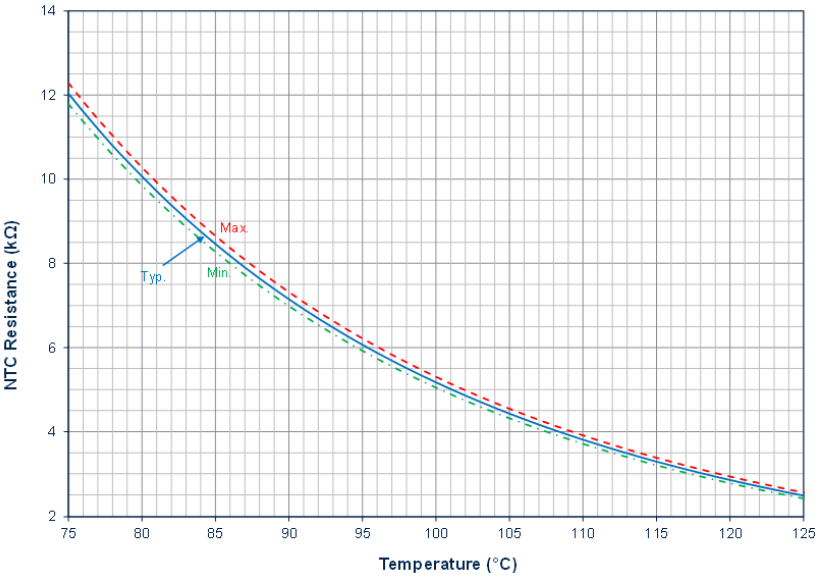


Figure 22. **NTC resistance vs temperature – zoom**

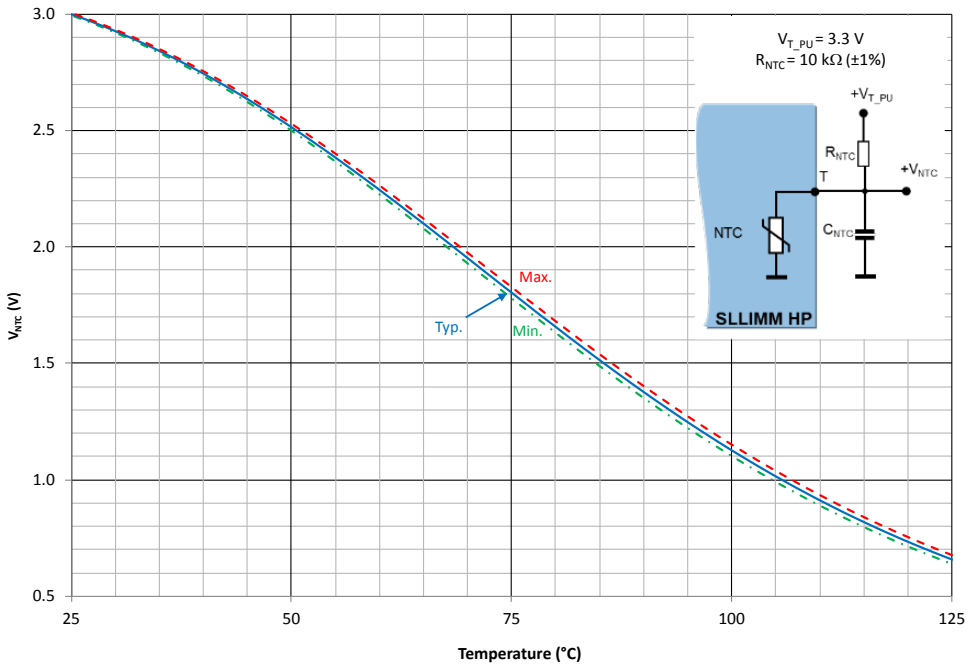


The maximum allowed power on the thermistor should not exceed 150 mW (T_{case} = 100 °C) across the entire operating range in order to guarantee safe operation and avoid power consumption affecting the temperature measurement through self-heating.

To increase the noise immunity of the NTC thermistor, we recommend placing a decoupling capacitor (C_{OT}) in parallel, whose value must be between 10 and 100 nF.

The NTC thermistor is internally grounded and it requires an external pull up network. Its corresponding voltage output as function of temperature is shown in the Figure 23. V_{NTC} vs temperature. The curves include the maximum spread according to the tolerance of the NTC and R_{NTC} resistance.

Figure 23. V_{NTC} vs temperature



2.13 Bootstrap circuit

In the 3-phase inverter, the emitters of the low-side IGBTs are connected to the negative DC bus as the common reference ground, which allows all low-side gate drivers to share the same power supply, while the emitter of the high-side IGBTs is alternately connected to the positive and negative DC bus during operation.

A bootstrap method is a simple and cheap solution to supply the high-voltage section. This function is normally accomplished by a high-voltage fast recovery diode.

The SLLIMM high power family includes a built-in bootstrap diode with current-limiting series resistor for each high-side section, which characteristics are shown in Figure 24. V_F - I_F curve of the bootstrap diode and Table 9. Electrical characteristic of bootstrap diode.

Figure 24. V_F - I_F curve of the bootstrap diode

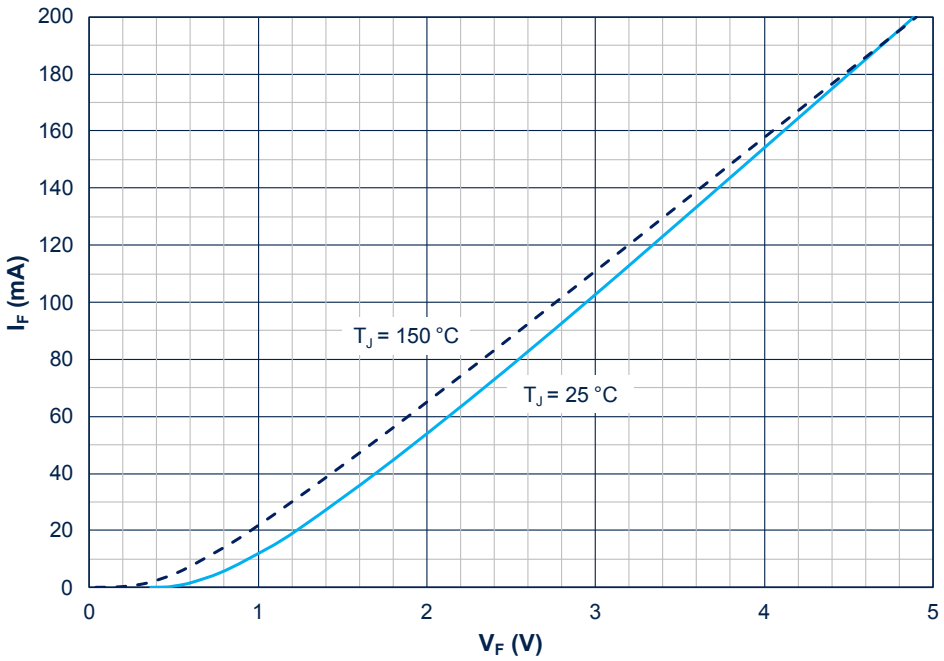
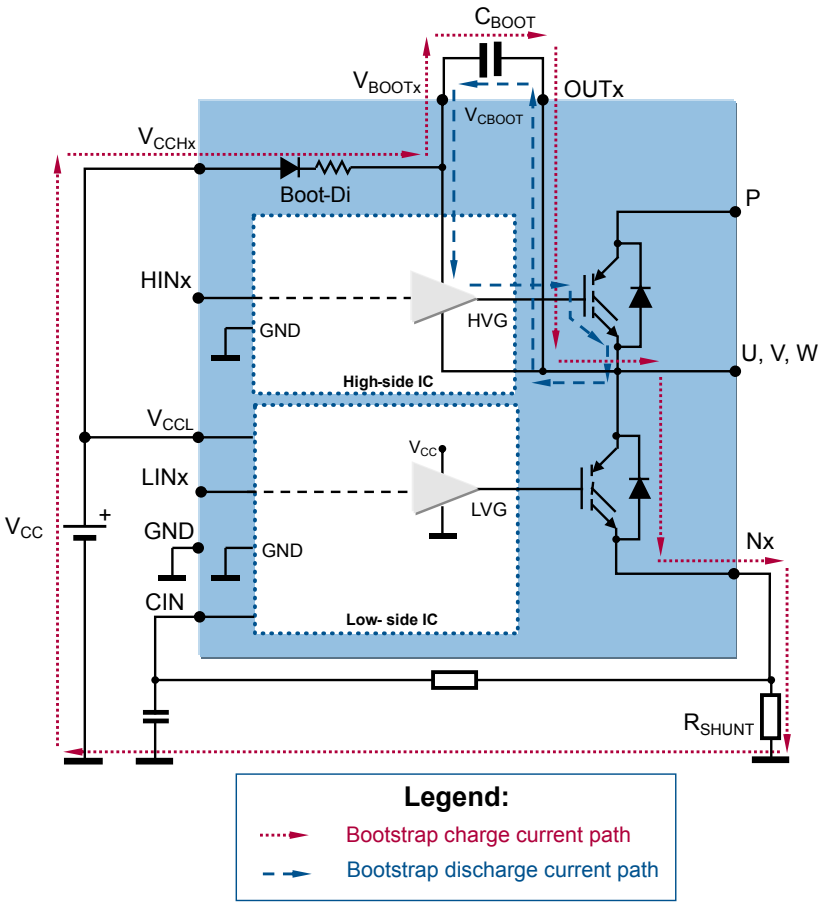


Table 9. **Electrical characteristic of bootstrap diode**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
V_{F_BS}	Bootstrap diode forward voltage	I_{F_BS} = 10 mA	0.4	0.9	1.4	V
R_{S_BS}	Bootstrap diode series resistor		12	20	28	Ω

The operation of the bootstrap circuit is shown in Figure 25. Bootstrap circuit. The floating supply capacitor C_{BOOT} is charged by the V_{CC} supply when V_{OUT} is lower than V_{CC} through the bootstrap diode with reference to the “bootstrap charge current path”. During the high-side IGBT on phase, the bootstrap circuit provides the right gate voltage to properly drive the IGBT (see “bootstrap discharge current path”). This circuit is iterated for all the three half-bridges.

Figure 25. **Bootstrap circuit**



2.14 Bootstrap capacitor selection

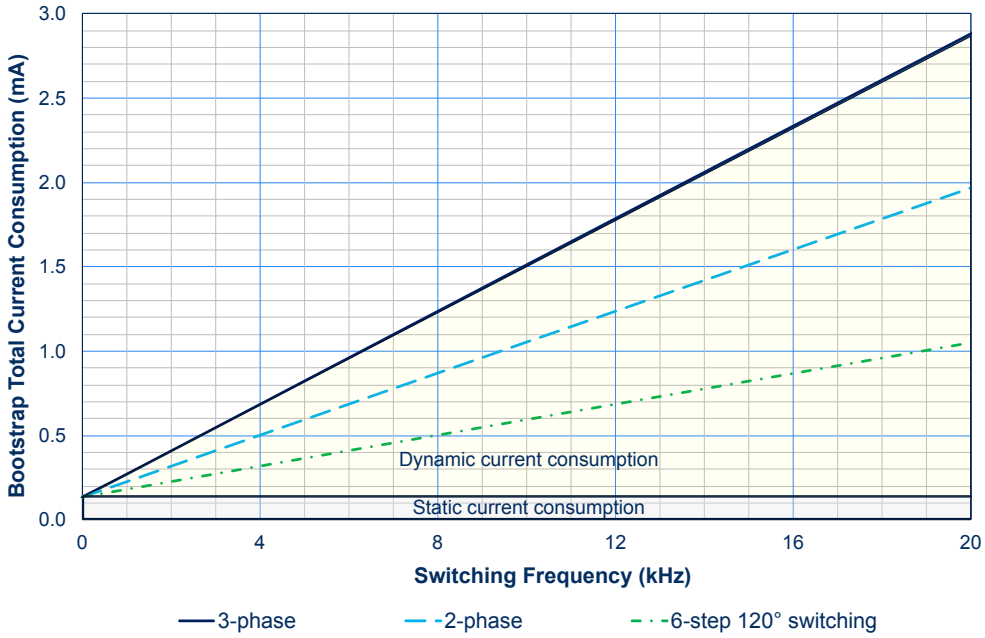
The value of the C_{BOOT} capacitor should be calculated according to the application condition and must take the following into account:

- The voltage across C_{BOOT} must be maintained at a value higher than the undervoltage lockout level ($V_{VBOOTx-OUTx\_H}$). This enables the high-side IGBT to work with the correct gate voltage (lower dissipation and better overall performances).
- The voltage across C_{BOOT} is affected by different components such as drop across the built-in bootstrap diode, drop across the low-side IGBT, and others (R_{SHUNT}, stray resistance, …).
- When the high-side IGBT is on, the C_{BOOT} capacitor discharges mainly to provide the right IGBT gate charge, but other phenomena must be considered such as leakage currents, quiescent current, etc.
- Bear in mind that if a voltage below the UVLO threshold is applied on the bootstrap channel, the HS gate driver disables its output without a fault signal.

A simple method to properly size the bootstrap capacitor involves the current absorbed by the bootstrap circuit during the normal operation and it includes a static consumption current, due to the IC gate driver and current leakages, and a dynamic consumption current, due to the IGBT gate charge operation mainly which is function of switching frequency.

Figure 26. Bootstrap total current consumption vs. switching frequency shows the total bootstrap consumption current of the STGIK50CH65T vs. switching frequency for the three main generic modulation techniques (3-phase, 2-phase and 6-step 120° switching), under the following conditions: V_{CC} = $V_{VBOOTx-OUTx}$ = 15 V, T_J = 125 °C and duty cycle of 50%.

Figure 26. **Bootstrap total current consumption vs. switching frequency**



The bootstrap voltage is referred to the inverter output voltage, which is function of IGBT $V_{CE(sat)}$ (in the case of current flowing out of the leg) or of the FRD V_F (in the case of current flowing into the leg). Both parameters are function of output currents and frequency, in addition to the switching frequency and the modulation techniques. Therefore, the bootstrap discharging voltage drop ($\Delta V_{CBOOT\_discharge}$) in one output period is given by:

Equation 12

$$\Delta V_{CBOOT\_discharge} = \frac{I_{BOOT} \cdot t_{discharge}}{C_{BOOT}} \quad (12)$$

Where I_{BOOT} is the total bootstrap consumption current, $t_{discharge}$ is the total discharging time in one output period.

Finally, the calculated bootstrap capacitor is showed in Figure 27. Calculated C_{BOOT} for 3-phase sinusoidal PWM, Figure 28. Calculated C_{BOOT} for 2-phase PWM (B type) and Figure 29. Calculated C_{BOOT} for 6-step 120° switching PWM according with the modulation techniques, as function of output frequency, switching frequency and bootstrap discharging voltage drop.

Figure 27. Calculated C_{BOOT} for 3-phase sinusoidal PWM

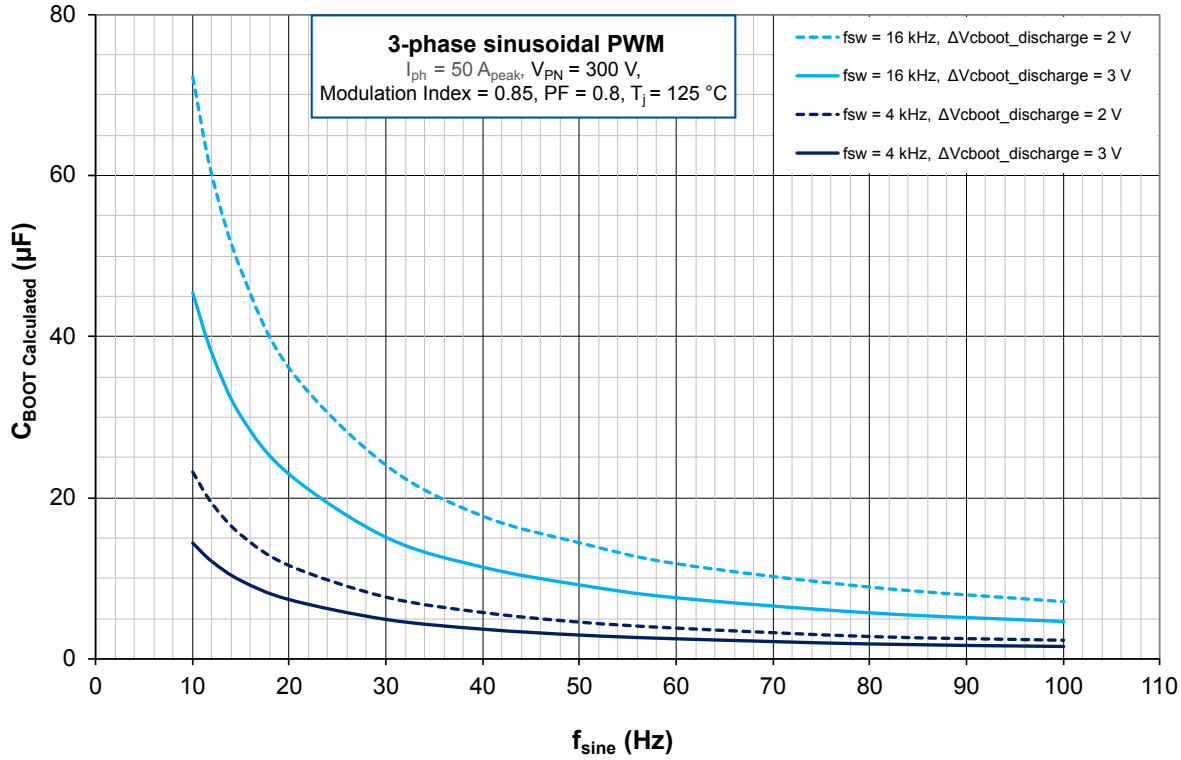


Figure 28. Calculated C_{BOOT} for 2-phase PWM (B type)

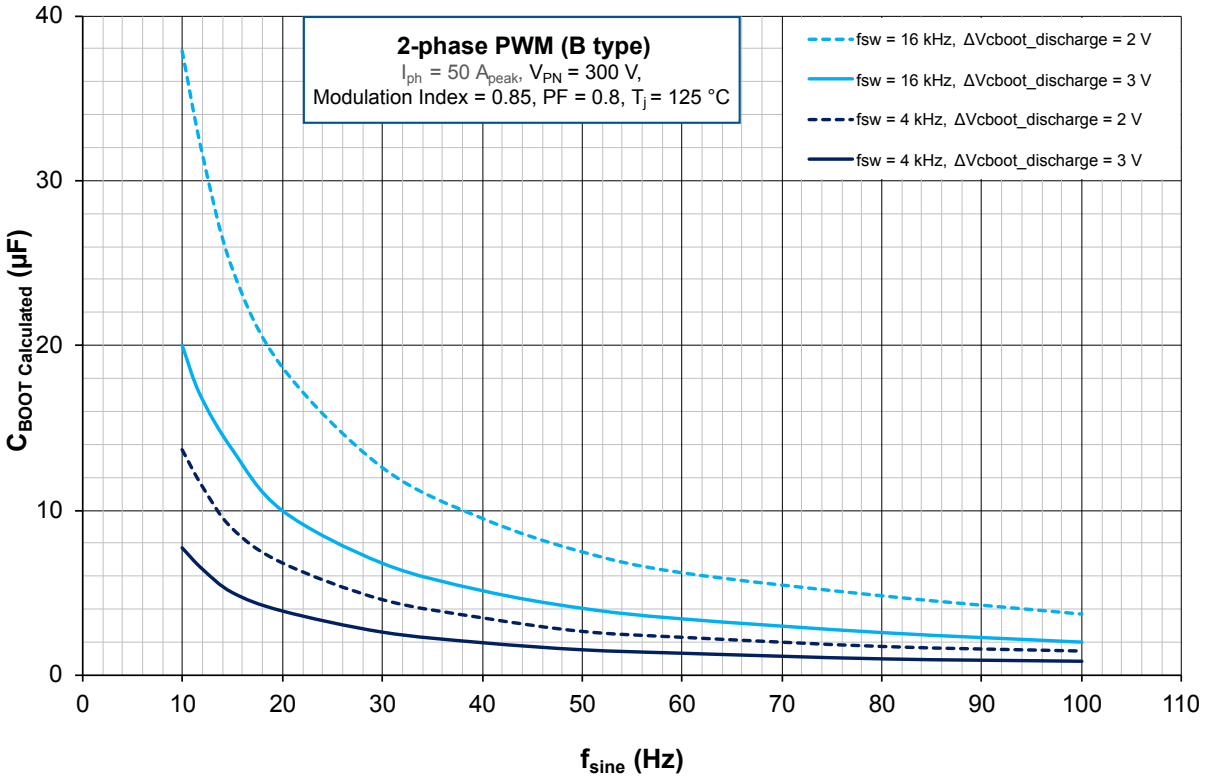
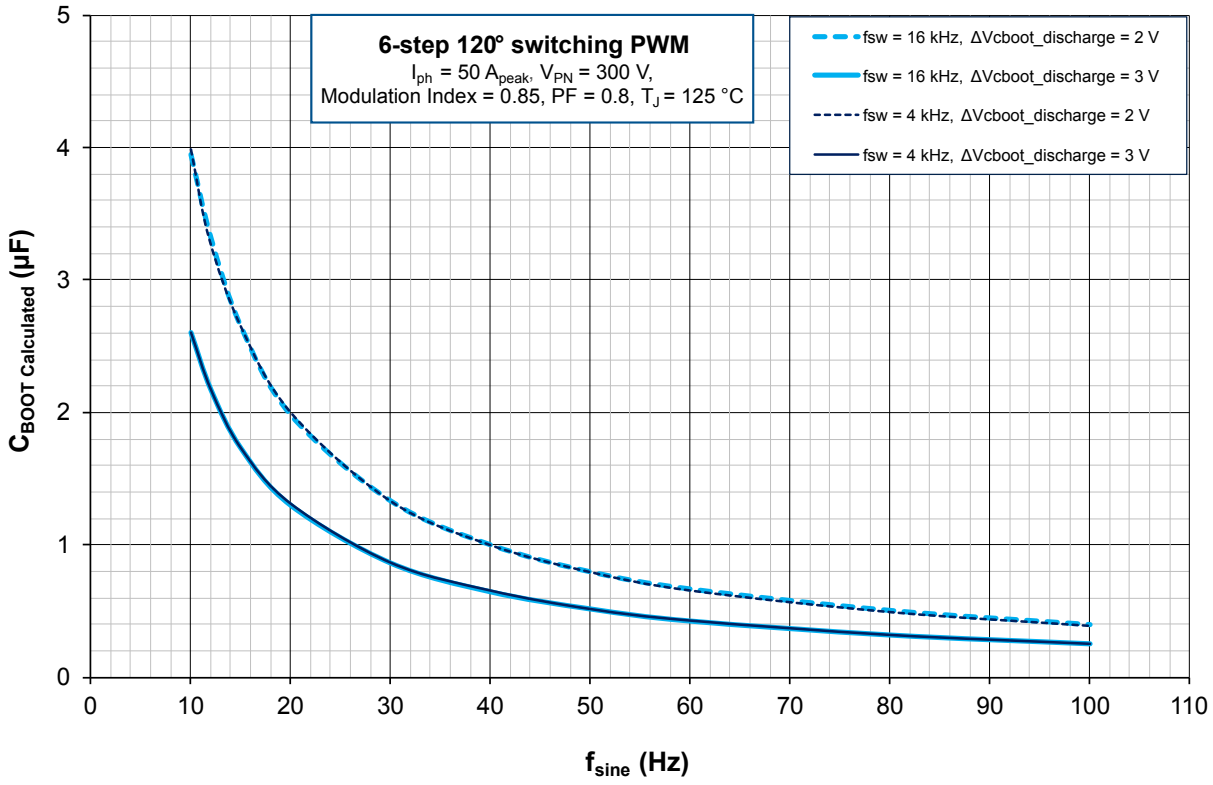


Figure 29. Calculated C_{BOOT} for 6-step 120° switching PWM



Since the bootstrap capacitor leakage is not taken into account in the calculations, and considering further leakage and dispersion in the board layout, the capacitance value for the bootstrap circuit should margined versus the calculated one.

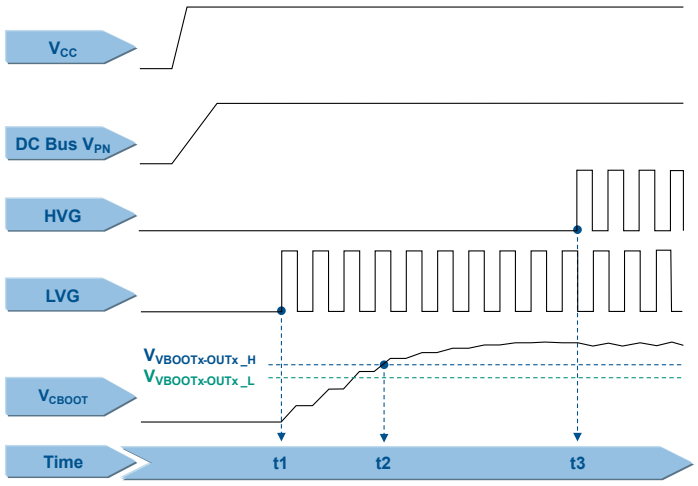
2.15 Initial bootstrap capacitor charging

During the startup phase, the bootstrap capacitor must be charged long enough to complete the initial charging time (t_{CHARGE}), which is at least the time V_{CBOOT} needs to exceed the turn-on undervoltage threshold $V_{VBOOTx-OUTx\_H}$.

For normal operation, the voltage across the bootstrap capacitor must never drop down to the turn-off undervoltage threshold $V_{VBOOTx-OUTx\_L}$.

During startup, only the low-side IGBT is switched on and the PWM is run immediately after this phase, as shown by the sequence in the Figure 30. Initial bootstrap charging time.

Figure 30. Initial bootstrap charging time



The timing chart is based on the following steps:

- t1: the bootstrap capacitor starts to charge through the low-side IGBT
- t2: the voltage across the bootstrap capacitor (V_{CBOOT}) reaches its turn-on undervoltage threshold $V_{BOOTx-OUTx\_H}$ in a time given by Equation 13.

Equation 13

$$t2 \approx \frac{C_{BOOT} \cdot R_{S\_BS}}{\delta} * ln\left(\frac{V_{CC}}{V_{CC} - V_{VBOOTx-OUTx\_HS}}\right) \quad (13)$$

Where δ is the duty cycle of the PWM signal and R_{S_BS} is the bootstrap diode series resistor (20 Ω typical value), as per the datasheet.

- t3: the bootstrap capacitor is fully charged, following Equation 14, this enables the high-side IGBT and the C_{BOOT} capacitor starts discharging in order to provide the right IGBT gate charge. The bootstrap capacitor recharges during the on state of the low-side IGBT.

Equation 14

$$t3 \geq 3 * \frac{C_{BOOT} \cdot R_{S\_BS}}{\delta} \quad (14)$$

A practical example can be analyzed by considering a motor drive application using a 3-phase PWM modulation, with a switching frequency of 10 kHz and output frequency of 60 Hz ($\Delta V_{CBOOT\_discarge}$ = 3 V). From the graph in Figure 27. Calculated C_{BOOT} for 3-phase sinusoidal PWM, the calculated bootstrap capacitance is 8 µF so C_{BOOT} can be chosen at least 10 µF.

Considering a V_{CC} = 15 V and a duty cycle of 0.5 for this initial charging phase, the initial charging time to reach the bootstrap voltage threshold (12.8 V max. value as per the datasheet) is:

Equation 15

$$t2 \approx \frac{10 \cdot 10^{-6} \cdot 20}{0.5} \cdot \ln\left(\frac{15}{15 - 12.8}\right) = 767\mu s \quad (15)$$

In addition, the time required to fully charge the bootstrap capacitor.

Equation 16

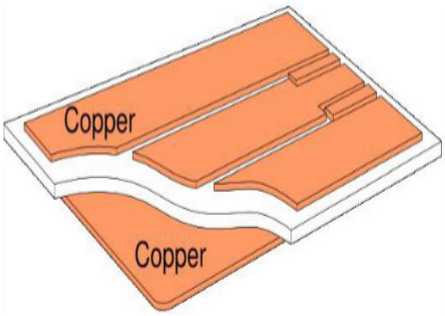
$$t3 \geq 3 * \frac{10 \cdot 10^{-6} \cdot 20}{0.5} = 1.2ms \quad (16)$$

3 SDIPHP-30L package

The SLLIMM high power benefits from a compact package while providing high power density, the best thermal performance, and high electrical isolation (≥ 2500 V_{RMS}).

The SDIPHP 30L is a dual in line 30 leads with DBC substrate (Direct Bonded Copper, see Figure 31. DBC structure) based on transfer mold package, able to achieve extremely low thermal resistance values, high quality and high stability in thermal cycling for the power stage along with a lead frame structure for the control stage.

Figure 31. DBC structure



The advantages of DBC substrates are:

- high current-carrying capability, due to thick copper metallization
- a thermal expansion coefficient close to the silicon value at the copper surface.

The DBC process yields a super-thin base and eliminates the need for the thick, heavy copper bases used prior to this process.

The main properties of DBC include:

- good adhesion
- corrosion resistance
- excellent electrical isolation
- high thermal conductivity
- a thermal expansion coefficient similar to that of the silicon, so no interface layers are required
- good heat diffusion
- environmentally friendly

A vacuum soldering process is used to avoid the inclusion of any gas (voids) during the soldering process that could cause potential hot spots. This results in a further increase in the reliability of the family due to the improved thermal and electrical conductivity.

3.1 Package structure

The Figure 32. SDIPHP-30L external and internal representation illustrates the external and internal structure of the SDIPHP-30L package.

Figure 32. SDIPHP-30L external and internal representation

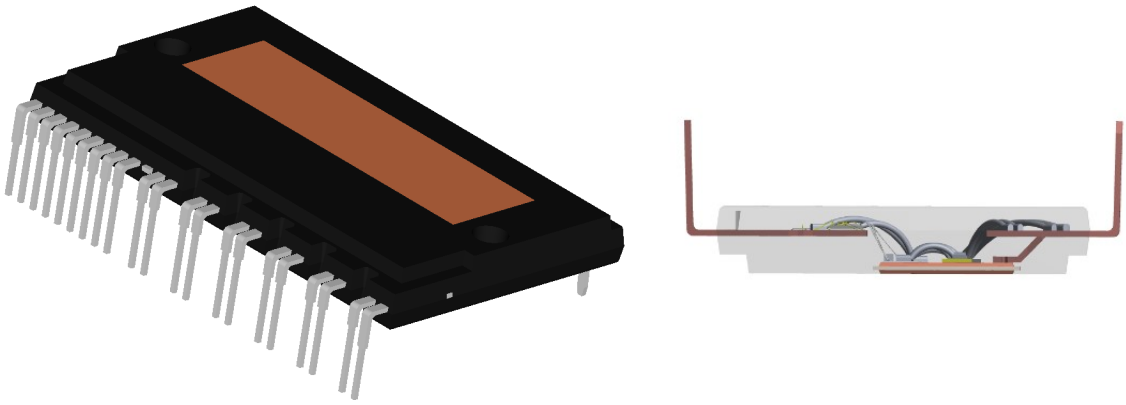
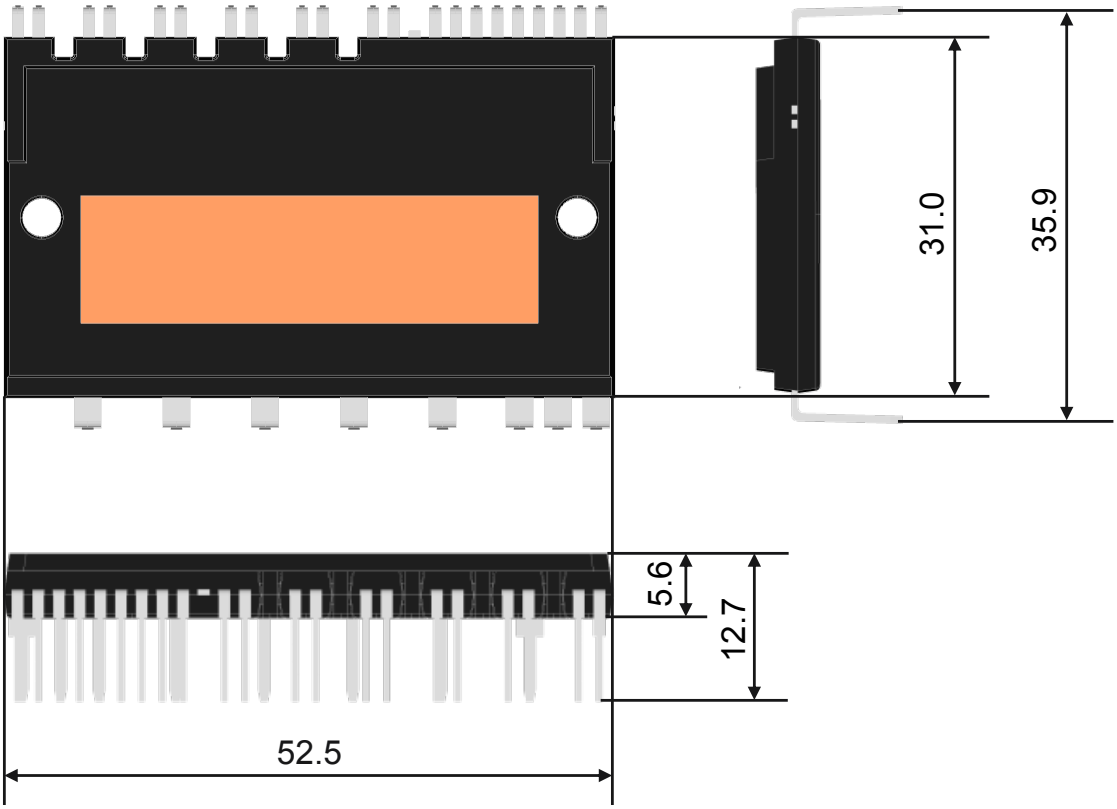


Figure 33. SDIPHP-30L main dimensions shows the main dimensions of the SDIPHP-30L package.

Figure 33. SDIPHP-30L main dimensions



All dimensions (typical measurements) are expressed in mm.

For further package outline details and dimensions, refer to the STGIK50CH65T datasheet.

3.2 Input and output pin descriptions

This section defines the SLLIMM high power input and output pins. For a more accurate description and layout suggestions, consult the relevant sections.

Table 10. SDIPHP-30L input and output pins

Pin	Symbol	Description
1	OUTu	High-side reference Output for U phase
2	VBOOTu	Bootstrap voltage for U phase (1)
3	VCCHu	High-side voltage power supply for U phase
4	HINu	High-side logic input for U phase
5	OUTv	High-side reference Output for V phase
6	VBOOTv	Bootstrap voltage for V phase (2)
7	VCCHv	High-side voltage power supply for V phase
8	HINv	High-side logic input for V phase
9	OUTw	High-side reference Output for W phase
10	VBOOTw	Bootstrap voltage for W phase (3)
11	VCCHw	High-side voltage power supply for W phase
12	HINw	High-side logic input for W phase
13	NC	Not Connected (Cut pin)
14	T	NTC Thermistor Output
15	LINu	Low-side logic input for U phase
16	LINv	Low-side logic input for V phase
17	LINw	Low-side logic input for W phase
18	FO	Shutdown/Fault output
19	CFO	Capacitor for Fault output setting
20	CIN	Comparator input
21	GND	Ground
22	VCCL	Low-side voltage power supply
23	NW	Negative DC input for W phase
24	NV	Negative DC input for V phase
25	NU	Negative DC input for U phase
26	W	W phase output
27	V	V phase output
28	U	U phase output
29	P	Positive DC input
30	NC	Not connected

1. *External connections between OUTu and U leads is requested*
2. *External connections between OUTv and V leads is requested*
3. *External connections between OUTw and W leads is requested*

3.2.1 High-side bootstrap voltage

Pins: VBOOTu, VBOOTv, VBOOTw

- The bootstrap section is designed to facilitate a simple and efficient floating power supply, in order to provide the gate voltage signal to the high-side IGBTs.
- The SLLIMM high power family integrates the bootstrap diodes to save on cost, board space and number of components.
- The advantage of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side IGBTs.
- Each bootstrap capacitor is charged from the V_{CC} supply.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to these pins.
- The size of the bootstrap capacitor is strictly related to the application conditions. See Section 2.13 Bootstrap circuit for more information.

3.2.2 High-side reference output

Pins: OUTu, OUTv, OUTw

- Reference voltage for the bootstrap section.
- An external connection between OUTu, OUTv, OUTw and U, V, W leads, respectively, is requested.

3.2.3 Gate driver bias voltage

Pins: VCCHu, VCCHv, VCCHw, VCCL

- Control supply pins for the built-in high-side and low-side ICs.
- Separate supply.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low ESR, low ESL) filter capacitor should be mounted close to this pin.

3.2.4 Gate driver supply ground

Pin: GND

- Ground reference pin for the built-in ICs.
- Four pads internally connected to the four ICs
- Ground pin is also the reference for NTC thermistor (T pin)
- To avoid being affected by noise, the main power circuit current should not be allowed to flow through this pin (see Section 5.2 Layout suggestions).

3.2.5 Signal input

Pins: HINu, HINv, HINw; LINu, LINv, LINw;

- These pins control the operation of the built-in IGBTs.
- The signal logic is active high. The IGBT associated with each of these pins is turned on when a sufficient logic voltage (higher than a specific threshold) is applied to these pins.
- The external routing of each input should be as short as possible to protect the SLLIMM high power against noise and an RC filter is suggested to be placed as close as possible to each pin.

3.2.6 Internal comparator non-inverting

Pin: CIN

- The current sensing shunt resistor connected on each phase leg may be used by the internal comparator (pin CIN) to detect short-circuit current.
- The shunt resistor should be selected to meet the detection level requirements for the specific application.
- An RC filter (typically ~1 µs) should be connected to the CIN pin to eliminate noise.
- The connection length between the shunt resistor and CIN pin should be minimized.
- If a voltage signal higher than the specified V_{CIN_H} (see datasheet) is applied to this pin, the low-side IGBTs automatically turn off and the FO pin is pulled down (to inform the microcontroller).

3.2.7 Shutdown/fault output

Pin: FO

- The FO pin acts as an enable/disable pin and as fault output signal.
- The signal logic of the FO pin is active low. The SLLIMM high power shuts down if a voltage lower than a specific threshold is applied to this pin, leading each low-side IGBTs in off state.
- The FO status is also connected to the internal comparator status (see Section 2.7 Comparator for fault sensing and short-circuit protection function). When the comparator triggers, the FO pin is pulled down and acts as a fault.
- The FO voltage should be pulled up to the 3.3 V or 5 V logic power supply through a pull-up resistor.

3.2.8 Thermistor

Pin: T

- A co-packaged NTC thermistor is available for temperature monitoring purposes and connected to the T pin.
- The second terminal is internally connected to the internal ground.
- A simple voltage divider can be made with an external resistor in order to create a temperature-dependent voltage signal.
- The NTC thermistor is not able to sense rapid variations in IGBT junction temperature (due to the slow thermal dynamics).

3.2.9 Positive DC

Pin: P

- This is the DC-link positive power supply pin of the inverter and is internally connected to the collectors of the high-side IGBTs.
- To suppress the surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a snubber capacitor close to this pin (typically, high voltage, metal film capacitors of about 0.1 or 0.22 µF).

3.2.10 Negative DC input

Pins: NU, NV, NW

- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side IGBT emitters of each phase.
- The low-side IGBT emitters are also internally coupled to the IC signal ground through an effective protection able to improve the IPM robustness against the emitter below ground phenomenon.
- The power ground of the application should be separated from the logic ground of the system and reconnected at one specific point (star connection).

3.2.11 Phase output

Pins: U, V, W

- Inverter output pins for connection to the inverter load (e.g., motors).

3.3 Electrical isolation distances

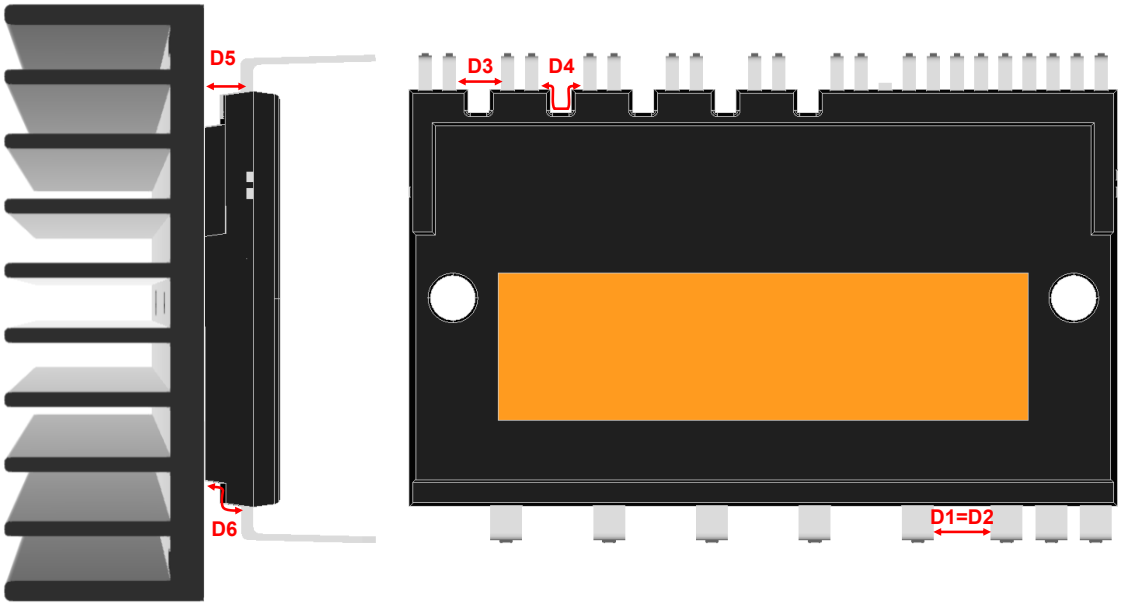
Table 11. Main electrical isolation distances (minimum values) shows the main electrical isolation distances (clearance and creepage) terminals to terminals and terminal to heat sink.

SLLIMM high power package benefits of transfer mold resin classified as material group I (CTI ≥ 600).

Table 11. Main electrical isolation distances (minimum values)

Clearance (mm)			Creepage (mm)		
D1	Between power terminals	3.6	D2	Between power terminals	3.6
D3	Between control terminals	2.67	D4	Between control terminals	6.17
D5	Between terminals and heat sink	3.0	D6	Between terminals and heat sink	4.2

Figure 34. Main isolation distances



4 Power loss and dissipation

The total power loss in an inverter is composed of conduction loss, switching loss and off-state loss and is essentially generated by the power devices of the inverter stage, such as the IGBTs and the fast recovery diodes. The conduction loss (P_{cond}) is the on-state loss generated during the conduction phase. The switching loss (P_{sw}) is the dynamic loss encountered during turn-on and turn-off. Off-state loss deriving from blocking voltage and leakage current can be ignored.

Total power loss is given by:

Equation 17

$$P_{tot} \approx P_{cond} + P_{sw} \quad (17)$$

Figure 35. Typical IGBT power losses and Figure 36. Typical FRD power losses show the typical waveforms for both IGBT and FRD and the major sources of power loss of an inductive hard switching application such as a motor drive.

Figure 35. Typical IGBT power losses

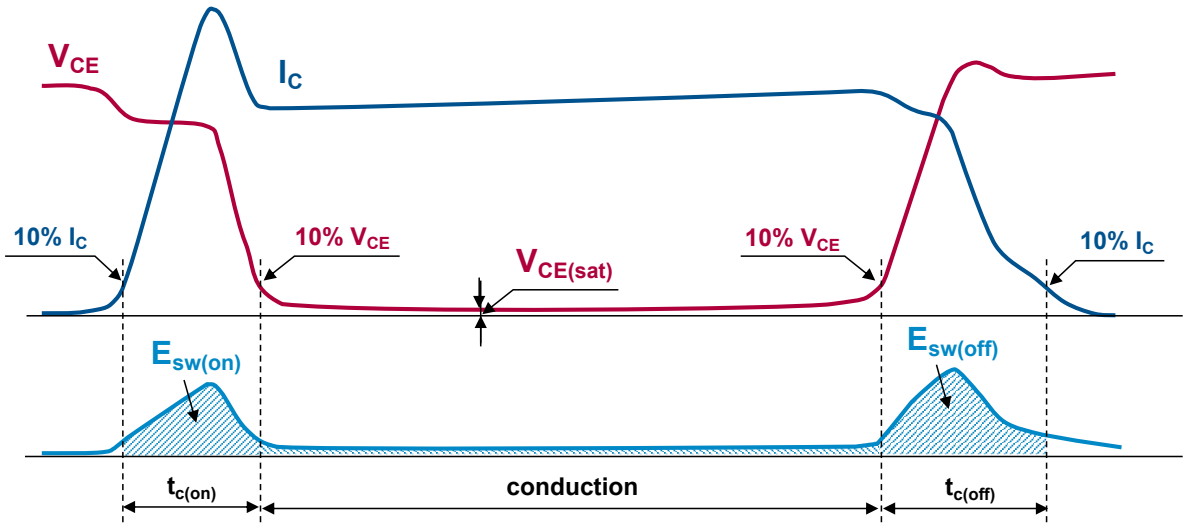
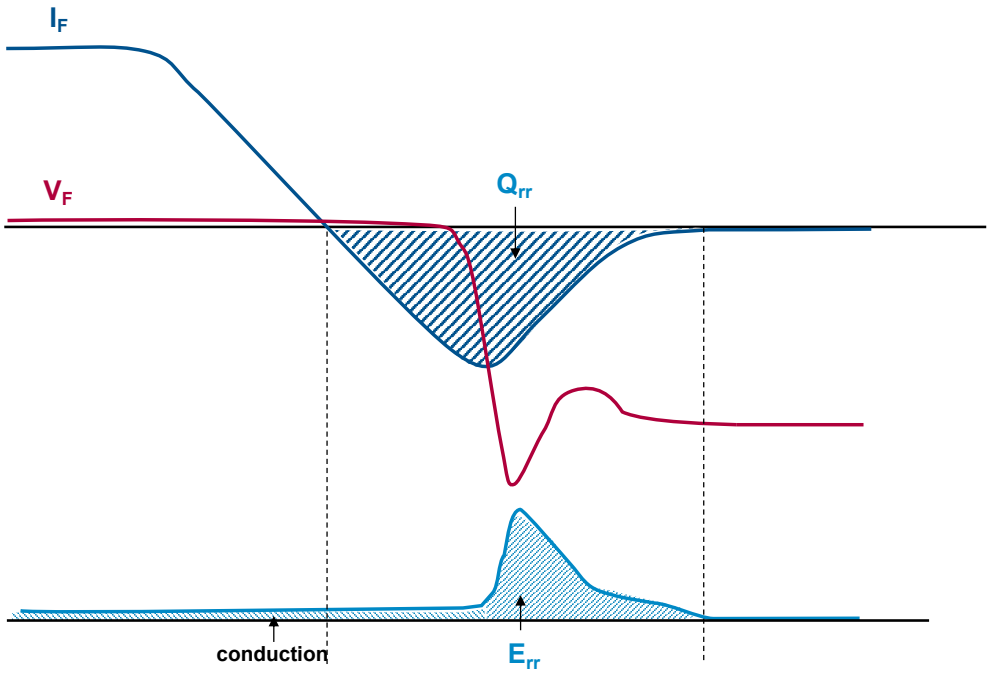


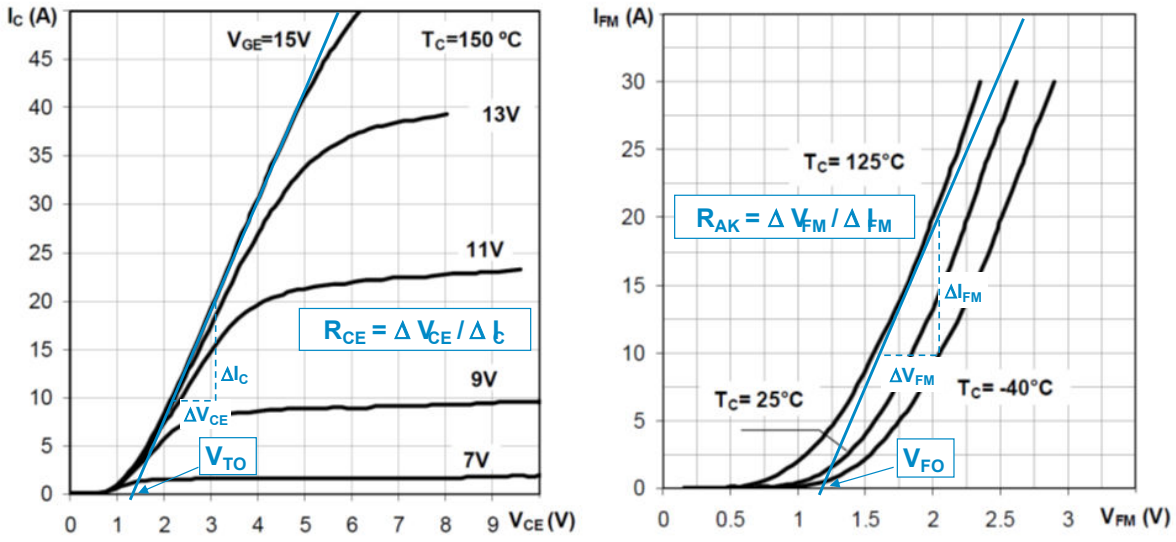
Figure 36. **Typical FRD power losses**



4.1 Conduction power loss

Conduction loss is caused by IGBT and fast recovery diode forward voltage drops at rated currents. They can be calculated using a linear approximation of the forward characteristics for both IGBT and diode, in a series connection with a DC voltage source representing the threshold voltage, V_{TO} for IGBT, (and V_{FO} for diode) and a collector emitter on-state resistance, R_{CE} (and R_{AK} anode cathode on-state resistance), as shown below for reference purposes.

Figure 37. **IGBT and diode generic output characteristics**



Both forward characteristics are temperature dependent, and so must be considered with respect to a specific temperature.

The linear approximations for IGBTs can be translated into the Equation 18:

Equation 18

$$v_{\mathrm{ce}}(i_c) = V_{\mathrm{TO}} + R_{\mathrm{CE}} \cdot i_c \quad (18)$$

and for fast recovery diodes:

Equation 19

$$v_{fm}(i_{fm}) = V_{FO} + R_{AK} \cdot i_{fm} \quad (19)$$

The conduction losses of IGBT and diode can be derived as the time integral of the product of conduction current and voltage across the devices, as such:

Equation 20

$$P_{\mathrm{cond\_IGBT}} = \frac{1}{T}\int_0^T v_{\mathrm{ce}} \cdot i_c(t)\mathrm{dt} = \frac{1}{T}\int_0^T \left(V_{\mathrm{TO}} \cdot i_c(t) + R_{\mathrm{ce}} \cdot i_c^2(t)\right)\mathrm{dt} \quad (20)$$

Equation 21

$$P_{cond\_Diode} = \frac{1}{T}\int_0^T v_f \cdot i_f(t)\,dt = \frac{1}{T}\int_0^T \left(V_{FO} \cdot i_f(t) + R_{AK} \cdot i_f^2(t)\right)dt \quad (21)$$

Where T is the fundamental period.

As differing SLLIMM utilization modes, modulation techniques and operating conditions complicate power loss estimation, it is necessary to set some initial conditions.

Assuming that:

- the application is a variable voltage variable frequency (VVVF) inverter based on sinusoidal PWM technique.
- the switching frequency is high and therefore the output currents are sinusoidal
- the load is ideal inductive

Under these conditions, the output inverter current is given by:

Equation 22

$$i = \hat{I}\cos(\theta\text{-}\varphi) \quad (22)$$

Where Î is the current peak, θ represents ωt and φ is the phase angle between output voltage and current.

The conduction power losses can be obtained from:

Equation 23

$$P_{\mathrm{cond\_IGBT}} = \frac{V_{\mathrm{TO}} \cdot \hat{I}}{2\pi}\int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} \xi\cos(\theta-\varphi)d\theta + \frac{R_{\mathrm{CE}} \cdot \hat{I}^2}{2\pi}\int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} \xi\cos^2(\theta-\varphi)d\theta \quad (23)$$

Equation 24

$$P_{cond\_Diode} = \frac{V_{FO} \cdot \hat{I}}{2\pi}\int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} (1-\xi)cos(\theta-\varphi)d\theta + \frac{R_{AK} \cdot \hat{I}^2}{2\pi}\int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi} (1-\xi)cos^2(\theta-\varphi)d\theta \quad (24)$$

Where ξ is the duty cycle for this PWM technique given by:

Equation 25

$$\xi = \frac{1 + m_a \cdot \cos\theta}{2} \quad (25)$$

Where m_a is the PWM amplitude modulation index.

Finally, solving for Equation 23 and Equation 24, we obtain:

Equation 26

$$P_{cond\_IGBT} = V_{TO} \cdot \hat{I}\left(\frac{1}{2\pi} + \frac{m_a \cdot cos\varphi}{8}\right) + R_{CE} \cdot \hat{I}^2\left(\frac{1}{8} + \frac{m_a \cdot cos\varphi}{3\pi}\right) \quad (26)$$

Equation 27

$$P_{cond\_Diode} = V_{FO} \cdot \hat{I}\left(\frac{1}{2\pi} - \frac{m_a \cdot cos\varphi}{8}\right) + R_{AK} \cdot \hat{I}^2\left(\frac{1}{8} - \frac{m_a \cdot cos\varphi}{3\pi}\right) \quad (27)$$

and therefore, the conduction power loss for a single device (IGBT and diode) is:

Equation 28

$$P_{cond} = P_{cond\_IGBT} + P_{cond\_Diode} \quad (28)$$

Of course, the total conduction loss for an inverter is the sum of the six switches contributions.

4.2 Switching power losses

The switching loss is the power consumption during the turn-on and turn-off transients. As already shown in Figure 37. IGBT and diode generic output characteristics, it is given by the pulse of power dissipated during turn-on (t_{on}) and turn-off (t_{off}).

Experimentally, it can be calculated by the time integral of the product of the collector current and collector-emitter voltage for the switching period. In any case, the dynamic performance is heavily dependent on several parameters including voltage, current temperature, so it is necessary to employ the same assumptions in Section 4.1 Conduction power loss to simplify the calculations.

Under these conditions, the switching energy losses for the IGBT are given by:

Equation 29

$$E_{on}(\theta) = \hat{E}_{on} cos(\theta\text{-}\varphi) \quad (29)$$

Equation 30

$$E_{off}(\theta) = \hat{E}_{off} cos(\theta\text{-}\varphi) \quad (30)$$

And for the FRD are:

Equation 31

$$E_{rr}(\theta) = \hat{E}_{rr} cos(\theta\text{-}\varphi) \quad (31)$$

Where $\hat{E}_{on}$, $\hat{E}_{off}$ and $\hat{E}_{rr}$ are the maximum values taken at $T_J$max. and $\hat{I}_C$ (or $\hat{I}_F$), θ equals ωt and φ is the phase angle between output voltage and current.

Finally, the switching power loss per device depends on the switching frequency (f_{sw}) and is calculated as follows:

Equation 32

$$P_{sw} = \frac{1}{2\pi}\int_{-\frac{\pi}{2}+\varphi}^{\frac{\pi}{2}+\varphi}\left(E_{on} + E_{off} + E_{rr}\right) \cdot f_{sw} d\theta = \frac{\left(E_{on} + E_{off} + E_{rr}\right) \cdot f_{sw}}{\pi} \quad (32)$$

Also in this case, the total switching loss per inverter is the sum of the six switches contributions.

A simple and fast way to calculate the power loss is using the simulation software ST PowerStudio (see Section 4.5 STPOWER Studio Simulation Software).

4.3 Thermal impedance overview

During operation, power losses generate heat which elevates the temperature in the internal semiconductor junctions, limiting its performance and lifetime. To ensure safe and reliable operation, the junction temperature of power devices must be kept below the limits defined in the datasheet, therefore, the generated heat must be conducted away from the power chips and into the environment using an adequate cooling system.

The most common schemes are based on one heat sink designed for free conventional air flow or, in some cases, for forced air circulation. Free conventional air flow systems require larger heat sinks (about 50% bigger) than a forced air based heat sink, for a given thermal resistance. Therefore, the choice of the cooling system becomes the starting point for the application designer and the thermal aspect of the system is one of the key factors in designing high efficiency and high reliability equipment. In this respect, the package and its thermal resistance play a fundamental role.

Thermal resistance quantifies the ability of a given thermal path to transfer heat in the steady-state and is generally expressed as the ratio between the temperature increase above the reference and the relevant power flow:

Equation 33

$$R_{th} = \frac{\Delta T}{\Delta P} \tag{33}$$

The thermal resistance specified in the datasheet is the junction-case R_{thJC}, defined as the temperature difference between the junction and case reference divided by the total power dissipation per device:

Equation 34

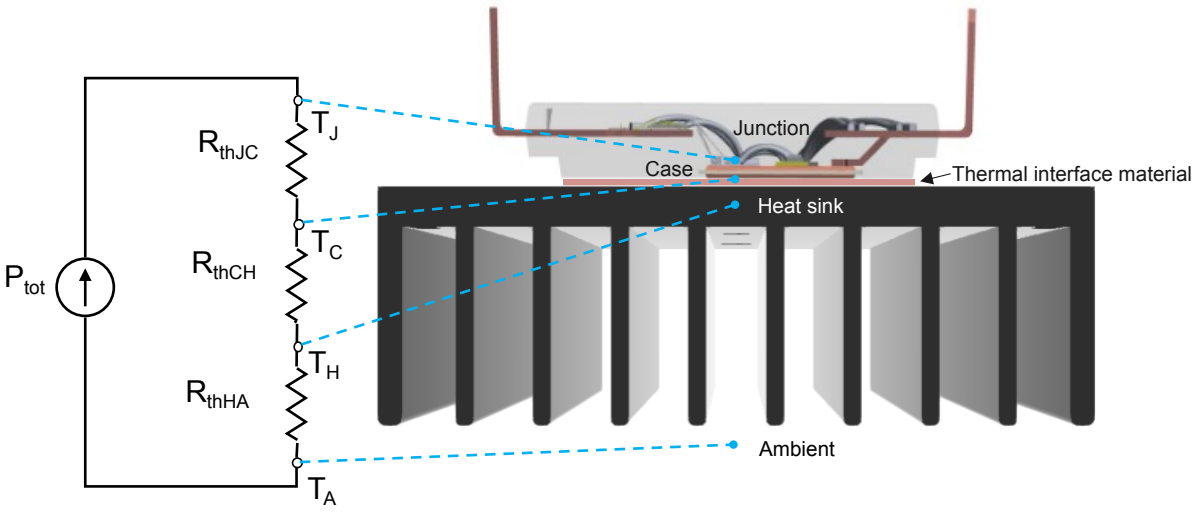
$$R_{thJC} = \frac{T_j - T_c}{P_{TOT\_IPM}} \tag{34}$$

The SLLIMM high power benefits from a state of the art DBC substrate offering a very low R_{thJC} value. The backside of the DBC substrate is used as the cooling interface to the heat sink.

Thermal grease or some other thermal interface material between the backside and the heat sink is used to reduce the thermal resistance of the interface (R_{thCH}) and, of course, depends on the material and its thickness.

Basically, the sum of the three thermal resistance components above gives the thermal resistance between junction and ambient R_{thJA}, as shown in the Figure 38. Equivalent thermal circuit with heat sink single IGBT.

Figure 38. Equivalent thermal circuit with heat sink single IGBT



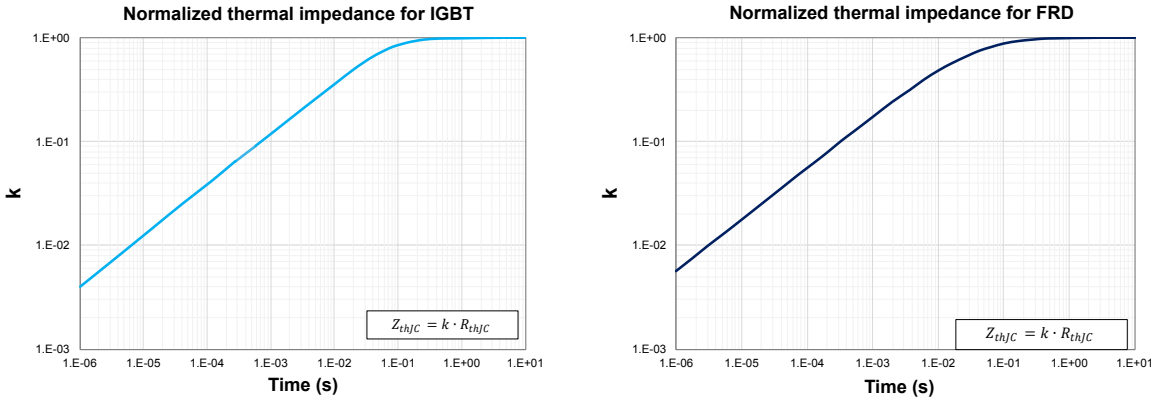
As the power loss P_{tot} is cyclic, the transient thermal impedance must also be considered. It is defined as the ratio of the time dependent temperature increase ΔT(t) above the reference and the relevant heat flow:

Equation 35

$$Z_{th}(t) = \frac{\Delta T(t)}{\Delta P} \tag{35}$$

Contrary to what we have already seen regarding thermal resistance, thermal impedance is typically represented by an RC equivalent circuit. For pulsed power loss, the thermal capacitance effect delays the rise in junction temperature and therefore the advantage of this behavior is the short-term overload capability of the SLLIMM high power.

Figure 39. Normalized thermal impedance curves



More generally, in the case of the device, power is time dependent too. The device temperature can be calculated via the convolution integral method applied to the Equation 36 thus:

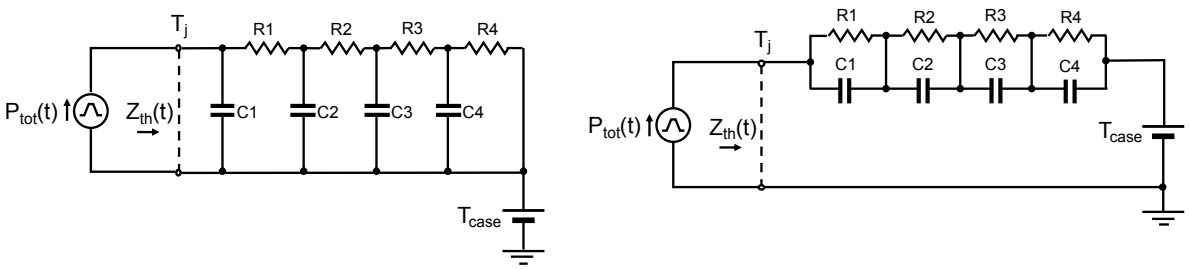
Equation 36

$$\Delta T(t) = \int_0^t Z_{\text{th}}(t-\tau) \cdot P(\tau) d\tau \tag{36}$$

An alternative and very useful method for simulator tools, is the transient thermal impedance model, which provides a simple method for estimating the junction temperature rise under a transient condition.

By using the thermo-electrical analogy, the transient thermal impedance Zth(t) can be transformed into an electrical equivalent RC network. The number of RC sections increases the model detail, therefore a fourth order models based on the Cauer and Foster networks have been adopted to improve the accuracy of the model, as shown in the Figure 40. Thermal impedance RC Cauer and Foster thermal networks.

Figure 40. Thermal impedance RC Cauer and Foster thermal networks



RC Cauer thermal network

RC Foster thermal network

Temperatures inside the electrical RC network represent voltages, power flows represent currents, electrical resistances and capacitances represent thermal resistances and capacitances, respectively. The case temperature is represented with a DC voltage source and can be interpreted as the initial junction temperature.

Transient thermal impedance models are derived by curve fitting an equation to the measured data. Values for the individual resistors and capacitors are the variables from this equation and are defined for each device in Table 12. RC Cauer and Foster thermal network elements of STGIK50CH65T.

Table 12. RC Cauer and Foster thermal network elements of STGIK50CH65T

Element	IGBT		FRD	
	Cauer	Foster	Cauer	Foster
R1 (°C/W)	9.75E-02	1.72E-01	1.81E-01	5.19E-01
R2 (°C/W)	4.10E-01	7.88E-02	7.20E-01	9.33E-01
R3 (°C/W)	4.00E-01	2.15E-01	8.25E-01	1.43E-01
R4 (°C/W)	8.88E-02	5.30E-01	2.68E-01	3.99E-01
C1 (W·s/°C)	2.36E-03	1.03E+00	5.30E-04	5.76E-03
C2 (W·s/°C)	2.18E-02	2.63E-03	4.43E-03	2.82E-02
C3 (W·s/°C)	8.36E-02	3.36E-02	2.84E-02	5.96E-04
C4 (W·s/°C)	1.85E+00	8.02E-02	5.74E-01	4.12E-01

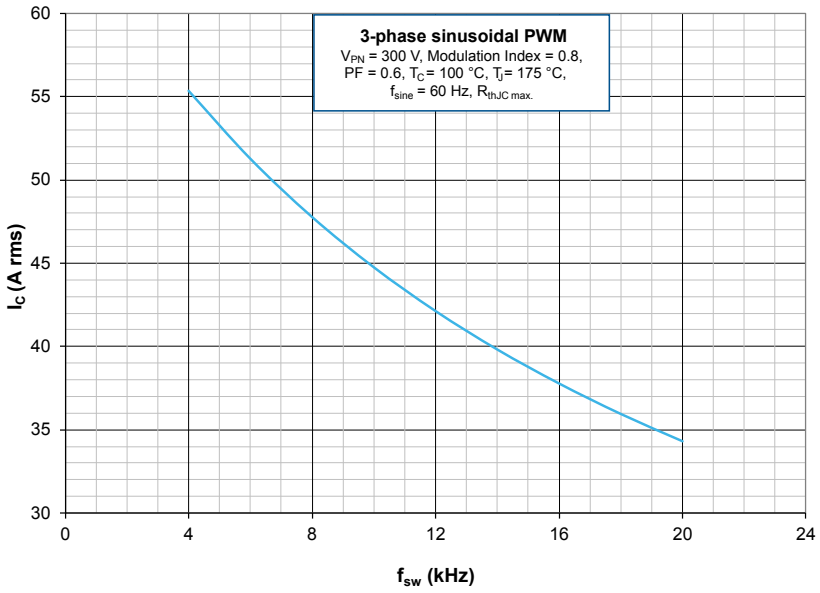
4.4 Power loss calculation example

From the power loss calculation and thermal aspects detailed in the previous sections, we can simulate the maximum $I_{C(RMS)}$ current versus switching frequency curves for an inverter using a 3-phase continuous PWM modulation to synthesize sinusoidal output currents.

The curve in Figure 41. Maximum I_C(RMS) vs. fsw simulated curves represents the maximum current managed by the SLLIMM high power under safe conditions, when the junction temperature rises to 50 °C (maintaining a good margin from the 175 °C maximum junction temperature for SLLIMM high power) and the case temperature is 100 °C, which is a typical operating condition to guarantee the reliability of the system.

This curve, function of the motor drive topology and control scheme, is simulated under the conditions reported in the figure, with typical power loss.

Figure 41. Maximum I_C(RMS) vs. fsw simulated curves



4.5 STPOWER Studio Simulation Software

STPOWER Studio is a dynamic electrothermal simulation tool dedicated to STPOWER devices. This tool is part of eDesignSuite, the ST official platform for the simulators, and it provides a comprehensive power and thermal analysis, which allows the user to predict the device performance, shorten the solution design and save time and resources. Furthermore, the tool helps to select the proper device that fits the application mission profile. The Figure 42. STPOWER Studio graphical user interface shows the GUI.

Figure 42. STPOWER Studio graphical user interface

GADG070220231320SA

Note: Please use this link www.st.com for eDesignSuite platform.

Based on a very precise built-in electrical and thermal model and on an iterative calculation, taking into account self-heating effects, STPOWER Studio provides a highly accurate estimation of the power loss as well as the junction and case temperatures.

The tool can simulate a mission profile by setting the input conditions and performing a very long simulation time.

STPOWER Studio allows the simulation of several thermal setup input conditions, such us:

- Devices without heat sink, by estimating the case and junction temperatures
- Fixed case temperature (with heat sink), by estimating the junction temperature and the heat sink Rth
- Fixed heat sink thermal resistance, by estimating the case and junction temperatures
- Fixed heat sink thermal impedance, by estimating the case and junction temperatures and considering the thermal inertia of the system

Simulation results are displayed in tables and dedicated scope views, in function of the time, the current load and the switching frequency. An output report can be generated, which summarizes all information and results to allow easy archiving.

STPOWER Studio currently enables the 3-phase 2-level topology with a sinusoidal PWM technique and supports a large selection of power devices (SLLIMM and ACEPAK) and facilitates the connectivity with st.com for dedicated documentations and resources. An on-line forum provides additional support to STPOWER Studio users.

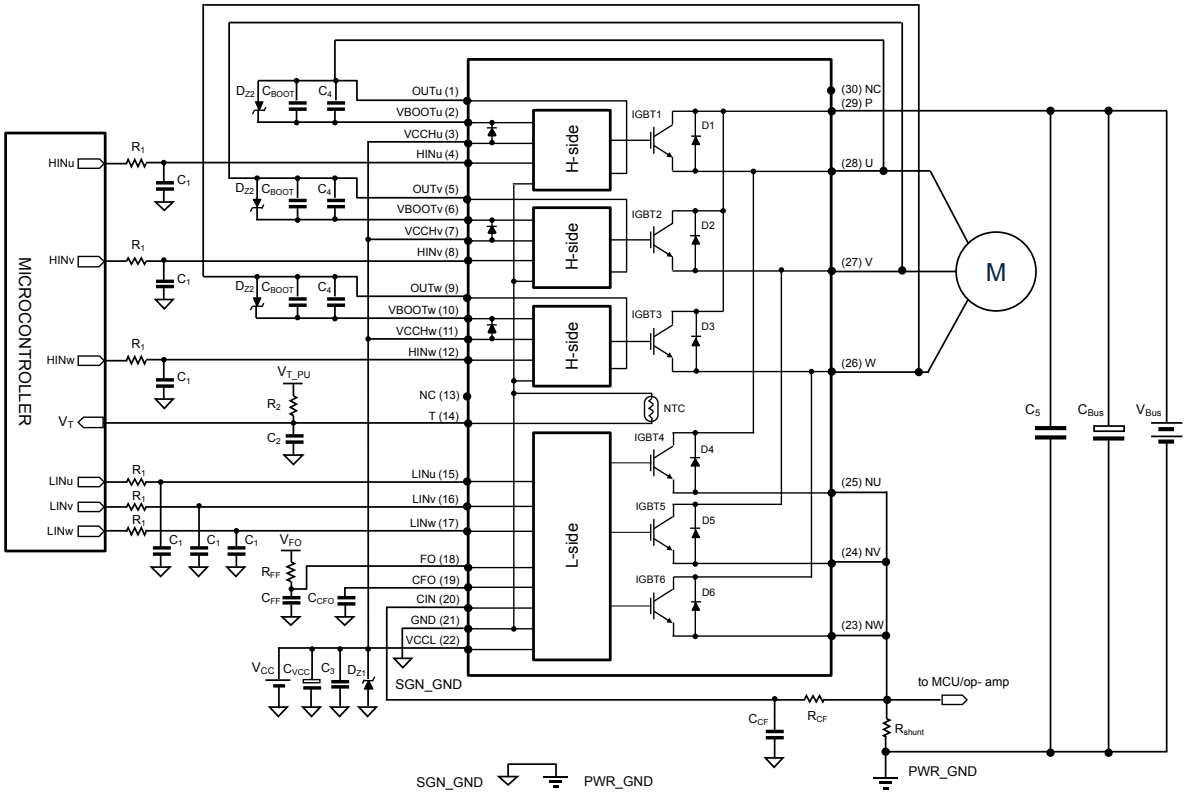
5 Design and mounting guidelines

This section provides suggestions regarding typical circuits, optimized design layouts and important mounting recommendations to aid in the appropriate handling and assembly of the SLLIMM high power series family.

5.1 Typical circuit and recommendations

Figure 43. Typical application circuit shows a typical application circuit using SLLIMM high power with signal interfaces with the MCU.

Figure 43. Typical application circuit



Below are some hardware and PCB layout recommendations:

1. External connections between the pins OUTu-U, OUTv-V and OUTw-w are required.
2. Input signals HIN, LIN are active-high logic. A 20 kΩ (typ.) pull-down resistor is built-in for each input pin. To prevent input signal oscillation, the wiring of each input should be as short as possible and the use of RC filters (R_1, C_1) on each input signal is suggested. The filters should be done with a time constant of about 100 ns and placed as close as possible to the IPM input pins.
3. The use of a bypass capacitor C_{VCC} (aluminum or tantalum) can help reduce the transient circuit demand on the power supply. Also, to reduce high frequency switching noise distributed on the power lines, it is suggested to place a decoupling capacitor C_3 (100 to 220 nF, with low ESR and low ESL), as close as possible to each V_{CC} pin and in parallel with the bypass capacitor.
4. The use of RC filter (R_{CF}, C_{CF}) for preventing protection circuit malfunction is suggested. The time constant (R_{CF} x C_{CF}) should be set to 1 µs and the filter must be placed as close as possible to the CIN pin.

5. The FO is an input/output pin. It should be pulled up to a power supply (i.e., MCU bias at 3.3/5 V) by a resistor value able to match the V_{FO_L} and V_{FO_H} threshold voltages mainly. In case of 3.3 or 5 V pull up voltage, the suggested resistor value is from 5.6 kΩ to 68 kΩ. The RC filter on FO could have also impact on the re-starting time after a fault event so it must be placed as close as possible to the FO pin.
6. A decoupling capacitor C_2 between 1 nF and 10 nF can be used to increase the noise immunity of the signal on the NTC thermistor. Its effectiveness is improved if the capacitor is placed close to the MCU.
7. The decoupling capacitor C_4 (100 to 220 nF with low ESR and low ESL) in parallel with each C_{BOOT} is useful to filter high frequency disturbances. Both C_{BOOT} and C_4 (if present) should be placed as close as possible to each U, V, W and respective V_{BOOT} pins.
8. To prevent overvoltage on the V_{CC} pins, a Zener diode (D_{Z1}) can be used. Similarly, on the V_{BOOT} pins, a Zener diode (D_{Z2}) can be placed in parallel with each C_{BOOT}.
9. The use of the decoupling capacitor C_5 (100 to 220 nF, with low ESR and low ESL) in parallel with the electrolytic capacitor C_{Bus} is useful to prevent surge destruction. Both capacitors C_5 and C_{Bus} should be placed as close as possible to the IPM (C_5 has priority over C_{Bus}).
10. When the application requires a galvanic isolation between low and high voltage, use of high speed (high CMR) opto-coupler is recommended.
11. Low inductance shunt resistors should be used for phase leg current sensing.
12. In order to avoid malfunction, the wiring between N pins, the shunt resistor and PWR_GND should be as short as possible.
13. The connection of SGN_GND to PWR_GND at only one point (close to the shunt resistor terminal) can help to reduce the impact of power ground fluctuation.
14. Parallel connection of switches or legs on the same or multiple IPMs is not suggested.

5.2 Layout suggestions

PCB layout optimization for high voltage, high current and high switching frequency applications is a critical factor. PCB layout is a complex matter involving several aspects such as track length and width and circuit areas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application function properly and achieve expected performance. On the other hand, PCBs without careful layout can generate EMI issues (both induced and perceived by the application), can provide overvoltage spikes due to parasitic inductances along the PCB traces, and can produce higher power loss and even malfunction in the control and sensing stages.

The compactness of the SLLIMM high power solution, which offers an optimized gate driving network and reduced parasitic elements, allows designers to concentrate on other issues such as the ground or noise filter. In any case, to avoid the aforementioned conditions, the following general PCB layout guidelines and suggestions should be followed for 3-phase applications.

For more information please refer to application note AN4694.

5.3 General suggestions

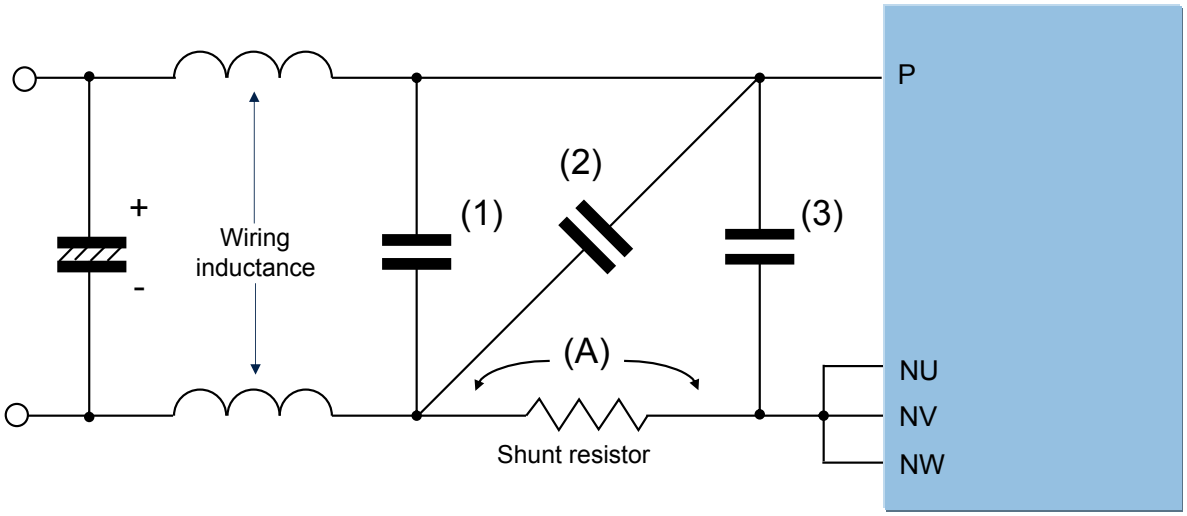
1. PCB traces should be designed as short as possible and the area of the circuit (power or signal) minimized to reduce the sensitivity of such structures to surrounding noise.
2. Ensure a good distance between switching lines with high voltage transitions and the signal lines sensitive to electrical noise. Specifically, the tracks of each OUT phase carrying significant currents and voltages should be separated from logic lines and analog op amp and comparator sensing circuits.
3. Place the R_{SHUNT} resistors as close as possible to the low-side pins of the SLLIMM high power (NU, NV and NW).

Parasitic inductance can be minimized by connecting the ground line (also called driver ground) of the IPM directly to the cold terminal of shunt resistors. Use a low inductance type resistor, such as an SMD resistor instead of long-lead type resistors, to help further decrease parasitic inductance.

1. Avoid any ground loop. Only a single path must connect two different ground nodes.
2. Place each RC filter as close as possible to the SLLIMM high power pins in order to increase their efficiency.
3. Fixed voltage tracks such as GND or HV lines can be used to shield the logic and analog lines from electrical noise produced by the switching lines (e.g., U, V and W).

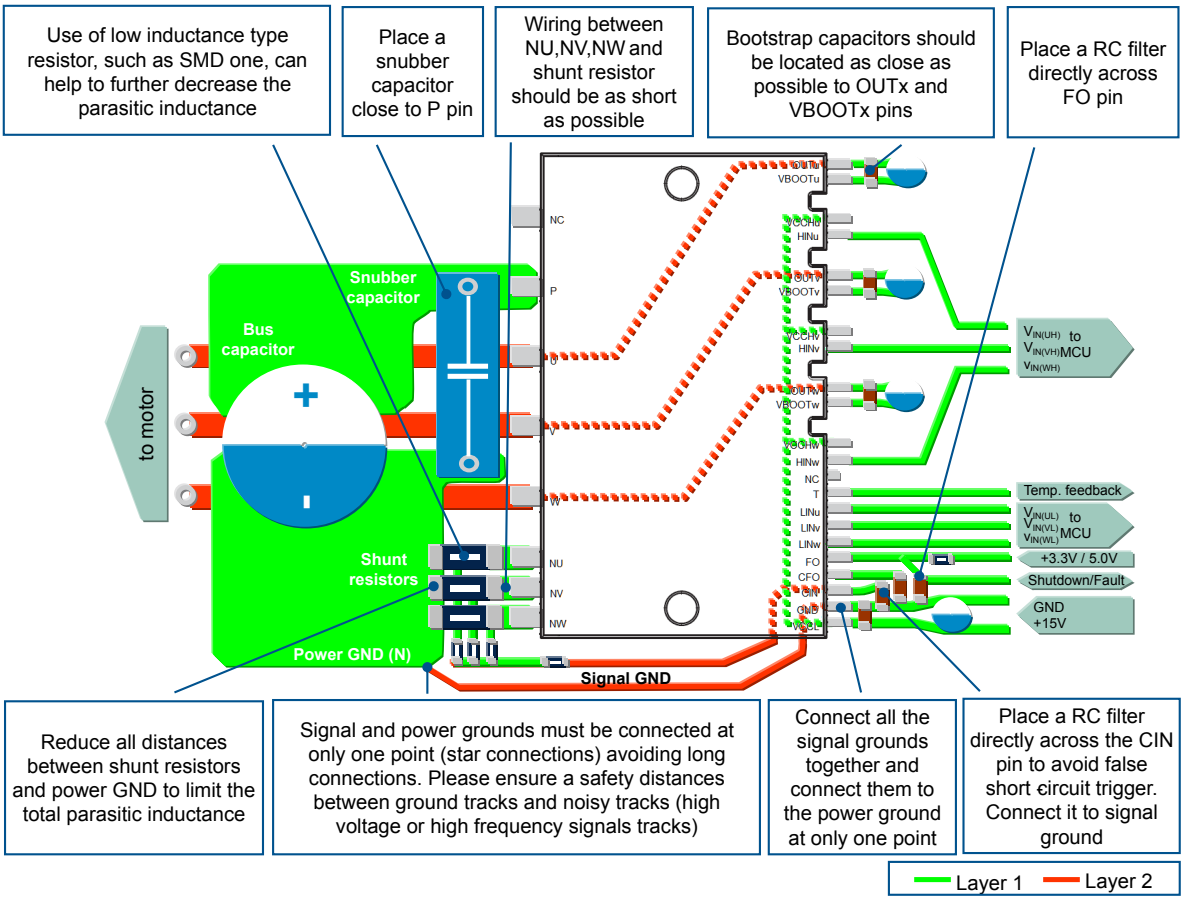
4. Generally, it is recommended to connect each half bridge ground in a star configuration and the three R_{SHUNT} very close to each other and to the power ground.
5. In order to prevent surge destruction, the wiring between the snubber capacitor and the P N pins must be as short as possible. The use of a high frequency, high voltage non-inductive capacitor of about 0.1 or 0.22 µF is recommended. In order to effectively suppress the surge voltage, the snubber capacitor has to be placed in position (2) in Figure 44. Recommended snubber capacitor position. The position (1) is incorrect for effective surge voltage suppression. If the capacitor is placed on the position (3), the charging and discharging currents generated by wiring inductance and the snubber capacitor appear on the shunt resistor with possible undesired protection activation, even if the surge suppression effect is the greatest. Finally, position (2) is the right compromise. The parasitic inductance on the A tracks (including that of the shunt resistor) should be as small as possible in order to suppress the surge voltage.

Figure 44. Recommended snubber capacitor position



The general suggestions for all SLLIMM high power products are summarized in Figure 45. PCB layout general suggestions.

Figure 45. PCB layout general suggestions



6 Mounting and handling instructions

Some basic assembly rules must be followed in order to limit thermal and mechanical stress and optimize the thermal conduction and electrical isolation for SDIPHP-30L package when mounting a heat sink.

Moreover, semiconductors are normally electrostatic discharge sensitive devices (ESDS) requiring specific precautionary measures regarding handling and processing. Static discharges caused by human touch or by processing tools may cause high-current and/or high-voltage pulses which may damage or even destroy sensitive semiconductor structures. Integrated circuits (ICs) may also be charged by static during processing. If discharging takes place too quickly (“hard” discharge), it may cause peak loads and consequent damage.

Make careful choices regarding workspaces, personal equipment and processing and assembly equipment.

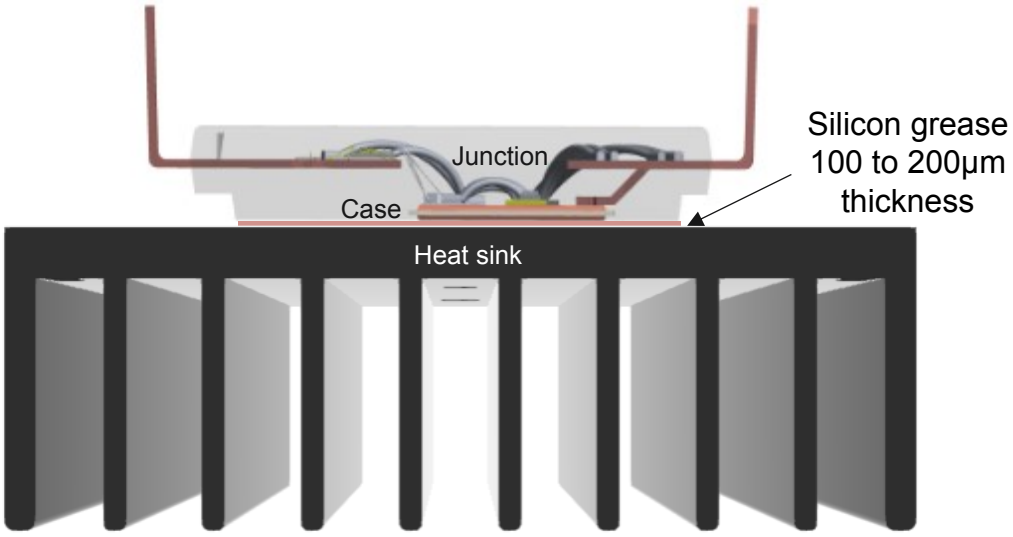
6.1 Heat sink mounting

When attaching a heat sink to a SLLIMM, do not apply excessive force to the device for assembly. Drill holes for screws in the heat sink exactly as specified. Smooth the surface by removing burrs and protrusions Do not touch the heat-sink when the SLLIMM is operational to avoid burn injury.

To get the most effective heat dissipation, enlarge the contact area as much as possible to minimize the contact thermal resistance. Properly apply thermal-conductive grease over the contact surface between modules and heat sinks, is also useful for preventing contact surfaces from corrosion. Apply from 100 to 200 µm layer of thermal grease to the module base plate or to the heat sink, as shown in Figure 46. Recommended silicon grease thickness and positioning. Use a torque screwdriver to fasten up to the max. specified torque rating. Exceeding the maximum torque may lead to module damage or degradation. Remove any dirt from the contact surface.

Ensure the grease quality remains constant over time and is able to perform long-term over a wide operating temperature range.

Figure 46. Recommended silicon grease thickness and positioning



6.2 Mounting torque

Mounting torque and heat sink flatness specifies the correct fastening torque. Inappropriate mounting can damage the device and over tightening the screws may cause DBC substrate or molding compound cracks. Avoid mechanical stress due to tightening on one side only. It is recommended to first lightly fasten both screws fastening them permanently to the specified torque value with a torque wrench.

Table 13. Mounting torque and heat sink flatness

Parameter	Conditions	Min.	Typ.	Max.	Unit
Heat sink mounting screw torque	Mounting screw: M3 with plain washer 7 mm (φ)	0.64	0.80	0.96	N·m
		6.6	8.2	9.8	kgf·cm
Device flatness of heat sink attachment area (1)	See Figure 47. Device flatness specification	0	50	100	µm
Flatness of heat sink	See Figure 48. Heat sink flatness specification	-100	-	100	µm
Package weight		-	23	-	g

1. *Specified By Design – Not tested in production.*

The Figure 47. Device flatness specification and Figure 48. Heat sink flatness specification provide device and heat sink flatness details, respectively.

Figure 47. Device flatness specification

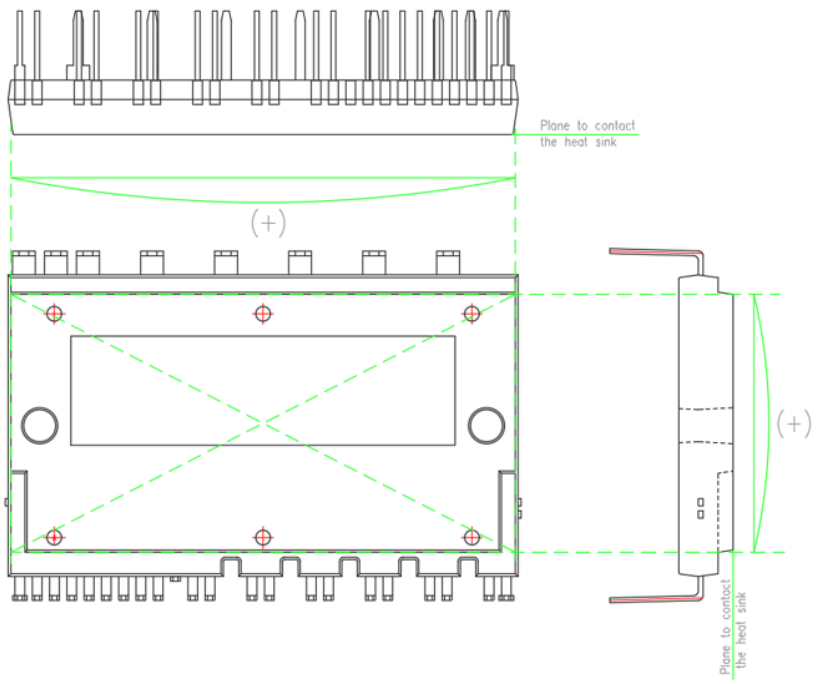
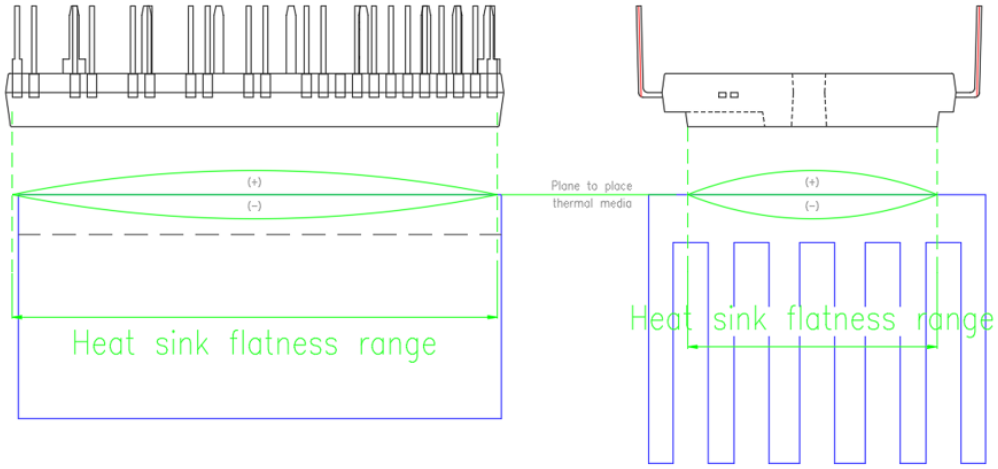


Figure 48. **Heat sink flatness specification**



Do not exceed the specified fastening torque. Over tightening the screws may cause ceramic or molding compound cracks and heat-fin threaded hole destruction.

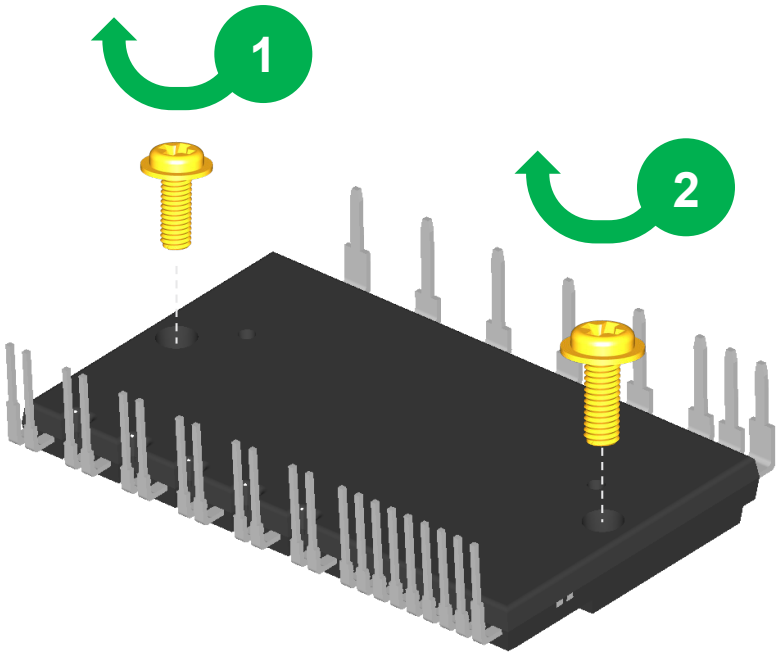
Tightening the screws beyond a certain torque can cause saturation of the contact thermal resistance.

Figure 49. Recommended mounting screw fastening sequence shows the recommended fastening sequence for mounting screws. ST recommends temporarily tightening mounting screws with the fixing torque set up to 20% to 30% of the maximum screw torque and then permanently screwing them up to 100% of prescribed maximum screw torque crosswise, as per the below steps:

1. Fasten temporarily in the sequence 1 → 2
2. Screw down permanently in the sequence 1 → 2

When using electrical or pneumatic screwdrivers, ST suggests limiting the revolution to 200 rpm as the rapid impact of the screw may damage the module plastic body.

Figure 49. **Recommended mounting screw fastening sequence**



Many other precautions regarding handling and contamination, ESD, storage, transportation and soldering should be considered.

6.3 Recommended screws

All mounting screws should have washers . Recommended diameter is M3 with plain washer 7 mm (φ).

However, an additional spring washer could assure an even better mounting result. Finally, the use of SEMS screws (included spring/plain washer M3, as shown in the Figure 50. SEMS screw (size M3, spring washer 5.0 Φ, plain washer 7.5 Φ)) is suggested.

Figure 50. SEMS screw (size M3, spring washer 5.0 Φ, plain washer 7.5 Φ)

7 Motor control power board based on the SLLIMM high power

The STEVAL-IPMHF50G interface demo board, belonging to the SLLIMM high power card family, is a compact motor drive power board based on the STGIK50CH65T device.

It provides an easy-to-use solution for driving high power motors for a wide range of applications such as air conditioner compressors, power fans and pumps, servo drives, high-end power tools and generally, 3-phase inverters for motor drives.

The main characteristics of this evaluation board are small size, minimal BOM list and easily testable and scalable. It consists of an interface circuit (BUS and VCC connectors), bootstrap capacitors, snubber capacitor, hardware short-circuit protection, fault event signal and temperature monitoring. In order to increase flexibility, it is designed to work with double current sensing options such as three dedicated op-amps onboard or op-amps embedded on the MCU. The Hall/encoder part completes the circuit.

Thanks to these advanced characteristics, the system has been specially designed to achieve accurate and fast conditioning of the current feedback, matching the typical requirements for field oriented control (FOC).

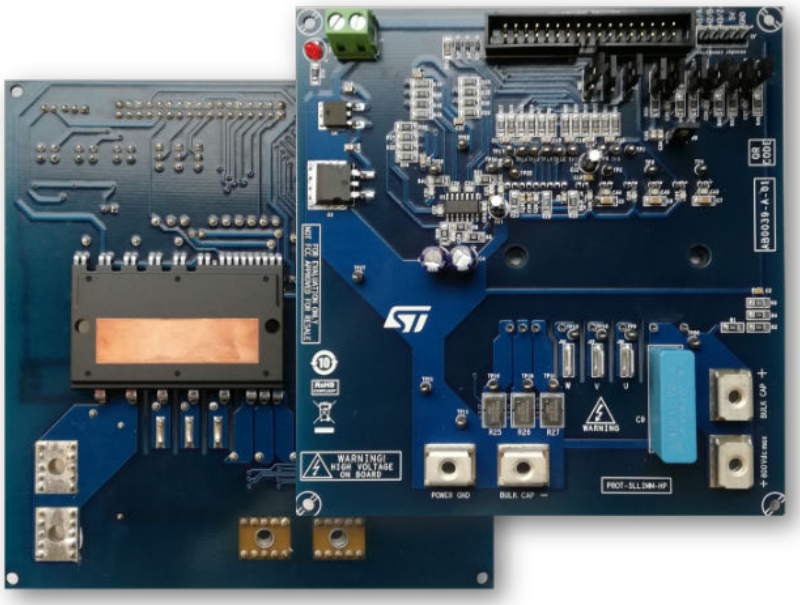
The STEVAL-IPMHF50G is compatible with ST's control board based on STM32, so as to provide a complete platform for motor control.

The main features are:

- input voltage: 125 to 400 VDC
- current rating: up to 50 A (peak)
- nominal power: up to 10 kW
- three-shunt resistors for current sensing (with sensing network)
- two options for current sensing: dedicated op-amps or through MCU
- overcurrent hardware protection
- IPM temperature monitoring and protection via MCU
- Hall sensor or encoder input
- motor control connector (32 pins) interfacing with ST MCU boards
- universal conception for further evaluation with bread board and testing pins very compact size

Figure 51. Top and bottom view of STEVAL-IPMHF50G shows a top and bottom view of the STEVAL-IPMHF50G board.

Figure 51. Top and bottom view of STEVAL-IPMHF50G



8 References

STGIK50CH65T datasheet

AN4768 – “SLLIMM 2nd series”

AN4694 – “EMC design guides for motor control applications”

AN4076 – “Two or three shunt resistor based current sensing circuit design in 3-phase inverters”

STEVAL-IPMHF50G evaluation board

Revision history

Table 14. **Document revision history**

Date	Revision	Changes
25-Jan-2022	1	First release.
13-Feb-2023	2	Modified Figure 18. Overcurrent protection waveforms, Figure 29. Calculated C_{BOOT} for 6-step 120° switching PWM Modified Section 3 SDIPHP-30L package Modified the entire Section 4.5 STPOWER Studio Simulation Software.

Contents

List of tables

List of figures