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Application note

Guidelines for DDR memory routing on STM32MP2 MPUs

Introduction

This application note guides the user on how to implement a DDR3L, DDR4, and LPDDR4 memory interface on application boards of the STM32MP2 MPUs. It provides interface schematics, layout implementation rules, and best practices.

1 General information

The STM32MP2 MPU devices embed an Arm® Cortex®-M0+ core, an Arm® Cortex®-M33 core and a dual Arm® Cortex®-A35 core[See 1 in the Table 2. Reference documents], with a 16/32 bits DDR interface.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The following table presents a non-exhaustive list of terms and acronyms used in this document.

Table 1. Terms and acronyms

Acronym	Definition
A/C	Addresses and commands
DDR3L SDRAM	Double data rate of third generation low-voltage SDRAM
DDR4 SDRAM	Double data rate of fourth generation SDRAM
DQ	Data
DQMx	Data mask
DQSx_N/DQSx_P	Data strobe N/Data strobe P
GND	Ground
HF	High frequency
LPDDR4 SDRAM	Low power double data rate of fourth generation SDRAM
MT/s	Mega transfers per second
PCB	Printed circuit board
SDRAM	Synchronous dynamic random access memory
STPMIC	Highly integrated power-management device for microprocessors
VTT	Termination voltage

Table 2. Reference documents

Document number	Title
[1]	*STM32MP25xx advanced Arm®-based 32/64-bit MPUs* reference manual (RM0457).
[2]	STPMIC25 datasheet (DS14278).
[3]	*Guidelines for DDR configuration on STM32MP2 MPUs* (AN5723).

2 Design interface constraints

The external DDR interface of the STM32MP2 MPU devices can address different types of memory:

- DDR3L with a data rate of 2133 MT/s, voltage at 1.35 V. More information on DDR3L SDRAM can be found on the JEDEC DDR3 SDRAM Standard JESD79-3F.
- DDR4 with a data rate of 2400 MT/s, voltage at 1.2 V. More information on DDR4 can be found on the JEDEC DDR4 Standard JESD79-4B.
- LPDDR4 with a data rate of 2400 MT/s, voltage at 1.1 V. More information on LPDDR4 can be found on the JEDEC LPDDR4 SDRAM Standard JESD209-4D.

Low-voltage and high data-rate speed narrow the tolerances in terms of eye diagram, and contribute to a higher risk of system instability. As a result, there are many constraints and design sensitivities to consider when working with memory interfaces. For example:

- Most signals are single-ended: only the clocks and stobes are differential signals.
- Signals can be connected either point-to-point or in fly-by topology.

Continuous board size reductions usually impose performance limitations on the interfaces, and increase challenges when designing a DDR interface.

Given that DDR connections on both the STM32MP2 MPU device and the memory device interface are fixed, the physical layout has very limited flexibility:

- There is a minimum amount of signal routing required, which cannot be reduced further.
- There are impedance constraints to be managed.

To ensure correct signal and power integrity, basic design rules regarding trace isolation, length equalization, power distribution and decoupling, and impedance matching must be respected.

This document lists the rules that must be applied in order to implement a state-of-the-art memory interface in 4- or 6-layer boards.

STMicroelectronics highly recommends reusing the layout of the STM32 device reference designs. These layouts have been tested and have been proven stable.

3 Memory architecture options

The DDR interface is different depending on the package. They can be connected to one or two DDR3L, one or two DDR4, or one LPDDR4 with different ways of connection:

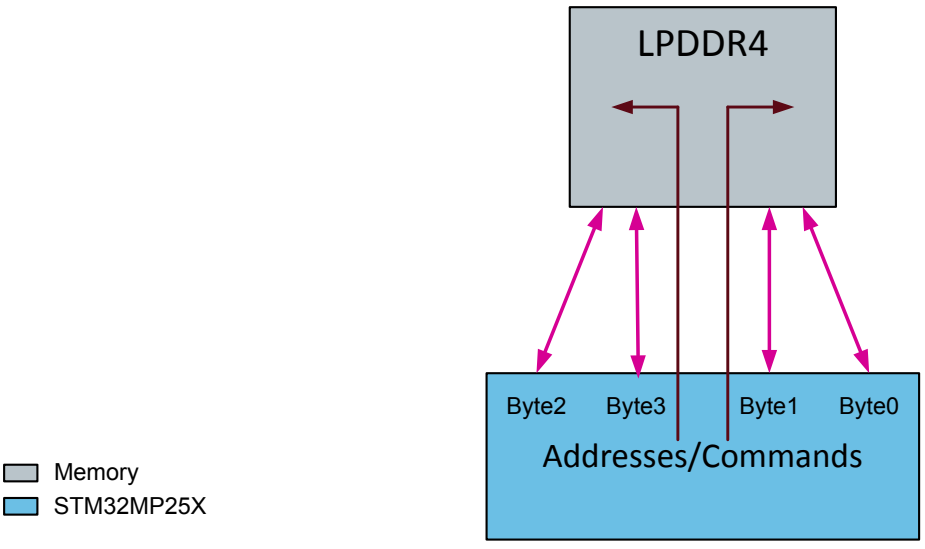
Table 3. Package summary of STM32MP2 MPUs

Package type	TFBGA361 (10 × 10 mm)	TFBGA424 (14 × 14 mm)	TFBGA436 (18 × 18 mm)
32-bit DDR interface	-	X	X
16-bit DDR interface	X	X	X

3.1 32-bit LPDDR4 interface

For the 32-bit LPDDR4 interface, one 32-bit LPDDR4 is used in point-to-point connection.
With this configuration, it can drive up to 4 Gbyte memory.

Figure 1. 32-bit LPDDR4 interface



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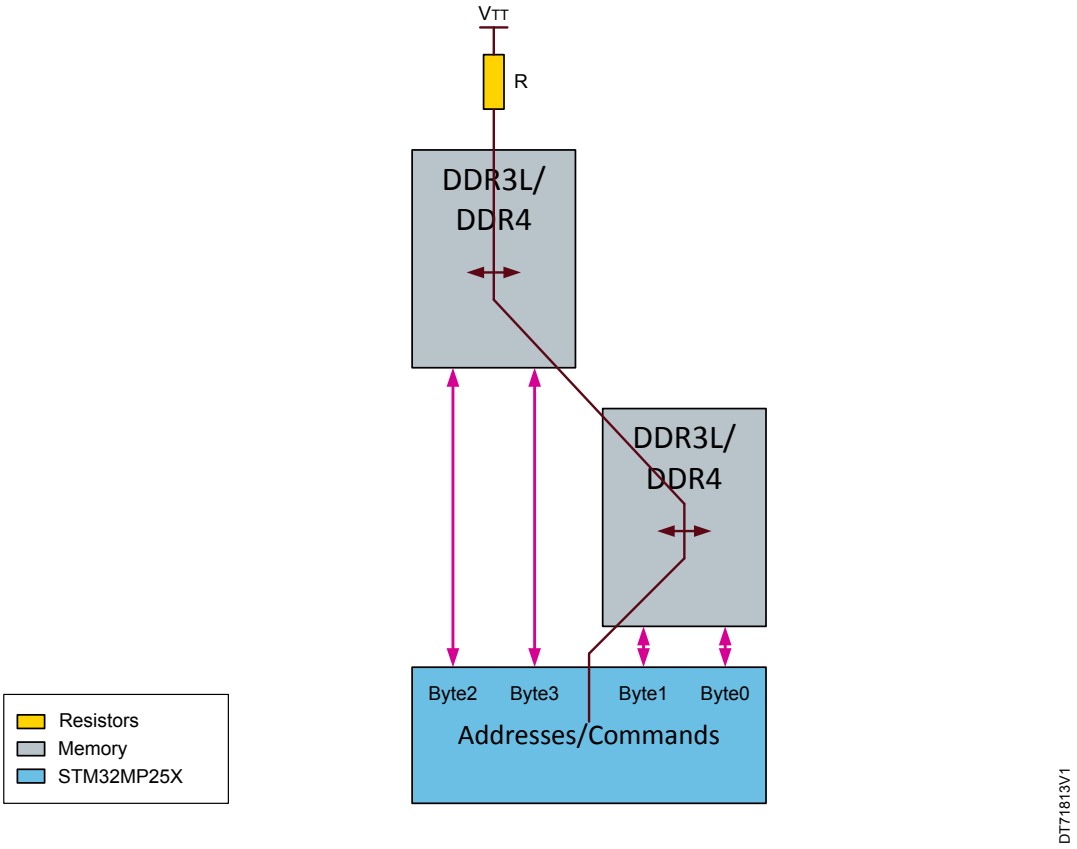
3.2 32-bit DDR3L/4 interface

For the 32-bit DDR3L/4 interface, two 16-bit DDR3L/4 are used in fly-by topology.
With this configuration it can drive up to 2 Gbyte memory with DDR3L, or 4 Gbyte memory with DDR4.

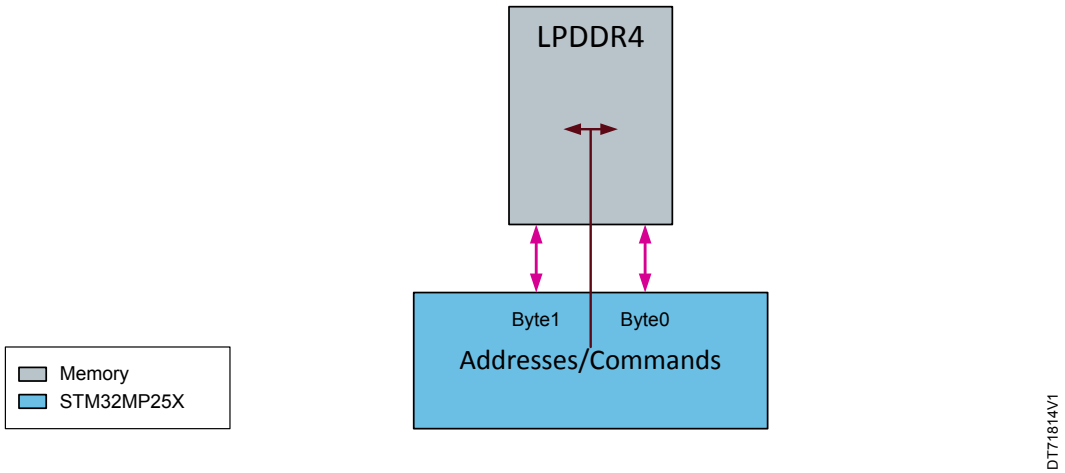
Figure 2. **32-bit DDR3L/4 interface**



3.3 16-bit LPDDR4 interface

For the 16-bit LPDDR4 interface, one 16-bit LPDDR4 is used in point-to-point connection. With this configuration it can drive up to 2 Gbyte memory.

Figure 3. **16-bit LPDDR4 interface**

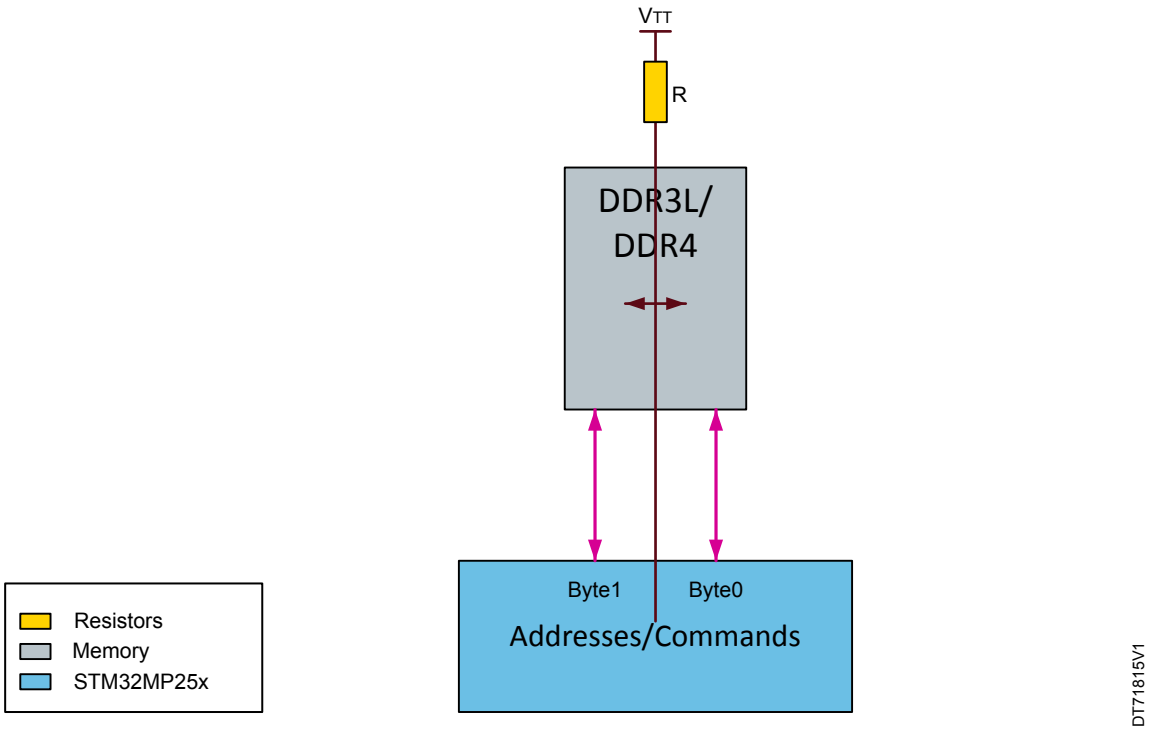


3.4 16-bit DDR3L/4 interface

For the 16-bit DDR3L or DDR4 interface, one 16-bit DDR3L/4 is used.

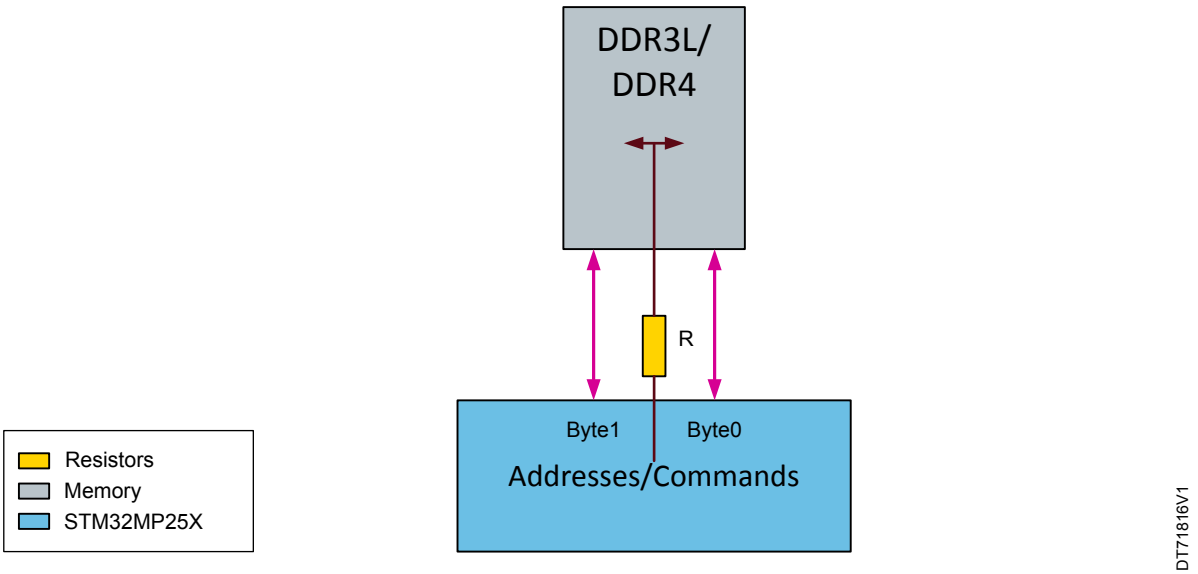
With this configuration, it can drive up to 1 Gbyte memory with DDR3L, or 4 Gbyte memory with DDR4.

Figure 4. 16-bit DDR3L/4 connection with termination resistors on address/command lines



Another possibility to connect one DDR3L/4 if termination resistors are not used: connect a serial resistor on each address/command line, close to the device. This solution depends of layout and frequency used and requires signal integrity simulation.

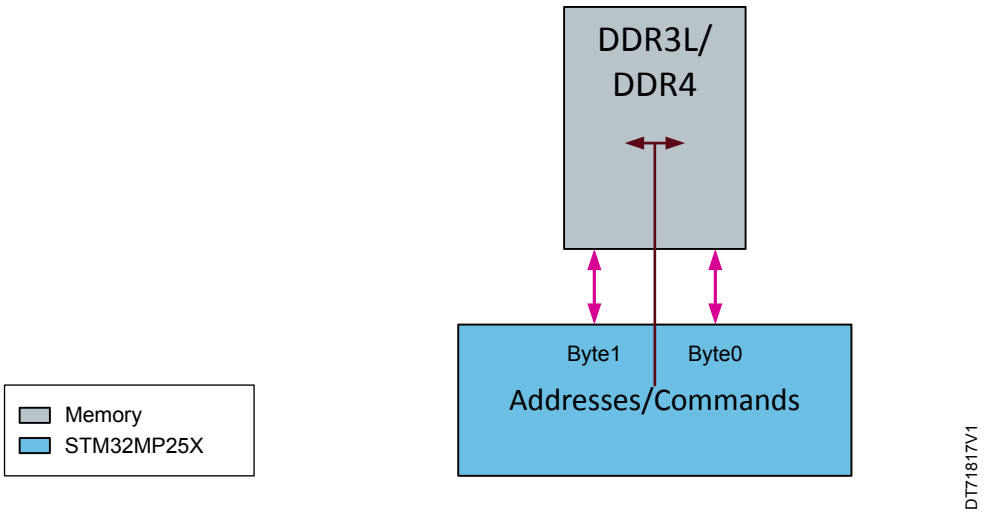
Figure 5. 16-bit DDR3L/4 connection with serial resistors on address/command lines



The last possibility is to connect each line to one DDR3L/4 directly, if termination resistors or serial resistors are not used on address/command lines..

This solution depends of layout and frequency used and requires signal integrity simulation.

Figure 6. 16-bit DDR3L/4 connection without resistors



4 DDR3L/DDR4 schematic implementation

A DDR3L/4 implementation must include the following elements:

- a single DDR3L/4 connection or a standard fly-by topology with two DDR3L/4,
- a cost-optimized point-to-point topology,
- miscellaneous signals,
- power supplies and reference voltage.

These elements are detailed below.

4.1 Single DDR3L/4 connection

A connection with one DDR3L/4 includes:

- a distributed A/C bus with 56 Ω on-board termination to V_{TT} (= V_{DD_DDR} / 2)
- a differential clock with differential termination of the CLK_N/CLK_P signals using one 100 Ω resistor.
- a mandatory point-to-point connection of the data bus (two swappable bytes, and swappable bits in the same byte), including:
  - 16 data signal bits (DQ)
  - two data mask signals (DQMx)
  - two differential pairs of strobes (DQSx_N/DQSx_P).

4.2 Cost-optimized point-to-point topology

This topology can be used with one DDR3L/4 and without V_{TT}. It includes:

- a point-to-point connection of every A/C bus, with no termination on-board,
- 33 Ω serial resistors, recommended for every A/C of the DDR, in order to reduce reflection. If DDR3L/4 is very close to the STM32MP2 MPU device, these resistors can be removed. Refer to the *ST reference design* or the *Examples of DDR memory routing on STM32MP2 MPUs*, available on *www.st.com*.
- CLK_N/CLK_P signals that are terminated differentially by one 100 Ω resistor,
- a point-to-point connection of the data bus (two swappable bytes, and swappable bits in the same byte), including:
  - 16 data signal bits (DQ)
  - two data mask signals (DQMx)
  - two differential pairs of strobes (DQSx_N/DQSx_P).

4.3 Standard fly-by topology with two DDR3L/4

A standard fly-by topology includes:

- a distributed A/C bus with 56 Ω on-board termination to V_{TT} (= V_{DD_DDR} / 2),
- a differential clock, distributed to all DDR devices, with a differential termination of the CLK_N/CLK_P signals using one 100 Ω resistor,
- a point-to-point connection of the data bus (four swappable bytes, byte 0 with byte 1 and byte 2 with byte 3, and swappable bits in the same byte on two 16-bit DDR3L/4), including:
  - 32 data signal bits (DQ)
  - four data mask signals (DQMx)
  - four differential pairs of strobes (DQSx_N/DQSx_P)

4.4 Miscellaneous signals

The following signals must be included in the schematic:

- DDR_RESETN: asynchronous low-speed reset signal from the DDR controller to DDR devices
  A 10 kΩ pull-down resistor is required. This signal is driven low during the power-on, or when a reset is required. Otherwise, the signal must be driven high by default.
- DDR_ZQ: requires, for DDR impedance calibration, that resistors are placed between the signal balls and ground as follows:
  - a 240 Ω (±1%) resistor must be placed between the ZQ ball on each DDR and ground plane.
  - a 240 Ω (±1%) resistor must also be placed between the ZQ ball of the STM32MP2 MPU device and ground plane.
- ALERTN (Alert output, pin on DDR4) is not used and let floated.
- PAR (parity for command and address, pin on DDR4) is not used and let floated or tie to the ground.
- TEN (connectivity test mode, pin on DDR4) is not used and let tie to the ground.

4.5 Power supplies and reference voltage

The following power supply and reference voltage components must be provided to the DDR:

- V_{REF} reference voltage (= V_{DD_DDR} / 2)
- V_{TT} power supply (= V_{DD_DDR} / 2)
- V_{DD_DDR} power plane
- V_{PP_DDR} power supply

V_{REF} reference voltage (= V_{DD_DDR} / 2)

This reference voltage is required by the DDR3L/4 devices in order to properly sample A/C (DDR3L/4) and data signals (DDR3L). Its noise level must remain very low, as described in the JEDEC standard. The DDR_VREF pin on the STM32MP2 MPU device is floating.

There are two possibilities:

- Independent V_{REF} generators (VREFCA, VREFDQ) for DDR3L, (VREFCA) for DDR4.
  Each V_{REF} generator is based on a resistance bridge with two 1 kΩ (±1%) resistors from V_{DD_DDR}, plus a local 100 nF decoupling capacitor. V_{REF} must be generated as close as possible to its corresponding ball.
- A common V_{REF} for DDR3L/4.
  The V_{REF} generator from an external device is delivered to DDR3L/4 with a local 100 nF decoupling capacitor. The STPMIC25 [See 2 in the Table 2. Reference documents] can deliver V_{REF}.

V_{TT} power supply (= V_{DD_DDR} / 2)

This power supply is used exclusively in DDR3L/4 interfaces. This is the termination voltage for address and control (A/C) signals.

An external V_{TT} voltage generator is recommended. The STPMIC25 can deliver V_{TT}. A strong V_{TT} decoupling is required. It must be as close as possible to the termination resistors.

V_{DD_DDR} power plane

This is the DDR interface power supply. It is equal to 1.35 V (1.28-1.45 V) for DDR3L and 1.2 V (1.14-1.26 V) for DDR4.

This plane requires mandatory decoupling capacitors relative to the ground plane, with bulk and HF capacitors. These capacitors must be close to the power supply pins for STM32MP2 MPU and DDR devices.

V_{PP_DDR} power supply (= 2.5 V)

This power supply is used exclusively in DDR4 interface. The STPMIC25 can deliver V_{PP_DDR}.

5 LPDDR4 schematic implementation

An LPDDR4 implementation requires the following elements:

- a point-to-point topology,
- miscellaneous signals,
- power supplies.

5.1 Point-to-point topology

A standard point-to-point topology comprises:

- 20 A/C signals (10 in half populated). Some but not all can be swapped but required software swizzle (see 3 in Table 2. Reference documents).
- two differential pairs of clocks of differential clocks (one pair in half populated).
- a point-to-point connection of the data bus (4 bytes with 32-bit LPDDR4 or 2 bytes with 16-bit LPDDR4, including:
  - 32 (16 in half populated) data signal bits (DQ). No swappable byte, bits can be swapped but required software swizzle.
  - four (two in half populated) data mask signals (DQMx).
  - four (two in half populated) differential pairs of strobes (DQSx_N/DQSx_P).

5.2 Miscellaneous signals

The following signals must be included in the schematic:

- DDR_RESETN: asynchronous low-speed reset signal from the DDR controller to DDR devices. A 10 kΩ pull-down resistor is required. This signal is driven low during the power-on, or when a reset is required. Otherwise, the signal must be driven high by default.
- DDR_ZQ: it requires resistors for DDR impedance calibrations:
  - a 240 Ω (±1%) resistor must be placed between the DDR_ZQ ball on the LPDDR4 and VDD2_DDR.
  - a 240 Ω (±1%) resistor must be placed between the DDR_ZQ ball of the STM32MP2 MPU device and ground plane.
- DDR_VREF pin on the STM32MP2 MPU device is floating.
- ODT_CA (on die termination for A/C, pin on LPDDR4) is connected to VDD2_DDR.

5.3 Power supplies

The following power supplies must be provided to the DDR:

- V_{DD2_DDR} power plane
- V_{DD1_DDR} power supply

V_{DD2_DDR} power plane

This is the LPDDR4 interface power supply. It is equal to 1.1 V (1.06-1.17 V).

This plane requires mandatory decoupling capacitors relative to ground plane, with bulk capacitors. The HF capacitors must be close to the power supply pins for both STM32MP2 MPU and LPDDR4.

V_{DD1_DDR} power supply

This is the core power supply of LPDDR4. It is equal to 1.8 V (1.7-1.95 V).

6 PCB design considerations

The basic PCB design considerations to take into account are detailed in the following sections. This is a non-exhaustive list of good practices to follow for sensitive-signal designs.

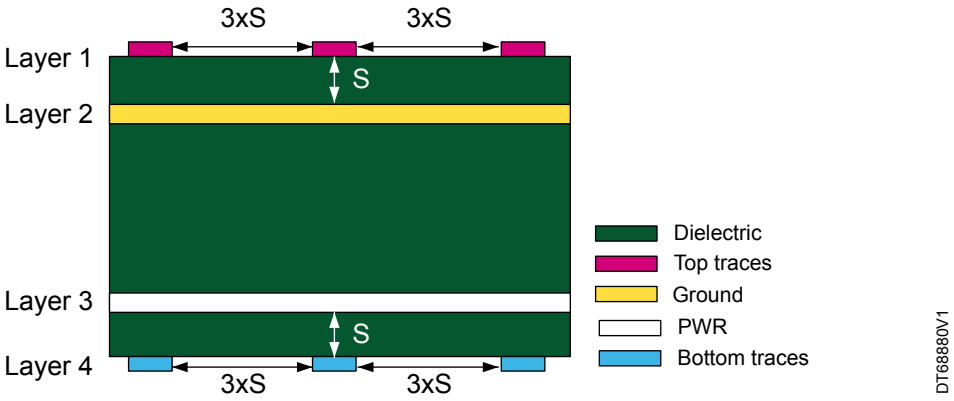
6.1 Trace isolation distance

In order to reduce crosstalk, glitches, and jitter caused by neighboring traces (sometimes referred to as *aggressors*), a minimum isolation distance must be provided around every trace.

S-3S isolation rule

If "S" is the distance between a trace and its reference plane (ground plane for top-layer traces, and PWR plane for bottom-layer traces), a trace is said to be isolated if the distance between it and its direct neighbor is greater than or equal to 3xS. The figure below shows this rule in practice.

Figure 7. S-3S isolation rule illustration



In other words, S-3S is the minimum isolation spacing rule. If more space between traces is available, it must be used to separate signals as much as possible (such as S-4S or S-10S).The more space there is between traces, the better the signal isolation and noise immunity is.

The S-3S rule is not applicable below BGA devices (memory and STM32MP2 MPU devices) because of fan-out constraints.

When the S-3S rule is not applicable, the length of the segments that are in conflict with the rule must be minimized.

Layouts using an S-1S spacing must be avoided as often as possible. If the S-3S rule is not applicable, maximizing the distance between traces as much as possible (S-2S rule) is preferable, instead of using an S-1S layout.

6.2 Length equalization

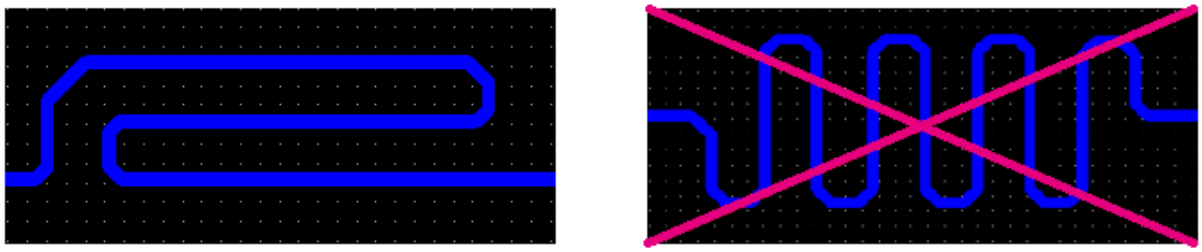
Signals of the same group must have matching setup and hold timings when they arrive at their destination. To meet these timing constraints, trace length equalization may be required.

The whole signal path from STM32MP2 MPU device to the memory must be taken into account, including the package and board trace lengths.

Length equalization patterns

When routing traces to equalize lengths, some patterns are recommended. For example, switchback patterns are preferred over serpentine shaped patterns, as the latter can provoke orthogonal propagation, which compromises the integrity of the signal.

Figure 8. Length equalization patterns



The S-3S isolation rule must also be applied within the equalization pattern, meaning that the minimum distance between sections of the same trace should be greater or equal to S-3S.

In the case of differential signals:

- Intra-pair length equalization is not allowed.
- The spacing between N and P must be constant.
- The mean value length of N and P signals that must be considered for a differential pair, is given by: Lsig = (LsigN + LsigP) / 2.

The STMicroelectronics templates and the length equalization tables can be used to simplify the task of equalizing signal trace lengths. These tables include the trace lengths of the packages and can be obtained on *Examples of DDR memory routing on STM32MP2 MPUs*, available on *www.st.com*

6.3 Impedance

In general, the driver impedance (ZDRV) is usually 34 Ω or 40 Ω, while the on-die termination impedance (ZODT) is usually 60 Ω.

The board impedance must be controlled in order to guarantee proper transmission line setup, in accordance with the trace geometry (width and spacing), and the stack-up of the board.

For DDR3L/4 and LPDDR4 interfaces, STMicroelectronics recommends the following impedances:

- for single-ended signals: 55 Ω ±10%.
- for differential signals: 100 Ω differential ±10%.

6.4 Layer allocation for 4-layer boards

Layers must be allocated and implemented as detailed below, without exception:

- Top layer:
  - This layer is dedicated to traces with the highest sensitivity.
  - The traces are referenced to the unified, internal ground plane.
  - There are no impedance breaks.
  - There is no coupling allowed to noisy power supplies.
- Layer 2 (GND) internal layer:
  - This is the unified internal ground plane.
  - It must be connected by a matrix of vias to the top and bottom ground areas.
- Layer 3 (V_{DD_DDR} for DDR3L/4 or V_{DD2_DDR} for LPDDR4) internal layer:
  - This is the dedicated power supply plane, which supplies on board power distribution.
- Bottom layer:
  - This is a second signal layer used for traces. It is possible to have impedance breaks in this layer, due to the discontinuity of the reference power supply plane.

6.5 Layer allocation for 6-layer boards with TFBGA361

Layers must be allocated and implemented as detailed below, without exception.

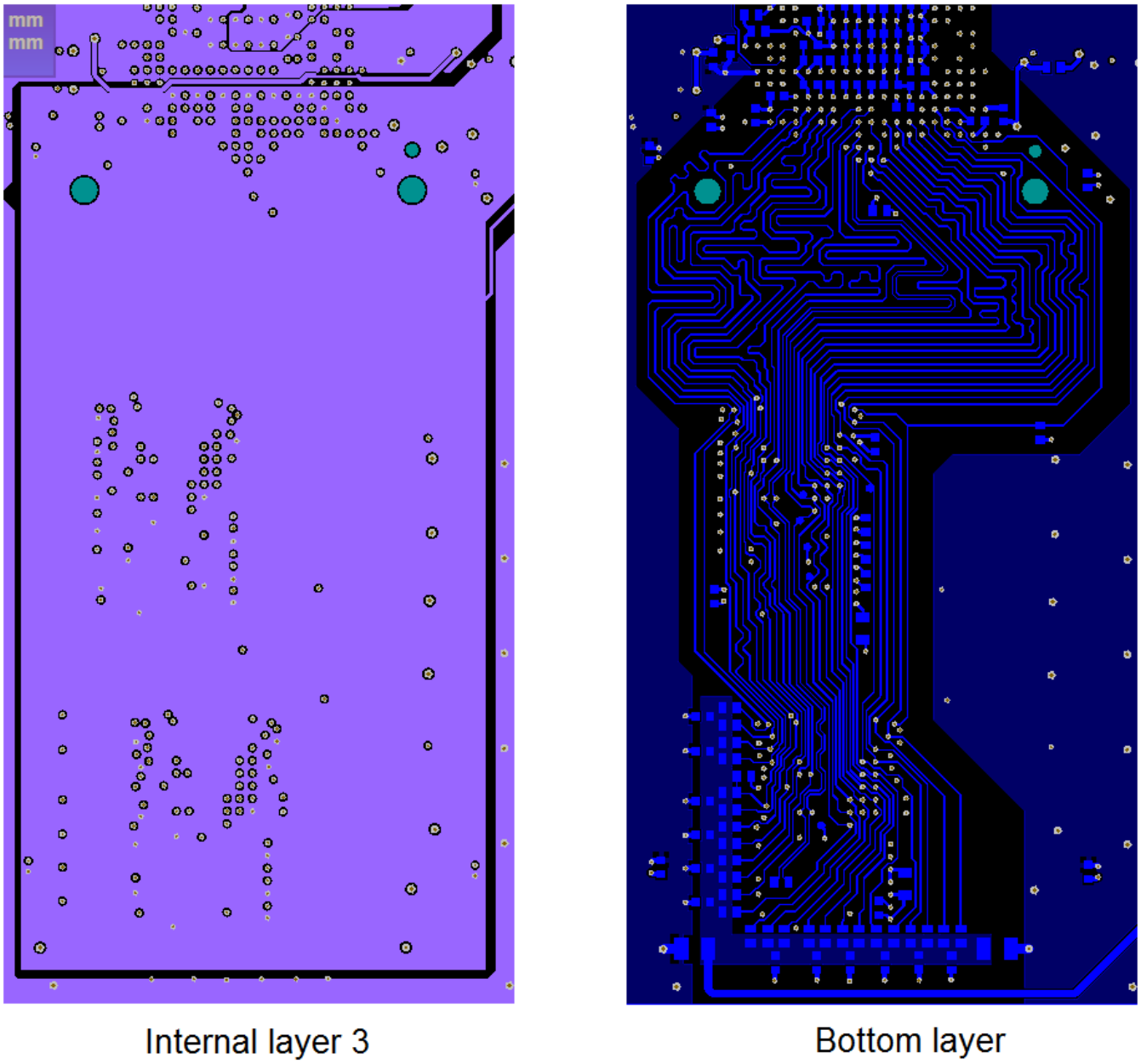
- Top layer:
  - This layer is dedicated to data traces.
  - The traces are referenced to the unified, internal ground (GND) plane.
  - There are no impedance breaks.
  - There is no coupling allowed to noisy power supplies.
- Layer 2 (GND) internal layer:
  - This is the unified internal ground plane.
  - It must be connected by a matrix of vias to the top and bottom ground areas.
- Layer 3 internal layer:
  - This layer is dedicated to A/C traces.
- Layer 4 internal layer:
  - This layer has a ground plane above the V_{DD_DDR} or V_{DD2_DDR} power plane.
- Layer 5 (V_{DD_DDR} for DDR3L/4 or V_{DD2_DDR} for LPDDR4) internal layer:
  - This is the dedicated power supply plane, which supplies on board power distribution.
- Bottom layer:
  - Decoupling capacitors use this layer.

6.6 V_{DD_DDR} power plane specification

A/C signals are laid out on the bottom layer of the 4-layer PCB.

The internal layer 3 must be a unified V_{DD_DDR} (V_{DD2_DDR} for LPDDR4) power plane, which fully overlaps the memory bottom-layer signals, in order to avoid any impedance breaks due to traces referenced to multiple power planes.

Figure 9. Example of DDR3L A/C signal layout and corresponding power plane



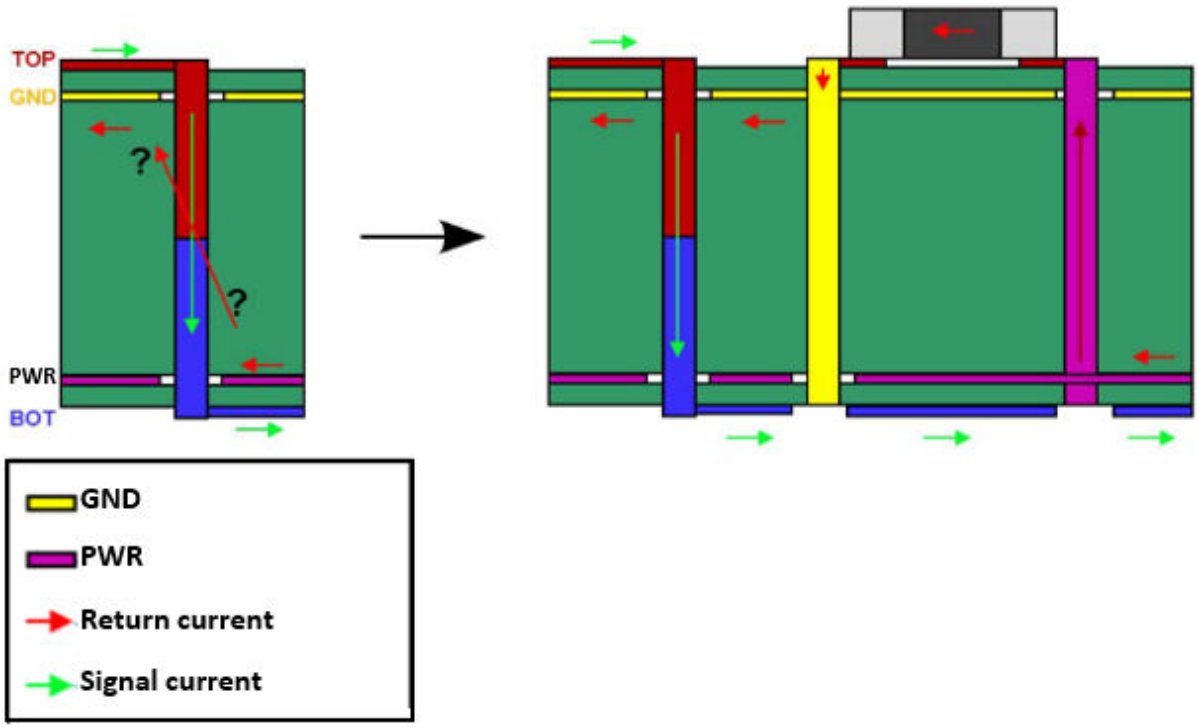
6.7 Layer change capacitors

When a sensitive signal moves from the top layer of the board to the bottom layer (or vice versa), a 100 nF capacitor must be placed as close as possible to the signal via. It must be connected from one side to the layer 2 (GND), and from the other side to the layer 3 (V_{DD_DDR} for DDR3L/4, V_{DD2_DDR} for LPDDR4).

This design requirement is absolutely necessary in order to provide an HF return current reference path to the signal.

The capacitor can be placed on either the bottom or top layer, as shown in the figure below.

Figure 10. Use of layer change capacitors



When multiple signals are changing layers in the same area of the board (such as in the case of A/C bus distribution), it may become impossible to place a single capacitor close to each via. The solution in this case is to add a single capacitor for a group of vias. The number of capacitors must be as high as needed for the specific board design, and they must be placed as close as possible to the via area.

6.8 Types of decoupling capacitors

Power integrity is essential for avoiding voltage drops and, by consequence, eye closure, and erroneous data transmission.

Core and sensitive power supplies (like V_{DD_DDR}) must be laid out by using internal power planes, and by using maximum width, in order to minimize the distribution impedance.

In addition, decoupling capacitors are required. There are two types of capacitors:

- Bulk capacitors
  These capacitors provide an on-board energy tank for low-frequency, high-current needs. Capacitance values can range from 10 µF to 100 µF. Refer to the *ST reference design* or the *Examples of DDR memory routing on STM32MP2 MPUs*, available on *www.st.com* to choose a capacitor value appropriate for the specific power supply used. Bulk capacitors do not need to be placed very close to their destination.
- High-frequency (HF) capacitors
  These capacitors provide a local energy tank for high-frequency current bursts. They must be placed as close as possible to the destination (power pins or balls). A better practice is to implement fewer capacitors, but placed in optimum positions, in order to reduce the connection inductance.

6.9 Minimizing connection inductance with HF capacitors as decoupling capacitors

The decoupling capacitors placement must ensure minimum connection inductance.

The closer the capacitor is to its destination, the more efficient it is. This is particularly true for HF capacitors.

Putting capacitors on the top layer can provide far better decoupling efficiency than placement on the bottom layer.

However, the location of these capacitors can be constrained by BGA fan-out.

This section provides best practices for capacitor placement in order to minimize connection inductance, and to improve decoupling efficiency, for both top and bottom layers.

6.9.1 Placing capacitors on the top layer

Capacitors placed on the PCB top layer cannot be very close to BGA balls due to package constraints.

However, if a capacitor is connected by a direct top-layer power trace to the BGA ball, its connection inductance remains smaller than if the capacitor is located much closer, but on the bottom layer, owing to the GND layer position in the stack-up (GND is the return current layer). The amount of connection inductance that results is directly linked to the area of the current loop.

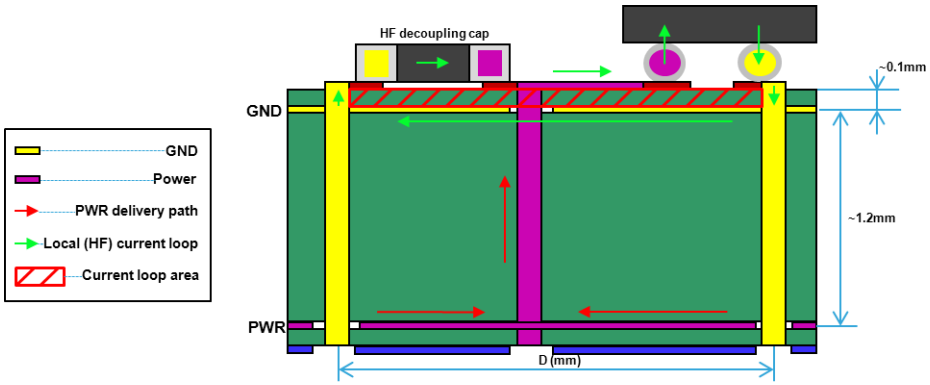
Therefore top layer placement offers:

- Pros
  - Small current loop area, resulting in low connection inductance, and good decoupling capability.
  - Free space on the bottom layer for other signal layouts. As memory A/C trace layouts are usually on the bottom layer, this allows more flexibility for A/C length equalization/spacing requirements.
- Cons
  - Placement of capacitors on the top layer is very often not possible for main BGA decoupling because of fan-out constraints.

When possible, HF capacitor must be placed on the top layer, with a top-layer direct power connection. The layer 2 (GND) provides a close return path, which results in a small current loop area and optimal decoupling efficiency.

For example, in the layout shown in the figure below, the resulting current loop area is: Current loop area = 0.1 × D. If D = 5 mm, the current loop area is in the region of 0.5 mm^2.

Figure 11. Placement of an HF capacitor on the top layer



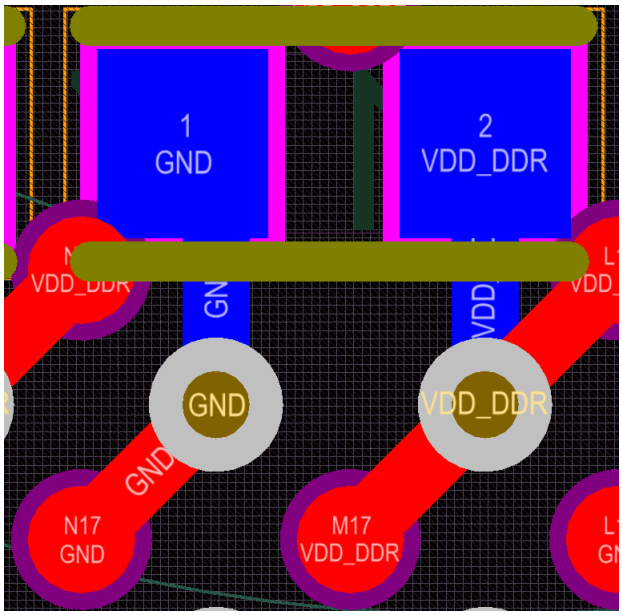
6.9.2 Placing capacitors on the bottom layer

When top-layer decoupling is not possible, placement of capacitors must be on the bottom layer.

While the connection inductance is higher than for top-layer capacitor placement, due to the bigger current loop area, bottom layer placement remains most of the time the only decoupling option for main BGA. Following some basic implementation rules allow for an optimization of this placement. For best results, the capacitor must be placed right below the BGA balls.

When placing HF capacitors on the bottom layer, aim to have the shortest possible connections, and a good via placement directly below the BGA, as shown in the figure below.

Figure 12. HF capacitor on bottom layer

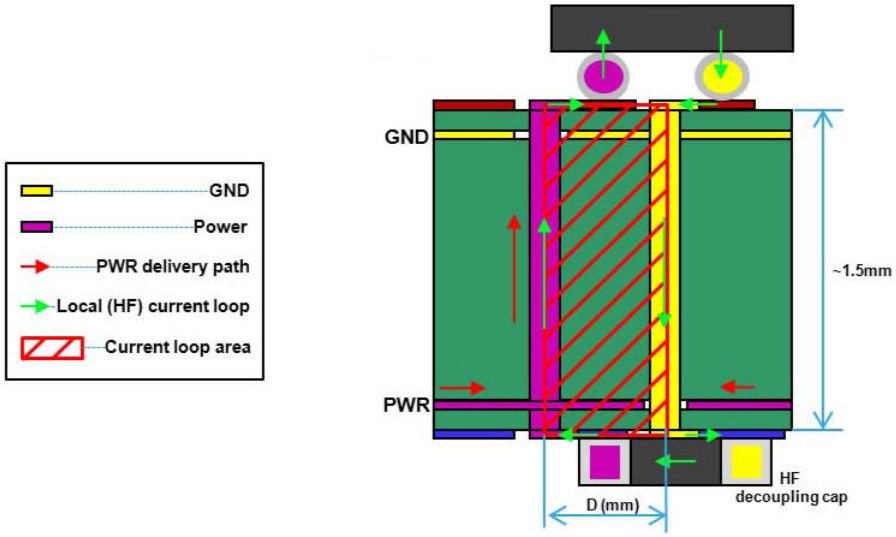


In the following example, the resulting current loop area is:

Current loop area = 1.5× D

If D equals 1.0 mm, the resulting current loop area is 1.5 mm^2, as compared to 0.5 mm^2 for a top-layer placement at a 5 mm distance. In other words, a capacitor situated on the top layer, 15 mm from the power ball, would have the same efficiency as a capacitor situated on the bottom layer, directly below the power ball. This illustrates the higher efficiency of top-layer capacitor placement relative to bottom-layer placement.

Figure 13. Placement of an HF capacitor on the bottom layer



7 Memory layout rules

This section presents a code of best practice rules to be applied by signal type on memory interfaces. These recommendations are based on the basic PCB design rules.

7.1 Data signal rules for 32-bit memory interfaces

There are four different (independent) signal groups over four bytes:

- Byte0 = DQ[7:0], DQM0, DQS0_N and DQS0_P
- Byte1 = DQ[15:8], DQM1, DQS1_N and DQS1_P
- Byte2 = DQ[23:16], DQM2, DQS2_N and DQS2_P
- Byte3 = DQ[31:24], DQM3, DQS3_N and DQS3_P

For these data signals, the following rules must be applied:

- These data signals must only be routed on the top layer of the PCB.
- Whenever possible, the S-3S isolation rule (as a minimum) must be applied.
  Due to the constraints of high via density and BGA pitch, exceptions can only be made when signals are very close to the memory or to the STM32MP2 MPU device.
  When the S-3S rule is not applicable, the layout must be designed to optimize the isolation rule (such as S-2S or S-1.5S). Segments where S-1S is the only option must be as short as possible.
- For DDR3L/4 and LPDDR4, apply the rules below to each byte:
  - DQ or DQM to DQS_N/DQS_P +/- 56 mils (1.42 mm)
  - DQS_N/DQS_P to CLK_N/ CLK_P +/- 475 mils (12.06 mm)
- For LPDDR4, channel A CLK_N/CLK_P versus channel B CLK_N/CLK_P +/-570 mils (14.5 mm) maximum.

7.2 Data signal rules for 16-bit memory interfaces

There are two different (independent) signal groups over 2 bytes:

- Byte0 = DQ[7:0], DQM0, DQS0_N and DQS0_P
- Byte1 = DQ[15:8], DQM1, DQS1_N and DQS1_P

For these data signals, the following rules must be applied:

With one 16-bit DDR3L/4 or LPDDR4, the rules below are applied to each byte:

- DQ or DQM to DQS_N/DQS_P +/-56 mils (1.42 mm).
- DQS_N/DQS_P to CLK_N/ CLK_P +/- 475 mils (12.06 mm)

7.3 Address and control (A/C) signal rules

The following signals are included in A/C groups:

- For DDR3L A[15:0], BA[2:0], RASN, CASN, WEN, CSN, CKE, ODT, CLK_N, CLK_P
- For DDR4 A[13:0], BA[1:0], BG[1:0], RASN, CASN, WEN, CSN, CKE, ODT, ACTN, CLK_N, CLK_P, ALERTN, PAR, TEN
- For LPDDR4 CA[5:0]_A, CS[1:0]_A, CKE[1:0]_A, CLK_A_N, CLK_A_P, CA[5:0]_B, CS[1:0]_B, CKE[1:0]_B, CLK_B_N, CLK_B_P

The following design rules must be applied for A/C signals:

- Except with TFBGA361, the PCB bottom layer must be used for A/C distribution to memory devices. The top layer is reserved for connections to the memory (stubs) and A/C bus crossing.
- The S-3S isolation rule as a minimum must be applied wherever possible.
  When the S-3S rule is not applicable, the layout must be designed to optimize the isolation rule (such as S-2S, S-1.5S). Segments where S-1S is the only option must be as short as possible.
  Due to constraints of high via density and BGA pitch, exceptions can only be made when signals are very close to the memory or the STM32MP2 MPU device.
- Length equalization rules:
  - A/C to CLK_N/ CLK_P +/- 140 mils (3.55 mm) with DDR3L/4 and LPDDR4.
  - Equalization is from STM32MP25 to memory and it does not include length from memory to 100R for differential clocks or length from memory to termination resistors for A/C signals.

  Trace length = STM32MP2 MPU substrate length + board via length + board track length
  Differential trace length (CLK_N/CLK_P) = (Trace length N + Trace length P) / 2

Note: Always refer to the ST reference design or the Examples of DDR memory routing on STM32MP2 MPUs, available on www.st.com for signal ordering, BGA fan-out, and layout examples.

7.4 DDR_ZQ signal

This signal must be laid out, so that the trace from the ball to the reference resistor is as short as possible. Good isolation from any noisy aggressor signals must be ensured.

7.5 Power plane rules

This section describes the rules to follow to design the power planes.

7.5.1 V_{DD_DDR} (V_{DD2_DDR} for LPDDR4) power plane

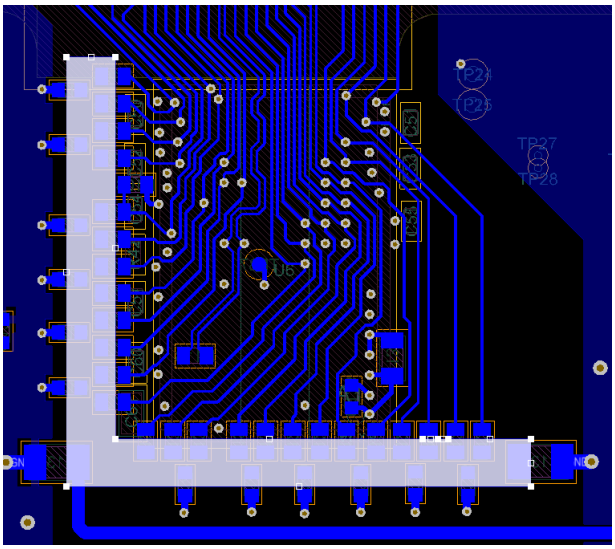
- Power plane must be unified at layer 3 for 4-layer boards and layer 5 for 6-layer boards.
- This power plane must overlap every DDR3L/4 (LPDDR4) trace on the bottom layer for 4-layer boards, in order to avoid impedance discontinuities.
- The V_{DD_DDR} power plane connection to the V_{DD_DDR} power supply, to STM32MP2 devices, and to each memory, must be done by multiple vias.
- Standard decoupling rules must be applied:
  - Bulk capacitors must be placed between the voltage regulator, the STM32MP2 device and the memories.
  - HF decoupling capacitors must be placed as close as possible to each of the power pins, following the low-inductance connection recommendations outlined in Section 6.9: Minimizing connection inductance with HF capacitors as decoupling capacitors.

7.5.2 V_{TT} power plane rules

The V_{TT} power supply is used in DDR3L/4 interfaces.

- The V_{TT} termination voltage must be considered as a power supply.
- Due to V_{DD_DDR} constraints (an unified plane in layer 3 for 4-layer boards, overlapping the DDR area), the V_{TT} layout must be managed as an island on the bottom layer. Refer to the figure at the end of this section.
- The V_{TT} regulator must be located close to the RTT terminations.
- One HF capacitor must be reserved for two RTT termination resistors, and must be placed as close as possible to them.
- Bulk capacitors can be placed anywhere between the V_{TT} regulator and terminations.
- Leave sufficient spacing around the V_{TT} island, to reduce crosstalk.

Figure 14. Layout of V_{TT} power plane island



Revision history

Table 4. **Document revision history**

Date	Version	Changes
22-Mar-2024	1	Initial release.

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