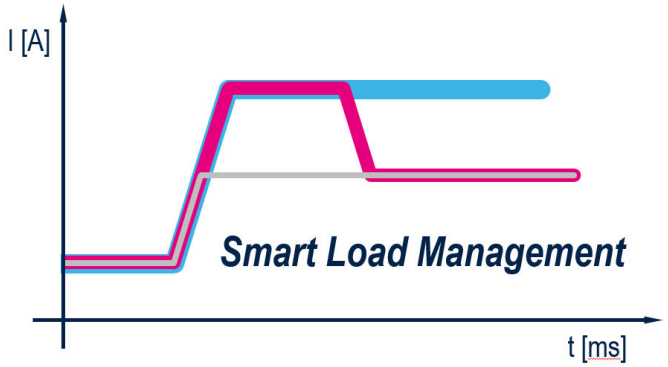
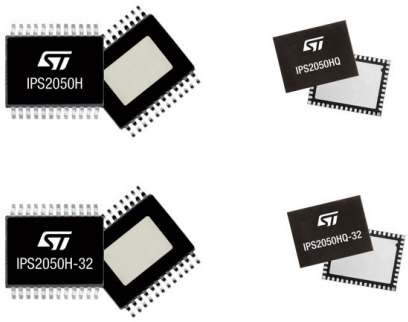
Understanding the Smart Load Management for IPS2050 family

Abstract

This document introduces the new ST devices IPS2050H and IPS2050H-32 (as well as the equivalent QFN48L 8x6 mm package options IPS2050HQ and IPS2050HQ-32) and focuses, with a practical example, on their market-unique *Smart Load Management* feature.

Driving efficiently the wide set of industrial loads with diverse electrical parameters by a single chip is a typical challenge in industrial digital I/O applications: the Smart Load Management responds to this requirement.





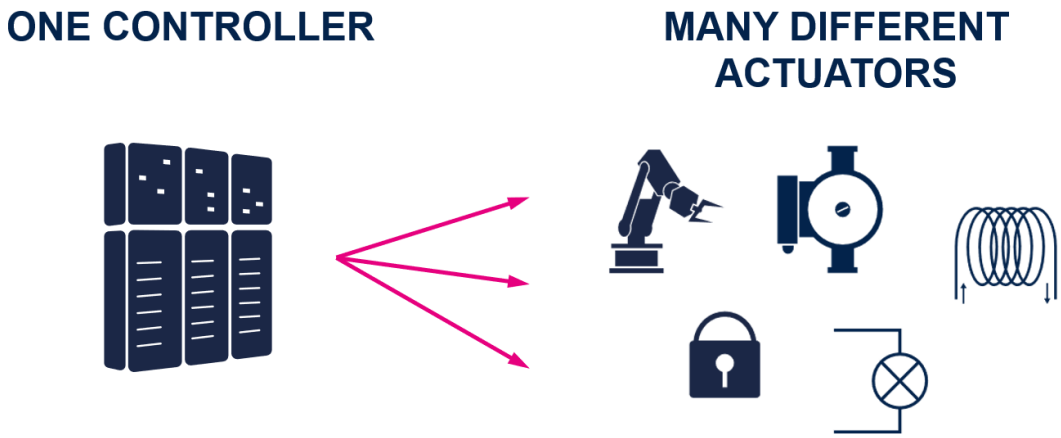
1 Introduction

Industrial digital I/O ICs are used in electronic control systems accompanying our everyday life. While they typically drive automation tasks in smart factories and home & building automation, there are also wide application domains in transportation industries and even city & traffic infrastructure control.

Actuators in automation are endpoint, field-layer components allowing the control system to execute electrical and electro-mechanical actions based on information and data received from smart sensors. In general, an actuator can be seen as an electrical load with an impedance of certain character and parameters (resistance, capacitance, inductance). Industrial digital output modules, which drive actuators, therefore need to operate with any actuator installed in the field, regardless of its specific electrical parameters (see Figure 2).

Figure 1. Fields application examples

Figure 2. Variety of industrial actuators

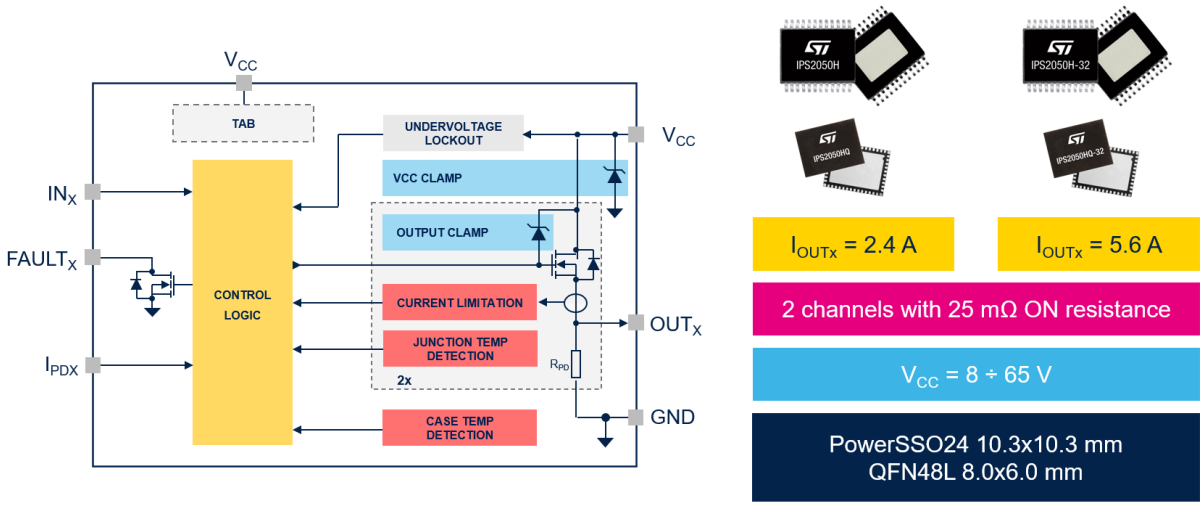


In order to address this technical challenge and to provide design engineers with added flexibility, ST developed a new generation of Intelligent Power Switches (IPS) implementing a unique active current limitation control function called Smart Load Management.

The new ICs IPS2050H and IPS2050H-32 (as well as the equivalent QFN48L 8x6 mm package options IPS2050HQ and IPS2050HQ-32) offer three configurable operation modes for managing current limitation in overload conditions. Whenever turning-on actuators with inrush current (like capacitive loads, or filament lamps) or in the event of failure of an actuator or its wiring (overload, short-circuit), the Smart Load Management comes into action. The following sections explain this feature.

2 IPS2050 family in brief

Figure 3. **IPS2050H/HQ, IPS2050H-32/HQ-32**



The IPS2050H in general represents the new family of dual-channel high-side switches with very low on-resistance and an extensive set of protection features securing reliable operation in harsh industrial environments.

The two ICs in PowerSSO24 package (IPS2050H and IPS2050H-32) are pin-to-pin compatible as well as the equivalent ones in QFN48L package (IPS2050HQ and IPS2050HQ-32), and they are also equivalent in terms of chip architecture and electrical characteristics. The difference lies in the setting of their current limitation levels: IPS2050H/HQ are suitable for load currents up to 2.4 A, while IPS2050H-32/HQ-32 fit for currents as high as 5.6 A.

Key features

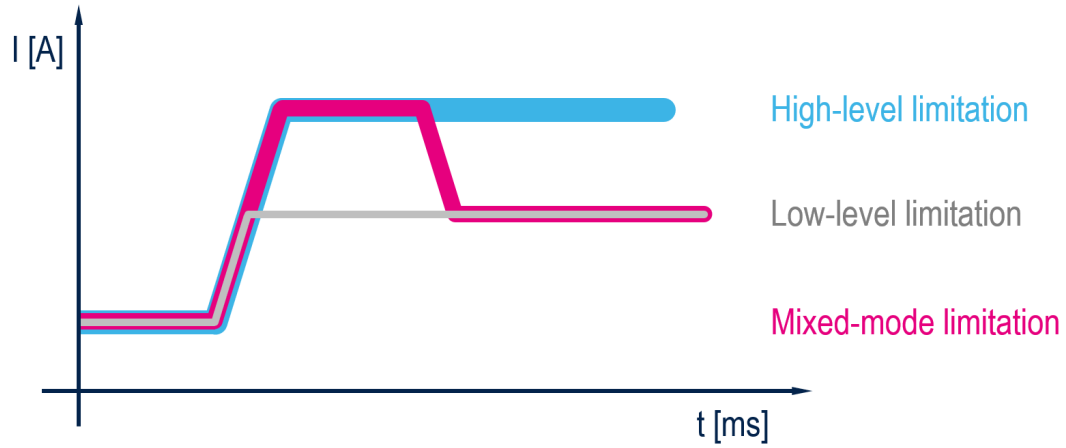
- Selectable output currents
- Extensive protections
- Adjustable inrush current timing
- Ultra-fast demagnetization of inductive loads
- High switch-OFF energy
- EMC-proof

One key important performance indicator of the IPS2050 family is that each IC is fully operational within an extended supply voltage range (up to 60 V). Compliance of all electrical parameters in this range is therefore verified for each chip during its manufacture. An additional safety margin is achieved by the Absolute Maximum Rating set to 65 V. This feature is especially convenient for designing safety-critical applications and systems operating under strong EMC and environmental disturbance, where it helps to significantly reduce product certification efforts, time-to-market and overall development costs.

3 Smart load management

The IPS2050H/HQ (as well as the IPS2050H-32/HQ-32) has three configurable operation modes which determine how the IC behaves in the event of overload. Based on its configuration it can either limit the current at a low value, reducing power dissipation and PCB components stress (low-level limitation, gray line in Figure 4), or it can be set to a higher current limitation level in order to support loads with inrush currents (high-level limitation, blue line in Figure 4). Finally, the third operation mode (Mixed limitation) combines the benefits of both the previous options (magenta line in Figure 4). In this mode, the IC allows to supply its load with an initial current of “high-level” magnitude which it eventually reduces to low-level limitation after a certain time. In order to ensure the true application flexibility, the duration of the initial high-level current supply is adjustable in a range from 100 µs to 100 ms.

Figure 4. IPS2050H/HQ and IPS2050H-32/HQ-32



Limitation mode configuration

The selection of operation mode is done for each channel by a specific connection of pins IN_X and I_{PDX}. Low-level current limitation mode is configured using a resistor R_{PDX} connected between IN_X and IPD_X (Figure 5).

Figure 5. Low-level limitation mode setting

R_{PDX} resistance 220k is selected to limit the current in full applicable voltage range up to 60V. Otherwise, a lower value (e.g. 10k) can be used.

The second mode (high-level limitation) is set by coupling the I_{PDX} pin to GND via an external pull-down resistor (Figure 6).

Figure 6. **High-level limitation mode setting**

Mixed mode limitation mode is configured by connecting a capacitor instead of pull-down resistor as shown in Figure 7.

Figure 7. **Mixed limitation mode setting**

Duration of the initial high-level limitation phase (configurable in a range from 100 µs to 100 ms) is defined by capacitance of C_{PDX} as follows:

D_{PKX}[µs] = 215 x C_{PDX}[nF]

It is recommended to select the C_{PDX} in the following range of capacities in order to maintain precision of the above calculation:

470 pF ≤ C_{PD} ≤ 470 nF

Calculated duration times for most common capacitors are shown in Table 1 and Figure 8.

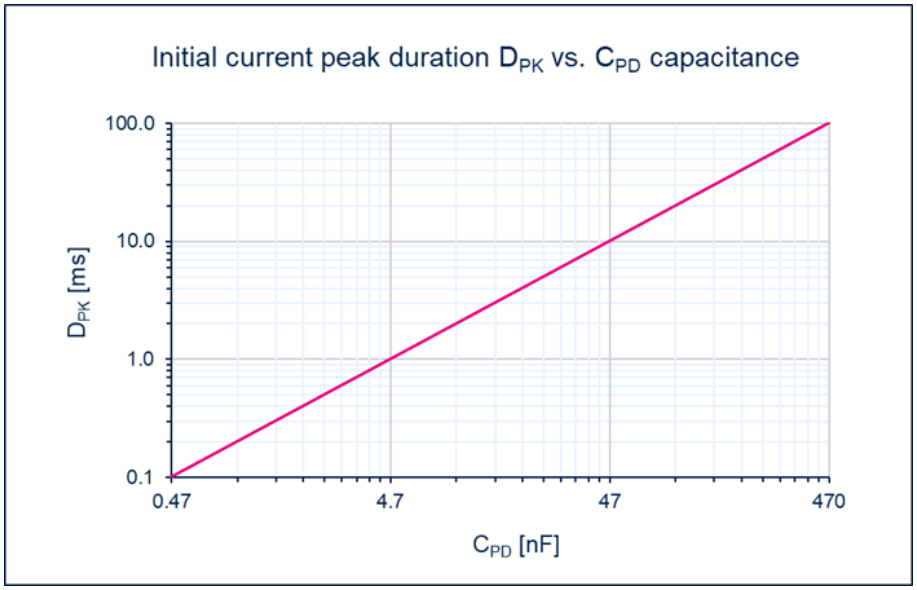
Table 1. Initial peak duration setting

C_{PD} [nF]	D_{PK} [µs]
0.47	101.1
0.68	146.2
1	215.0
1.5	322.5
2.2	473.0
3.3	709.5

C_{PD} [nF]	D_{PK} [ms]
4.7	1.0
6.8	1.5
10	2.2
15	3.2
22	4.7
33	7.1

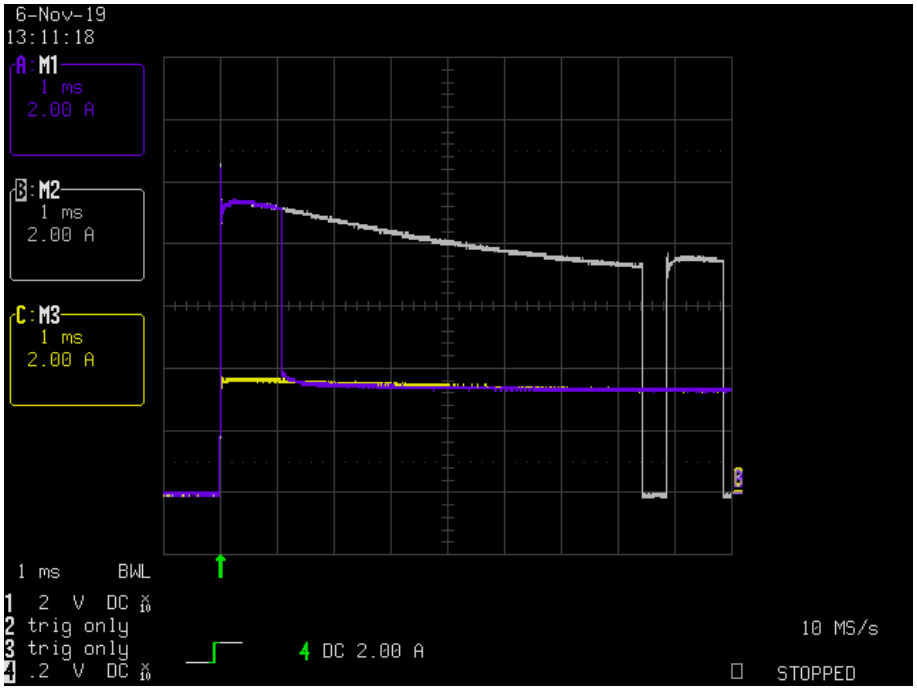
C_{PD} [nF]	D_{PK} [ms]
47	10.1
68	14.6
100	21.5
150	32.3
220	47.3
470	101.1

Figure 8. Initial peak duration setting



Comparison of all three current limitation modes in operation is shown on the scope capture in Figure 9.

Figure 9. **Comparison of current limitation modes**



It is important to note that during active current limitation the integrated power switch operates in linear mode, generating a significant voltage drop V_{DS}. This results in power dissipation proportional to the conducted current I_{LIM}:

$P_{LIM} = V_{DS} \times I_{LIM}$

In order to protect the IC and the PCB from overheating, each IC of the IPS2050 family integrates an additional protection mechanism called Two-level thermal shutdown.

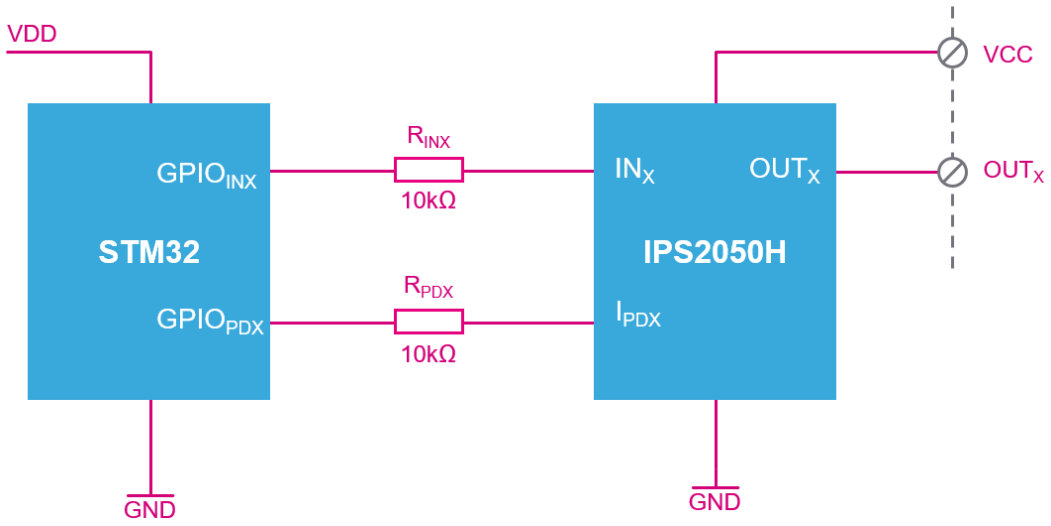
This protection operates on a two-level basis protecting both IC channels independently, and also the temperature of the IC itself. The shutdown effect of this feature is visible in Figure 9 after approximately 7.5 ms with high-level limitation setting (gray waveform).

Dynamic limitation mode control

The previous section described the standard way of configuring the current limitation mode on the system level. There is, however, one additional possibility which brings an additional level of freedom into the digital I/O systems controlling: Dynamic configuration of the current limitation mode.

With this approach, current limitation mode can be individually configured for each IC channel during application runtime by the host microcontroller. In Figure 10 each device's output is controlled by two dedicated signals of the host microcontroller ($GPIO_{INX}$ and $GPIO_{PDX}$). This configuration allows to flexibly select between low ($GPIO_{PDX}$ = HIGH) and high-level limitation ($GPIO_{PDX}$ = LOW) mode based on application conditions.

Figure 10. **Dynamic configuration of current limitation mode**



Understanding datasheet parameters

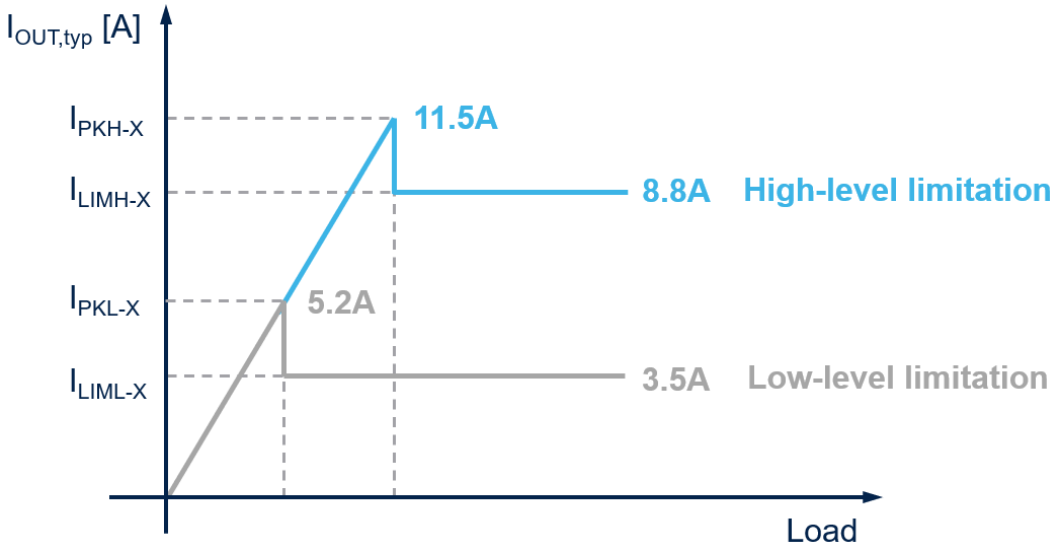
Although the Smart Load Management function and its configuration is relatively simple, there are several current level parameters that come into play. The overall picture is further complicated by the fact that two IC part numbers are available with different current limitation levels (IPS2050H/HQ and the 'IPS2050H-32/HQ-32' option). The list of related electrical parameters in the datasheet [1] might look slightly exhaustive at first glance so let's clarify the situation using a few simple illustrations.

IPS2050H/HQ

The specification of the IPS2050H/HQ was tuned to fit with most 2A industrial digital output applications in general. Its overall current levels are lower compared to the 'H-32' complement IC.

In order to activate the current limitation mechanism a certain triggering threshold is always defined. On the IPS2050H/HQ two such thresholds are defined: one for low-level limitation and a second one for high-level limitation (see Figure 10).

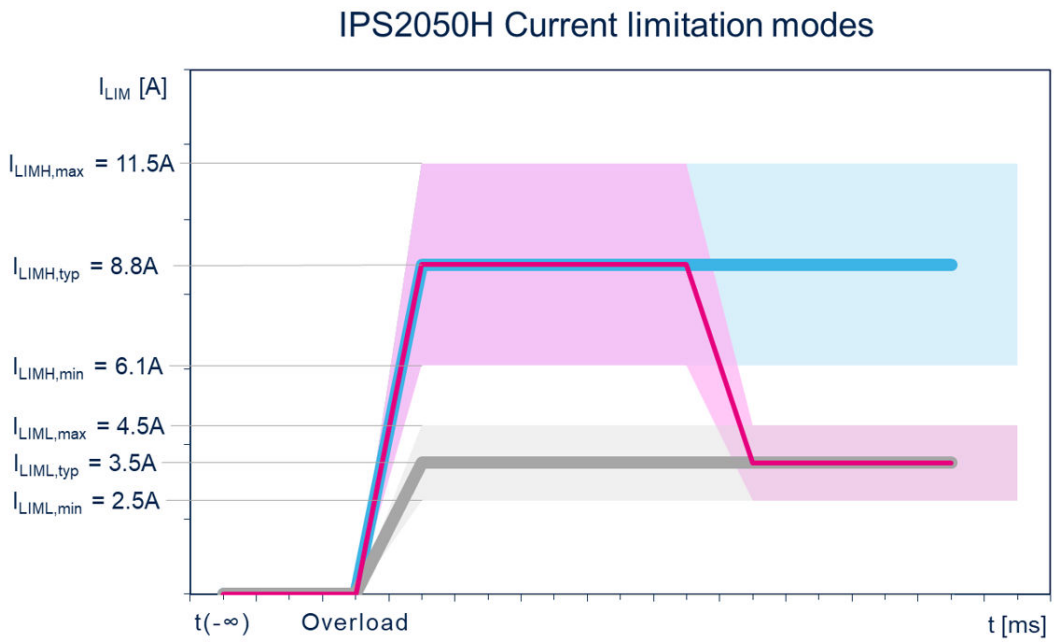
Figure 11. **Current limitation activation thresholds (IPS2050H/HQ)**



When the current limitation threshold is exceeded, the power switch starts to limit the current at its specified level according to the selected operation mode. This constant current level is, by principle, lower than the activation peak as is also shown in Figure 11.

Figure 12 shows the current limitation levels for each of the three operation modes. Each line, showing the typical values, is accompanied by the distribution band reflecting the possible spread in IC production process (minimum and maximum values, [1]).

Figure 12. Current limitation levels (IPS2050H/HQ)



IPS2050H-32/HQ-32

The IPS2050H-32/HQ-32 allows to deliver higher load currents compared to the standard version. This is especially beneficial in applications where we need to temporarily supply currents of higher magnitude (for example when we need to power-up some actuator with significant input capacity in a very short time).

Figure 13. Current limitation activation thresholds (IPS2050H-32/HQ-32)

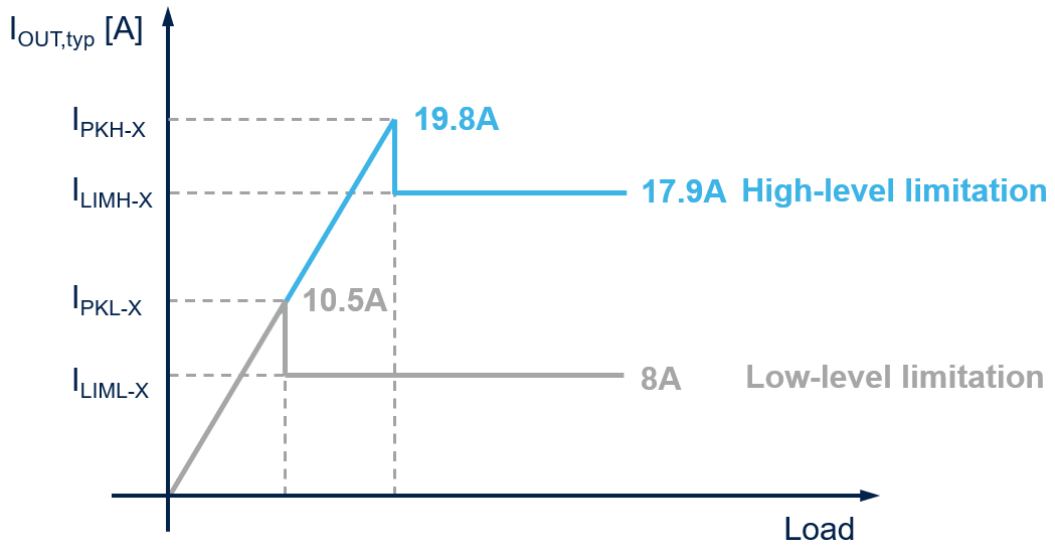
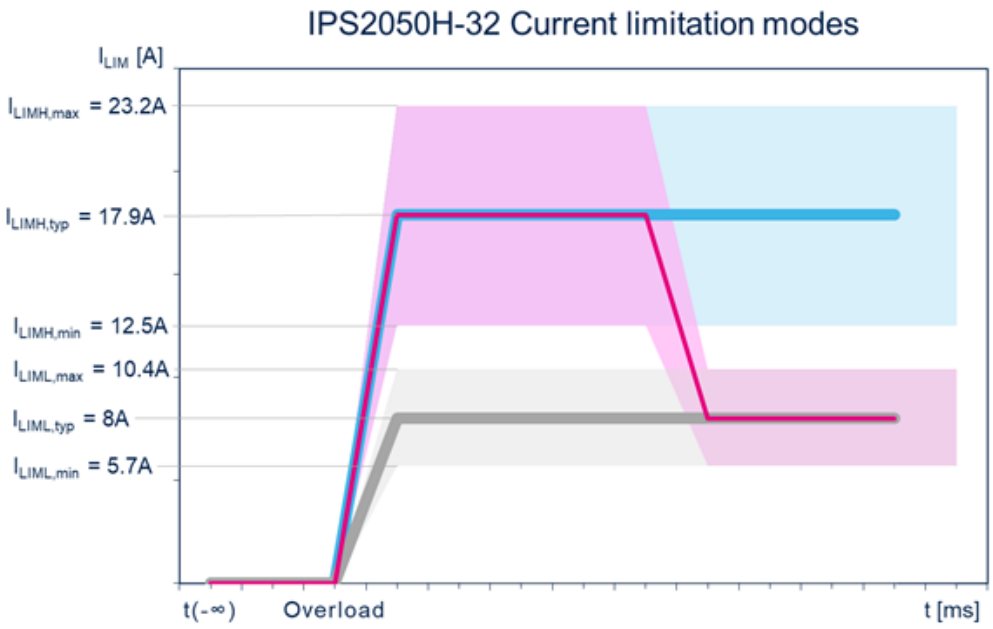


Figure 14. **Current limitation levels (IPS2050H-32/HQ-32)**

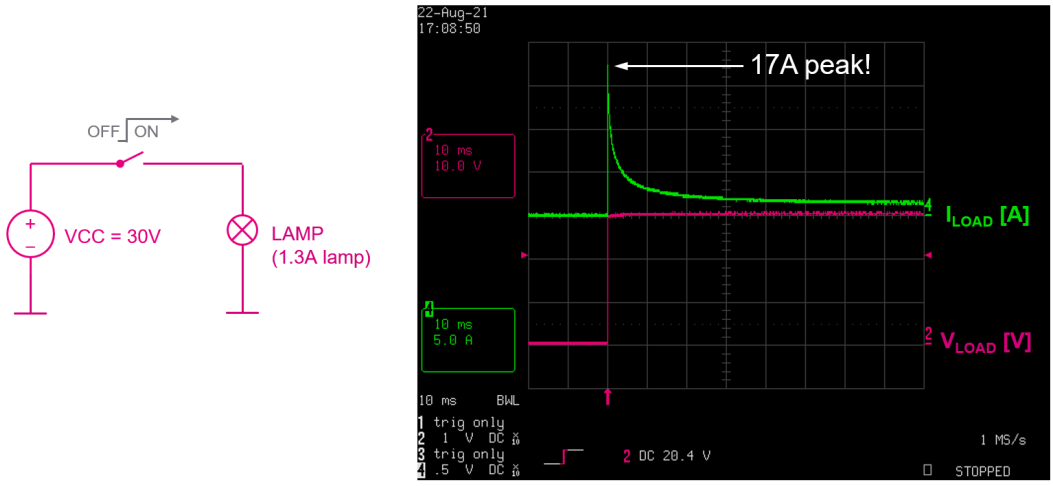


Current limitation activation thresholds and steady-state limit values of the IPS2050H-32/HQ-32 are shown in Figure 13 and Figure 14.

4 Function example: driving filament lamps

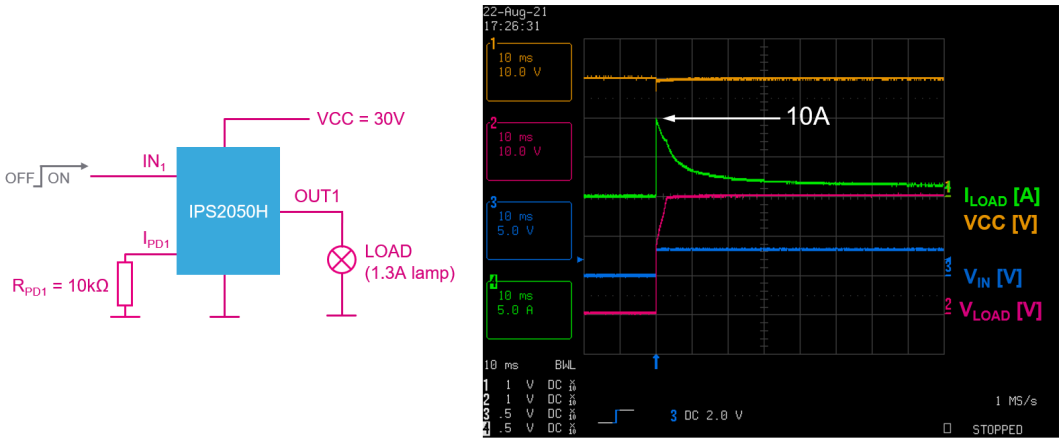
Let's examine the Smart Load Management in practice when driving lamps. A filament lamp can serve as a simple model example since it is characterized by a high current peak at switch-on. This effect is caused by a very low resistance of the filament until it is heated-up.

Figure 15. Cold lamp turn-on



In Figure 15 we see that the initial current transient reaches 17A during turn-on. Such a peak, if it occurs in a digital I/O system, can overload PCB tracks and components but it might also negatively affect power supply stability or contribute to severe EMC issues in the system.

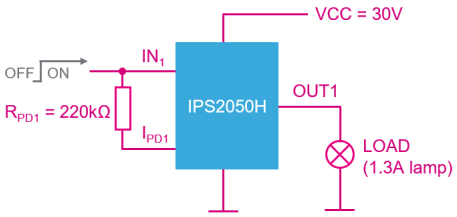
Figure 16. Current transient reduction using high-level limitation

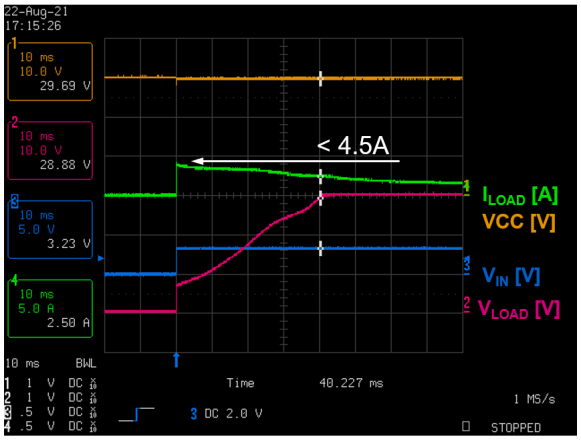


Using the high-level limitation, we can reduce the amplitude below 10A while still turning the lamp on in a comparable time (Figure 16). With this approach we can achieve a reasonable trade-off between current transient amplitude and switching dynamics.

However: 10A might still be too high an overcurrent for some designs (e.g. dense multichannel I/O modules with tiny connectors). In such cases, we can benefit from the low-level limitation mode. While this approach results in a slightly prolonged heat-up phase, it minimizes current transients and prevents associated EMC issues (Figure 17).

Figure 17. **dI/dt minimization using low-level limitation**





5 Package effects

As previously mentioned, the IPS2050 device family is available in two package options: PowerSSO 24 and QFN48L. The dimensions and the related differences in terms of thermal performances between the two packages are highlighted in this section.

Table 2 shows the values of thermal resistance, evaluated on a Jedec board; the thermal models that the $R_{TH(JA)}$ is calculated from are shown in Figure 18 and Figure 19.

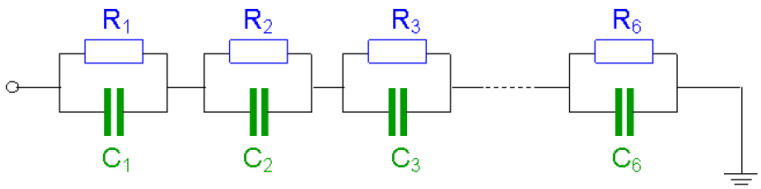
Table 2. IPS2050 family: package dimensions and thermal resistance

Device	Package	$R_{TH(JA)}$(1)
IPS2050H	PowerSSO 24 10.3 X 10.3 mm	22 °C/W
IPS2050H-32	PowerSSO 24 10.3 X 10.3 mm	22 °C/W
IPS2050HQ	QFN48L 8.0 X 6.0 mm	26 °C/W
IPS2050HQ-32	QFN48L 8.0 X 6.0 mm	26 °C/W

1. *Device mounted on a 2s2p Jedec board.*

Figure 18. IPS2050H/H-32 thermal model on 2s2p Jedec board

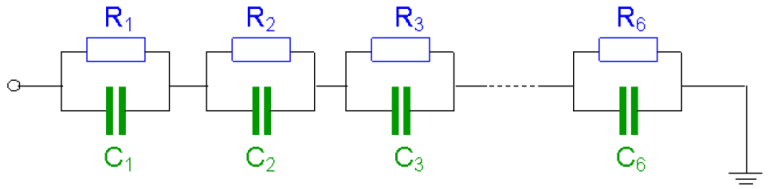
RC Ladder



	R1	R2	R3	R4	R5	R6
R (°C/W)	0.1419	0.59575	1.32612	3.40583	7.77506	11.1872
	C1	C2	C3	C4	C5	C6
C (Ws/°C)	7.09E-03	2.37E-02	6.95E-02	1.71E-01	8.21E-01	9.29
τ (s)	1.0061E-03	1.412E-02	9.213E-02	0.58128	6.38063	103.978

Figure 19. **IPS2050HQ/HQ-32 thermal model on 2s2p Jedec board**

RC Ladder



R (°C/W)	**R_1**	**R_2**	**R_3**	**R_4**	**R_5**	**R_6**
	0.1233	0.5111	1.535	5.196	7.76	11.35
C (Ws/°C)	**C_1**	**C_2**	**C_3**	**C_4**	**C_5**	**C_6**
	7.73E-03	2.46E-02	5.53E-02	1.49E-01	4.70E-01	8.68
τ (s)	9.5311E-04	1.257E-02	8.4886E-02	0.7742	3.6472	98.518

6 Max operating frequency

All electronic switches have a limit in terms of maximum operating frequency due to the switching losses and consequent device overheating, causing the thermal protection intervention.

The following figures summarize the maximum operating frequency versus the ambient temperature in the case of IPS2050H/HQ (Iout=2.4 A) and IPS2050H-32/HQ-32 (Iout=5.0 A).

The values are referred to a resistive load and input signal duty cycle of 50%.

Figure 20. IPS2050H and IPS2050HQ max. operating frequency vs. T_{AMB}

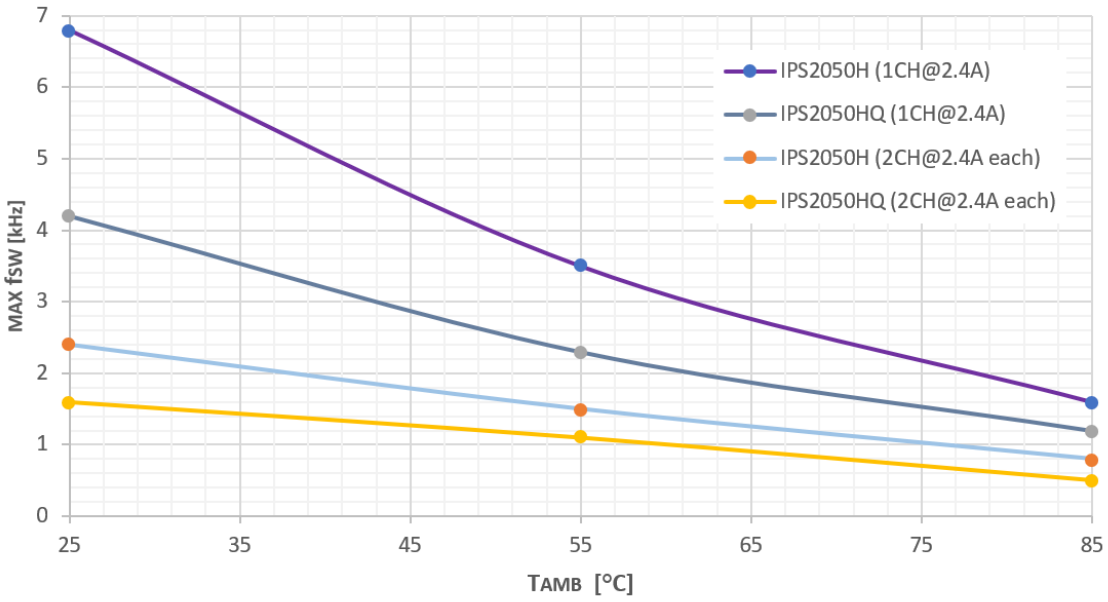
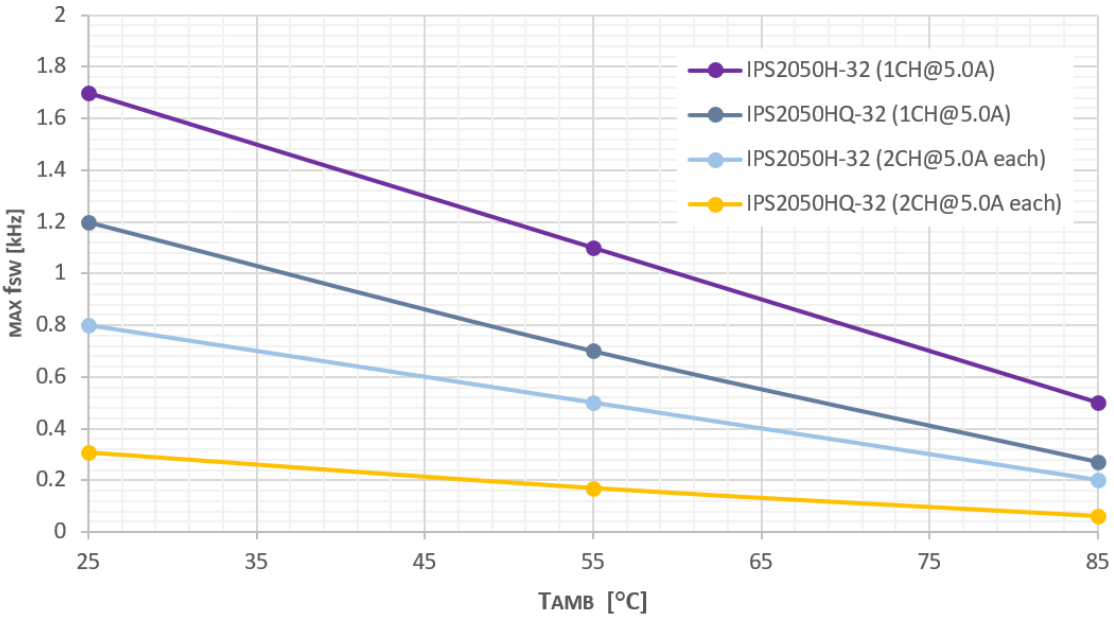


Figure 21. IPS2050-32 and IPS2050HQ-32 max. operating frequency vs. T_{AMB}



7 Summary

In this document, we introduced ST's new generation of Intelligent Power Switches, IPS2050H/HQ and IPS2050H-32/HQ-32, featuring an active inrush current control mechanism called Smart Load Management.

We outlined a common technical challenge in industrial digital I/O systems and proposed how it can be effectively solved with the new IPS. After a brief overview of the main IC parameters, we explained how it can be configured to one of three available operation modes and which are the datasheet parameters corresponding to each operation mode.

We demonstrated the effect of different configurations on a practical example using a filament lamp as a model of electrical load with inrush current.

Section 5 is dedicated to the effects of different packages (PowerSSO24 and QFN48L) on the IC's thermal performances. The thermal resistances $R_{TH(JA)}$ and related thermal models are reported.

The last section shows the maximum operating frequencies versus the ambient temperature for the different devices of the IPS2050 family.

The IPS2050H and IPS2050H-32 ICs were developed from many years of experience with industrial digital I/O design in mind, resulting in chips that are a perfect fit for long-lasting, reliable operation in the most challenging industrial applications.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
05-May-2022	1	Initial release.
15-Jul-2024	2	Changed title; added the reference to QFN package option in the whole document; added Section 5 and Section 6; some minor changes.

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