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Application note

Migrating from STM32F401, STM32F410, and STM32F411 to STM32H503 MCUs

Introduction

Designers of STM32 microcontroller applications must be able to easily replace one microcontroller type by another in the same product family or products from a different family.

Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on performance, new features, or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note analyzes the steps required to migrate from an existing design based on the STM32F401, STM32F410, or STM32F411 lines, to the STM32H503 line microcontrollers.

This document lists the full set of features available for the STM32F401, STM32F410 and STM32F411 devices, and the equivalent features on the STM32H503 line, and provides a guideline on both hardware and peripheral migration.

To fully benefit from this application note, the user must be familiar with the STM32 microcontroller family. For additional information, refer to the product datasheets and reference manuals.

1 General information

This document applies to Arm®-based devices.

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Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 STM32H503 overview

2.1 Main features

The STM32H503 devices include a larger set of peripherals with more advanced features compared to the STM32F401, STM32F410 and STM32F411 devices, such as the ones listed below:

- Security:
  - Flexible lifecycle scheme with secure debug authentication
  - True random number generator (RNG)
  - HASH processor, supporting SHA-1 checksums and SHA-2 secure hash ((SHA-1, SHA-224, SHA-256) and HMAC)
  - Active tamper
- Performance:
  - CPU, the Cortex®-M33
  - Frequency up to 250 MHz
  - Direct access to flash memory interface through ICACHE (without passing by AHB bus)
  - ICACHE for internal memories
- New peripherals:
  - New communication interface: I3C, FDCAN, LPUART
  - Low-power timer (LPTIM)
  - Clock recovery system (CRS)
  - Operational amplifiers (OPAMP)
  - Comparator (COMP)

Note: This document only manages the differences between the STM32F401, STM32F410, STM32F411 devices, and STM32H503 for the common features. The new features of STM32H503 are not covered. The detailed list of available features and packages for each product is available in the respective product datasheet.

2.2 System architecture

The STM32H503 devices embed memories (128 Kbytes of dual bank flash memory and 32 Kbytes of SRAM) and an extensive range of enhanced I/Os and peripherals connected to three APB buses, three AHB buses and a 32-bit multi-AHB bus matrix.

The following table illustrates the bus matrix differences between STM32F401/410/411 and STM32H503.

Table 1. Bus matrix

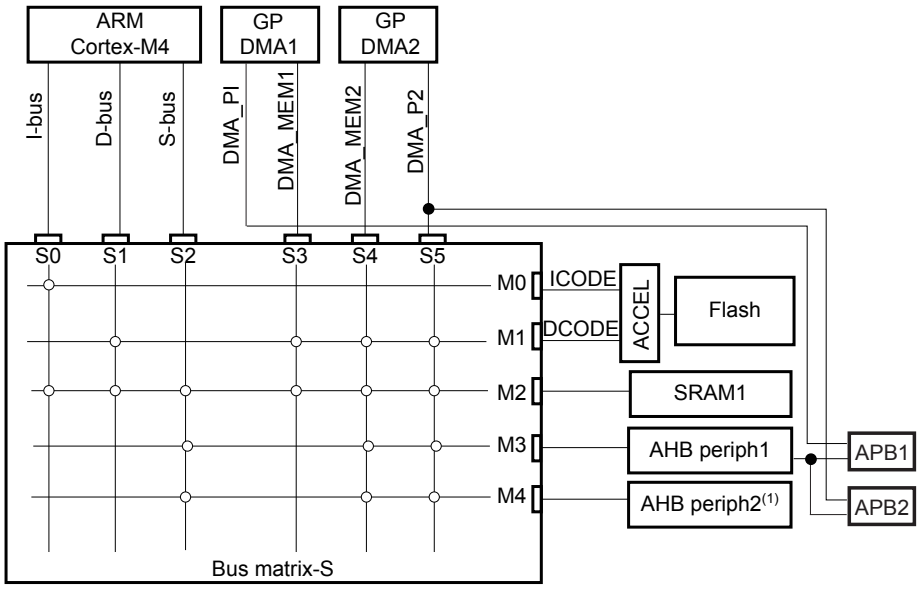
Bus type	STM32F401/410/411	STM32H503
AHB bus matrix masters	Up to 6 masters: CPU I-bus, D-bus, and S-bus, DMA1 memory bus, DMA2 memory bus, DMA2 peripheral bus	Up to 7 masters: Fast C-bus, CPU S-bus for internal memories, GPDMA1 (featuring two master ports), GPDMA2 (featuring two master ports)
AHB bus matrix slaves	Up to 5 slaves: Internal flash memory ICode bus, internal flash memory DCode bus, main internal SRAM, AHB1 peripherals (including AHB to APB bridges and APB peripherals), AHB2 peripherals(1)	up to 6 slaves: Internal flash memory, SRAM1, SRAM2, AHB1 peripherals (including APB1 and APB2), backup RAM, AHB2 peripherals, AHB3 peripherals

1. *Not available for STM32F410 line*

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

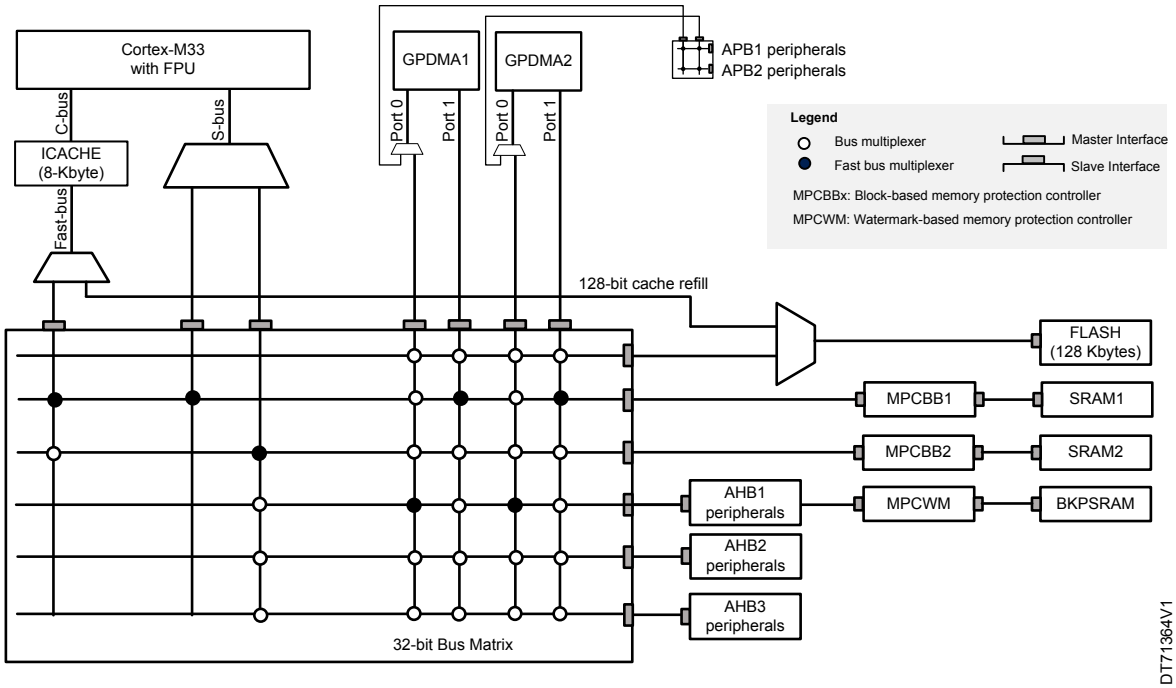
The system architectures of STM32F401/410/411 and STM32H503 are shown in the figures below.

Figure 1. STM32F401/410/411 devices system architecture



1. Only for STM32F401/411 devices

Figure 2. STM32H503 devices system architecture



3 Hardware migration

3.1 Package availability

The STM32H503 devices offer five packages from 25 to 64 pins.

The table below lists the available packages on the STM32H503 line compared to STM32F401, STM32F410, and STM32F411.

Table 2. Packages available

Package[1] (size in mm x mm)	STM32F401/411	STM32F410	STM32H503
LQFP100 (14 x 14 mm)	X	NA	NA
LQFP64 (10 x 10 mm)	X	X	X
LQFP48 (7 x 7 mm)	NA	X	X
UFQFPN48 (7 x 7 mm)	X	X	X
UFQFPN32 (5 x 5 mm)	NA	NA	X
UFBGA100 (7 x 7 mm)	X	NA	NA
UFBGA64 (5 x 5 mm)	NA	X	NA
WLCSP	WLCSP49	WLCSP36	WLCSP25

1. *X = available. NA = not available.*

3.2 Pinout compatibility

The STM32F401, STM32F410 and STM32F411 lines are not identical with the STM32H503 devices in term of MCU port assignment to package terminals, that is, in term of pinout. This holds for all common package types of the package list in Table 2.

For the LQFP64 and UFQFPN48 packages, the PB9 pin is replaced in the STM32H503 devices with a VCAP pin.

3.2.1 LQFP64 package

Figure 3. STM32H503 LQFP64 pinout

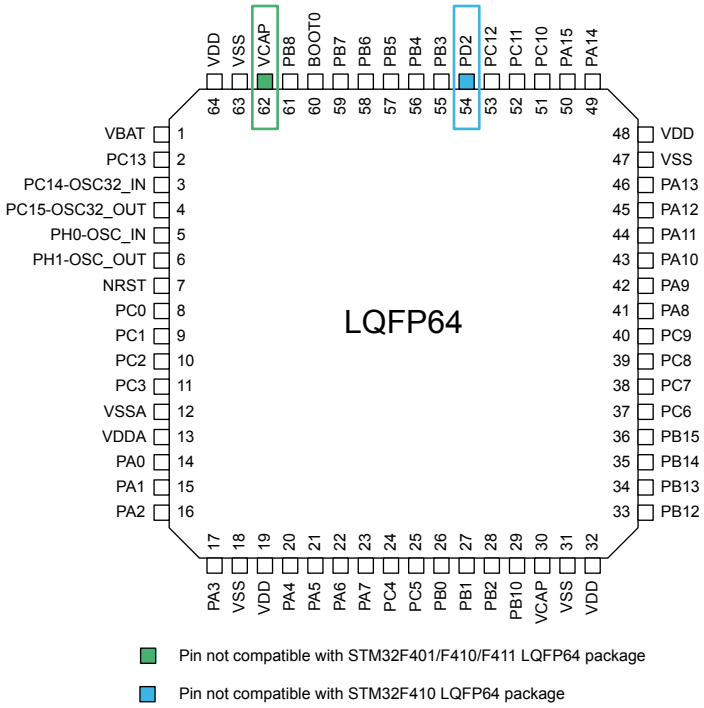


Table 3. LQFP64 pinout difference

LQFP64 pin number	STM32F401/411 pinout	STM32F410 pinout	STM32H503 pinout
62	PB9	PB9	VCAP
54	PD2	PB11	PD2

3.2.2 LQFP48 package

Figure 4. **STM32H503 LQFP48 pinout**

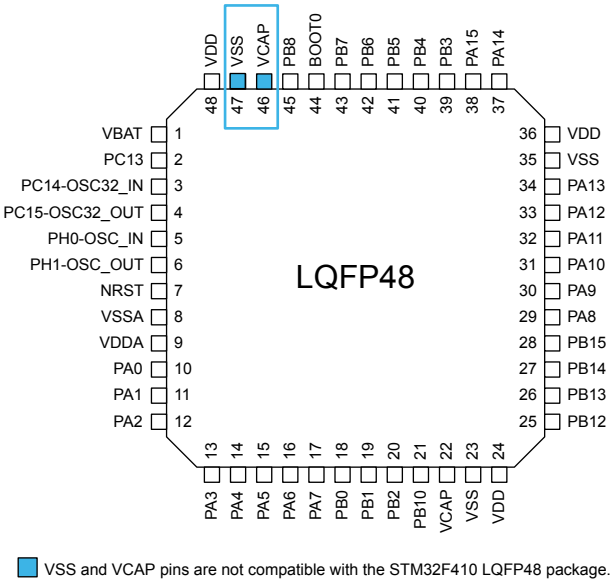


Table 4. **LQFP48 pinout difference**

LQFP48 pin number	STM32F410 pinout	STM32H503 pinout
47	PDR-ON	VSS
46	VSS	VCAP

3.2.3 UFQFPN48 package

Figure 5. STM32H503 UFQFPN48 pinout

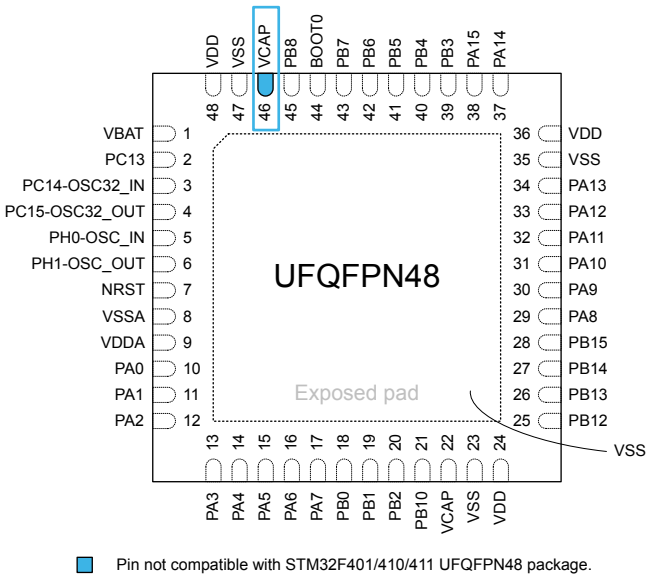


Table 5. UFQFPN48 pinout difference

UFQFPN48 pin number	STM32F401/410/411 pinout	STM32H503 pinout
46	PB9	VCAP

4 Boot mode compatibility

4.1 Boot mode selection for STM32F401/410/411 devices

In the STM32F4xx, three different boot modes can be selected through the BOOT[1:0] pins as shown in the table below.

Table 6. Boot modes for STM32F401, STM32F410, and STM32F411 devices

Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
X	0	Main flash memory	Main flash memory is selected as the boot space
0	1	System memory	System memory is selected as the boot space
1	1	Embedded SRAM	Embedded SRAM is selected as the boot space

4.2 Boot mode selection for STMH503 devices

At startup, a BOOT0 pin and NSBOOTADD[31:8] option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory
  - Bootloader
  - Debug authentication library (ST-DA)

When boot from user flash memory is selected, the boot address is defined by NSBOOTADD. This address can be locked thanks to NSBOOT_LOCK.

Table 7. Boot modes for STM32H503

PRODUCT_STATE	BOOT0 pin	Boot address option byte selection	Boot area	ST programmed default value
Open	0	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000
	1	NA	Bootloader	Bootloader
Provisioning	X	NA	Bootloader	Bootloader
Provisioned, closed, locked	X	NSBOOTADD[31:8]	Boot address defined by user option byte NSBOOTADD[31:8]	Flash: 0x0800 0000

4.3 System bootloader

The system bootloader is located in the system memory, programmed by ST during the production. It is used to reprogram the flash memory using one of the following serial interfaces.

Table 8 shows the supported communication peripherals by the system bootloader.

For more details, refer to the "STM32 microcontroller system memory boot mode" application note (AN2606) available on www.st.com.

Table 8. Bootloader communication peripherals

System bootloader peripherals	STM32F410 I/O pin	STM32F401 and STM32F411 I/O pin	STM32H503 I/O pin
DFU	NA	PA11/PA12	
USART1	PA10/PA9		
USART2	PA2/PA3	PD5/PD6	PA15/PA5
USART3	NA	NA	PA3/PA4

System bootloader peripherals	STM32F410 I/O pin	STM32F401 and STM32F411 I/O pin	STM32H503 I/O pin
CAN	NA		FDCAN1 (PB5/PB15)
I2C1	PB6/PB7		NA
I2C2	PB10/PB11		PB3/PB4
I2C3	NA	PA8/PB4	NA
I2C4	PB10/PB3(1) And PB15/PB14(2)	NA	NA
I3C1	NA	NA	PB6/PB7
SPI1	PA15/PA5/PB4/PB5(1) PA4/PA5/PA6/PA7(2)	PA4/PA5 /PA6/PA7	PA7/PA0/PA8/PB8
SPI2	PB12/PB13/PC2/PC3	PB12/PB13/PB14/PB15	PB1/PB14/PB10/PB12
SPI3	NA	PA15/PC10/PC11/PC12	PC12/PC11/PC10/PD2

1. *For STM32F410Tx devices.*
2. *For STM32F410Cx/Rx devices.*

5 Peripheral migration

5.1 Cross-compatibility between STM32 products

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group1: peripherals by definition common to all products.
  Those peripherals are identical. They have the same structure, registers, and control bits. There is no need to perform any firmware changes to keep the same application level functionality after migration. All the features and behavior remain the same.
- Group2: peripherals shared by all products but with only minor differences (in general to support new features).
  The migration from one product to another is very easy and does not need any significant new development effort.
- Group3: peripherals that have considerable changes from one product to another (new architecture or new features for example.
  For this group of peripherals, the migration requires a new development at application level.

The following table summarizes the available peripherals in STM32F401/410/411 compared to STM32H503.

Table 9. STM32 peripheral compatibility between products

Peripherals		STM32F401/ 411	STM32F410	STM32H503
Core		Cortex-M4		Cortex-M33
Maximum CPU frequency		Up to 100 MHz (for STM32F410/F411 lines) Up to 84 MHz (for STM32F401 line)	Up to 100 MHz	up to 250 MHz
Flash memory (Kbytes)		Up to 512 Kbytes	Up to 128 Kbytes	128 Kbytes
SRAMs (Kbytes)	System	64 Kbytes (for STM32F401xB/C devices) 96 Kbytes (for STM32F411xC/E devices) 128Kbytes(for STM32F401xD/E devices)	32 Kbytes	32 Kbytes
	Backup	NA		2 Kbytes
Timers	General purpose	5(16-bit) and 2(32-bit)	2 (16-bit) and 1(32-bit)	1 (32 bits) and 1 (16 bits)
	Advanced control	1(16 bits)		
	Basic	NA	1(16 bits)	2(16 bits)
	Low power	NA	1	2 (16 bits)
	SysTick timer	1		
	Watchdog timers (independent, window)	2		
Communication interfaces	SPI / I2S	Up to 5/5 (for STM32F411 line) Up to 4/2 (for STM32F401 line)	Up to 3/3	Up to 3x SPIs (up to 6x SPI adding 3x SPI from 3x USART when configured in synchronous mode)
	I2C	3 x I2C interfaces (SMBus/ PMBus)	3x I2C interfaces (SMBus/PMBus) including 1x I2C Fast-mode at 1 MHz	2 (FM + interfaces (SMBus/PMBus))

Peripherals		STM32F401/ 411	STM32F410	STM32H503
Communication interfaces	I3C	NA		2
	USART / UART	Up to 3 USARTs: 2 x 10.5 Mbit/s, 1 x 5.25 Mbit/s (for STM32F401 line) 2 x 12.5 Mbit/s, 1 x 6.25 Mbit/s (for STM32F411 line)	Up to 3 USARTs (2 x 12.5 Mbit/s, 1 x 6.25 Mbit/s)	3
	LPUART	NA		1
	USB	USB OTG FS	NA	USB
	FDCAN	NA		1
	SDIO	Yes	No	No
CRC		Yes		Yes
DMA		2		2 GPDMA (general purpose DMA featuring two master ports) Privileged/unprivileged support/ Linked-list
Real time clock (RTC)		Yes		Yes
random number generator (RNG)		No	Yes	Yes
HASH		No		Yes (SHA-256)
GPIOs		Up to 81	Up to 50	Up to 49
ADC (12bits)		1(12-bit, ADC, up to 2.4 MSPS) 16 channels		1(12-bit ADC, up to 2.5 MSPS in 12-bit) 16 channels
DAC (12bits)		NA	1	1
Operational amplifier (OPAMP)		NA		Yes(1x operational amplifier (up to 7 MHz bandwidth))
Comparator (COMP)		NA		Yes (1x ultra-low-power comparators)
RCC		Yes		Yes
Operating temperatures		Ambient temperatures: –40 to +85 °C/–40 to +105 °C/–40 to +125 °C –40 to +85 °C/–40 to +105 °C(1)	Ambient temperatures: – 40 to +85 °C / – 40 to + 105 °C / – 40 to + 125 °C	Ambient operating temperature: -40 to 85 °C/105 °C, and up to 125 °C at low dissipation
		Junction temperature: –40 to + 130 °C –40 to + 125 °C(1)	Junction temperature: –40 to + 130 °C	Junction temperature: -40 to 130 °C
Operating voltage		1.7 V to 3.6 V	1.7 to 3.6 V or 1.8 to 3.6 V(2)	1.71 to 3.6 V

1. *Only for STM32F401xD/xE devices.*
2. *Only for STM32F410CxU/RxT devices.*

5.2 System peripherals

5.2.1 Embedded flash memory (FLASH)

The following table compares the flash memory interface on the STM32F401/410/411 and STM32H503 devices.

Table 10. Flash memory features

Flash memory	STM32F401, STM32F410, and STM32F411	STM32H503
Main / Program memory	• Up to 128 Kbytes (for STM32F410 line) • Up to 512 Kbytes (for STM32F401/411 lines) • Programming granularity: 8, 16, 32, 64-bit • Read granularity: 128-bit	• Up to 128 Kbytes (dual bank) • Flash memory read operations supporting multiple lengths: 128 bits, 64 bits, 32 bits, 16 bits, or one byte • 8 Kbytes sector erase, bank erase, and dual-bank mass erase
Read while write (RWW)	No	Yes
Error code correction (ECC)	No	• One error detection/correction or two error detections per 128-bit flash word using 9 ECC bits
Wait states	Configurable wait states depending on the supply voltage and frequency	
One time programmable (OTP) memory	• 512 OTP bytes for user data	• 2 Kbytes (OTP) area
FLASH security and protections	• Read protection (RDP) • Write protections • Proprietary code readout protection (PCROP)	• Life cycle management • Write protections • HDP protection providing temporal isolation • Privilege protection • OTP locking
User option bytes(1)	nRST_STDBY nRST_STOP WDG_SW BOR_LEV OPTSTRT OPTLOCK nWRP RDP USER SPRMOD	NRST_STBY NRST_STOP IWDG_SW WWDG_SW IWDG_STBY, IWDG_STOP BOR_LEV BORH_EN PRODUCT_STATE IO_VDDIO2_HSLV IO_VDD_HSLV SWAP_BANK SRAM1_RST SRAM2_RST BKPRAM_ECC SRAM1_ECC SRAM2_ECC WRPx Bank1, WRPx Bank2

1. *Refer to the “Option-byte organization” table in the reference manual that provides all user option bytes.*

5.2.2 SRAMs

In the STM32F401, STM32F410, and STM32F411, the control of SRAM is integrated within the SYSCFG.

However, in STM32H503, a new peripheral, the RAMCFG controller, is dedicated to control SRAM1, SRAM2, and BKPSRAM. For more details, refer to the "RAM's configuration controller" section of the product reference manual.

Table 11. SRAM features

Features	STM32F401, STM32F410 and STM32F411	STM32H503
Size	• 32 Kbytes (for STM32F410 line) • Up to 96 Kbytes (for STM32F401 line) • 128 Kbytes (for STM32F411 line)	34-Kbyte SRAMs and BKPSRAM: • 16-Kbyte SRAM1 • 16-Kbyte SRAM2 • 2-Kbyte BKPSRAM
Access by DMA and CPU	Bytes, half-words (16 bits), or full words (32 bits) possible access.	
CPU access bus	System bus or I-Code/D-Code buses	System bus or C-bus BKPSRAM (only system bus)
Retention	NA	• Optional retention in standby mode (BKPSRAM) • Optional retention in VBAT mode (BKPSRAM) • Optional retention in stop mode (SRAM1, SRAM2, BKPSRAM)
Privilege protection	NA	• The SRAM1 and SRAM2 can be programmed as privileged or unprivileged by blocks, using the MPCBB with a block granularity of 512 bytes. • Backup SRAM regions can be programmed as privileged or unprivileged with watermark, using the MPCWM with 32 bytes granularity.
Hardware and software erase conditions	NA	• SRAM1 and SRAM2 erase can be requested by executing a specific software sequence, detailed in section ‘RAMCFG’ of the product reference manual. • SRAM2 and optionally backup SRAM are protected by the tamper detection circuit, and are erased by hardware in case of tamper detection. The SRAM1, SRAM2, and BKPSRAM are erased in case of regression.
System reset erase	NA	• SRAM2 can be erased with a system reset using the option bit SRAM2_RST option bit in the flash memory user option bytes. • SRAM1 is erased when a system reset occurs if the SRAM1_RST option bit is selected in the flash memory user option bytes.
Error detection and correction	NA	• Single error detection and correction with interrupt generation • Double error detection with interrupt or NMI generation • ECC is supported by SRAM1, SRAM2, and BKPSRAM when enabled with the SRAM1_ECC, SRAM2_ECC and BKPRAM_ECC user option bit • ECC: 7 bits are added per 32 bits • Interrupts are generated when single- and/or double-ECC errors are detected: – Two ECC RAMCFG interrupts – One ECC NMI interrupt
Write protection	NA	• SRAM2 can be write-protected with a page granularity of 1 Kbyte. Each 1-Kbyte page can be write-protected by setting its corresponding PxWP (x = 0 to 15) bit in RAMCFG registers.

5.2.3 System configuration controller (SYSCFG/SBS)

The table below illustrates the system configuration controller (SYSCFG) main differences between STM32F401, STM32F410, STM32F411, and STM32H503 devices.

For STM32H503 devices, the SYSCFG (system configuration controller) is integrated in the SBS (system configuration, boot, and security).

Table 12. System configuration features

STM32F401, STM32F410, and STM32F411	STM32H503
• Managing the I/O compensation cell	
• Remap the memory accessible in the code area • Manage the external interrupt line connection to the GPIOs	NA
NA	• Enabling/disabling the FMP high-drive mode of some I/Os and voltage booster for I/O analog switches • Configuring security register access • Tracking the PVT conditions to control the current slew-rate and output impedance in the I/O buffer through compensations cells • Two compensation cells are embedded, one for the I/Os supplied by VDDIO power rail and one for the I/Os supplied by VDDIO2 power rail

5.2.4 Instruction caches (ICACHE)

The STM32H503 embeds an ICACHE (8 Kbytes).

The instruction cache (ICACHE) is introduced on the C-AHB code bus of the Cortex-M33 processor to improve performance when fetching instructions and data from internal memories.

The STM32F401, STM32F410, and STM32F411 devices do not embed this cache.

5.2.5 Direct memory access controller (DMA)

The STM32F401, STM32F410, STM32F411, and STM32H503 have different DMA architecture and features.

All devices embed two DMA controllers:

- DMA1 (eight channels) and DMA2 (eight channels) for STM32F401, STM32F410, and STM32F411
  Each channel is dedicated to manage the memory access requests from one or more peripherals.
  The devices embed also an arbiter for handling the priorities among the DMA requests
- GPDMA1 (eight channels) and GPDMA2 (eight channels) for STM32H503
  Each GPDMA instance has the same channel-based implementation and is connected to the same requests and triggers.

The following table illustrates the main differences between DMA requests in STM32F401, STM32F410, STM32F411, and STM32H503.

Table 13. DMA features

Peripherals	STM32F401, STM32F410, and STM32F411		STM32H503	
	DMA1	DMA2	GDMA1	GDMA2
Architecture	Each instance of DMA controllers can access memory and peripherals			
Number of instances	1	1	1	1
Number of masters	Dual AHB master bus		Dual bidirectional AHB master	
Number of channels	8	8	8	8
Privileged/unprivileged DMA	No		Yes	
Linked-list				

5.2.6 Reset and clock control (RCC)

The table below presents the main differences related to the RCC (reset and clock controller) between the STM32F401, STM32F410, STM32F411 devices, and STM32H503 devices.

Table 14. RCC features

RCC	STM32F401, STM32F410, and STM32F411	STM32H503
HSI	16 MHz RC oscillator	64 MHz RC oscillator
CSI	NA	CSI: low-power RC oscillator that can be used directly as system clock, peripheral clock, or PLL input: • Low-cost clock source since no external crystal is required • Faster startup time than HSI (a few microseconds) • Very low-power consumption, The CSI provides a clock frequency of approximately 4 MHz.
HSI48	NA	48 MHz RC oscillator HSI48 can drive USB and RNG.
LSI	32 kHz RC Lower consumption	
HSE	From 4 to 26 MHz	From 4 to 50 MHz
LSE	32.768 kHz	32.768 kHz Configurable drive/consumption
PLL	Two PLLs: • A main PLL (PLL) clocked by the HSE or HSI oscillator • A dedicated PLL (PLLI2S) generates an accurate clock	• Two PLLs: – Main PLL (PLL1) provides clocks for CPU and some peripherals – PLL2 used to generate the kernel clock for peripherals • Each PLL offers two outputs with post-dividers. • Input frequency range: – 2 to 16 MHz for the VCO in wide-range mode – 1 to 2 MHz for the VCO in low-range mode
AHB frequency	Up to 100 MHz (for STM32F410/411 lines) Up to 84 MHz (for STM32F401 line)	Up to 250 MHz
APB1 frequency	Up to 42 MHz (STM32F401 line) Up to 50 MHz (STM32F410/411 lines)	Up to 250 MHz
APB2 frequency	Up to 84 MHz (STM32F401 line) Up to 100 MHz (STM32F410/F411 lines)	Up to 250 MHz
RTC clock source	LSI, LSE, or HSE (1 MHz) using 1/2, 1/3, ¼ clock predivider	LSE, LSI, or HSE/ 32
System clock source	HSI, HSE, or PLL	HSI, CSI, HSE, or PLL1
Clock security system	CSS (clock security system) on HSE and CSS on LSE	
MCO clock source	• MCO1 pin (PA8): HSI, LSE, HSE, PLLCLK • MCO2 pin (PC9): HSE, PLLCLK, SYSCLK, PLLI2S	• MCO1 pin (PA8): HSI, LSE, HSE, PLL1 or HSI48 • MCO2 pin (PC9): SYSCLK, PLL2, HSE, PLL1, CSI, or LSI

5.2.7 Peripheral clock configuration

The peripherals presented below have a dedicated clock source, which is used to generate the clock required for their operation. This section presents the difference between STM32F401, STM32F410, STM32F411, and STM32H503 devices for some peripherals with different clock sources.

Table 15. Peripherals with different clock sources

Peripherals	STM32F401, STM32F410 and STM32F411	STM32H503
U(S)ART	APB1 or APB2 clock (PCLK1 or PCLK2)	rcc_pclk1(1) rcc_pclk2(2) pll2_q_ck hsi_ker_ck csi_ker_ck lse_ck
I2Cs	APB1 clock (PCLK1)	rcc_pclk1 pll2_r_ck hsi_ker_ck csi_ker_ck
SPI	APB Clock (PCLK)	Pll1_q_ck pll2_p_ck AUDIOCLK per_ck
I2S	PLLI2S External clock mapped on I2S_CKIN pin	pll1_q_ck pll2_p_ck AUDIOCLK per_ck
ADC	APB2 clock (PCLK2)	rcc_hclk sys_ck pll2_r_ck hse_ck hsi_ker_ck csi_ker_ck
USB FS	PLL 48 MHz derived from main PLL VCO (PLLQ clock) (USB is not available for STM32F410 line)	hsi48_ker_ck pll1_q_ck pll2_q_ck
IWDG	LSI	

1. *Only for UARTx (x=2,3) and USARTx.*
2. *Only for USART1.*

5.2.8 Power (PWR)

The table below presents the PWR controller differences between STM32F401, STM32F410, STM32F411 devices, and STM32H503 devices. Both dynamic and static power-consumption had been optimized for the STM32H503 devices.

Table 16. PWR features

PWR	STM32F401, STM32F410, and STM32F411	STM32H503
Power supplies	• VDD = 1.7 to 3.6 V (when internal voltage regulator is disabled) • VDD = 1.8 to 3.6 V (when internal voltage regulator is enabled) • External power supply for I/Os, flash memory, and internal regulator. It is provided externally through VDD pins	• VDD = 1.71 V to 3.6 V: external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through the VDD pins. • Regulator OFF (LDO bypass)
	• VSSA and VDDA = 1.7 to 3.6 V: external analog power supply for A/D and D/A converters. VDDA and VSSA must be connected to VDD and VSS respectively.	• VDDA = 1.62 V (ADC, COMP) / 1.8 V (DAC), or 2.0 V (OPAMP) to 3.6 V: external analog power supply for A/D converters, D/A converters, operational amplifier, and comparator. The VDDA voltage level is independent from the VDD voltage.
	V12: voltage source through VCAP_1 and VCAP_2 pins (when available)/around 1.2 V	• VCAP: power supply for digital peripherals, SRAMs (except BKPSRAM), and embedded flash memory.
	• VBAT = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when VDD is not present.	• VBAT = 1.2 to 3.6 V: when VDD is not present. VBAT is the power supply for RTC, external clock 32 kHz oscillator, backup registers, and optionally backup SRAM
	NA	• VDDIO2 = 1.08 V to 3.6 V: external power supply for 9 I/Os (PA8, PA9, PA15, PB3:8). This voltage is independent from the VDD voltage
Battery backup domain	RTC with backup registers LSE PC13 to PC15 I/Os	
Power supply supervisor	POR, PDR, BOR, PVD	
	NA	• VDDIO2 voltage monitor • Analog voltage detector (AVD) • Backup domain voltage and temperature monitoring
Sleep mode wakeup sources	Any peripheral interrupt/wakeup event	
Standby mode wakeup sources	• WKUP pin on rising edge, RTC event (RTC ALARM, tamper event, time stamp event), IWDG reset, external reset in NRST pin	• WKUPx pin edge, RTC event, external reset in NRST pin, and IWDG reset.
Stop mode wakeup sources	• Any EXTI line (configured in the EXTI registers, internal and external lines)	• Any EXTI line (configured in the EXTI registers) specific peripherals events.
Wakeup system clock	Stop: HSI RC oscillator	• Stop: CSI when STOPWUCK = 1 in RCC_CFGR, HSI with the frequency before entering the stop mode, up to 64 MHz, when STOPWUCK • Standby: HSI clock at 64 MHz

PWR	STM32F401, STM32F410, and STM32F411	STM32H503
Low power modes	The devices feature these low-power modes: • Sleep mode: Cortex®-M4 with FPU core stopped, peripherals kept running • Stop mode: all clocks are stopped • Standby mode: 1.2 V domain powered off • Batch acquisition mode (BAM): the devices are in sleep mode, the flash memory is off, the needed peripheral are kept running, and data transfer are still possible through DMA (this mode is only available for the STM32F410 line).	The devices feature these low-power modes: • Sleep mode: CPU clock off, all peripherals including the Cortex-M33 core such as NVIC and SysTick can run and wake up the CPU when an interrupt or an event occurs. • Stop mode: To further optimize the power consumption, the unused RAMs (SRAM1 or SRAM2) can be shut-off • Standby mode: – VCORE domain powered OFF. – I/Os output state can be retained.

The following figures present the power supply for the STM32F401, STM32F410, STM32F411, and STM32H503 devices. The differences are summarized in the previous table.

Figure 6. **STM32H503 power supply overview**

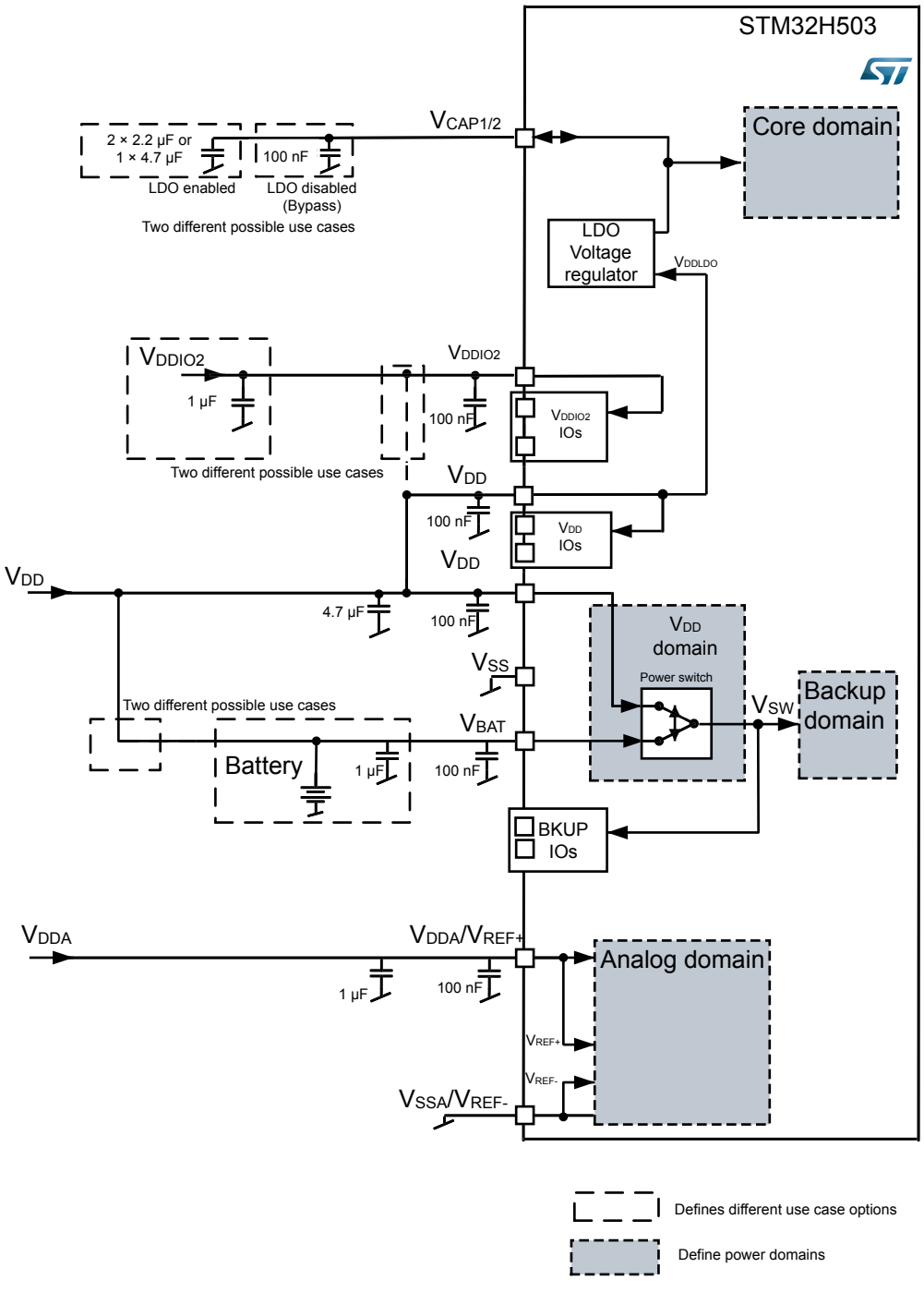
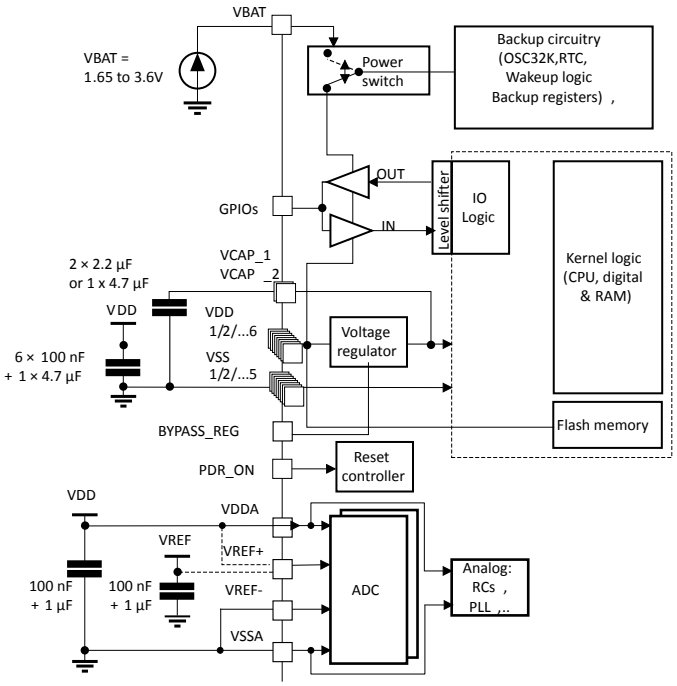


Figure 7. **Power supply overview for STM32F401/F410/F411**



5.2.9 General-purpose I/Os (GPIO)

The STM32H503 implements the same GPIO features than STM32F401, STM32F410, and STM32F411, but with the main differences. For STM32H503, each general-purpose I/O port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR), a 16 bits reset register (GPIOx_BRR), and a 32-bit set/reset register (GPIOx_BSRR). In addition, all GPIOs have a 32-bit locking register (GPIOx_LCKR), two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL) and a high-speed low-voltage register (GPIOx_HSLVR).

I/Os output digital state retention during standby mode

In the standby mode, the I/Os are by default in the floating state. If the IORETEN bit in the PWR_IORETR register is set, the I/Os state is sampled during standby entry. The state of I/Os is applied to the pin via pull-up and pull-down resistors. The pull-up and pull-down resistors remain applied after the standby wakeup until the IORETEN bit in the PWR_IORETR register is cleared by software.

High-speed low-voltage mode (HSLV)

Some I/Os have the capability to increase their maximum speed at low voltage by configuring them in HSLV mode. The I/O HSLV bit controls whether the I/O output speed is optimized to operate at 3.3 V (default setting) or at 1.8 V (HSLV = 1).

For more information about the STM32H503 GPIO, refer to the “General-purpose I/Os (GPIO)” section of the reference manual, and to the product datasheet for detailed description of the pinout and alternate function mapping.

5.2.10 Extended interrupt and event controller (EXTI)

5.2.10.1 EXTI main features in STM32H503 devices

The extended interrupts and event controller (EXTI) manages the individual CPU and system wakeup through configurable event inputs. It provides wakeup requests to the power control and generates an interrupt request to the CPU NVIC and events to the CPU event input. For the CPU, an additional event generation block (EVG) is needed to generate the CPU event signal.

EXTI privilege protection

When the privilege is enabled for an input event, the associated input event configuration and control bits can only be modified and read by a privileged access. An unprivileged write access is discarded and a read returns 0.

The table below describes the difference of EXTI features between STM32F401, STM32F410, STM32F411 devices and STM32H503 devices.

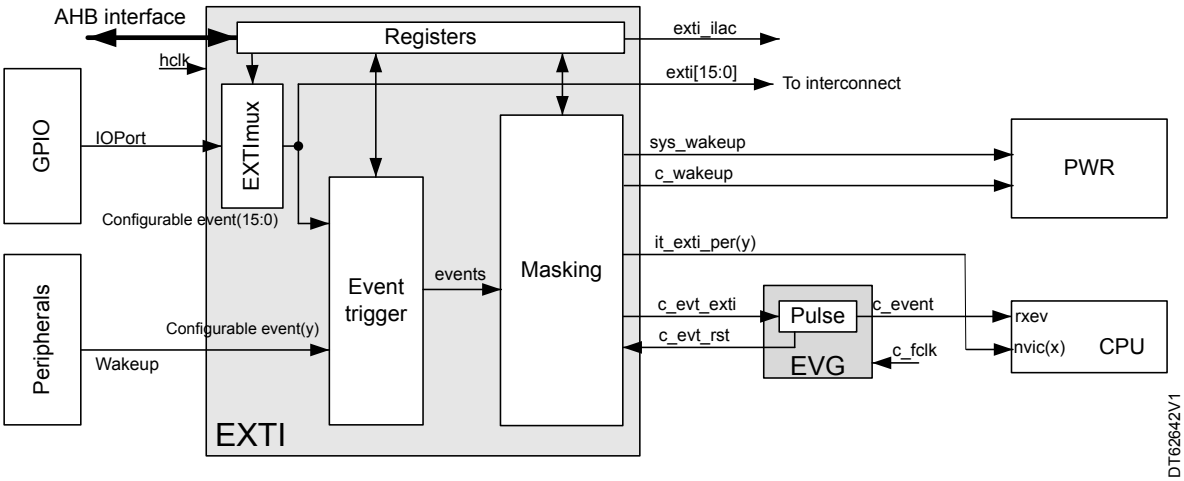
Table 17. EXTI features

EXTI	STM32F401, STM32F410 and STM32F411	STM32H503
Features	• Generation of up to 23 software event/interrupt requests	• 54 input events supported • Privileged/unprivileged mode

5.2.10.2 *EXTI block diagram in STM32H503 devices*

As shown in Figure 8, the EXTI consists of a register block accessed via an AHB interface, an event input trigger block, a masking block and EXTI mux. The register block contains all the EXTI registers. The event input trigger block provides event input edge trigger logic.

Figure 8. EXTI block diagram on STM32H503 devices



The table below presents the EXTI line differences between STM32F401, STM32F410, STM32F411 and STM32H503 devices.

Table 18. EXTI line differences

EXTI line	STM32F401 and STM32F411	STM32F410	STM32H503
0-15	16 external interrupt lines		GPIO
16	PVD output		PVD/AVD output
17	RTC alarm event		RTC
18	USB OTG FS wakeup event	NA	Reserved
19	NA	NA	TAMP
20	NA	NA	Reserved
21	RTC tamper and TimeStamp events		I2C1 wakeup
22	RTC wakeup event		I2C2 wakeup
23	NA	LPTIM1 asynchronous interrupt	Reserved
24	NA	NA	I3C wakeup
25			USART1 wakeup
26			USART2 wakeup
27			USART3 wakeup
28			I3C2 wakeup
29			COMP1 output wakeup
30-36			Reserved
37			LPUART1 wakeup
38			LPTIM1
39			LPTIM2

EXTI line	STM32F401 and STM32F411	STM32F410	STM32H503
40	NA	NA	SPI1 wakeup
41			SPI2 wakeup
42			SPI3 wakeup
43-46			Reserved
47			USB wakeup
48			Reserved
49			LPTIM2 CH1
50			DTS wakeup
51-52			Reserved
53			VDDIO2 voltage monitor

5.2.10.3 *CRC calculation unit*

The table below presents the CRC differences between the STM32F401, STM32F410, STM32F411 and STM32H503 devices.

Table 19. CRC features

CRC	STM32F401, STM32F410 and STM32F411	STM32H503
Features	• Uses CRC-32 (ethernet) polynomial: – Single input/output 32-bit data register – CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size – General-purpose 8-bit register (can be used for temporary storage)	
	• Handles 32-bit data size	• Handles 8-,16-, 32-bit data size fully programmable polynomial with programmable size (7, 8, 16, 32 bits) • Programmable CRC initial value • Input buffer to avoid bus stall during calculation • Reversibility option on I/O data • Accessed through AHB slave peripheral by 32-bit words only, with the exception of CRC_DR register that can be accessed by words, right-aligned half-words and right-aligned bytes
CRC Registers	• CRC data register (CRC_DR) • CRC independent data register (CRC_IDR) • CRC control register (CRC_CR) • CRC register map	
	NA	• CRC initial value (CRC_INIT) • CRC polynomial (CRC_POL)

5.3 Security peripherals

5.3.1 Random number generator (RNG)

The STM32H503 and STM32F410 embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit. The table 20 presents the RNG features of STM32H503 and STM32F410.

Note: RNG is not available on STM32F401 and STM32F411.

Table 20. RNG features

RNG	STM32F410	STM32H503
Features	• RNG delivers 32-bit random numbers • RNG produces one 32-bit random samples every 42 RNG clock cycles • RNG allows embedded continuous basic health tests with associated error management	• RNG delivers 32-bit true random numbers • Can be used as entropy source to construct a nondeterministic random bit generator (NDRBG) • Tested using German BSI statistical tests of AIS-31 (T0 to T8) • Embeds start-up and NIST SP800-90B approved continuous health tests • RNG internal tamper event signal to TAMP • Can be enabled with an automatic low-power mode (default configuration)
	AHB slave peripheral, accessible through 32-bit word single accesses only can be disabled to reduce power consumption	

5.3.2 Processor (HASH)

The STM32H503 devices implement a new feature compared to the STM32F401, STM32F410, and STM32F411 devices, which is the hash processor (HASH), refer to the Hash processor section of the product reference manual.

5.4 Communication peripherals

Compared to STM32F401/410/411 devices, the STM32H503 has the possibility to operate communication interfaces (mapped on PA8, PA9, PA15, and PB[3:8]), with dedicated VDDIO2 (typical 1.2V). This feature is only available in WLCSP25 package.

5.4.1 Serial peripheral interface (SPI)

The following table illustrates the differences between SPI features in STM32F401, STM32F410, STM32F411, and STM32H503.

Table 21. SPI features

SPI	STM32F401, STM32F410, and STM32F411(1)	STM32H503(1)
Instances	x4 SPIs (for STM32F401 line) x3 SPIs (for STM32F410 line) x5 SPIs (for STM32F411 line)	3x SPIs
Features	SPI + I2S	
	Including 2 muxed with full-duplex (for STM32F401/411 lines)	Including 3 muxed with full-duplex I2S
Full-duplex synchronous transfer on three lines	X	X
Half-duplex	X	X
Simplex synchronous transfer on two lines	With or without a bidirectional data line (for STM32F401/411 lines)	With unidirectional data line

SPI	STM32F401, STM32F410, and STM32F411(1)	STM32H503(1)
	With unidirectional data line for STM32F410 line)	
Data size	8- or 16-bit transfer frame format selection	From 4-bit up to 32-bit data size selection or fixed to multiply of 8-bit
Multimaster mode capability	X	X
Baudrate prescalers	8 master mode baud rate prescalers (fPCLK/2 max.)	Baud rate prescaler up to kernel frequency/2 or bypass from RCC in master mode
Protection of configuration and settings	NA	X
Slave select (SS) management	NSS management by hardware or software for both master and slave: dynamic change of master/slave operations	Hardware or software management of SS for both master and slave
Configurable SS signal polarity and timing	NA	Configurable SS signal polarity and timing, MISO x MOSI swap capability
Programmable transaction data	NA	Programmable number of data within a transaction to control SS and CRC
Programmable data order with MSB-first or LSB-first Shifting	X	X
Programmable clock polarity and phase	X	X
Dedicated transmission and reception flags with interrupt capability	X	X
SPI Motorola and TI formats Support	X	X
Hardware CRC feature for reliable communication: • CRC value can be transmitted as the last byte in Tx mode • Automatic CRC error checking for last received byte	X	X
Interrupt events and error detection with interrupt capability	Interrupts: • For the STM32F401/F411 lines: – Transmit buffer empty flag – Receive buffer not empty flag – Master mode fault event – Overrun error – CRC error flag – TI frame format error • For the STM32F410 line: – Transmit Tx buffer ready to be loaded – Data received in Rx buffer – Master mode fault – Overrun error – TI frame format error	Interrupts: • TxFIFO ready to be loaded • Data received in RxFIFO • Both TXP and RXP active • Transmission transfer filled • Overrun error • Underrun error • TI frame format error • CRC error • Mode fault • End of transfer • Master mode suspended • TxFIFO transmission complete All the interrupt events are capable to wakeup the system from sleep mode at each instance.
Configurable behavior at slave underrun condition	NA	X (support of cascaded circular buffers)

SPI	STM32F401, STM32F410, and STM32F411(1)	STM32H503(1)
FIFOs	NA	• Two multiply of 8-bit embedded Rx and Tx FIFOs (FIFO size depends on instance) • Configurable FIFO thresholds (data packing)
RDY status pin	NA	Optional status pin RDY signalizing the slave device ready to handle the data flow

1. *X = available, and NA = not available.*

5.4.2 Inter-integrated circuit (I2C)

The STM32H503 devices implement the same I2C features than the STM32F401, STM32F410, and STM32F411 devices but with some enhancements. The main differences are stated in the table below.

Table 22. I2C differences

I2C	STM32F401, STM32F410, and STM32F411	STM32H503
Instances	• x3 (I2C1, I2C2, I2C3) for the STM32F401/411 lines • x3 (I2C1, I2C2, I2C4) for the STM32F410 line	• x2 (I2C1 and I2C2)
Features	• SMBus/PMBus • Standard mode (up to 100 kbit/s) • Fast mode (up to 400 kbit/s)	
	• Fast mode plus (up to 1 MHz) (for STM32F410 line)	• Fast mode plus (up to 1 MHz) I2C bus.
	• Wakeup from stop mode (for STM32F410 line)	• Wakeup from stop mode only (no autonomous mode)
	NA	• Independent clock

5.4.3 Improved inter-integrated circuit (I3C)

The STM32H503 devices implement a new feature compared to the STM32F401, STM32F410, and STM32F411 devices, which is the I3C peripherals.

5.4.4 Universal synchronous/asynchronous receiver transmitter (USART/LPUART)

The STM32H503 devices implement several new features on the USART compared to the STM32F401, STM32F410, and STM32F411 devices. The following table shows the USART differences.

Table 23. USART features

USART	STM32F401, STM32F410, and STM32F411	STM32H503
Instances	3 x USART	• 3 USARTs • LPUART
Baud rate	• Up to 2 x 10.5 Mbit/s + 1 x 5.25 Mbit/s (STM32F401 line) • Up to 2 x 12.5 Mbit/s + 1 x 6.25 Mbit/s (STM32F410/411 lines)	Depends on the frequency (oversampling by 16 or by 8)(1)
Clock	• Single clock domain	Dual clock domain and wakeup from low-power mode.
Data	• Word length: programmable (8 or 9 bits)	• Word length: programmable (7, 8 or 9 bits) • Programmable data order with MSB-first or LSB-first shifting
Interrupt	• 10 interrupt sources with flags	• 23 interrupt sources with flags
Others features	• Hardware flow control (CTS/RTS)	• RS232 hardware flow control • RS485 hardware control mode

USART	STM32F401, STM32F410, and STM32F411	STM32H503
Others features	• LIN mode • IrDA SIR encoder block • Continuous communication using DMA • Multiprocessor communications • Single-wire half-duplex communication	
	NA	• Modbus communication: Timeout feature, CR/LF character recognition • Two internal FIFOs for transmit and receive data. • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable Tx/Rx pin configuration • Wakeup from stop mode
	• Smartcard mode T = 0 and T = 1 is to be implemented by the software • Number of stop bits: 0.5, 1, 1.5, and 2	• Smartcard mode: Support the T=0 and T=1 asynchronous protocols. • Number of stop bits: 0.5, 1, 1.5, and 2

1. *Refer to the USART section in the reference manual.*

5.4.5 FD controller area network (FDCAN)

The STM32H503 devices implement a new feature compared to the STM32F401, STM32F410, and STM32F411 devices, which is the FD controller area network (FDCAN).

5.4.6 Universal serial-bus interface (USB)

The STM32F401, STM32F411, and STM32H503 devices have different USB peripherals.

Most features supported by the STM32F401 and STM32F411 devices are also supported by the STM32H503 devices.

Note: Universal serial-bus interface is not supported by STM32F410.

The main USB differences between the STM32F401, STM32F411, and STM32H503 devices are listed in the table below.

Table 24. USB differences

USB	STM32F401 and STM32F411	STM32H503
General	Full support for the USB on-the-go (USB OTG_FS)	USB with clock recovery
	FS mode: • 1 bidirectional control endpoint • 3 IN endpoints (bulk, interrupt, isochronous) • 3 OUT endpoints (bulk, interrupt, isochronous	Up to 8 bidirectional endpoints
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D + (USB_DP) line	USB connect / disconnect capability (controllable embedded pull-up resistor on USB_DP line)
	NA	Battery charging detection (BCD) support for the device
Buffer memory	• 1.25 Kbytes data FIFOs • Management of up to 4 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO	2048 bytes of dedicated packet buffer memory SRAM
Low-power modes	• USB suspends and resumes	USB revision 2.0 including link power management support

5.5 Analog peripherals

5.5.1 Analog-to-digital converter (ADC)

Table 25 details the differences between the ADC peripherals of the STM32F401, STM32F410, and STM32F411 lines compared to the STM32H503 devices.

Table 25. ADC differences between devices

ADC	STM32F401, STM32F410, and STM32F411	STM32H503
Instances	x1	x1
Resolution	12-bit	
Number of channels	Up to 16 channels	Up to 16 channels
Configurable resolution	12-bit, 10-bit, 8-bit, or 6-bit	
Maximum sampling speed	2.4 MSPS	2.5 MSPS
Conversion Modes	• Single • Continuous • Scan • Discontinuous	
DMA support	Yes	
Data register	16-bit data register	
Analog watchdog feature	This feature allows the application to detect if the input voltage goes outside the user-defined high or low threshold	
ADC input range:	VREF– ≤ VIN ≤ VREF+	VSSA ≤ VIN ≤ VREF+
New features	NA	• ADC conversion time independent from the AHB bus clock frequency • Manage single-ended or differential inputs • Low-power features • Three analog watchdogs per ADC • Self-calibration oversampling ratio adjustable from 2 to 256 • Programmable data shift up to 8 bits

5.5.2 Digital-to-analog converter (DAC)

The STM32H503 devices implement some enhanced DAC compared to the STM32F410 devices. Refer to the table below for the main DAC differences between them.

Table 26. DAC differences between devices

DAC	STM32F410	STM32H503
Instances	x1	x1 maximum two output channels
Resolution	12 bits	
Output buffer	Yes	
New features	NA	• Double-data DMA • Dual DAC channel for independent or simultaneous conversions • Buffer offset calibration • Sample and hold mode for low power operation in stop mode

5.5.3 Operational amplifier (OPAMP)

The STM32H503 devices embed one operational amplifier with two inputs and one output. The three I/Os can be connected to the external pins, thus enabling any type of external interconnections.

The OPAMP can be configured internally as a follower or as an amplifier with a non-inverting gain ranging from 2 to 16 or as an amplifier with inverting gain ranging from -1 to -15.

5.5.4 Comparator (COMP)

The STM32H503 device embeds an ultra-low-power comparator.

It can be used for a variety of functions including:

- Wake-up from low-power mode triggered by an analog signal
- Analog signal conditioning
- Cycle-by-cycle current control loop when combined with a PWM output from a timer

5.6 Timer peripherals

The STM32F410 devices include one advanced-control timer, up to three general-purpose timers, one basic timer, one low-power timer, two watchdog timers and one SysTick timer.

The STM32F401 and STM32F411 devices include one advanced-control timer, up to seven general-purpose timers, two watchdog timers and one SysTick timer. Furthermore, the STM32H503 devices include one advanced-control timer, two general-purpose timers, two basic timers, two low-power timers, two watchdog timers and one SysTick timer.

This section compares the features of the above listed timers and RTC in STM32H503, STM32F401, STM32F410, and STM32F411 devices.

5.6.1 Advanced-control timers (TIM1)

The STM32H503, STM32F401, STM32F410, and STM32F411 include one advanced-control timer TIM1, with almost identical features detailed in the table below.

Table 27. Advanced-control timer (TIM1) features

Feature	STM32F401, STM32F410, and STM32F411	STM32H503
Counter resolution and type	16-bit up, down, up/down auto-reload counter	
Prescaler factor	16-bit programmable prescaler allowing dividing (also “on the fly”) the counter clock frequency either by any factor between 1 and 65536	
Channels	Up to 4 independent channels for: • Input capture • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output	Up to 6 independent channels for: • Input capture (but channels 5 and 6) • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output
Complementary outputs	Complementary outputs with programmable dead-time	
Synchronization with external Signals and general-purpose Timers	Synchronization circuit to control the timer with external signals and to interconnect several timers together The advanced-control (TIM1) and general-purpose timers are completely independent, and do not share any resources	
Repetition counter	Repetition counter to update the timer registers only after a given number of cycles of the counter	
Break inputs	Break input to put the timer’s output signals in reset state or in a known state	
Interrupt/DMA generation	Interrupt/DMA generation on the following events	

Feature	STM32F401, STM32F410, and STM32F411	STM32H503
Interrupt/DMA generation	• Update: counter overflow/underflow, counter initialization (by software, or internal/external trigger) • Trigger event (counter start, stop, initialization, or count by internal/external trigger) • Input capture • Output compare • Break input	• Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization, or count by internal/external trigger) • Input capture • Output compare • Encoders and sensors Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes
Encoders and sensors	Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes	
Trigger input	Trigger input for external clock or cycle-by-cycle current management	
Application examples	Measuring the pulse lengths of input signals (input capture). Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)	

5.6.2 GP timers with up, down, and up-down auto-reload counter

The GP (general-purpose) timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler.

The STM32H503, STM32F401, STM32F410, and STM32F411 devices include GP timers with up, down or up-down auto-reload counter with identical features:

- For STM32H503: TIM2 and TIM3
- For STM32F401/F411: TIM2, TIM3, TIM4, and TIM5
- For STM32F410: TIM5

Table 28. GP timer features

Feature	STM32F410	STM32F401 and STM32F411	STM32H503
32-bit resolution	TIM5	TIM2 and TIM5	TIM2
16-bit resolution	NA	TIM3 and TIM4	TIM3
Counter resolution and type	32-bit up, down, up/down auto-reload counter	16-bit or 32-bit up, down, up/down auto-reload counter	
Prescaler factor	16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535		
Channels	Up to 4 independent channels for: • Input capture • Output compare • PWM generation (Edge- and center-aligned modes) • One-pulse mode output		
Synchronization with external Signals and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers		
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization, or count by internal/external trigger) • Input capture • Output compare		
Encoders and sensors	Supports incremental (quadrature) encoder and hall-sensor circuitry for positioning purposes		
Trigger input	Trigger input for external clock or cycle-by-cycle current management		

Feature	STM32F410	STM32F401 and STM32F411	STM32H503
Application examples	Measuring the pulse lengths of input signals (input capture) generating output waveforms (output compare and PWM)		

5.6.3 Basic timers (TIM6/7)

The basic timers consist in a 16-bit auto-reload counter driven by a programmable prescaler.

These timers are completely independent, and do not share any resources.

- For STM32H503: TIM6 and TIM7
- For STM32F410: TIM6

The basic timers are not available for STM32F401 and STM32F411 devices.

Table 29. Basic timer features of STM32H503 and STM32F410

Feature	STM32F410	STM32H503
TIMx	TIM6	TIM6 and TIM7
Counter resolution and type	16-bit auto-reload upcounter	
Prescaler factor	16-bit programmable prescaler used to divide (also “on the fly”) the counter clock frequency by any factor between 1 and 65535	
Synchronization signals	Synchronization circuit to trigger the DAC	
Interrupt/DMA generation	Interrupt/DMA generation on the update event: counter overflow	

5.6.4 Low-power timers (LPTIM)

The LPTIM is a 16-bit timer that benefits from the ultimate developments in power-consumption reduction. This feature is not available in STM32F401 and STM32F411.

Table 30 describes LPTIM features on STM32H503 and STM32F410 devices.

Table 30. LP timer (LPTIMx) features of STM32H503 and STM32F410 devices

Feature	STM32F410	STM32H503
LPTIMx	LPTIM1	LPTIM1 and LPTIM2
Counter resolution and type	16 bit upcounter	
Prescaler factor	3-bit prescaler with 8 possible dividing factors (1,2,4,8,16,32,64,128)	
Selectable clock	• Internal clock sources: configurable internal clock source (see RCC section) • External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)	
Auto-reload	16 bit ARR auto reload register	
Capture/compare	16 bit capture/compare register	
Continuous mode	Continuous/One-shot mode	
Trigger mode	Selectable software/hardware input trigger	
Glitch filter	Programmable digital glitch filter	
Configurable output	Configurable output: Pulse, PWM	
Polarity	Configurable I/O polarity	
Encoder mode	Yes	
Repetition counter	NA	Yes

Feature	STM32F410	STM32H503
Input capture, PWM and one-pulse channels	NA	• Up to 2 independent channels for: – Input capture – PWM generation (edge-aligned mode) – One-pulse mode output
DMA requests	NA	• DMA request generation on the following events: – Update event – Input capture

5.6.5 Watchdogs (WWDG/IWDG)

The STM32H503, STM32F401, STM32F410, and STM32F411 devices embed two watchdogs:

- a system window watchdog (WWDG) with the same features
- an independent watchdog (IWDG) with the main differences

Table 31. IDWG features

Feature	STM32F401, STM32F410, and STM32F411	STM32H503
Clock	clocked from an independent RC oscillator	Independent clock LSI used as IWDG kernel clock (iwdg_ker_ck)
Window OPTION	NA	X
Early wakeup interrupt generation	NA	X
Reset generation	X	

5.6.6 Real-time clock (RTC)

The below table describes the difference of RTC features between STM32F401, STM32F410, STM32F411, and STM32H503 devices. For more information about RTC, refer to the RTC section of the product reference manual.

Table 32. RTC features

RTC	STM32F401, STM32F410, and STM32F411	STM32H503
Feature	Calendar with subsecond, seconds, minutes, hours (12 or 24 format), weekday, date, month, year	
	Two programmable alarms	
	Reference clock detection: a more precise second source clock (50 or 60 Hz) can be used to enhance the calendar precision	
	Timestamp function	
	Daylight saving time	
	Automatic wakeup	
	Digital calibration circuit with 0.95 ppm resolution	
	• Alarm A, alarm B, wakeup interrupt, timestamp, and tamper detection	• Alarm A, alarm B, wakeup timer, and timestamp individual privilege protection
	NA	• Binary mode with 32-bit free-running counter. • On-the-fly correction from 1 to 32767 RTC clock pulses
Tamper and backup registers	• 20 32-bit backup registers	• 32 32-bit backup registers • 2 tamper pins

RTC	STM32F401, STM32F410, and STM32F411	STM32H503
	• Tamper detection input: – One for STM31F401/411 lines – Two for STM32F410 line • Edge or level detection with configurable filtering	• 13 internal tamper events

5.6.7 SysTick timer

The SysTick timer is dedicated to real-time operating systems but can also be used as a standard down-counter.

The STM32H503 embeds a Cortex-M33 with one SysTick timer.

The STM32F401, STM32F410, and STM32F411 embed a Cortex-M4 with one SysTick timer.

6 Conclusion

This application note is a complement to the STM32F401, STM32F410, STM32F411, and STM32H503 datasheets and reference manuals.

This document provides a simple guideline to migrate an existing product based on the STM32F401, STM32F410, STM32F411 devices to the STM32H503 devices.

Revision history

Table 33. **Document revision history**

Date	Version	Changes
02-Mar-2023	1	Initial release.

Contents

List of tables

List of figures

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