life.augmented

AN5938

Application note

Getting started with STM32U0 MCUs hardware development

Introduction

This application note is intended for system designers who require a hardware implementation overview of the development board features: power supply, clock management, reset control, boot mode settings, and debug management.

It details how to use the STM32U0 microcontrollers, named STM32U0, and describes the minimum hardware resources required to develop an application using these MCUs.

This document also includes detailed reference design schematics with the description of the main components, interfaces, and modes.

1 General information

This document applies to the STM32U0 Arm® Cortex®-M0+-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

Reference documents

[1] Reference manual *STM32U0 Arm®-based 32-bit MCUs* (RM0503)

[2] Application note *STM32 microcontroller system memory boot mode* (AN2606)

[3] Application note *Oscillator design guide for STM8AF/AL/S and STM32 microcontrollers* (AN2867)

2 Power supply management

2.1 Power supplies

The STM32U0 devices require a 1.71 to 3.6 V operating voltage supply (V_{DD}).

The independent supplies listed below can be provided for specific peripherals:

- **V_{DD}** = 1.71 V to 3.6 V
  V_{DD} is the external power supply for the I/Os, the internal regulator, and the system analog such as reset, power management, and internal clocks. V_{DD} is provided externally through the VDD pins.
- **V_{DDA}** = 1.62 V (ADC/COMP)/1.80 V (DAC/OPAMP)/2.4 V (VREFBUF) to 3.6 V: external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers, and comparators. The V_{DDA} voltage level is independent from the V_{DD} voltage. The VDDA pin must preferably be connected to the V_{DD} voltage supply when these peripherals are not used.

Note: In case the VDDA pin is left at high-Z or is tied to VSS, the maximum input voltage that can be applied on the I/Os with "_a" I/O structure, is reduced (refer to the device datasheet for more details).

- **V_{DDUSB}** = 3.0 V to 3.6 V
  V_{DDUSB} is the external-independent power supply for USB transceivers. The V_{DDUSB} voltage level is independent from the V_{DD} voltage. The VDDUSB pin must preferably be connected to the V_{DD} voltage supply when the USB is not used.

Note: In case the VDDUSB pin is left at high-Z or is tied to VSS, the maximum input voltage that can be applied on the I/Os with "_u" I/O structure, is reduced (refer to the device datasheet for more details).

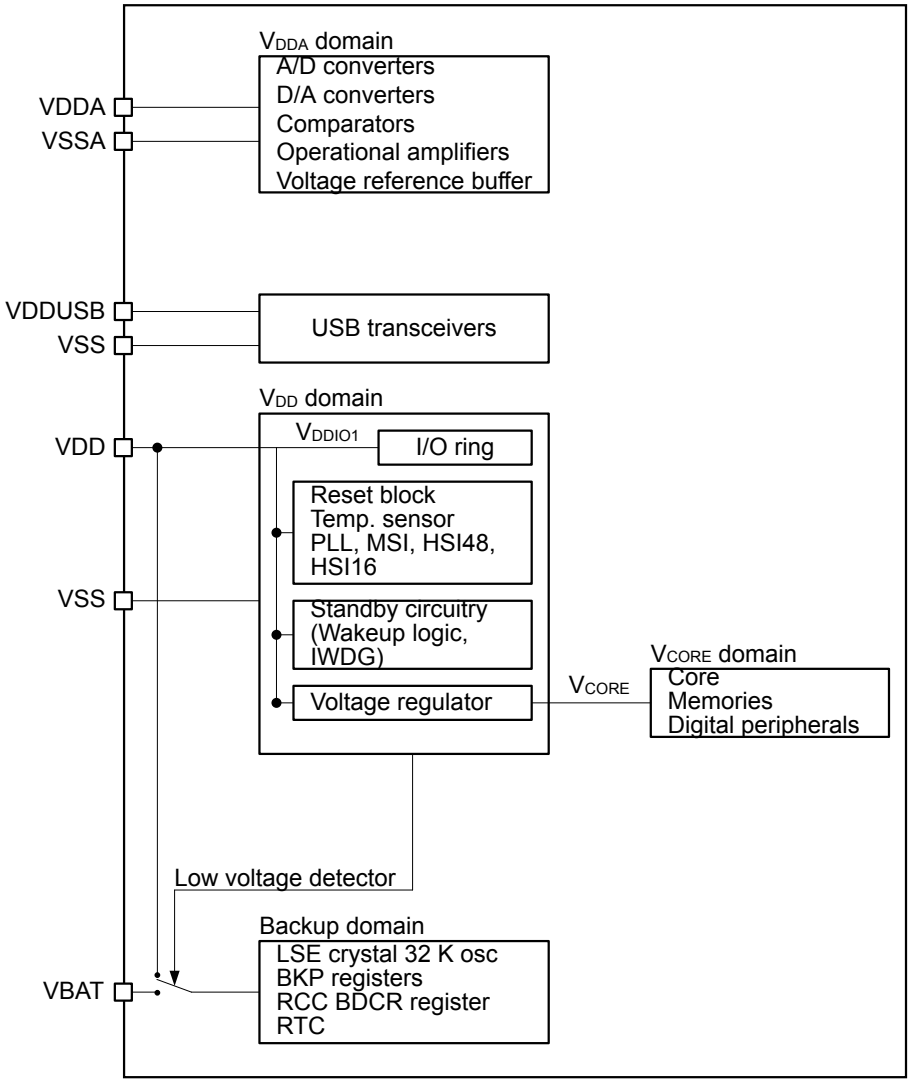
Note: On small packages, V_{DDA} or V_{DDUSB} independent power supplies may not be present as a dedicated pin, and are internally bonded to a VDD pin. They are neither present when the related features are not supported on the product.

- **V_{LCD}** = 2.5 V to 3.6 V
  The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter. VLCD is multiplexed with PC3 that can be used as GPIO when the LCD is not used.
- **V_{BAT}** = 1.55 V to 3.6 V
  The power supply is V_{BAT} when V_{DD} is not present (through power switch) for RTC, TAMP, external clock 32 kHz oscillator, backup registers, and optionally backup SRAM.
- **V_{REF-}**, **V_{REF+}**
  V_{REF+} is the analog peripheral input reference voltage, or the output of the internal voltage reference buffer (when enabled). When V_{DDA} < 2 V, V_{REF+} must be equal to V_{DDA}. When V_{DDA} ≥ 2 V, V_{REF+} must be between 2 V and V_{DDA}. It can be grounded when the analog peripherals using V_{REF+} are not active. The internal voltage reference buffer supports two output voltages, which is configured with the VRS bit of the VREFBUF_CSR register:
  – V_{REF+} around 2.048 V (requiring V_{DDA} equal to or higher than 2.4 V)
  – V_{REF+} around 2.5 V (requiring V_{DDA} equal to or higher than 2.8 V)

  VREF- and VREF+ pins are not available on all packages. When not available, they are bonded to VSSA and VDDA pins, respectively.
  When the V_{REF+} pin is double-bonded to V_{DDA} in a package, the internal VREFBUF is not available, and must be kept disabled.
  V_{REF-} must always be equal to V_{SSA}.

Figure 1 presents an overview of the STM32U0 devices power supply.

Figure 1. **STM32U0 series power supply overview**



DT71259V2

The V_{DD} supply source feeds the I/Os and system analog peripherals (such as PLLs and reset block). The V_{CORE} power supply for digital peripherals and memories is generated from the LDO.

2.1.1 Independent analog peripherals supply

To improve ADC and DAC conversion accuracy and to extend the supply flexibility, the analog peripherals have an independent power supply that can be separately filtered and shielded from noise on the PCB.

The voltage supply input of the analog peripherals is available on a separate V_{DDA} pin. An isolated supply ground connection is provided on V_{SSA} pin.

The V_{DDA} supply voltage can be different from V_{DD}.

The V_{DDA} supply can be monitored by analog voltage monitors (AVM), and compared with two thresholds (1.6 V for AVM1 or 1.8 V for AVM2). For more details, refer to the device datasheet and section *Peripheral voltage monitoring (PVM)* of document [1].

When a single supply is used, the V_{DDA} pin can be externally connected to the same V_{DD} supply, through an external filtering circuit, to ensure a noise-free V_{DD} reference voltage.

ADC and DAC reference voltage

To ensure a better accuracy on low-voltage inputs and outputs, the user can connect to V_{REF+} pin, a separate reference voltage lower than V_{DDA}.

V_{REF+} is the highest voltage, represented by the full-scale value, for an analog input (ADC) or output (DAC) signal. V_{REF+} can be provided either by an external reference or by the VREFBUF that can output a configurable voltage: 2.048 or 2.5 V. The VREFBUF can also provide the voltage to external components through the V_{REF+} pin. This available on some packages.

For further information, refer to the device datasheet and section *Voltage reference buffer (VREFBUF)* of document [1].

2.1.2 Independent USB transceiver supply

The USB transceivers are supplied from a separate V_{DDUSB} power supply. The V_{DDUSB} range is from 3.0 V to 3.6 V and is completely independent from V_{DD} or V_{DDA}.

After reset, the USB features supplied by V_{DDUSB} are logically and electrically isolated, and are therefore not available. The isolation must be removed before using the USB peripheral, by setting the USV bit in PWR_CR2, once the V_{DDUSB} supply is present.

The USB voltage monitoring (UVM) monitors the V_{DDUSB} supply. It also compares the internal reference voltage (V_{REFINT}, around 1.2 V). For more details, refer to the device datasheet and section Peripheral voltage monitoring (PVM) of document [1].

2.1.3 Independent LCD supply

The VLCD pin is provided to control the contrast of the glass LCD. This pin can be used in two ways:

- It can receive from an external circuitry the desired maximum voltage that is provided on segment and common lines to the glass LCD by the microcontroller.
- It can also be used to connect an external capacitor that is used by the microcontroller for its voltage step-up converter. This step-up converter is controlled by software to provide the desired voltage to segment and common lines of the glass LCD.

The voltage provided to segment and common lines defines the contrast of the glass LCD pixels. This contrast can be reduced when the user configures the dead between frames.

- When an external power supply is provided to the VLCD pin, it should range from 2.5 V to 3.6 V. It does not depend on V_{DD}.
- When the LCD is based on the internal step-up converter, the VLCD pin should be connected to a capacitor (see the product datasheet for further information).

Note: The independent LCD supply is available only with STM32U0x3 devices.

2.1.4 Battery backup domain

To retain the content of the backup registers and supply the RTC when V_{DD} is turned off, the VBAT pin can be connected to an optional backup voltage, supplied by a battery or by another source.

The VBAT pin powers RTC, TAMP, LSE oscillator, and PC13 to PC15 I/Os. That allows the RTC to operate even when the main power supply is turned off.

The backup SRAM is optionally powered through the VBAT pin, when the BREN bit is set in PWR_BDCR1.

The switch to the V_{BAT} supply is controlled by the power-down reset embedded in the reset block.

Caution:

- During $t_{RSTTEMPO}$ (at V_{DD} startup) or after a PDR (power-down reset) detection, the power switch between V_{BAT} and V_{DD} remains connected to the VBAT pin.
- During the startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ (refer to the datasheet for $t_{RSTTEMPO}$ value), and $V_{DD} > V_{BAT} + 0.6$ V, a current may be injected into the VBAT pin through an internal diode connected between the VDD pin and the power switch (V_{BAT}). If the power supply/battery connected to the VBAT pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the VBAT pin.
- It is not advisable to have a charged battery assembled on board during the reflow process. The presence of the battery on board can cause biasing of the MCU when the temperature exceeds the AMR during the reflow soldering process.

If no external battery is used in the application, it is recommended to connect the VBAT pin externally to V_{DD} with a 100 nF external ceramic decoupling capacitor.

When the backup domain is supplied by V_{DD} (analog switch connected to the VDD pin), the following pins are available:

- PC13, PC14, and PC15 that can be used as GPIO pins
- PC13, PC14, and PC15 that can be configured by RTC or LSE (refer to the RTC section of document [1])
- Pins listed below, that are configured by TAMP as tamper pins:
  - PA0 (TAMP_IN2/TAMP_OUT1)
  - PC13 (TAMP_IN1/TAMP_OUT2)
  - PA1 (TAMP_IN5/TAMP_OUT4)
  - PC5 (TAMP_IN4/TAMP_OUT5)
  - PB15 (TAMP_IN3/TAMP_OUT6)

Note:

- *Because the power switch can transfer only a limited amount of current (3 mA), the use of PC13 to PC15 I/Os in output mode is restricted: the speed must be limited to 2 MHz with a maximum load of 30 pF. These I/Os must not be used as current source (for example to drive an LED).*
- *Under V_{DD}, TAMP_OUTx pins (PA0, PA1, PC5) keep the same speed features as the GPIOs to which they are connected. However, under V_{BAT}, the speed of TAMP_OUTx pins must be limited to 500 kHz.*
- *The speed of the PC13 pin is always limited to 2 MHz, under V_{DD} or under V_{BAT}.*

Backup domain access

After a system reset, the backup domain (RCC_BDCR, PWR_CR1, RTC, TAMP and backup registers, plus backup SRAM) is protected against possible unwanted write accesses. To enable access to the backup domain, proceed as follows:

1. Enable the power interface clock by setting the PWREN bit RCC_APBENR1.
2. Set the DBP bit in PWR_CR1 to enable access to the backup domain.

2.1.5 Voltage regulator

The STM32U0 devices embed two internal linear voltage regulators in parallel to provide the V_{CORE} supply for digital peripherals, SRAMs, and the embedded flash memory, except for the Standby circuitry. The main regulator output voltage (V_{CORE}) can be programmed by software to two different power ranges (range 1 and range 2) in order to optimize the consumption depending on the system maximum operating frequency. It can be selected when the application runs, depending on immediate application requirements. Refer to the reference manual [1] sections: *Clock source frequency versus voltage scaling* and *Read access latency*.

Dynamic voltage scaling management

The LDO regulator can provide a different voltage (voltage scaling) and can operate in all Stop modes. This regulator also can operate in the following ranges:

- **Range 1 (1.2 V, 56 MHz)**, high performance: provides a typical output voltage at 1.2 V. It is used when the system clock frequency is up to 56 MHz.
- **Range 2 (1.0 V, 16 MHz)**, low power: provides a typical output voltage at 1.0 V. It is used when the system clock frequency is up to 16 MHz when running from MSI, or up to 18 MHz when running from PLL or HSE.

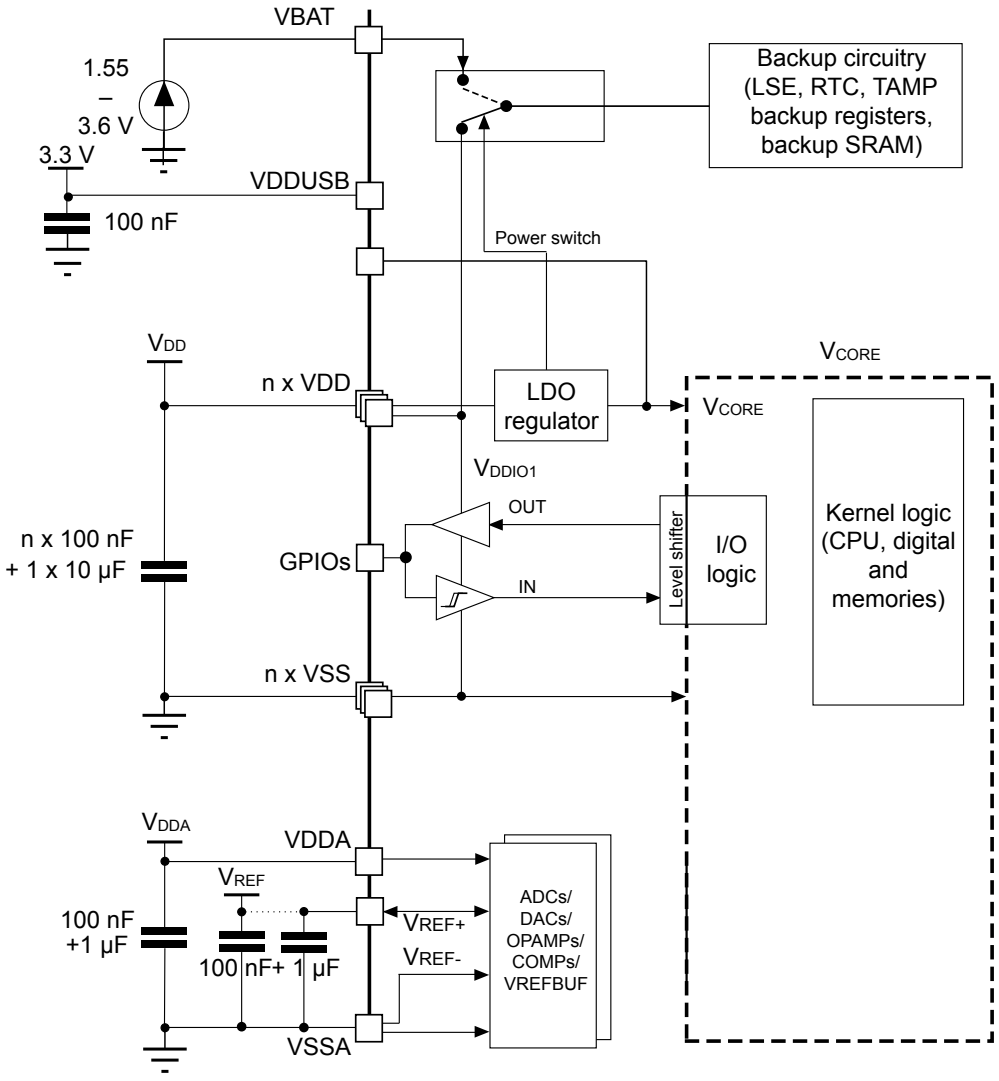
The voltage scaling is selected through the VOS bit in PWR_VOSR.

2.2 Power supply schemes

The device is powered by a stabilized V_{DD} power supply as described below:

- The **VDD pins** must be connected to V_{DD} with external decoupling capacitors: a 10 µF (typical value, 4.7 µF minimum) single tantalum or ceramic capacitor for the package, and a 100 nF ceramic capacitor for each V_{DD} pin.
- The **VDDA pin** must be connected to two external decoupling capacitors: 100 nF ceramic and 1 µF tantalum or ceramic.
  Additional precautions can be taken to filter digital noise: V_{DDA} can be connected to V_{DD} through a ferrite bead.
- The **VREF+ pin** can be provided by an external voltage reference. In this case, an external 100 nF + 1 µF tantalum or ceramic capacitor must be connected on this pin.
  It can also be provided internally by the VREFBUF. In this case, an external 1 µF (typical) capacitor must be connected on this pin.
- The **VLCD pin** can be provided by an external voltage reference in which case an external capacitor of 100 nF and a 1 µF capacitor must be connected on this pin.
  It can also be provided internally by the step-up converter in which case an external capacitor of 1 µF (typical) must be connected on this pin.
- The **VBAT pin** can be connected to an external battery to preserve the content of the Backup domain:
  - When V_{DD} is present, the external battery can be charged on V_{BAT} through a 5 kΩ or 1.5 kΩ internal resistor. In this case, the user can insert a capacitor according to the expected discharging time (1 µF is recommended).
  - If no external battery is used in the application, it is recommended to connect the VBAT pin to V_{DD} with a 100 nF external ceramic decoupling capacitor.
- The **VDDUSB pin** when present in a package can be connected to a ceramic capacitor of 100 nF.

Figure 2. Power supply scheme for STM32U0



2.3 Power supply sequence between V_{DDA}, V_{DDUSB}, and V_{DD}

2.3.1 Power supply isolation

The devices feature a powerful reset system that ensures the main power supply (V_{DD}) has reached a valid operating range before releasing the MCU reset.

This reset system is also in charge of isolating the independent power domains: V_{DDA}, V_{DDUSB} and V_{DD}. This reset system is supplied by V_{DD} and is not functional before V_{DD} reaches a minimal voltage (1 V in worse-case conditions).

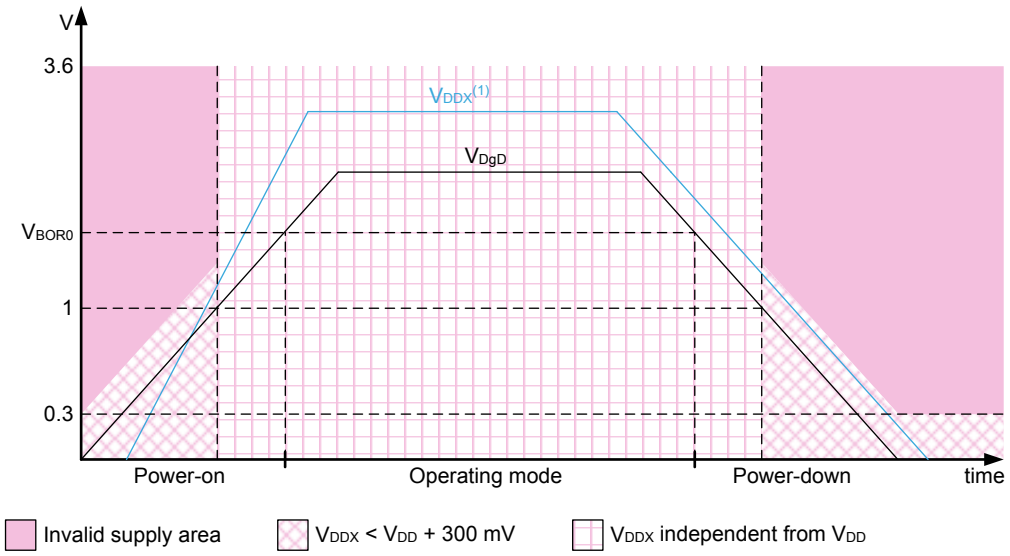
To avoid leakage currents between the available supplies and V_{DD} (or ground), V_{DD} must be provided first to the MCU, and then released with tolerance during power down (see Particular conditions during the power-down phase).

2.3.2 General requirements

During power-up and power-down phases, the following power sequence requirements must be respected:

- When V_{DD} is below 1 V, other power supplies (V_{DDA} and V_{DDUSB}) must remain below V_{DD} + 300 mV.
- When V_{DD} is above 1 V, all power supplies are independent.

Figure 3. **Power-up/power-down sequence**



DT71661V1

(1) V_{DDX} refers to any power supply among V_{DDA} and V_{DDUSB}.

Note: V_{BAT} is an independent supply and has no constraint versus V_{DD}. All power supply rails can be tied together.

2.3.3 Particular conditions during the power-down phase

During the power-down phase, V_{DD} can temporarily become lower than other supplies only if the energy provided to the MCU remains below 1 mJ. This allows external decoupling capacitors to be discharged with different time constants during the power-down transient phase (see Figure 3).

V_{DDX} (V_{DDA} or V_{DDUSB}) power rails must be switched off before V_{DD}.

Note: During the power-down transient phase, V_{DDX} can remain temporarily above V_{DD} (see Figure 3).

Example: computation of the energy provided to the MCU during the power-down phase

If the sum of decoupling capacitors on V_{DDX} is 10 µF and V_{DD} drops below 1 V while V_{DDX} is still at 3.3 V, the energy remaining in the decoupling capacitors is:

$$E = \frac{1}{2} C \times V^2 = \frac{1}{2} \times 10^{-5} \times 3.3^2 = 0.05\, mJ$$

The energy remaining in the decoupling capacitors is below 1 mJ, so it is acceptable for the MCU to absorb it.

2.4 Reset and power-supply supervisor

2.4.1 Brownout reset (BOR)

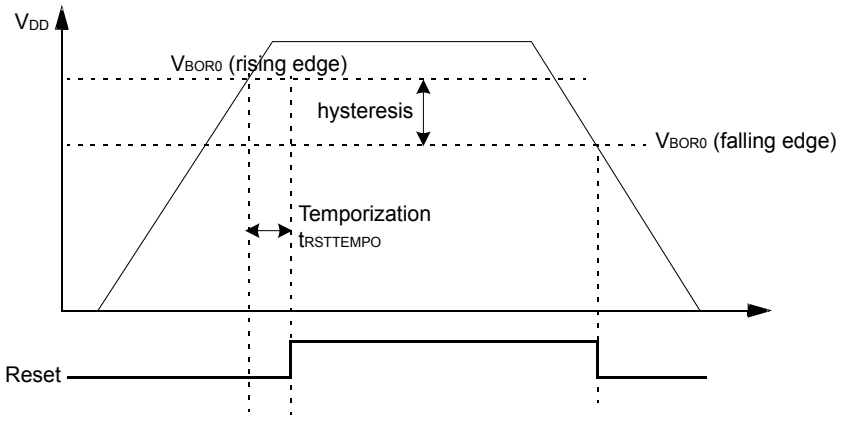
The devices have a brownout reset (BOR) circuitry. The BOR is active in all power modes except Shutdown mode, and cannot be disabled. The BOR monitors the backup domain supply voltage that is V_{DD} when present, V_{BAT} otherwise.

Five BOR thresholds can be selected through option bytes.

During power-on, the BOR keeps the device under reset until the supply voltage V_{DD} reaches the specified V_{BORx} threshold. When V_{DD} drops below the selected threshold, a device reset is generated. When V_{DD} is above the V_{BORx} upper limit, the device reset is released, and the system can start.

For more details on the brownout reset thresholds, refer to the electrical characteristics section in the datasheet.

Figure 4. Brownout reset waveform



Note: The reset temporization $t_{RSTTEMPO}$ is present only for the BOR lowest threshold (V_{BOR0}).

2.4.2 System reset

A system reset sets all registers to their reset values except the reset flags in RCC_CSR and the registers in the backup domain.

A system reset is generated when one of the following events occurs (refer to document for more details):

- a low level on the NRST pin (external reset)
- a window watchdog event (WWDG reset)
- an independent watchdog event (IWDG reset)
- System reset
- a software reset
- a low-power mode security reset
- an option-byte loader reset
- a brownout reset

These sources act on the NRST pin that is always kept low during the delay phase. The reset service routine vector is selected via the boot option bytes.

The system reset signal provided to the device is output on the NRST pin. The pulse generator guarantees a minimum reset pulse duration of 20 µs for each internal reset source. In case of an external reset, the reset pulse is generated while the NRST pin is asserted low.

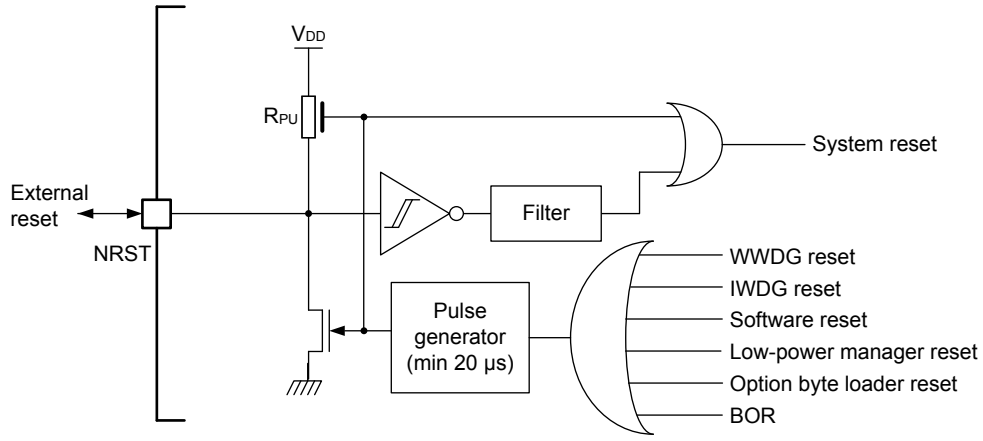
In case of an internal reset, the internal pull-up RPU is deactivated in order to save the power consumption through the pull-up resistor.

NRST pin

For STM32U0, NRST pin is shared with GPIO. Selection is available through device option bytes. User could select legacy behavior, input only mode or GPIO mode.

As this configuration is loaded from option bytes after each power on, external circuitry must let NRST pin cross VIH level after power on or exit from deep low power modes.

Figure 5. **Simplified diagram of the reset circuit**



2.4.3 Backup domain reset

A backup domain reset is generated when one of the following events occurs:

- a software reset, triggered by setting the BDRST bit in RCC_BDCR
- a V_{DD} or V_{BAT} power-on, if both supplies have previously been powered off

A backup domain reset only affects:

- LSE oscillator
- RTC
- TAMP
- Backup registers
- Backup SRAM
- RCC_BDCR
- PWR_CR1

3 Packages

3.1 Package summary

The package selection must consider the constraints that are strongly dependent upon the application.

The list below summarizes the most frequent ones:

- Number of interfaces required: Some interfaces may not be available on some packages. Some interfaces combinations may not be possible on some packages.
- PCB technology constrains: Small pitch and high-ball density may require more PCB layers and higher-class PCB.
- Package height
- PCB available area
- Noise emission or signal integrity of high-speed interfaces
- Smaller packages usually provide better signal integrity. This is further enhanced as small-pitch and high-ball density requires multilayer PCBs that allow better supply/ground distribution.
- Compatibility with other devices

Table 1. Package summary for STM32U0 devices

Package	Size (mm)	Pitch (mm)	Height (mm)
TSSOP20	6.5 × 4.4	0.65	1.2
UFQFN32	5 × 5	0.5	0.6
UFQFN48	7 × 7	0.5	0.6
LQFP48	7 × 7	0.5	1.6
LQFP64	10 × 10	0.5	1.6
LQFP80	12 × 12	0.5	1.6
WLCSP27	2.55 × 2.34	0.4	0.59
WLCSP42	2.82 × 2.93	0.4	0.59
UFBGA64	5 × 5	0.5	0.6
UFBGA81	5 × 5	0.5	0.6

3.2 Pinout summary

Table 2. Pinout summary for STM32U0 devices

Pin name	STM32U0xxxx														
	STM32U031xx							STM32U073/83xx							
	TSSOP20	LQFP48	LQFP64	UFQFPN32	UFQFPN48	UFBGA64	WLCSP27	LQFP48	LQFP64	LQFP80	UFQFPN32	UFQFPN48	UFBGA64	UFBGA81	WLCSP42
	Specific I/Os														
PC14-OSC32_IN	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PC15-OSC32_OUT	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PF0-OSC_IN	-	X	X	-	X	X	-	X	X	X	-	X	X	X	X
PF1-OSC_OUT	-	X	X	-	X	X	-	X	X	X	-	X	X	X	X
	System pins														
PF2-NRST	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PF3-BOOT0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
	Power pins														
VBAT	-	X	X	-	X	X	-	X	X	X	-	X	X	X	X
VDDUSB	-	-	-	-	-	-	-	X	X	X	-	X	X	X	X
VSSA(1)	-	o	o	-	o	o	-	o	o	o	-	o	o	o	o
VREF-(1)	-	o	o	-	o	o	-	o	o	o	-	o	o	o	o
VREF+(2)	o	o	o	o	o	o	o	o	o	X	-	o	o	-	o
VDDA(2)	o	o	o	o	o	o	o	o	o	X	-	o	o	X	o
Number of VDD	1	3	3	2	3	4	1	2	3	3	1	2	3	3	2
Number of VSS	1	3	3	2	3	4	1	3	4	4	2	3	4	4	3

1. *'o' means that VSSA and VREF- are internally connected and available on a single pin.*
2. *'o' means that VDDA and VREF+ are internally connected and available on a single pin.*

4 Clocks

The following clock sources can be used to drive the system clock (SYSCLK):

- HSI16: high-speed internal 16 MHz RC oscillator clock
- MSI: multispeed internal RC oscillator clock
- HSE: high-speed external crystal or clock, from 4 to 56 MHz
- PLL clock

The MSI is used as a system clock source after startup from reset. It is configured at 4 MHz.

The devices have the following additional clock sources:

- LSI: 32 kHz low-speed internal RC that drives the independent watchdog. It drives also optionally the RTC used for autowakeup from Stop mode and Standby mode.
- LSE: 32.768 kHz low-speed external crystal or clock that optionally drives the real-time clock (rtc_ck).
- HSI48: internal 56 MHz RC that potentially drives the USB and the RNG.

Each clock source can be switched on or off independently when it is not used in order to optimize power consumption.

Several prescalers can be used to configure the AHB and the APB frequencies domains with a maximum frequency of 56 MHz.

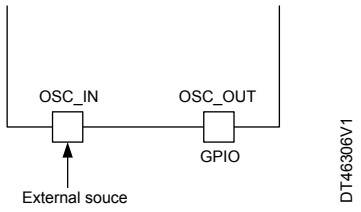
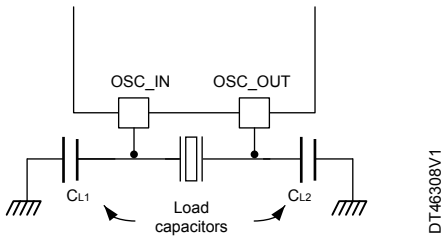
4.1 HSE clock

The high-speed external clock signal (HSE) can be generated from the following clock sources:

- HSE external crystal/ceramic resonator
- HSE user external clock that feeds OSC_IN pin

The resonator and the load capacitors must be placed as close as possible to the oscillator pins. It enables minimizing output distortion and startup stabilization time. The loading capacitance values must be adjusted according to the selected oscillator.

Table 3. HSE/LSE clock sources

Clock source	Hardware configuration
External clock	
Crystal/ceramic resonators	 CL1 and CL2 values depend on the quartz. Refer to document [3] for more details.

4.1.1 External crystal/ceramic resonator (HSE crystal)

The 4 to 56 MHz external oscillator has the advantage of producing a very accurate rate on the main clock. The associated hardware configuration is shown in Table 3. Refer to the electrical characteristics section of the datasheet for more details.

4.1.2 External source (HSE bypass)

In this mode, an external clock source must be provided with a frequency up to 56 MHz. The external clock signal (square, sinus, or triangle) with ~40 to 60 % duty cycle depending on the frequency (refer to the datasheet) must drive the OSC_IN pin, while the OSC_OUT pin can be used as a GPIO (see Table 3).

Note: For details on pin availability, refer to the pinout section of the datasheet. To minimize the consumption, the square signal is recommended.

4.2 HSI16 clock

The HSI16 clock signal is generated from an internal 16 MHz RC oscillator. The HSI16 RC oscillator provides a clock source at low cost. There are no external components. It also has a faster startup time than the HSE crystal oscillator. However, even with calibration, the frequency is less accurate than an external crystal oscillator or ceramic resonator.

The HSI16 clock can be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails.

For more details, refer to section *Clock security system (CSS)* in the document [1].

4.3 MSI clock

The MSI clock signal is generated from an internal RC oscillator. Its frequency range can be adjusted by software by using the MSIRANGE[3:0] bits in the clock control register (RCC_CR). Twelve frequency ranges are available: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz, and 56 MHz.

The MSI RC oscillator has the advantage of providing a low-cost (no external components) low-power clock source. In addition, when trimmed by the 32.768 kHz external oscillator (LSE), the MSI can provide the USB device with very accurate clock removing the need for an external high speed crystal (HSE).

Hardware auto calibration with LSE (PLL-mode)

When a 32.768 kHz crystal is present in the application, it is possible to configure the MSI in a PLL-mode by setting the MSIPLLEN bit in the clock control register (RCC_CR). When configured in PLL-mode, the MSI automatically calibrates itself thanks to the LSE. This mode is available for all MSI frequency ranges. At 56 MHz, the MSI in PLL-mode can be used for the USB OTG_FS device, saving the need of an external high-speed crystal.

For more details on how to calibrate the MSI frequency variation, refer to the reference manual [1] section *Internal/external clock measurement with TIM15/TIM16/TIM17*.

4.4 LSE clock

The LSE crystal is a 32.768 kHz low-speed external crystal or ceramic resonator (see Table 3). It provides a low-power but highly accurate clock source to the RTC (real-time clock) peripheral for clock/calendar or other timing functions.

The crystal oscillator driving strength can be changed at runtime using the LSEDRV[1:0] bits in RCC_BDCR. The goal is to obtain the best compromise between robustness and short startup time on one side, and low-power-consumption on the other side.

External source (LSE bypass)

In this mode, an external clock source must be provided, with a frequency up to 1 MHz. The external clock signal (square, sinus, or triangle) with ~50% duty cycle, must drive the OSC32_IN pin while the OSC32_OUT pin can be used as GPIO (see Table 3).

PLL clock

To achieve maximum performance of the product, system clock may go up to 56 MHz. In this case, PLL needs to be used, with one of the available clock sources - MSI, HSE or HSI16.

5 Boot configuration

5.1 Boot mode selection

At startup, a BOOT0 pin and nBOOT0 option bytes are used to select the boot memory address that includes:

- Boot from any address in user flash memory
- Boot from system memory (bootloader)
- Boot from any address in embedded SRAM

The BOOT0 value may come from the PF3-BOOT0 pin, or from an option bit depending on the value of a user option bit to free the GPIO pad if needed.

Table 4. Boot modes

Boot mode configuration					Selected boot area
BOOT_LOCK bit	nBOOT1 bit	BOOT0 pin	nBOOT_SEL bit	nBOOT0 bit	
0	X	0	0	X	Main flash memory
0	1	1	0	X	System memory
0	0	1	0	X	Embedded SRAM
0	X	X	1	1	Main flash memory
0	1	X	1	0	System memory
0	0	X	1	0	Embedded SRAM
0	X	X	X	X	Main flash memory forced

5.2 Embedded bootloader

The embedded bootloader is located in the system memory and programmed by STMicroelectronics during production. It is used to reprogram the flash memory by using the following serial interfaces:

- **USART**: USART1 on pins PA9/PA10, USART2 on pins PA2/PA3, USART3 on pins PC10/PC11
- **I2C**: I2C1 on pins PB6/PB7, I2C2 on pins PB10/PB11, I2C3 on pins PB3/PB4
- **SPI**: SPI1 on pins PA4/PA5/PA6/PA7, SPI2 on pins PB12/PB13/PB14/PB15
- **USB** in device mode through the DFU (device firmware upgrade) interface, on pins PA11/PA12

For further details on the STM32 bootloader, refer to document [2].

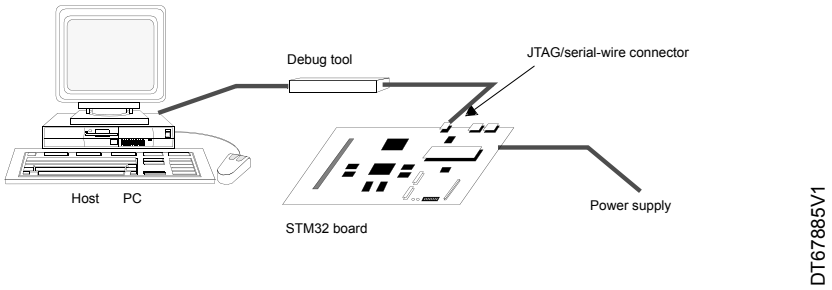
6 Debug management

The serial wire/JTAG debug port (SWJ-DP) is an Arm® standard CoreSight™ debug port.

The host/target interface is the hardware equipment that connects the host to the application board. This interface is made of three components: a hardware debug tool, a serial-wire connector, and a cable connecting the host to the debug tool.

Figure 1 shows the connection of the host to a development board.

Figure 6. Host-to-board connection



The Nucleo demonstration board embeds the debug tools (STLINK), so it can be directly connected to the computer through a USB cable.

6.1 SW-DP (serial-wire debug port)

The STM32U0 core integrates the serial wire debug port (SW-DP). It is an Arm® standard CoreSight™ debug port with a 2-pin (clock + data) interface to the debug access port.

Note: The software can configure all SWJ-DP port I/Os to other functions, but debugging is no longer possible.

6.2 Pinout and debug port pins

The devices are offered in various packages with different numbers of available pins. These provide debug capability on all of them.

6.3 Serial-wire debug (SWD) pin assignment

The same SWD pin assignment, detailed in Table 5, is available on all packages.

Table 5. SWD port pins

SWD pin	SWD port		Pin assignment
	Type	Debug assignment	
SWDIO	Input/Output	Serial-wire data input/output	PA13
SWCLK	Input	Serial-wire clock	PA14

After reset, the pins used for the SWD are assigned as dedicated pins that can be immediately used by the debugger host.

However, the MCU offers the possibility to disable the SWD, therefore releasing the associated pins for GPIO use.

For more details on how to disable SWD port, refer to section *I/O pin alternate function multiplexer and mapping* of the document [1].

6.3.1 Internal pull-up and pull-down on SWD pins

Once the user software releases the SWD I/O, the GPIO controller takes control of it. The reset states of the GPIO control registers put the I/Os in the equivalent states:

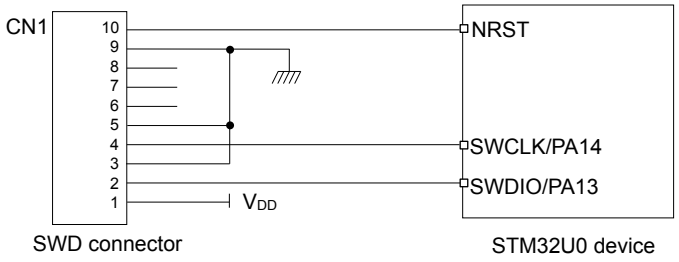
- SWDIO: alternate function pull-up
- SWCLK: alternate function pull-down

Having embedded pull-up and pull-down resistors removes the need to add external resistors.

6.3.2 SWD port connection with standard SWD connector

Figure 7 shows the connection between the device and a standard SWD connector.

Figure 7. SWD connector implementation



7 Recommendations

7.1 PCB (printed circuit board)

For technical reasons, it is best to use a multilayer PCB, with a separate layer dedicated to ground (V_{SS}) and another dedicated to the V_{DD} supply.

This provides a good decoupling and a good shielding effect. For many applications, economical reasons prohibit the use of this type of board. In this case, the major requirement is to ensure a good structure for ground and power supply.

7.2 Component position

A preliminary layout of the PCB must separate circuits into different blocks:

- high-current circuits
- low-voltage circuits
- digital component circuits
- circuits separated according to their EMI contribution, in order to reduce noise due to cross-coupling on the PCB

7.3 Ground and power supply

The following rules related to grounding must be respected:

- Ground every block (noisy, low-level sensitive, digital, or others) individually.
- Return all grounds to a single point.
- Avoid loops (or ensure they have a minimum area).

In order to improve analog performance, the user must use separate supply sources for V_{DD} and V_{DDA}, and place the decoupling capacitors as close as possible to the device.

The power supplies (V_{SS}, V_{DD}, V_{SSA}, V_{DDA}, or V_{DDUSB}) must be implemented close to the ground line to minimize the area of the supplies loop. This is because the supply loop acts as an antenna, and acts as the main transmitter and receiver of EMI. All component-free PCB areas must be filled with additional grounding to create a type of shielding, especially when using single-layer PCBs.

7.4 Decoupling

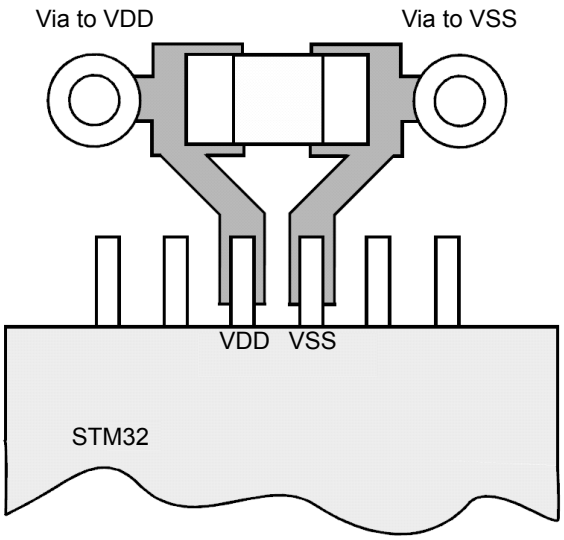
All power supply and ground pins must be properly connected to the power supplies. These connections (including pads, tracks, and vias) must have the lowest possible impedance. This is typically achieved with thick track widths and, preferably, the use of dedicated power supply planes in multilayer PCBs.

In addition, each power supply pair must be decoupled with filtering ceramic capacitors (100 nF) and a tantalum or ceramic capacitor of about 10 µF, connected in parallel on the device.

Some packages use a common VSS pin for several VDD pins, instead of a pair of power pins (one VSS for each VDD). In that case, the capacitors must be between each VDD pin and the common VSS pin. These capacitors must be placed as close as possible to, or below the appropriate pins on the underside of the PCB. Typical values are 10 to 100 nF, but exact values depend on the application needs.

Figure 1 shows the typical layout of such a VDD/VSS pin pair.

Figure 8. Typical layout for VDD/VSS pin pair



DT63912V1

7.5 Other signals

When designing an application, there are possible improvements for the EMC performance by closely studying the following:

- Signals for which a temporary disturbance affects the running process permanently. It is the case for interrupts and handshaking strobe signals but not the case for LED commands.
  For these signals, a surrounding ground trace, shorter lengths, and the absence of noisy and sensitive traces nearby (crosstalk effect) improve EMC performance.
  For digital signals, the best possible electrical margin must be reached for the two logical states. Slow Schmitt triggers are recommended to eliminate parasitic states.
- Noisy signals, such as clock, can be studied.
- Sensitive signals, such as high-Z, can be studied.

7.6 Unused I/Os and features

All microcontrollers are designed for a variety of applications and often a particular application does not use 100% of the MCU resources.

To increase the EMC performance and avoid extra power consumption, the unused features of the device must be disabled and disconnected from the clock tree, as follows:

- The unused clock source must be disabled.
- The unused I/O pins must not be left floating.
- The unused I/O pins must be configured as an analog input by software. They must also be connected to a fixed logic level 0 or 1 by an external or internal pull-up or pull-down, or configured as output mode using software.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
29-Feb-2024	1	Initial release.
18-Mar-2024	2	Updated: • Documentation classification to Public • Document title

Contents

List of tables

List of figures