SR5 E1 Line - Getting started with analog comparators

Introduction

SR5E1 microcontroller contains eight analogs comparators COMP1 to COMP8 controlled by two digital blocks.

They provide a binary output (0,1) which indicates if the analog voltage on the non-inverting input is larger than the voltage on the negative input.

The comparators can be used for a variety of functions including:

- Wake-up from CSleep mode triggered by an analog signal,
- Analog signal conditioning,
- Cycle-by-cycle current control loop when combined with a PWM output from a timer.

In this document are the described the use cases to show analog comparators main features:

1. Cycle-by-cycle current control
2. Frequency and pulse width measurement
3. Analog voltage monitoring
4. Preventing false overcurrent detections in motor control applications

The four application cases demonstrate the usefulness of analog comparators and show how they are integrated with other peripherals, for example, the digital-to-analog converter (DAC) and timers.

Note: This document is not intended to replace the analog comparator (COMP) section in the product reference manual.

All the values given in this document are for guidance only.

Refer to the related datasheet for guaranteed and up-to-date the performance and electrical values.

1 General information

This document applies to Arm® -based devices.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 Overview of analog comparators

2.1 SR5E1 comparator feature summary

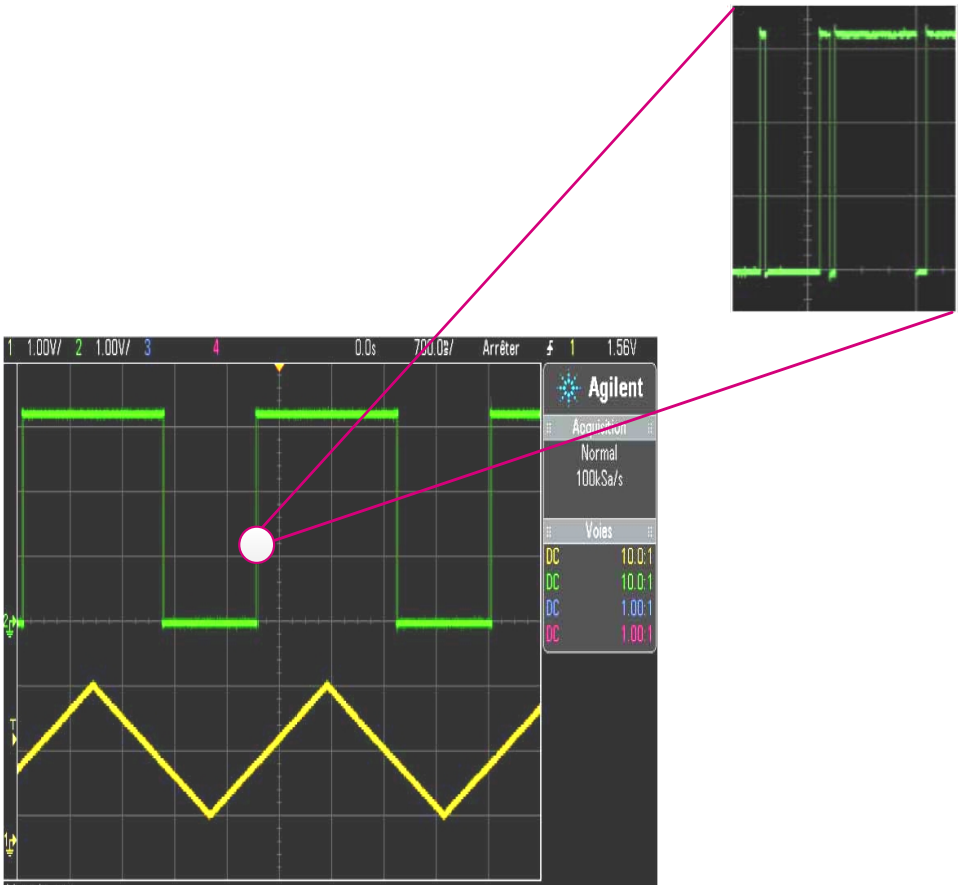
Table 1. SR5E1 comparator feature summary

Feature	SR5E1
Configurable non-inverting and inverting input	Yes
Programmable speed/consumption	No
Programmable hysteresis	Yes
Output redirection to I/Os and timer inputs for triggering break events for fast PWM shutdowns	Yes
Output blanking for immunity to switching noise	Yes
Window mode	No

2.2 Hysteresis

A comparator compares the inverting input with the non-inverting input and even small voltage fluctuations cause bounce on the comparator output. This bounce is not acceptable in many applications. The hysteresis functionality is non-symmetrical and only acts to falling edge of comparator output. The following figure shows the output bouncing when the input is noisy.

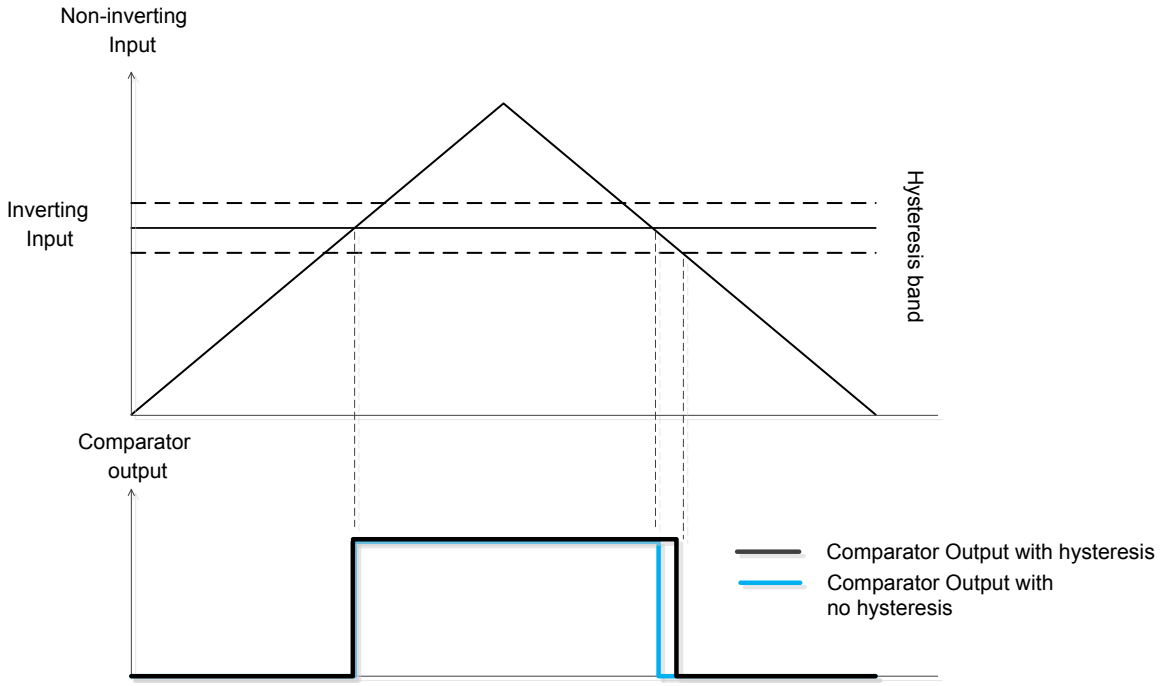
Figure 1. Effect of a noisy input on a comparator output



This bounce on the comparator output can be prevented by adding hysteresis into comparators. The analog comparators in SR5E1 devices have a configurable hysteresis value: No, 10 mV, 20 mV, 30 mV, 40 mV, 50 mV, 60 mV, 70 mV hysteresis values.

Caution: For hysteresis feature availability, refer to Section 2.1 SR5E1comparator feature summary.

Figure 2. Waveform of a comparator output with and without an hysteresis



3 Application examples

This section describes how the analog comparators embedded in the SR5E1 devices are used in applicative examples such as humidity measurement, cycle-by-cycle motor control, voltage monitoring, and PWM control.

3.1 Cycle-by-cycle current control (peak current control)

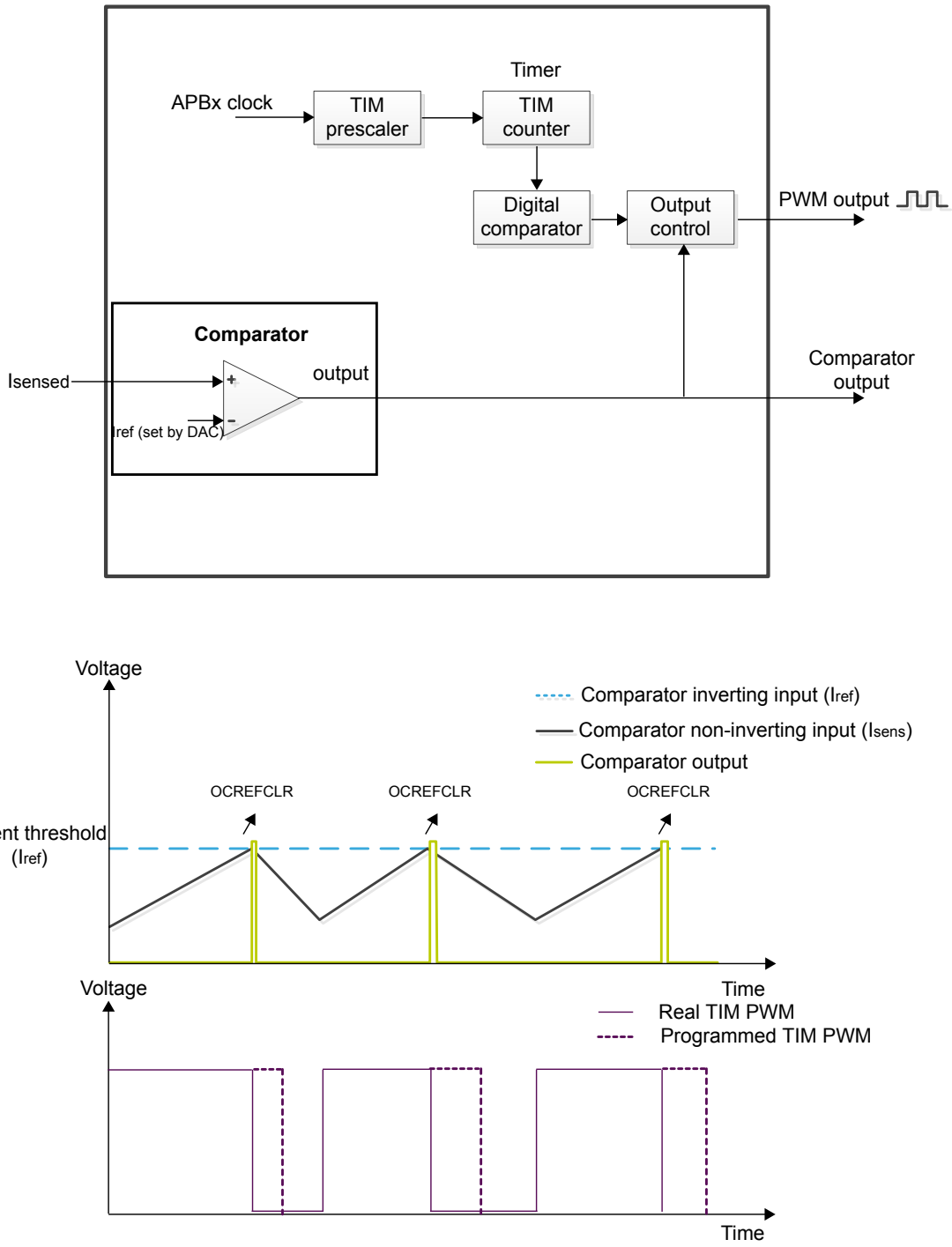
The cycle-by-cycle current control (also called peak current control) is a technique broadly used for power conversion, typically for DC-DC converters, lighting or motor drives.

The current sensor output (for instance a shunt or a current transformer) is connected to the comparator non-inverting (I_{SENSED}) input and compared against a current limit which is set on the inverting input (either a simple resistor divider or the embedded DAC if the set-point has to be adjusted dynamically). When the monitored current exceeds the current limit, the comparator output goes high and disables the PWM outputs for the remaining time in the PWM cycle. On the next cycle, if the comparator output is back to zero (i.e. the current is below the limit), the PWM output is enabled again.

As displayed in Figure 3, the SR5E1 devices are designed for these kinds of applications, where the timer is used in PWM mode to control the motor. The analog comparator is used to monitor the motor current on-the-fly. The comparator output is internally redirected to the OCREF_CLR signal which controls the PWM state. The embedded digital analog converter is internally connected to the inverting input of the comparator.

In Figure 3 both the real PWM (solid line) and the programmed PWM (dotted line) values (if there were no tim_ocref_clr_int feedback) are displayed.

Figure 3. **Block diagram of cycle-by-cycle current control**



3.2 Frequency and pulse width measurement

In the SR5E1 devices, the comparator output can be redirected to the input capture of the embedded timers. This feature allows a pulse width and/or frequency measurement. The input signal,whose signal width/frequency must be measured, is connected to the non-inverting input of the analog comparator. The threshold (reference) can be powered by:

- The internal reference voltage VREFH - VREFL(3.3V) and sub-multiples (1/3 VREFH - VREFL,2/3 VREFH - VREFL)
- The embedded digital-to-analog (DAC) converters
- An external pin

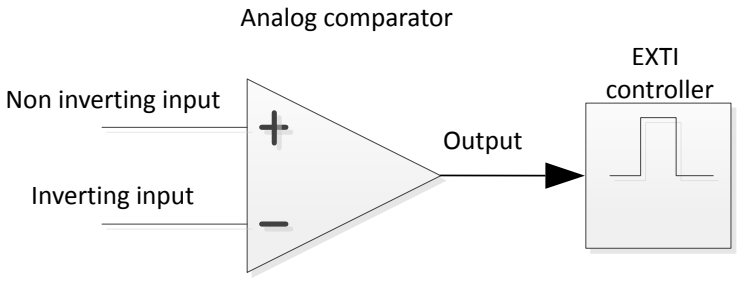
The comparator output is redirected internally to the input capture. In this mode, the timer counter is captured at each effective edge. When the input signal goes higher than the reference voltage, the comparator output is set to a high level generating a rising edge on the timer input capture, and the timer counter is captured in the internal register. When the input signal goes lower than the reference voltage, the comparator output is set to a low level generating a falling edge and the timer counter is captured a second time in the internal register. The time elapsed between the two consecutive captures represents the pulse width. Hence, the pulse width measurement is performed by a simple subtraction of the second and the first capture.

3.3 Analog voltage monitoring

The SR5E1 devices embed a 12-bit analog-to-digital converter (ADC) which is very fast with a sampling rate in the order of several mega samples per second. However, with a typical consumption of 2.65 mA, it may not be suitable for battery-powered applications if it is left powered-on continuously. It is therefore useful to use an analog comparator in application cases where an analog voltage (sensor output) needs to be measured only when a predefined threshold is exceeded.

In the SR5E1 devices, the analog comparators are designed to work even in CSleep mode. In CSleep mode, comparators are still powered-on and so they can wake up the MCU. In fact, the comparator output is connected to the EXTI controller which also remains powered-on in CSleep mode.

Figure 4. Comparatoroutput capability in CSleep mode

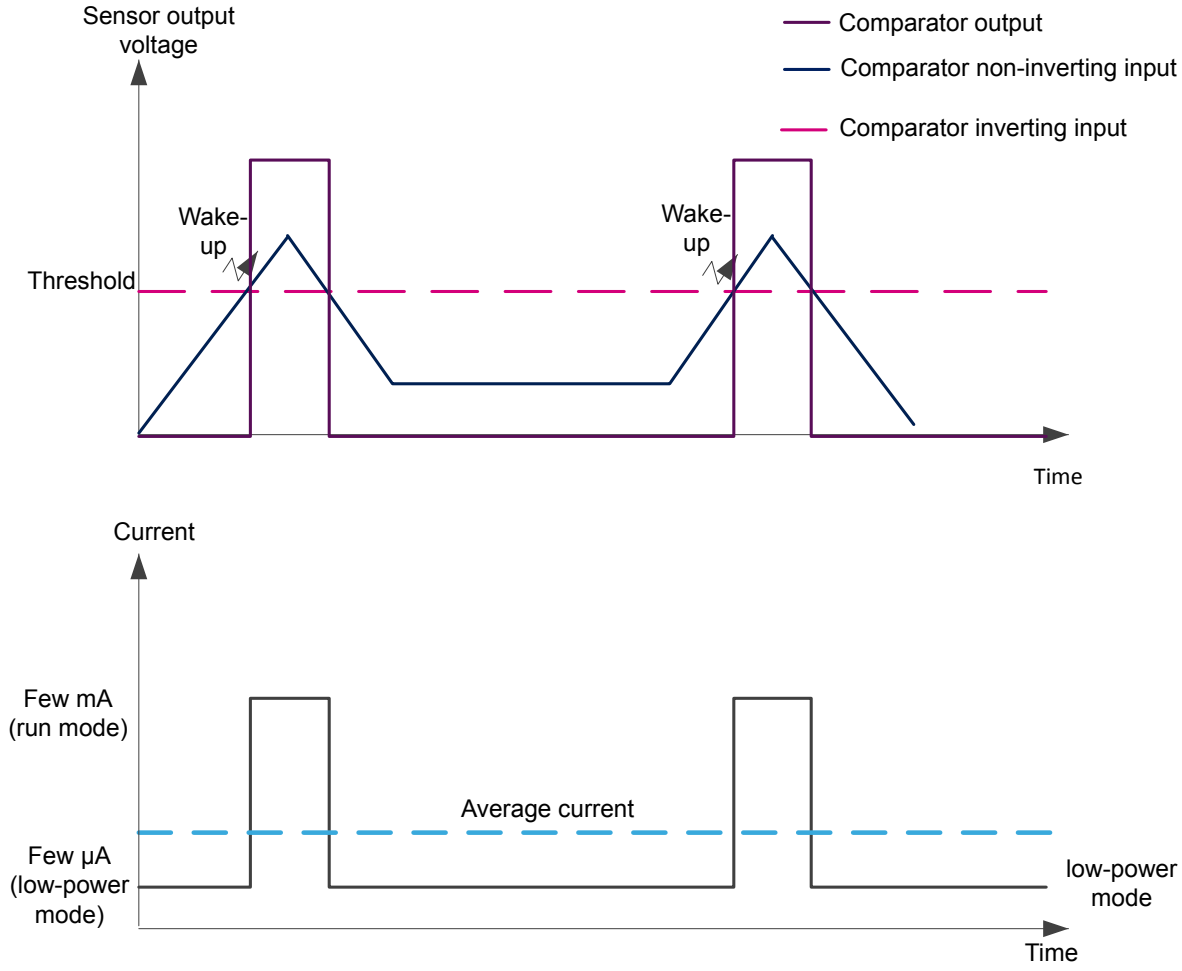


Moreover,the comparator input is an ADC channel so PCB designer does not need to make an external connection between the comparator input and the ADC channel.

In an analog voltage monitoring application where the sensor output voltage is lower than the threshold, the MCU remains in CSleep mode thereby saving power. As soon as the sensor output exceeds the threshold, the analog comparator wakes up the MCU, the ADC is powered on, and the analog input voltage is measured.

Enabling the ADC only when required (analog voltage higher than a threshold) dramatically reduces the average power consumption, as compared to an application where the ADC is always enabled whatever the analog voltage.

Figure 5. Current consumption in an analog voltage monitoring application



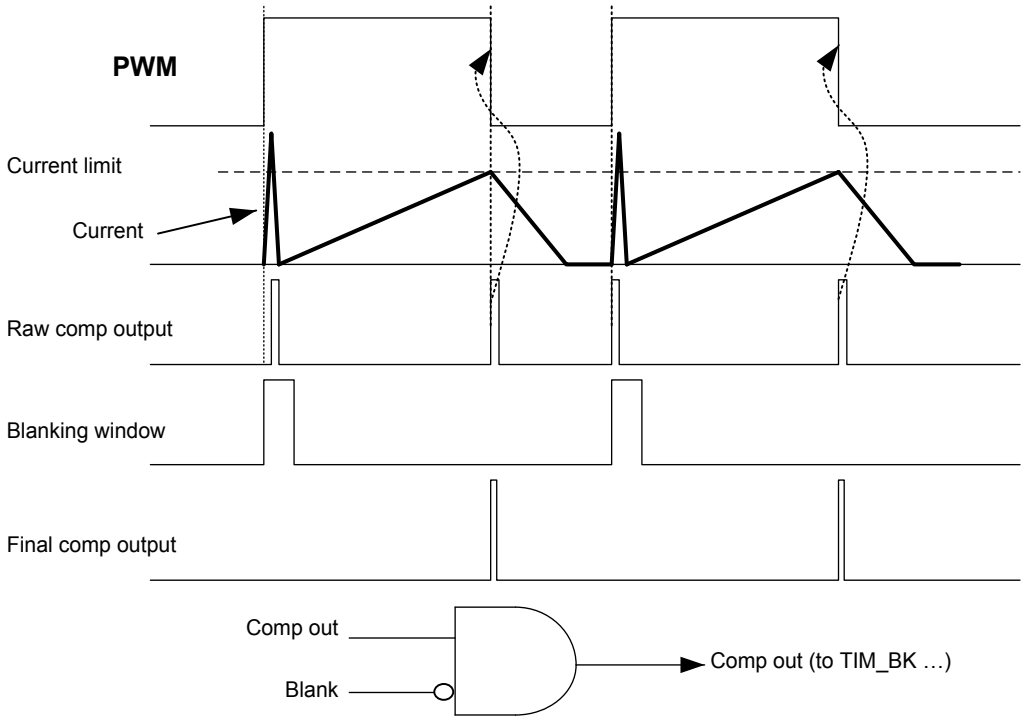
3.4 Preventing false over-current detections in motor control applications

At PWM startup, a very high current flows through the current shunt during a short time and may be seen by the comparator as greater than the inverting input. In this case, the comparator output is set and may generate an unwanted emergency stop if the comparator is connected to the timer break input. This startup current is acceptable at the beginning of PWM periods and must not be managed by the comparator as a fault current (short-circuit, overload, ground fault, etc.)

The analog comparator output can be blanked using a timer output as a blanking source. The blanking source is selected/configured by software and is ANDed with the comparator output, resulting in a final comparator output which is not high during the peaks at the beginning of the PWM periods.

Figure 6. Comparator output blanking shows how the comparator output is ANDed with a timer output in order to blank the comparator output for a programmed duration. The same TIM as the one used for the PWM generation can also be used for comparator blanking.

Figure 6. Comparator output blanking



An example is provided below.

The COMP_Output Blanking example aims at showing how the blanking feature is used. Below, details about this example for StellarE,

COMP1 is configured as follows:

- The non-inverting input is connected to PB2
- The inverting input is connected to 1/3 VREFH(1.1V)
- The output is available on PC5
- The output generate a break event when the non-inverting input is at a higher voltage than the inverting input (1/3 VREFH)
- TIM2OC3 is used as a blanking source

TIM2 is configured as follows:

- TIM2 period is APB2 clock / period = (300000000/2)/5000 = 3000 Hz
- TIM2 CH1 (PH2) configured in PWM mode with a frequency equal to 3000 Hz and a duty cycle pulse/ period =100 * (37500/50000) = 75%.
- TIM2OC3 (PH4) configured in PWM mode with a frequency equal to 3000 Hz and a high level equal to pulse/period = 4000/(300000000/2)= 26.88 microseconds
- A break event is generated at a high polarity (when the non-inverting input is at a higher voltage than the Inverting input)

Test configuration and expected results:

- Connect COMP1 non-inverting input (PB2) to TIM2 CH1 (PH2).
- TIM2CH1 PWM has a duty cycle of 250 microseconds.
- The COMP1 output (PC5) is the logical AND operation between TIM2 CH1 PWM and negative TIM2 CH3 PWM, resulting in a PWM with duty cycle equal to 68%.

Revision history

Table 2. **Document revision history**

Date	Revision	Changes
07-Jun-2023	1	Initial release.

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