Introduction to MB1971 LLC HAT 12 V to 7.5 V/1 A for F334 G474 Nucleo board

Introduction

This application note describes the MB1971 X-NUCLEO LLC DC/DC expansion board for converter shield designed specifically for the STM32F334/STM32G474 Nucleo boards. It is a low-cost and easy-to-use development kit useful to quickly evaluate and start develop application with the microcontrollers of the STM32F334/STM32G474 series. It plugs directly onto the MORPHO sockets, adding all the necessary hardware to evaluate the hi-resolution timer for the half-bridge LLC power converters.

The STM32F334 & STM32G474 Arm® Cortex®-M4 microcontrollers, embedding a hi-resolution timer, combines high integration and performance. They have been designed for digital power conversion applications. This LLC DC/DC converter board illustrates how they can control a half-bridge LLC topology on both the primary and secondary side.

This demonstration needs an external 12 V/1.5 A power supply that is connected to the add-on board.

The firmware associated to this example needs to be programmed into your STM32F334/STM32G474 Nucleo board prior to the demonstration.

1 Application description

1.1 Required hardware

This application uses the STM32F334 or the STM32G474 Nucleo board. An external DC power supply (12 V dc 1.5 A minimum) is required for the demonstration.

The external power supply must be connected to the CN1 or CN2 socket, while the Vout DC voltage is the output on CN3.

Caution: when connecting an external power supply, make sure that the polarity is correct.

1.2 Overview of the LLC stage

The purpose of this DC/DC stage is to step the 12 V dc input down to a 7.5 V dc output. The general overview of the LLC half-bridge topology used for this conversion stage is shown in Figure 2. The power stage of the converter is formed by:

- The input and output capacitors C4 and C9.
- The two MOSFETs Q2 and Q9.
- The transformer T1.
- The inductor L1.
- The resonant capacitors C12, C13, C14, and C15 in parallel.

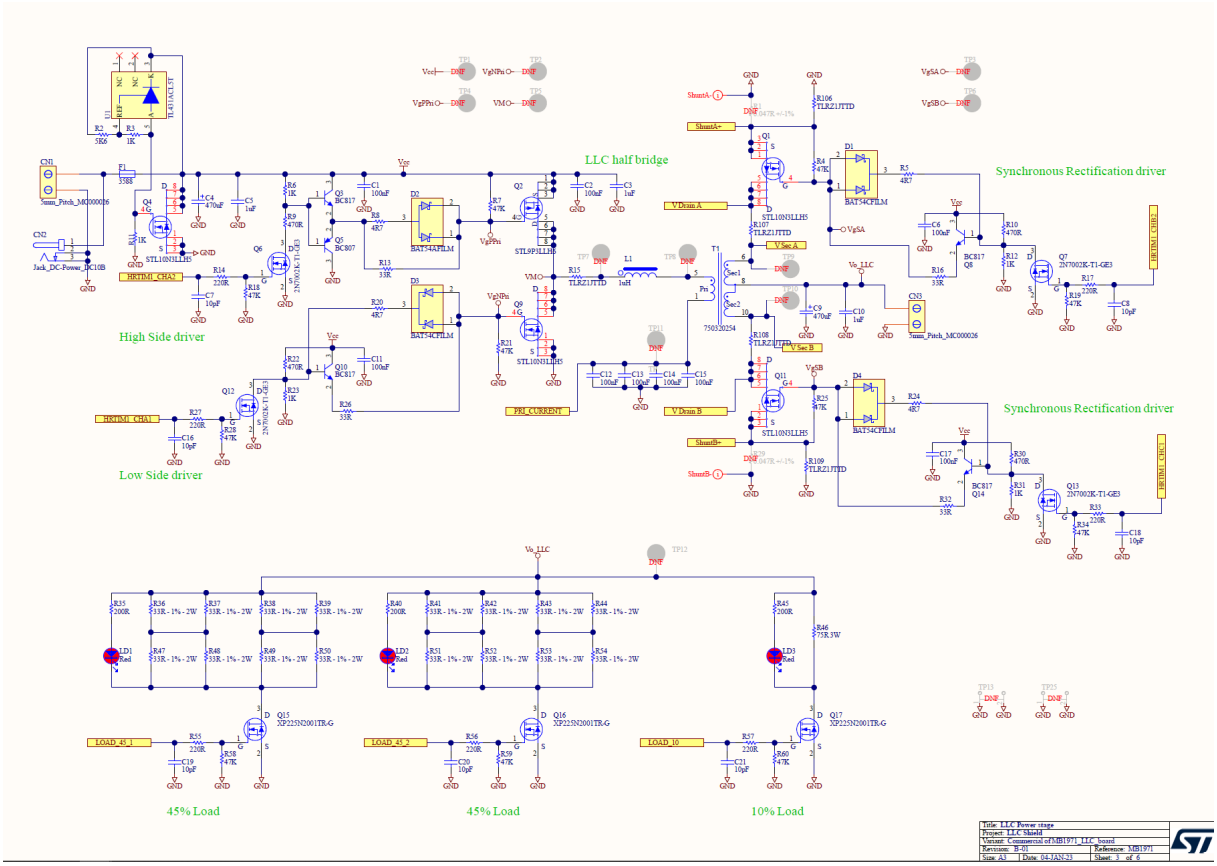
The resonant inductor Lr and the magnetizing inductor Lm depicted in Figure 2 are integrated into the LLC transformer as:

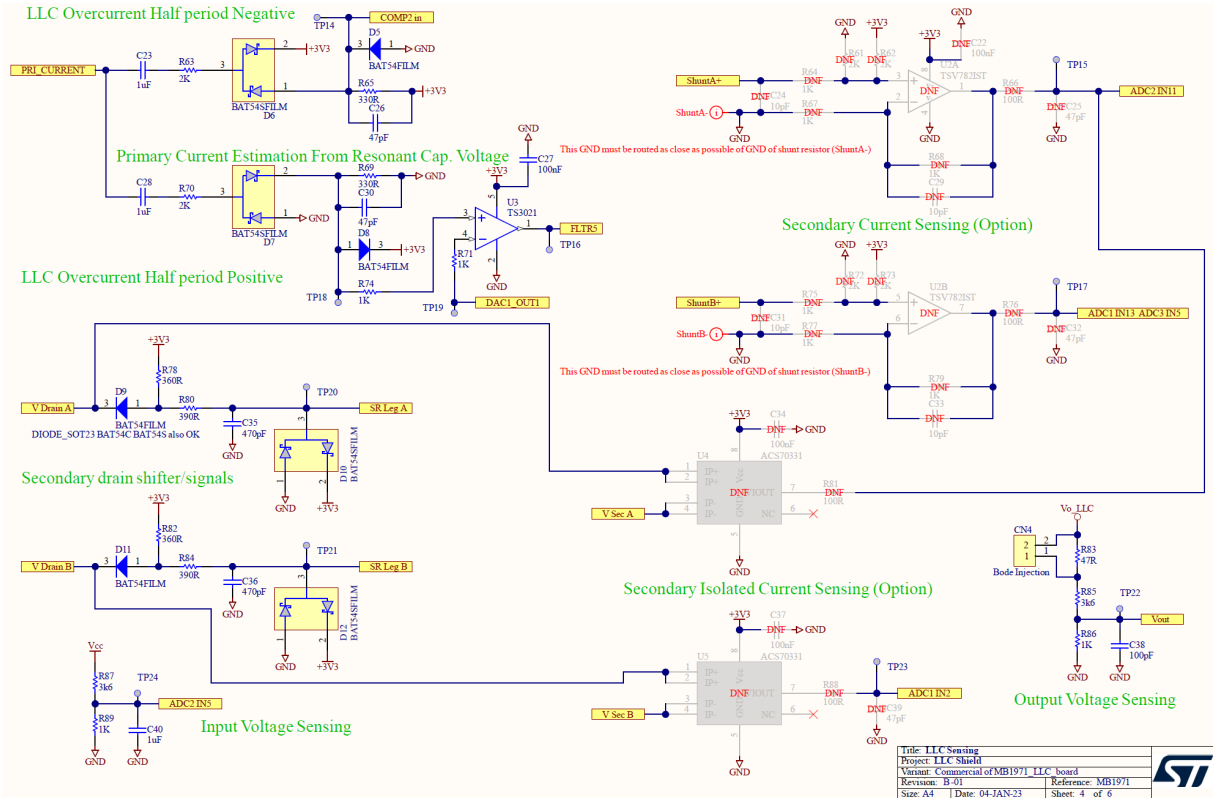
Lm = 6.4uH, Lr = 0.3uH.

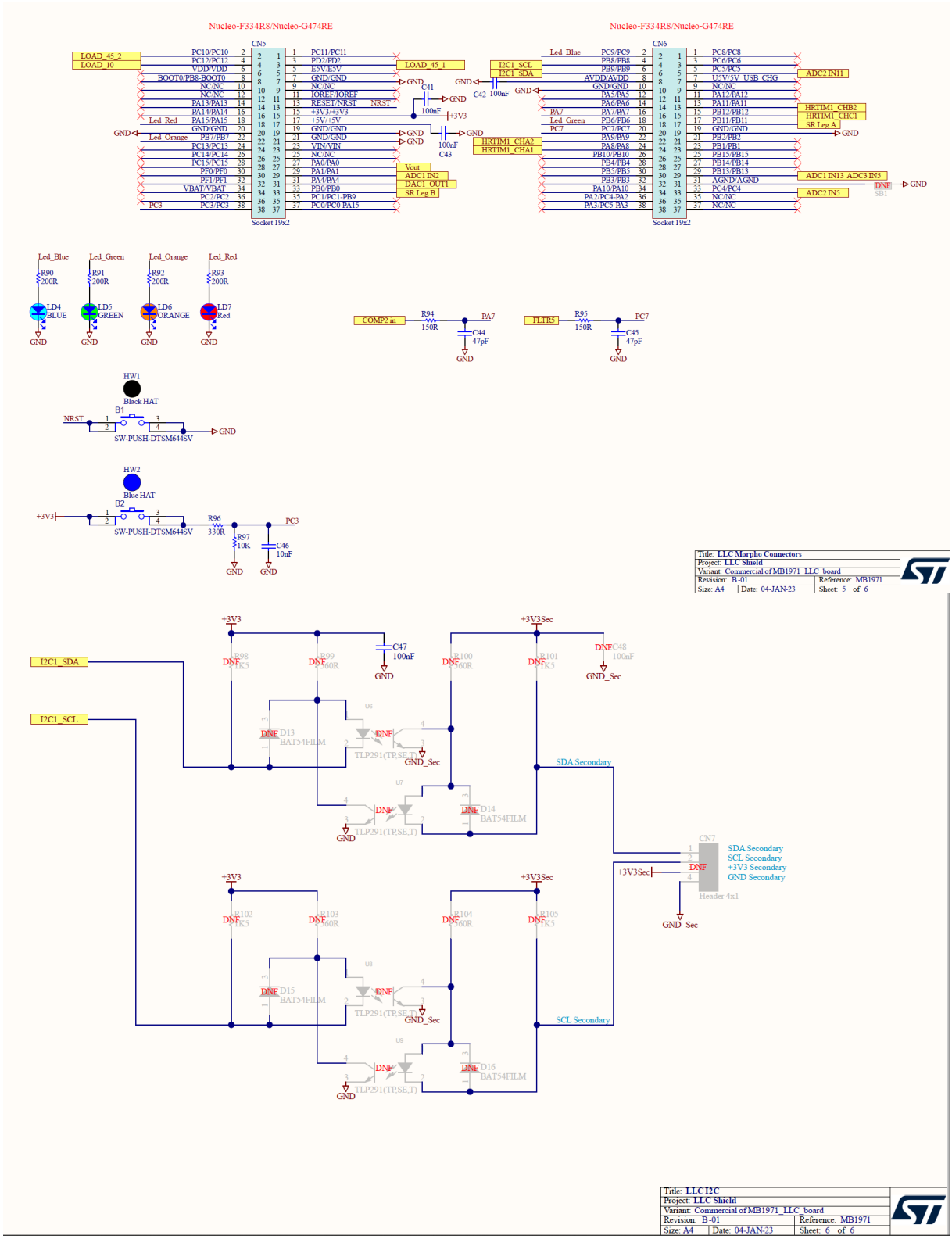
The extra inductor L1 is used to increase the leakage inductance.

The output rectification stage is implemented with two N channels MOSFETs Q1 and Q11. They are switched alternatively within each PWM period while the transformer secondary mid tap is connected to the DC output.

Figure 1. Schematics of the LLC DC/DC converter







The main advantages of the LLC topology are:

- ZVS switching for the primary side.
- ZCS switching for the secondary side.
- High efficiency.

The main drawback is the high sensitivity to input voltage variations, which generally requires some design trade-offs to optimize the circuit for a wider input voltage range.

The specifications used for this design are reported in the Table 1.

Note: This design is intended for evaluation and training purposes. Therefore, the power stage transistors have been oversized to sustain the electrical stress inherent to harsh testing environments. No isolation is provided in between the primary and the secondary for evaluating the hi-resolution timer IP. The main goal of this demonstration board is to propose a low-voltage evaluation solution with a rugged hardware. A legacy discrete approach has been chosen for the gate drivers for educational purpose.

Table 1. Main specifications

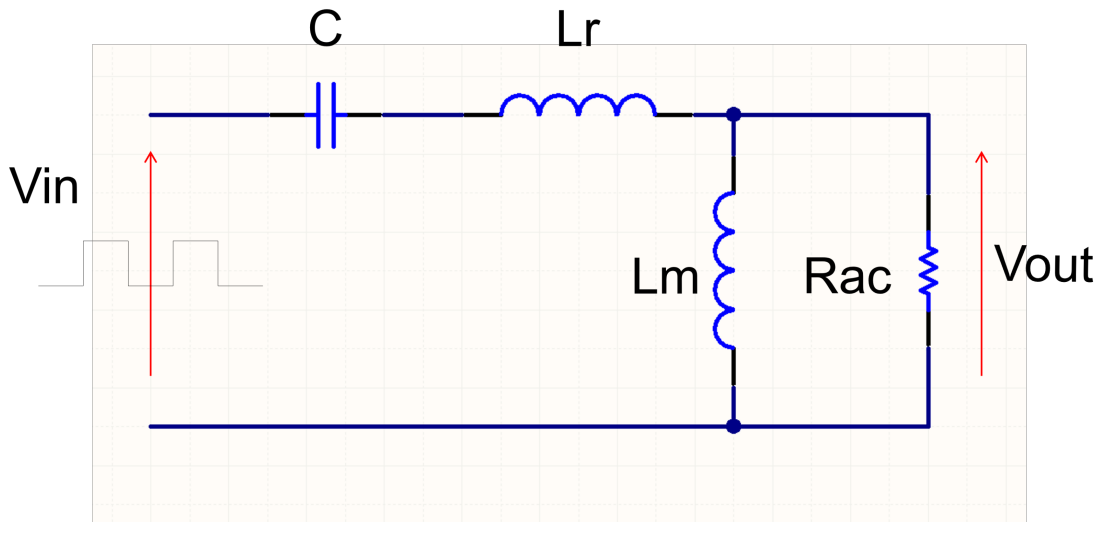
Input voltage	12 V +/- 0.5 V
Output voltage	7.5 V
Output power	7.5 Watts/1 A
Switching frequency	Within 100 kHz - 300 kHz range
Regulation and secondary rectification	PI(D) controller for primary switching frequency. Two strategies for secondary MOSFET rectification (SR): • Fixed ON time • Variable ON time with drain voltage monitoring
Input short-circuit protection	2 A fuse
Output short-circuit protection	Managed by the STM32F334/STM32G474.
Input under/overvoltage	Managed by the STM32F334/STM32G474. DC IN shorted to ground if the input voltage goes above 15 V (by MOSFET Q4).
Output under/overvoltage	Managed by the STM32F334/STM32G474.
Embedded load resistors	10 %, 45 %, 45 % GPIO controlled dummy resistor loads (100 ma/450 mA/450 mA @7.5 V dc)
Transformer, WURTH Electronics, P/N 750320254	• 1:1.33:1.33 turns ratio • Lm 6.4uH, Lr 0.3 uH • Core material: TP5 • 8 A pk-pk primary saturation current

2 Initial design steps

The voltage gain of the LLC converter resonant tank can be expressed as depicted in the figure below:

Note: Readers are assumed to have a basic knowledge of power converter topologies.

Figure 2. Representation of the LLC passive components with the load



3 Equations

Overall gain:

$$M\left(F_n, \lambda, Q\right) = \left|\frac{Vout}{Vin}\right| = \frac{1}{\sqrt{\left(\left(1+\frac{1}{\lambda}\right)-\frac{1}{\lambda F_n^2}\right)^2 + Q^2 x\left(F_n-\frac{1}{F_n}\right)^2}} \quad (1)$$

Where:

$$F_n = \frac{F_{sw}}{F_r} \quad (2)$$

is the normalized frequency ratio between the switching frequency Fsw and the resonant frequency Fr. Fr being the resonant frequency (in hertz) varying depending on the load in between:

$$\frac{1}{\left(2\pi\sqrt{C(L_r+L_m)}\right)} \leq Fr \leq \frac{1}{2\pi\sqrt{CLr}} \quad (3)$$

$$\lambda = \frac{L_m}{L_r} \quad (4)$$

is the inductance ratio between the transformer magnetizing inductance and the total resonant tank inductance.

$$Q = \frac{1}{R_{ac}}\left(\sqrt{\frac{Lr}{C}}\right) \quad (5)$$

is the quality factor. The typical range is from 0.1 to 1.

The load resistance at full load (using first harmonic approximation) is equal to:

$$R_{ac} = \frac{8n^2V^2out}{\Pi^2 P_{out}}\Omega \quad (6)$$

Note: 'n = n.prim/n.sec' is the primary to secondary turns ratio of the transformer.

3.1 No load condition

Under no load conditions (Q=0), the equation can be written as:

$$M_{0L}\left(F_n, \lambda\right) = \frac{1}{\left|1+\frac{1}{\lambda}-\frac{\lambda}{F_n^2}\right|} \quad (8)$$

In this operating condition, a second resonant frequency can be defined as:

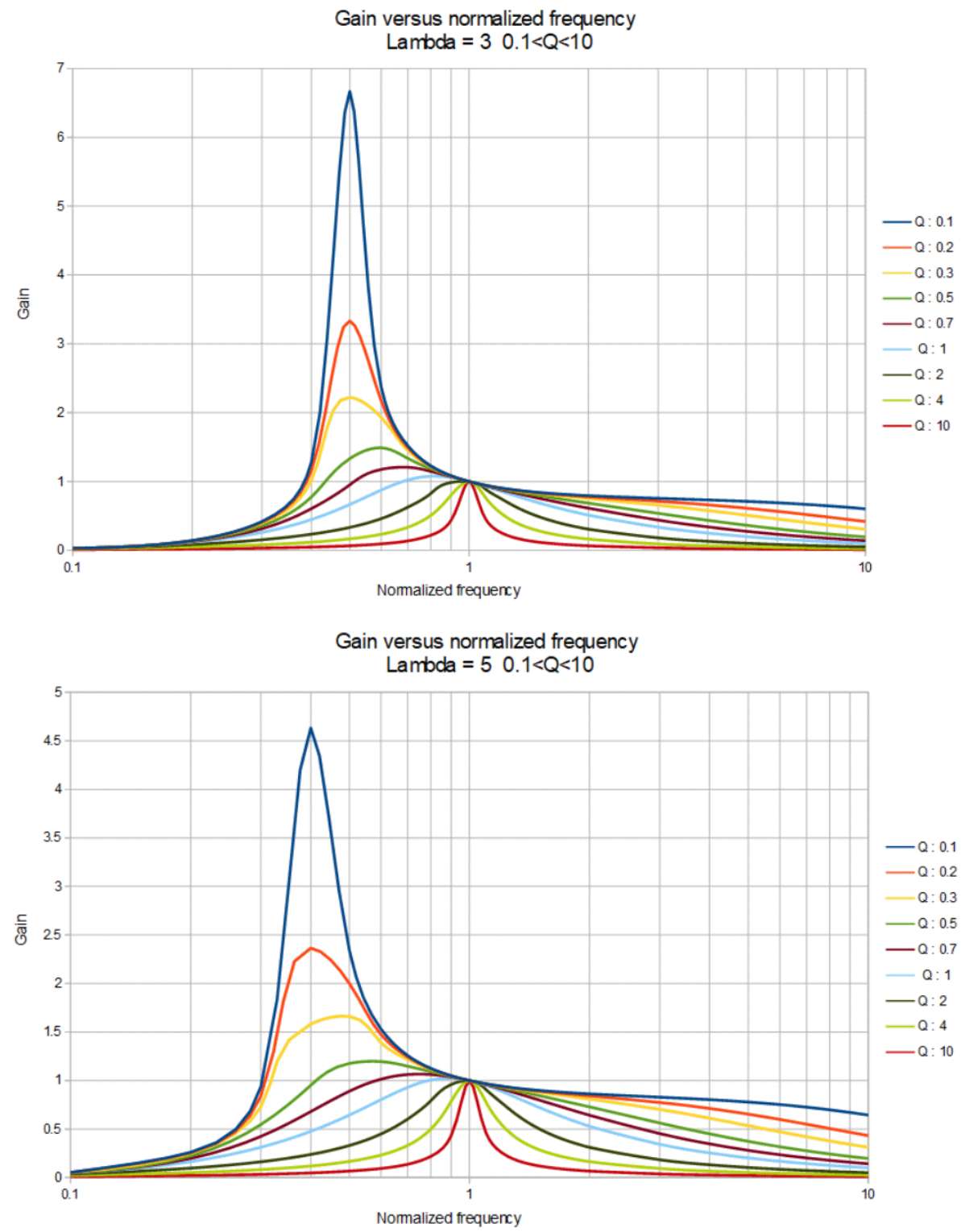
$$F_{0L} = \frac{1}{\left(2\Pi\sqrt{C(L_r+L_m)}\right)} = F_r\sqrt{\frac{\lambda}{1+\lambda}}\,\text{Hz} \quad (9)$$

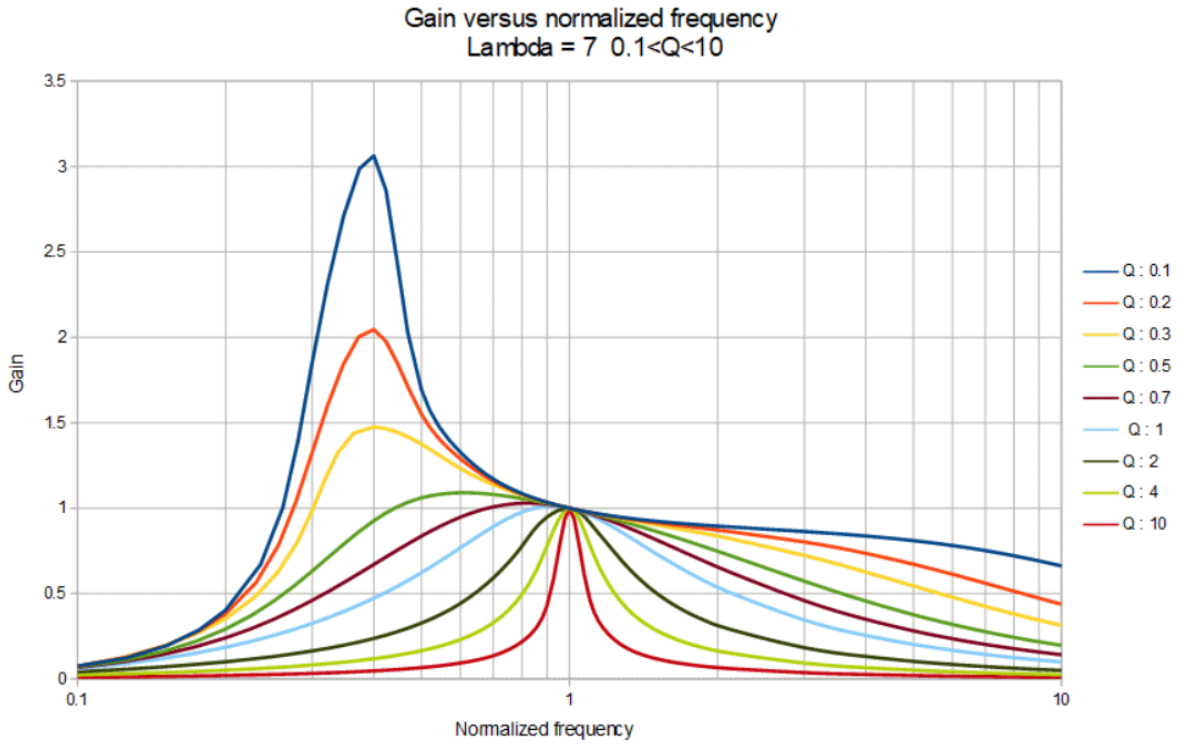
In no load conditions, the rectifier is actually not conducting. Therefore, the total primary inductance (magnetizing plus leakage inductance) resonates with the capacitor.

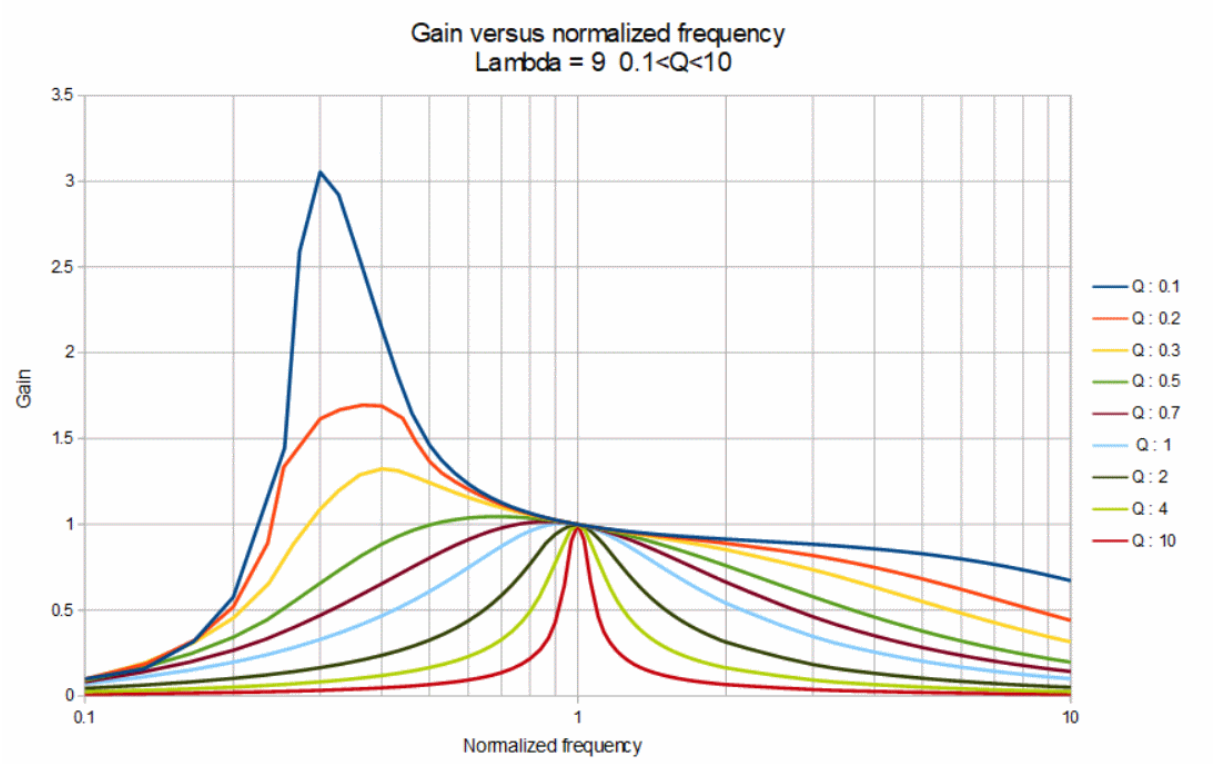
3.2 Voltage gain function M(Fn, l, Q) for different values of lambda and Q

The following figure shows the same resonant tank gain plots for the lambda values 3, 5, 7, 9 and Q values:

Figure 3. **Resonant tank gain for different lamda values (3, 5, 7, 9)**







It is possible to achieve higher gains for lower values of lambda while narrowing the frequency modulation range that may be used to achieve regulation over a smaller frequency range.

Note: At lower input voltage, the transformer current ripple becomes higher and must be maintained at all times lower than the transformer saturation current. Higher circulating energy and conduction losses is induced in that case.

4 Design steps

The design steps are summarized here after:

Switching frequency

According to the core material specifications, the transformer is able to work with a switching frequencies range within 100 kHz - 1 MHz. For the purpose of this demo, the target Fsw is within the 100 to 300 kHz operating range. Other considerations for mass market and final applications are involved, such as form factor increase at lower frequencies due to bulky magnetic parts, higher switching losses at higher frequencies, etc.

At max load, choose a switching frequency Fsw = Fr being within 100 - 150 kHz.

Transformer turns ratio at minimum required input voltage

To calculate the transformer turns ratio, it is assumed that the required gain at the minimum input voltage is unitary:

$$n = \frac{V_{in\min}}{2V_{out}} = \frac{11.5}{2(7.5)} = 0.77 \quad (9)$$

The actual transformer turns ratio provided by WURTH ELECTRONICS is equal to 0.75 (Np:Ns:Ns -> 0.75:1:1 equivalent to 1:1.33:1.33).

To calculate the minimum and maximum voltage gain, it is assumed that there is a +/- 0.5 V margin on Vin -> Vin_min = 11.5 V, Vin_max = 12.5):

- Minimum gain:

$$M_{\min} = 2n\frac{V_{out}}{V_{in\max}} = 2 \times 0.75\frac{7.5}{12.5} = 0.9 \quad (10)$$

- Maximum gain:

$$M_{\max} = 2n\frac{V_{out}}{V_{in\min}} = 2 \times 0.75\frac{7.5}{11.5} = 0.98 \quad (11)$$

The maximum input current assumes 80 % of efficiency. The efficiency is expected to be in a lower range because of a power stage intentionally oversized, which leads to higher commutation losses. Additionally, a discrete gate driver approach with pull-up/down resistors is used.

$$I_{in\max} = \frac{P_{out}}{0.8 \times V_{in\min}} = 0.81\text{A} \quad (12)$$

Equivalent load resistance at full load with FHA (first harmonic approximation):

$$R_{ac} = \frac{8n^2V_{out}^2}{2_{P_{out}}} = 3.11\Omega \quad (13)$$

*Note: At full load, Pout is dissipated into the dummy load resistors (7.5 W). Also, the three LEDs that have series resistors are taken into considerations, and adds 0.25 W per LED leg. Thus, Pout is actually 7.5+3*0.25 = 8.25 W.*

Based on the graphic shown in Figure 3, having previous maximum gain being at least equal to 0.98 and adding extra margin 20 % (for example Gain > 1.2), select as a first trial lambda = 5, and Qmax = 0.4. The value of Qmax is a trade-off in between the curve of 0.3 and 0.5 as shown on Figure 3).

It is possible then to calculate the 'theoretical' resonant tank components:

- Equivalent load resistance at max power output:

$$Z_0 = Q_{\max} \times R_{ac} = 3.11(0.4) = 1.244\Omega \quad (14)$$

- Lm has a fixed specification defined by WURTH manufacturer:

$$L_m = 6.4\text{uH} \quad (15)$$

- The total leakage inductance is (with an extra inductor L1 fitted):

$$L_r = \frac{L_m}{\lambda} = \frac{6.4}{5} = 1.28\text{uH} \quad (16)$$

- With the equivalent load resistance Z0 and Lr calculated above, theoretical Fr is deduced from:

$$F_r = \frac{Z_0}{2 \times \Pi \times L_r}\text{Hz} \quad (17)$$

- The theoretical resonant capacitor is calculated from:

$$C_R = \frac{1}{2 \times \Pi \times F_r \times Z_0} = 905\text{nF} \quad (18)$$

4.1 Resonant tank

The first harmonic approximation (FHA) method assumes a pure sinusoidal/single frequency content signal fed into the resonant tank without all the harmonics content of the square wave used in the actual application: it leads undeniably to errors, but these errors are maintained in an acceptable domain as long as we are 'approximating' our circuit close to the resonant frequency.

Tune the theoretical calculated values from the LLC tank on the bench once they are done. For that purpose, the system is set at max load condition under 12 V dc input. After a few trials, a resonant capacitor of 1uF achieves to get a (resonant) switching frequency of 132 kHz with a 12 V dc input and a switching frequency of 117 kHz with a 11.5 V dc input.

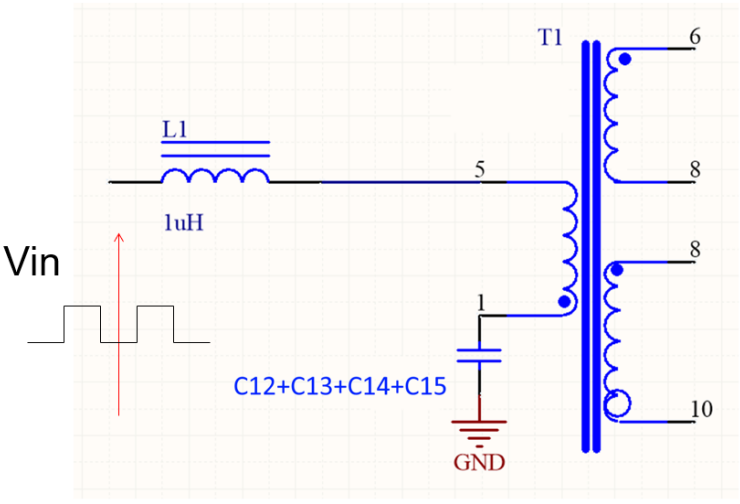
In low or no load condition, the MCU enters automatically in the 'burst' mode in order to reduce the switching losses and the maximum frequency to be applied.

The selected values are chosen within capacitors and inductors standard values. Also, the transformer characteristics are fixed values provided by WURTH electronics (Lm=6.4 uH, Lr = 0.3 uH).

The chosen values are:

- Lr = 1.3 µH (1uH external + 0.3uH within the transformer)
- C = 1uf theoretically, 3 capacitors of 330nF are in parallel

Figure 4. Schematics of the resonant tank



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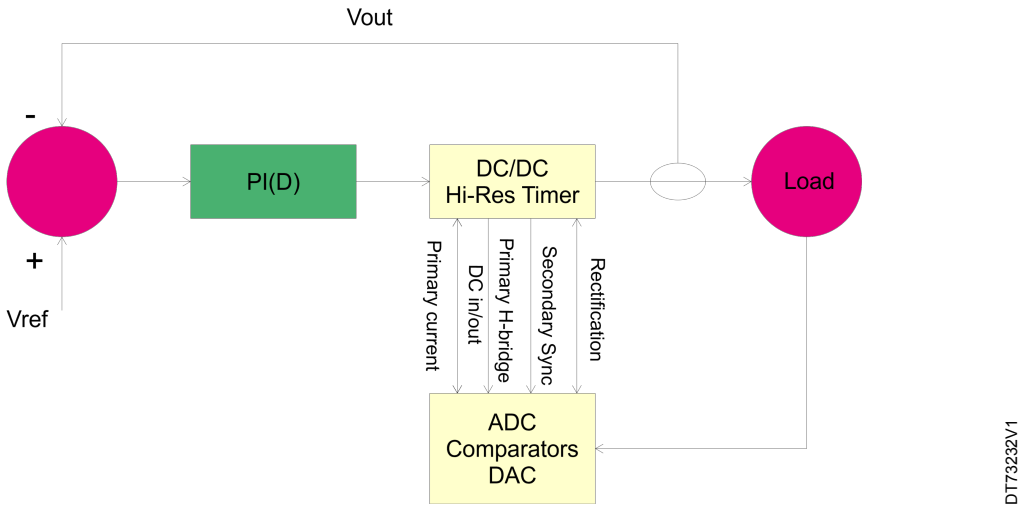
5 LLC converter firmware overview and control algorithm

The LLC firmware is implemented on the MCU, which is embedded on the Nucleo board. They are the STM32F334 or the STM32G474 32-bit microcontrollers from the STM32 family. The control strategy generates the gate signals for both primary and secondary side MOSFETs. The goal is to ensure precise output voltage regulation at 7.5 V DC thanks to a PI(D) regulation.

The secondary side MOSFETs are used to reduce the conduction losses over standard output rectifier diodes solution. The MCU controls the synchronous rectification ("SR") MOSFETs by deducing timings from the one applied on the primary side (which is a fixed percentage of the PWM period) or by monitoring the voltage on the drains of MOSFET Q1 & Q11. See the compiler option `#define USE_COMP_DAC_SECONDARY_RECTIF` in the "app_dpower.h" header file.

The overall block diagram of the control scheme is shown down below:

Figure 5. Overall control principle



The design uses a voltage control loop that relies on a PI(D) regulator. The regulator takes the difference between the reference voltage and the LLC converter output voltage as its input. The MCU high-resolution timer (HRTIM) generates the driving signal pattern to control the primary and the secondary MOSFETs. The HRTIM is specifically designed to drive power conversion systems. It is characterized by a modular architecture and can generate digital signals with either independent or coupled waveforms.

The HRTIM has a timing measure functionality and is connected to built-in ADC, DAC converters, and embedded comparators. It features “burst” light load management mode: it is able to handle various fault schemes for safe shutdown purposes. The HRTIM can be partitioned into several sub modules:

- The master timer
- The timing units (timer A/B/C/...)
- The output stage
- The burst mode controller
- An external event and fault signal conditioning logic
- The system interface

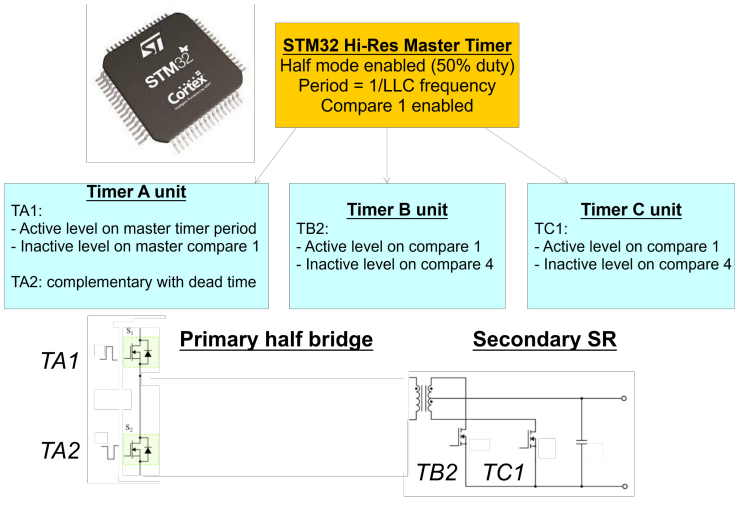
5.1 HRTIM configuration

The HRTIM is configured to drive the LLC stage with the secondary side-synchronous rectification as follows:

- The HRTIM master timer is used for synchronization of timers A, B, and C.
- The HRTIM timer A is used for the primary half-bridge drive. It is configured in half mode and drives the two complementary outputs CHA1 and CHA2 with 50 % duty cycle and an appropriate dead time.

- The HRTIM timer B and timer C are used for the secondary synchronous rectification signals. The ON and OFF time of these two signals can be computed in two ways. Set at compilation level, see `USE_COMP_DAC_SECONDARY_RECTIF` in the main.h header file:
  - SR ON time is fixed by firmware (`#define USE_COMP_DAC_SECONDARY_RECTIF 0`)
  - SR ON time is dynamically adjusted by monitoring the drain voltages of the 2 SR MOSFETs Q1 & Q11 (`#define USE_COMP_DAC_SECONDARY_RECTIF 1`).

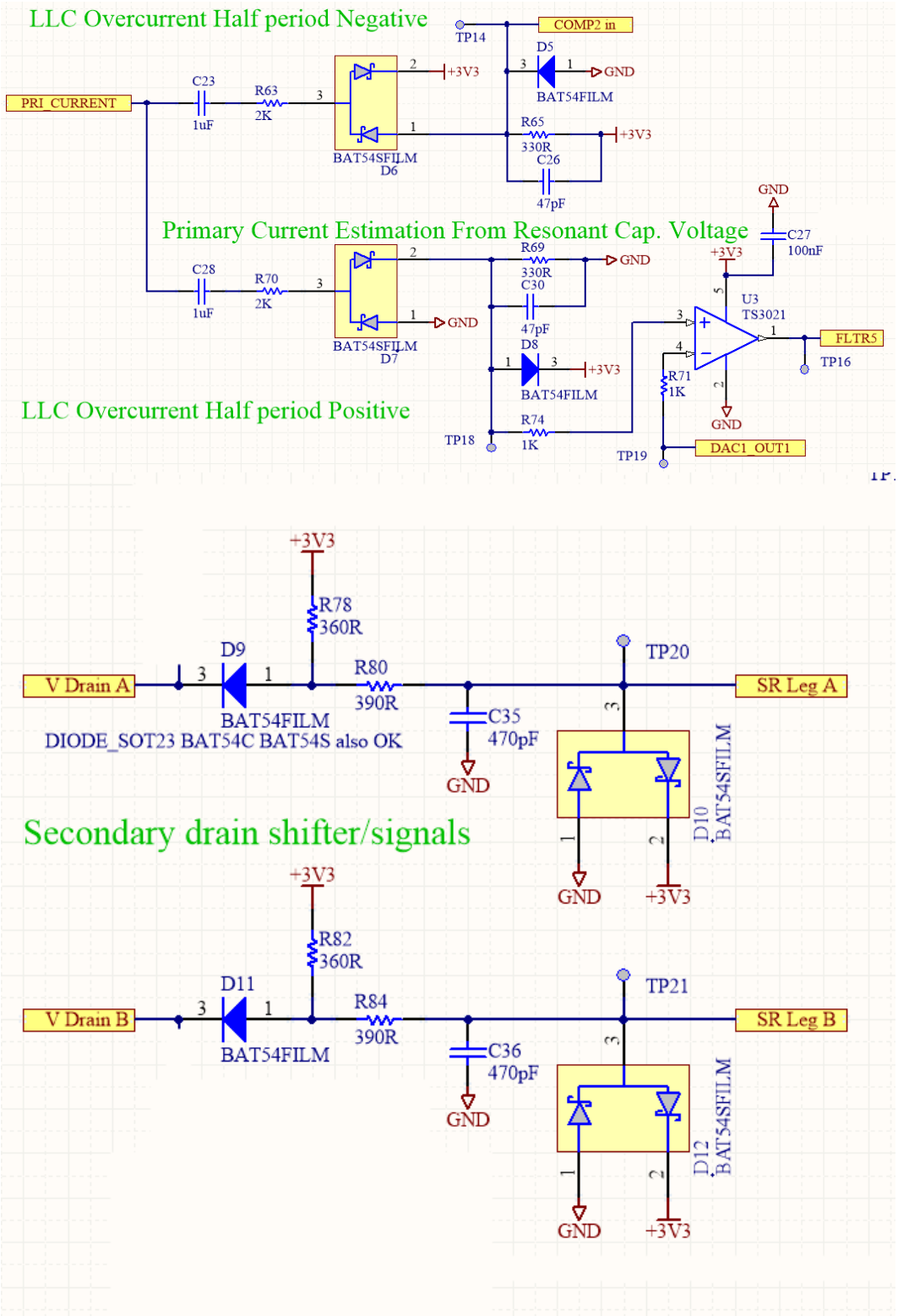
Figure 6. Hi-res timer usage



The hardware is configured to acquire some other measurements such as:

- The LLC transformer primary current (DAC 1 channel 1 & 2 + comparator 2 + 1 external comparator).
- The drain voltages of the SR MOSFETs Q1 & Q11.
- ADC1 CH1 acquires the DC output voltage in continuous regular mode that is used for computation of error from target voltage fed into the PI(D) regulator.
- ADC2 CH5 acquires the DC input voltage in continuous regular mode.

Figure 7. Schematics of the feedback networks for primary current and secondary rectification



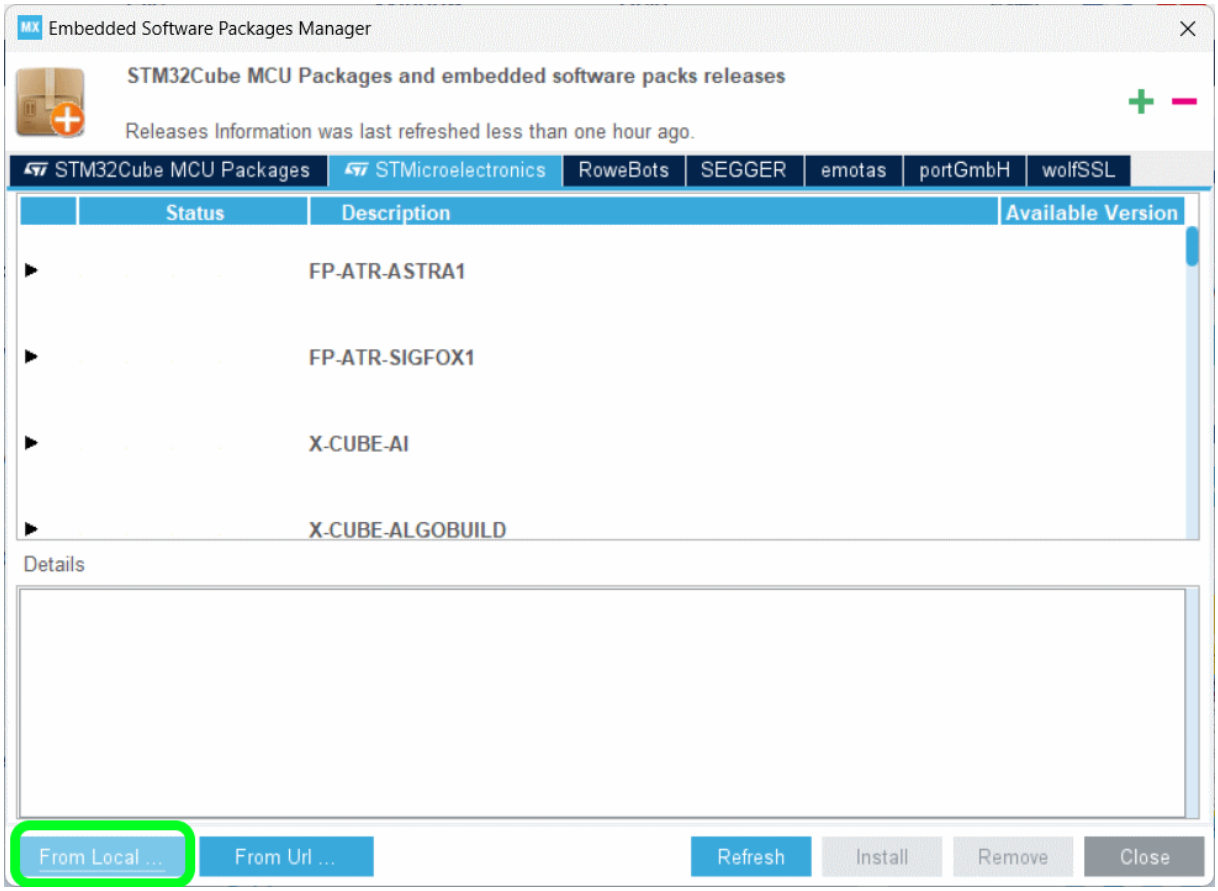
Note: The full MCU IPs' configuration can be retrieved graphically thanks to the STM32CubeMX project file provided within the application project folder (.ioc extension).

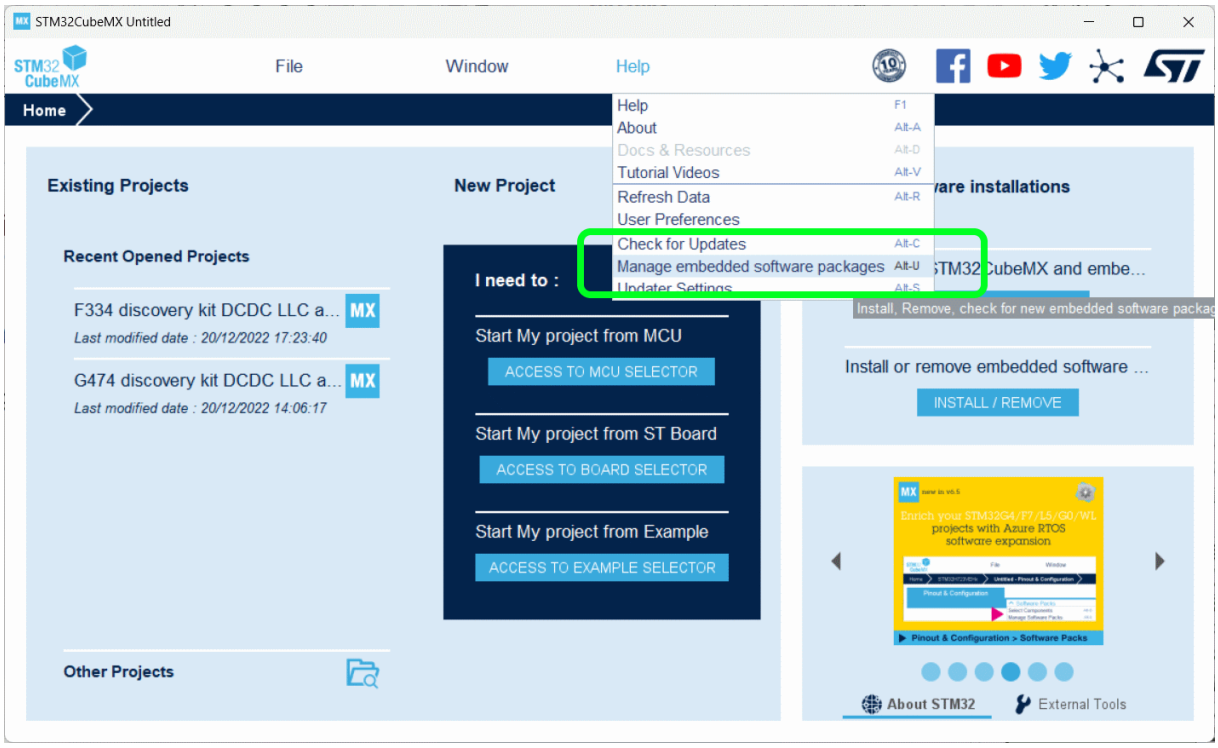
6 STM32CubeMX support

Before opening the STM32CubeMX ‘ioc’ file, make sure that the X-CUBE-DPOWER pack has been installed.

- Download the pack at https://www.st.com/en/embedded-software/x-cube-dpower.html
- Open the help tab and install the pack.

Figure 8. STM32G474 CubeMX pack installation example





Once the pack has been installed, it is possible to check, change, modify the default workspace, and generate the code for the IAR, Keil® or STM32CubeIDE compiler toolchains using the tab `GENERATE CODE` in the main interface.

7 Regulation

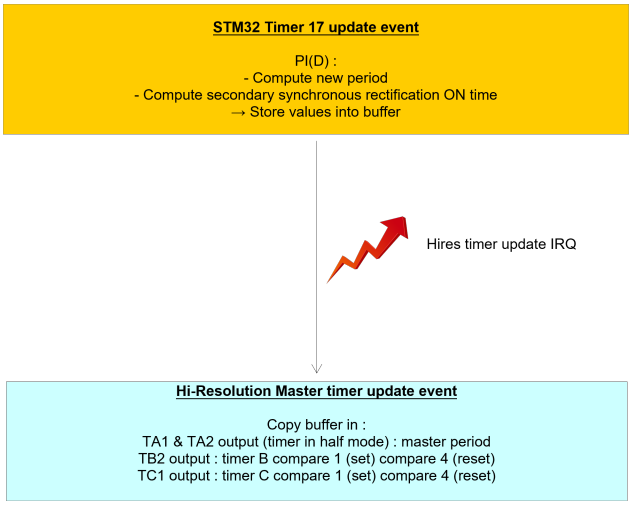
The voltage control loop consists of a standard PI(D) regulator, and is executed at a general purpose timer update frequency (general purpose timer n°17, 50 kHz by default, see `#define DPC_LLC_VOLTAGE_LOOP_FREQUENCY` in “main.h” header file). The actual regulation loop is a PI without differential term in this application. The corresponding code is located in the “CNTRL_PI_Regulator” function in the “DPC_Pid.c” file.

Note: A PI(D) with differential term is available in the “DPC_Pid.c” file. See “CNTRL_pid” routine.

Once executed, the PI(D) output (new computed period) is then fed to the master timer on the next HRTIM update event.

Note: The PI(D) regulator output the updated period value of the primary MOSFET Q2 & Q9 gate signals (new value of HRTIM_MPER register). The frequency can vary from 110 kHz to 230 kHz (clamped by software) while the duty cycle is fixed at all time to 50 %. This updated period is then used to compute the ON time for the secondary side rectification.

Figure 9. PI(D) execution and hi-res timer update event



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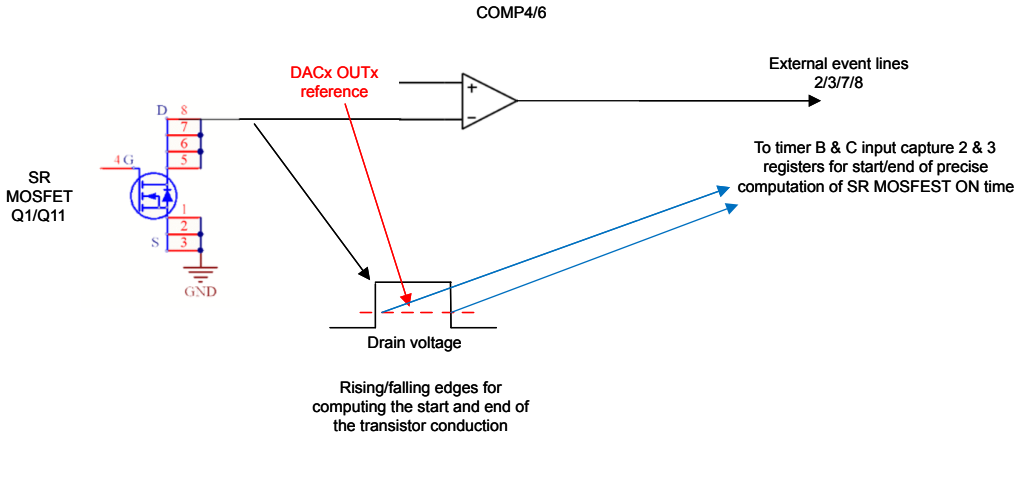
8 Synchronous rectification strategy on secondary

The PI(D) routine computes the period, which computes the start and end of the rising and falling edges (ON time of the MOSFETs Q1 and Q11) for the secondary synchronous rectifier signals:

- Either by setting a fixed ON time computed by the software, and based on a percentage of the new period applied onto the power stage primary side.
- Either being based on the SR MOSFETs drain-to-source falling/rising voltage signals. The control algorithm of the SR monitors alternatively the two drain-to-source voltages (rising and falling edges) around a predefined level set by the DAC2 reference output `DPC_DAC2_REF_SYNC_REC_SECONDARY` in the 'main.h' file, and by capturing these events into the input capture registers 2 & 3 of the hi-res timer B and C. The new turn ON and OFF events are then computed based on these values with margins (see timer n°17 IRQ handler) to avoid turning ON too early and turning OFF too late.

Figure 10. MCU internal analog configuration for SR MOSFET drain voltage monitoring



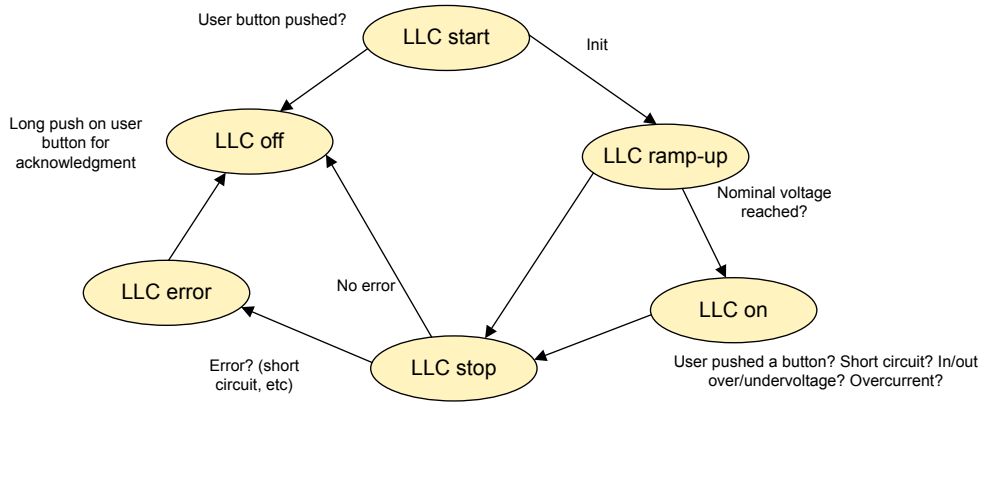
9 Firmware structure

The LLC converter firmware structure and its main tasks are highlighted in this section.

If there is no error like under/over voltage conditions, the LLC converter remains in IDLE state until the user pushes the B2 button (with the blue hat).

Note: The B1 button (with the black hat) is connected to the reset signal of the MCU.

Figure 11. LLC flowchart overview



The main routines for controlling the LLC converter in runtime are highlighted in the following table.

Table 2. LLC main firmware tasks

Function	Task	Execution frequency	Priority
TIM1_TRG_COM_ TIM17_IRQHandler()	• PI(D) execution (voltage control loop) • Burst mode management • Computation of secondary synchronous rectification ON time based on Q1 & Q11 drain voltages	50 kHz (default), see `DPC_LLC_VOLTAGE_LOOP_FREQUENCY` in 'main.h'	IRQ, high
HRTIM_MASTER_ IRQHandle()	Set hi-res timer period and compare registers based on computed values within timer 17 IRQ	IRQ enabled by the GP timer n°17 update interrupt, 50 kHz (default)	IRQ, high
MX_DPower_Process()	• User state machine • Process overcurrent/ under-overvoltage events	Main level	Main level
SysTick_Handler()	• 1 ms timebase • LED/Load/button/short circuit management	1 kHz	IRQ, low

10 'Half-period by half-period' overcurrent protection

The STM32F334/STM32G474 embeds respectively 3/7 comparators that can be used as standalone peripherals (all terminals are available on I/Os). They can also be combined with the timers. They can be used for a variety of functions such as

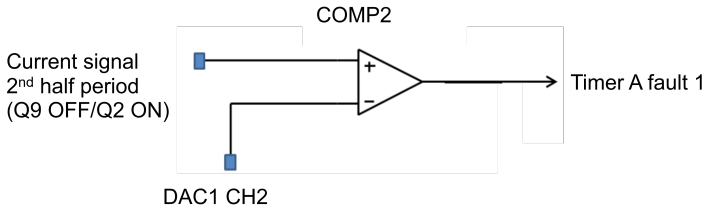
- Wake up from a low-power mode triggered by an analog signal.
- Analog signal conditioning.
- Cycle-by-cycle current control loop when combined with the DAC and a PWM output from a timer.

Standards overcurrent detections use an RC filter to feed back part of the resonant capacitor voltage to the MCU, which can cause delays. In contrast, the overcurrent protection in this application monitors the same resonant capacitor voltage within each half PWM period while the primary high or low side MOSFET Q2/Q9 is turned ON. Thanks to an internal comparator (COMP2) + 1 external comparator, a precise half-period by half-period overcurrent protection is achieved.

The corresponding hardware configuration is shown in the figure below. An external comparator has been added on this application to add one extra to the three already available into the STM32F334, as we need a total of 4 comparators for this project:

- The inverting pin of the microcontroller internal comparator COMP2 is connected to the channel 2 of the DAC1, and the non-inverting pin is connected to the output of the voltage sense circuit used to measure the LLC converter primary current (second half period, C23 R63 D6 R65 network).

Figure 12. Internal comparator configuration for overcurrent protection, second half period



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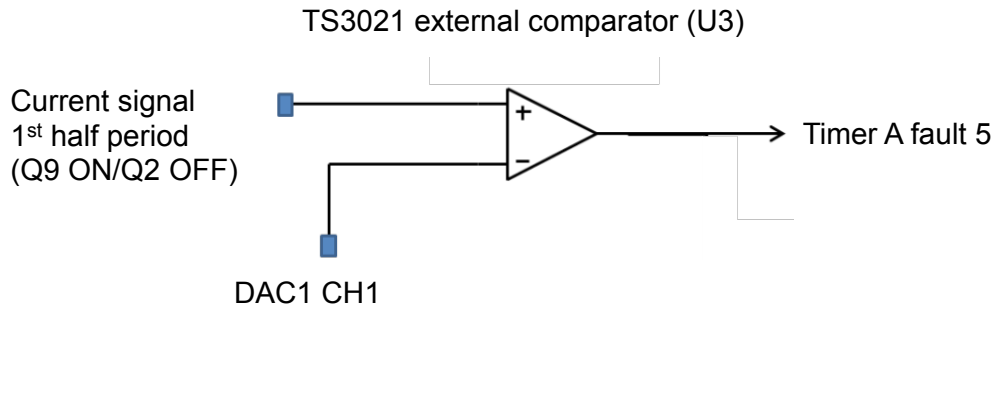
- The inverting pin of the external comparator U3 is connected to CH1 of DAC1, and the non-inverting pin is connected to the output of the voltage sense circuit used to measure the LLC converter primary current (first half period, C28 R70 D7 R69 network).

Figure 13. External comparator configuration for overcurrent protection, first half period



When the sensed voltage is higher/lower than the preset threshold by the DAC CH1 & CH2 (see `#define DAC1_CH1_CH2_OVC_VALUE` in 'main.h' file), a fault event is generated to set the timer A output channels in an inactive state automatically.

Note: *A HRTIM timer A interruption can be generated.*
An overcurrent flag is raised into the dedicated `HRTIM_ISR_FLTxPos` bit of the HRTIM COMMON hardware register.

Once the fault event is over, the LLC DC/DC state is updated to DCDC_FAULT, and is pending for user acknowledgment input (long push onto the B2 button). Then, if no fault is pending nor detected, the LLC converter can be restarted again.

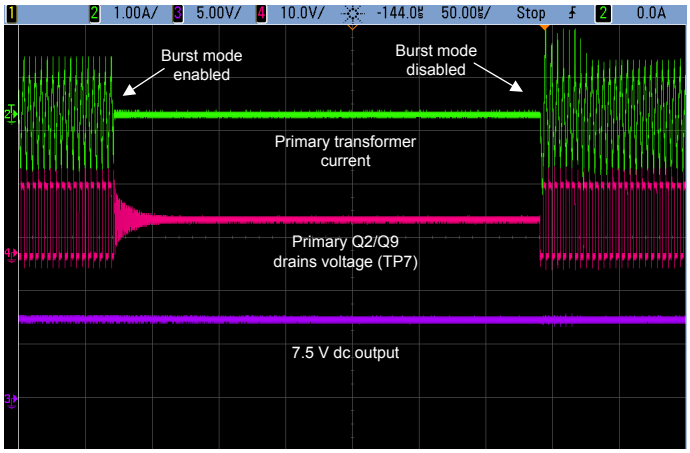
Note: *The DAC channel 1 and 2 is using the same over current reference `DAC1_CH1_CH2_OVC_VALUE` but are referenced to GND or VCC (first or second half of the period corresponding to Q2 ON Q9 OFF and Q2 OFF Q9 ON). Therefore, the channel 1 and 2 is set to `DAC1_CH1_CH2_OVC_VALUE` and `4095 – DAC1_CH1_CH2_OVC_VALUE`. See the 'main.h' header file.*

11 Burst mode

The burst mode operation is implemented for light load management. The main purpose is to reduce the number of transitions on the power stage and the associated switching power losses in order to increase the efficiency of the converter at light or no load condition.

The STM32 burst mode controller can switch the outputs alternatively between IDLE or RUN state using the hardware, so that some switching periods are skipped with a programmable periodicity and duty cycle.

Figure 14. Burst mode operation at light load



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The burst mode operation is enabled when the period output of the PI(D) regulator is lower than a predefined threshold (switching period) corresponding to a switching frequency of 200 kHz. Similarly, it is disabled when the PI regulator output is greater than a threshold set to 180 kHz. In this way, the output voltage is regulated at 7.5 V during no-load and light-load operations. These thresholds are declared in the ‘main.h’ header file:

```
#define BURST_FREQUENCY_ENTRY 200000
#define BURST_FREQUENCY_EXIT 180000
#define BURST_PULSES_ON_OFF_HYSTERESIS  (OUT_VOLT_ADC_VALUE(0.05))
```

12 Short circuit protection

The short circuit protection is implemented thanks to a 1 ms timebase that is decremented whenever the output voltage is getting abnormally low for an extended period of time. Once the timebase reaches zero, the MCU stops immediately the power stage and trigger a short circuit protection event.

The short circuit timebase is decremented in the systick IRQ (1 ms timebase). The control/check of this timebase is checked in the background task (main level) within the function DCDC_FaultCheck().

12.1 Over/undervoltage protections

DC output

The overvoltage output protection is implemented within the `DCDC_OutVoltageCheck()` routine. It allows the monitoring of the DC output even if the regulation is active. For example, there is a risk of overvoltage on the output whenever the BURST mode is disabled (at compiler level) and the frequency being clamped to the maximum with no or light load condition.

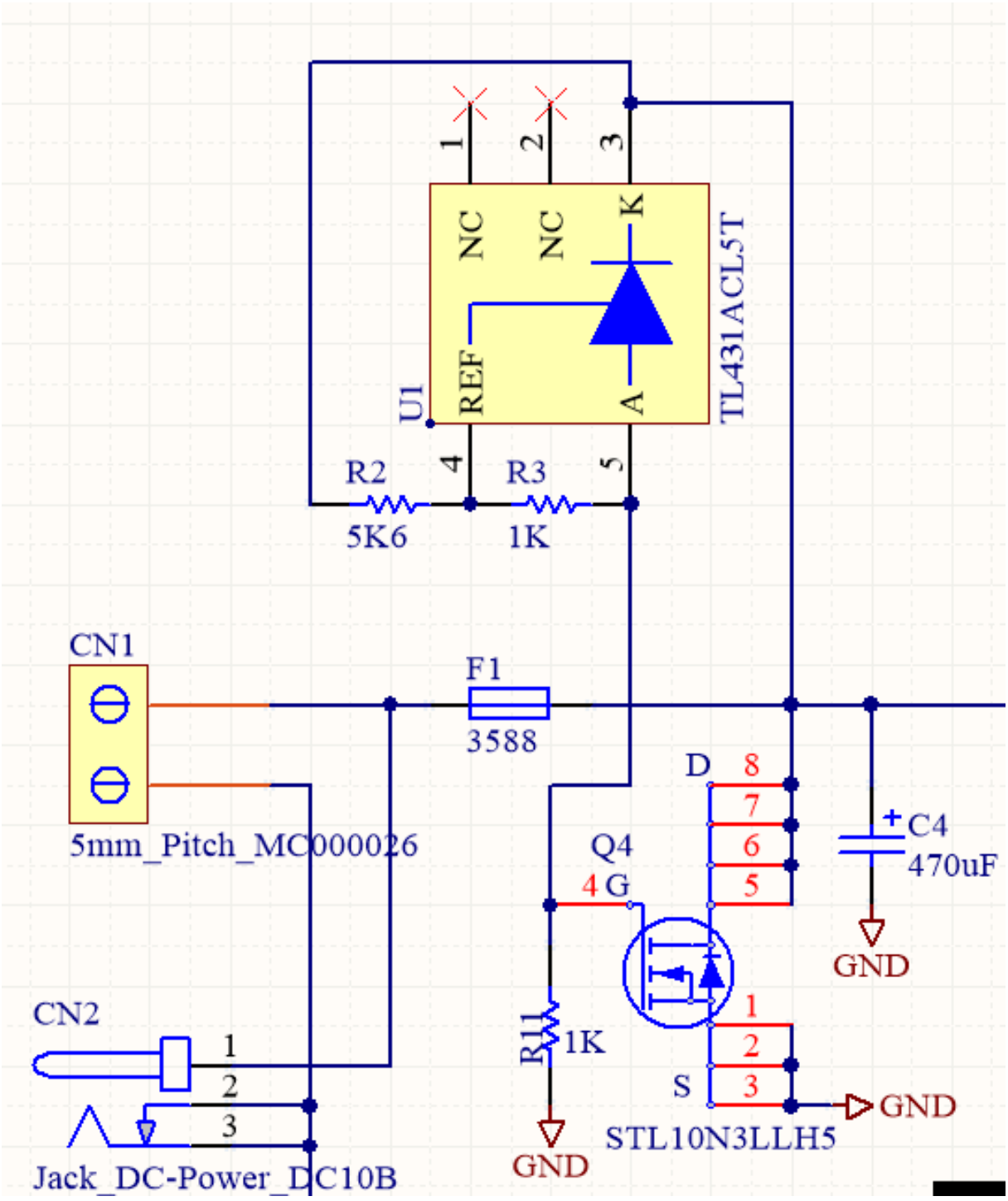
DC input

Overvoltage and undervoltage protections are implemented thanks to the `DCDC_InVoltageCheck()` routine. If the input voltage goes under/above a predefined threshold, the LLC DC/DC converter is turned OFF. See the below compiler option in the file “DCDC_Fault_Processing.c”:

```
#define IN_VOLTAGE_HYSTERESIS
#define IN_VOLTAGE_MAX_H
#define IN_VOLTAGE_MAX_L
#define IN_VOLTAGE_MIN_L
#define IN_VOLTAGE_MIN_H
```

Note: A hardware overvoltage protection (U1/Q4) has been added in order to short circuit the DC input whenever the external power supply voltage goes above 15 V. It protects the complete board against wrong/unintentional setup, and prevents, for example, applying voltages above the maximum MOSFETs Vgs.

Figure 15. **DC in overvoltage protection: short circuit applied by MOSFEST Q4 whenever the input goes above 15 V**



13 Operations

The LLC project offers different modes of operations and compiler options:

- Overcurrent protection
- Over/undervoltage protections
- Secondary synchronous rectification ON/OFF
- Fixed timings or standalone secondary rectification by MOSFET drain voltage monitoring
- Burst mode enabled/disabled
- Short circuit protection

The corresponding compiler definitions can be enabled (1) or disabled (0) in the header file “main.h”:

```
#define OVERCURRENT_PROTECTION 1
#define OUT_OVERVOLTAGE_PROTECTION 1
#define IN_OVER_UNDER_VOLTAGE_PROTECTION 1
#define SYNCH_RECTIFICATION 1
#define USE_COMP_DAC_SECONDARY_RECTIF 1
#define OUT_VOLTAGE_BURST_MODE 1
#define SHORT_CIRCUIT_PROTECTION 1
```

13.1 Push buttons

The board comes with one blue hat B2 button (user) and one black hat B1 button (reset), which function similarly to those embedded on the Nucleo board.

13.2 LEDs

Four LEDs allow the monitoring of the DC/DC stage:

- The red LED LD7 indicates the error status.
- The green LED LD5 indicates the idle/run status: steady state stands for ‘idle’, while blinking indicates that the PSU is running.
- The orange LED LD6 is not used.
- The BLUE LED LD4 indicates that the automatic load management is running.

13.2.1 Red LED

The red LED LD7 number of blinking indicates the error status:

Table 3. Red LED status and meaning

LED behavior	Status
Repeat/blinks one time	Overvoltage
Repeat/blinks two times	Short circuit
Repeat/blinks three times	Overcurrent
Repeat/blinks four times	DC input over/undervoltage

13.2.2 Green LED

The green LED LD5 indicates the DC output status:

Table 4. Green LED status and meaning

LED behavior	Status
Steady state ON	Idle, no DC output.
Blinking constantly	• DC/DC converter running or • Combined with the red LED. The DC/DC converter is OFF and is waiting for user error acknowledgment.

13.2.3 Blue LED

The BLUE LED LD4 indicates that the automatic load management is running:

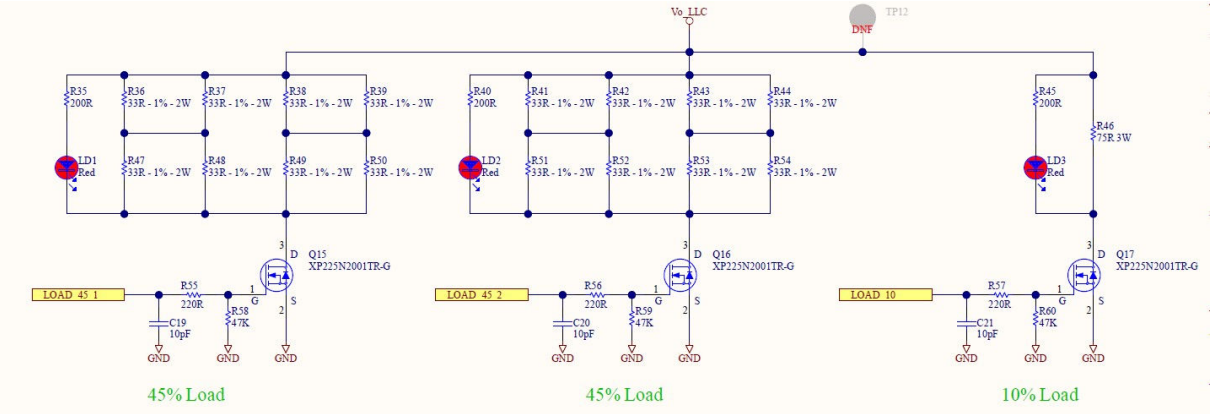
Table 5. Blue LED status and meaning

LED behavior	Status
OFF	The automated load management is not running.
Steady state ON	The automated load management is running.

13.2.4 Dummy loads

The LLC board is equipped with three networks of dummy load resistors able to load the 7.5 V DC output with 10%+45%+45% for a total power dissipation of 7.5 W(+ 0.25 W per LED status LD1 to LD3) as shown in the graphic below. These loads are selected through the GPIOs PC12 PC10 PD2.

Figure 16. Dummy load network resistors



14 Load management

During runtime (DC/DC converter running), the automatic load management can be enabled/disabled by a long push onto the B2 user button. The number of steps, the different load values at any steps, and the delay in between the steps can be modified in the 'InitControlParameters' routine. A mix of 0 %, 10 %, and 45 % loading can be achieved.

Here after is the declaration of the structure in the 'app_dpower.c' file:

```
LoadManagement.LOAD_Delay_ms_in_between_steps = LOAD_NEXT_STEP_TEMPO_MS;

// combinaison of LOAD_10_PERCENT LOAD_1_45_PERCENT LOAD_2_45_PERCENT
LoadManagement.LOAD_STEPS[0] = LOAD_10_PERCENT;
LoadManagement.LOAD_STEPS[1] = LOAD_10_PERCENT | LOAD_1_45_PERCENT | LOAD_2_45_PERCENT;
LoadManagement.LOAD_STEPS[2] = LOAD_10_PERCENT;
LoadManagement.LOAD_STEPS[3] = LOAD_10_PERCENT | LOAD_1_45_PERCENT;
LoadManagement.LOAD_STEPS[4] = LOAD_10_PERCENT | LOAD_1_45_PERCENT | LOAD_2_45_PERCENT;
LoadManagement.LOAD_STEPS[5] = LOAD_NULL;
```

The `LOAD_STEPS[10]` contains the definition of up to 10 steps with the possibility to define a combination of `LOAD_NONE/LOAD_10_PERCENT/LOAD_1_45_PERCENT/LOAD_2_45_PERCENT` in order to enable/disable the dummy resistors connected onto the DC output voltage of the DC/DC converter. At every step, a delay of `LOAD_NEXT_STEP_TEMPO_MS` is applied. If the `LOAD_NULL` condition is reached, the process restarts from the first step (`LOAD_STEPS[0]`).

Figure 17. **B2 user button to enable/disable automatic load stepping**

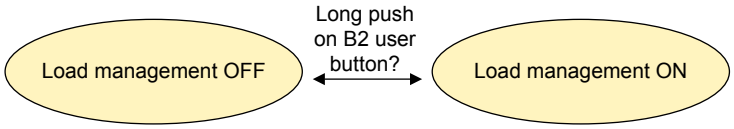


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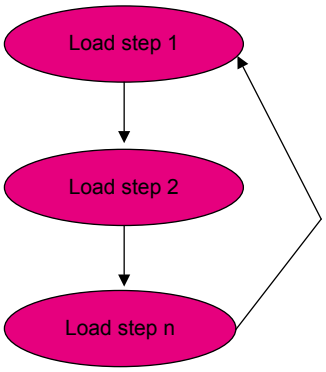
Figure 18. **Load step management state machine**



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15 Captured waveforms, soft start, and bode diagram

In this chapter, some waveforms have been captured to illustrate the LLC operation under different conditions. The first setup is in max loading condition. A zoom on the ZVS and ZCS area are shown in the next figures.

Figure 19. Current waveforms at max load under 12 V DC input, primary side

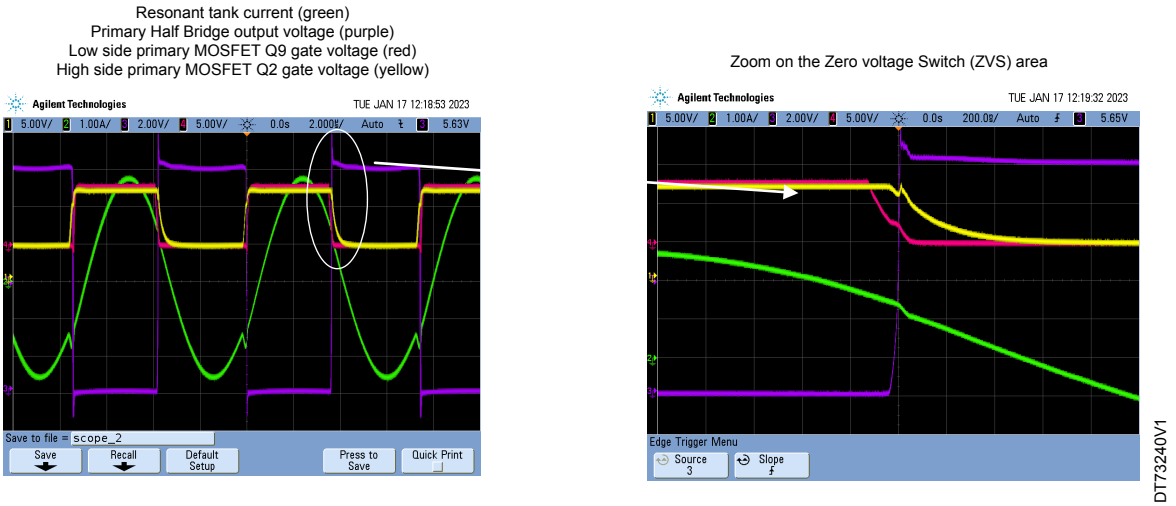

Figure 20. Tank capacitor voltage and primary current at max load under 12 V dc input

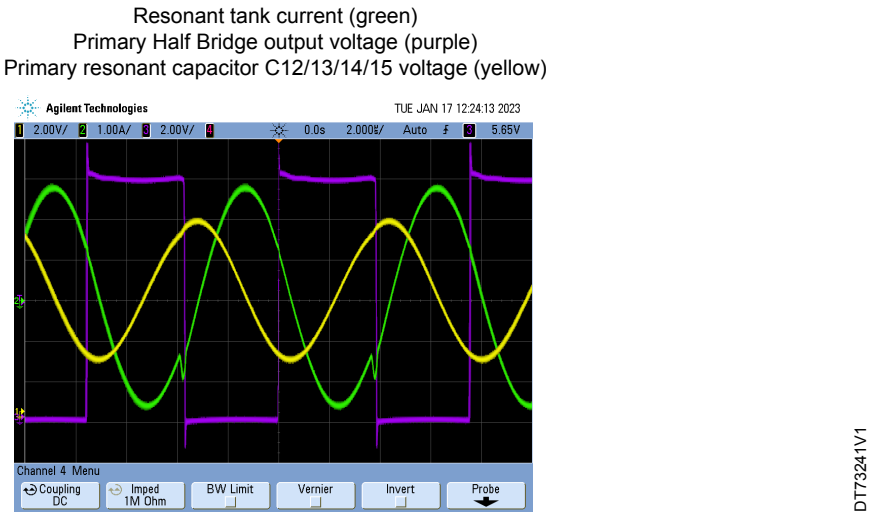

Figure 21. Current waveforms at max load under 11.5 V DC input

Resonant tank current (green)
SR MOSFET Q1/Q11 current through (yellow and purple)

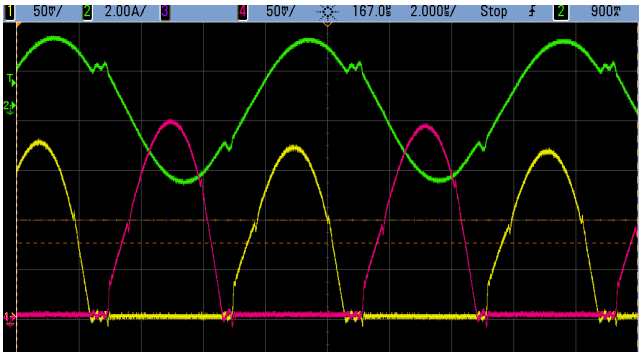

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Figure 22. Current waveform at max load under 12 V DC input, secondary side, secondary, ZCS switch area

SR MOSFET Q1/Q11
current through (yellow and green)
SR MOSFET Q1/Q11 gate voltages (purple and red)

Zero Current Switch (ZCS) area

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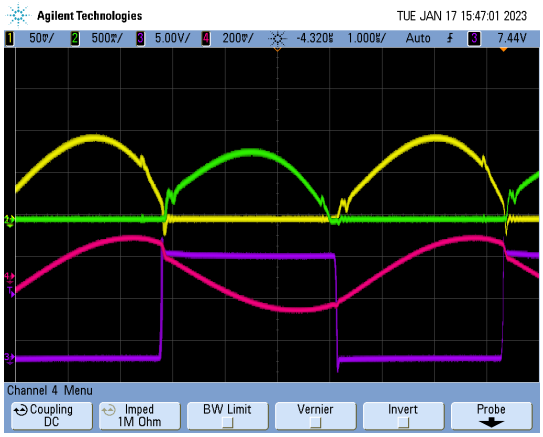
Figure 23. Waveform at 55% load under a 11.5 V DC input

Resonant tank current (red)
Primary Half Bridge output voltage (purple)
SR MOSFET Q1/Q11 current through (yellow and green)



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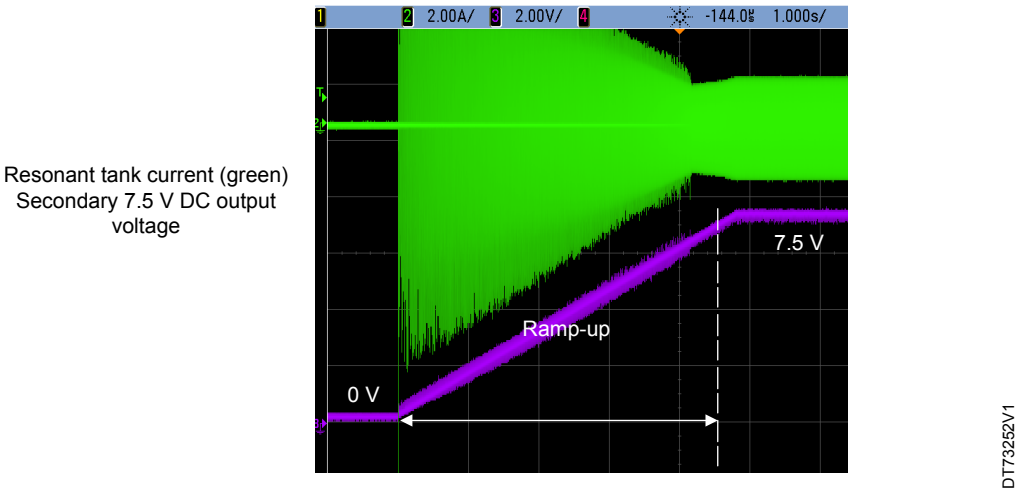
16 Soft start

At startup, a soft start is applied with a ramp-up of the voltage output. See the function `CNTRL_RampFloatConfig()` in the ‘dpwr_cntrl.c’ file to et up the ramp-up time from 0 V to nominal voltage . During the ramp-up, the target voltage of the PI(D) loop is increased following a linear curve as depicted in the figure below.

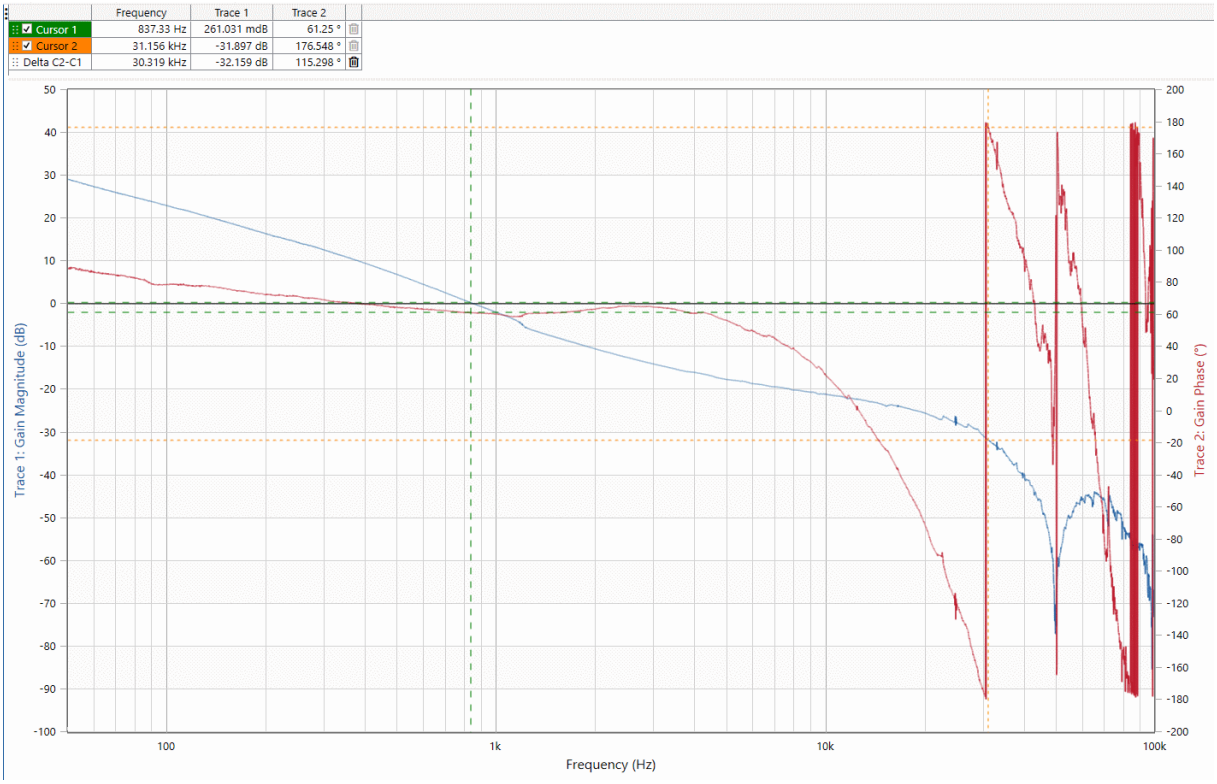
Figure 24. Focus on the soft start (55 % load)



17 Bode diagram response

The DC/DC converter has been tested with a bode tracer in order to characterize the gain and phase shift over 50 Hz-100 kHz (Figure 29). With the PI loop Kp gain set to 45.0 and the Ki gain set to 8.0, a cross over frequency of 800 Hz is obtained with a phase margin of 60 degrees, and a gain margin around 30 dB.

Figure 25. Bode diagram



18 Conclusion

This example around the STM32F334xx and the STM32G474xx advanced Arm®®-based 32-bit MCUs highlights some of the benefits of these microcontrollers and especially the embedded high-resolution timer mainly designed for digital power conversion applications. It includes a very high range of settings that makes this LLC converter application example easy to evaluate and adapt to any LLC topology converters. It also demonstrates the ability to control dynamically the secondary side with adaptive synchronous rectification signals thanks to the embedded analog comparators and DAC output linked directly to the high-resolution timer peripheral.

19 Reference documents

[0] Getting started with STM32 Nucleo board software development tools

These documents are available on STMicroelectronics web site (http://www.st.com).

Before installing and using the product, Accept the Evaluation Product License Agreement from http://www.st.com/epla.

For more information on the STM32F334/STM32G474 Nucleo boards and for demonstration software, visit https://www.st.com/en/evaluation-tools/stm32-nucleo-boards.html.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
26-Sep-2023	1	Initial release.

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