AN5984

Application note

Layout recommendations for the design of boards with the ST25R200 device

Introduction

This application note provides necessary information for the design of boards featuring the ST25R200 device. It gives important information and guidelines to properly implement ST25R200 ground handling, layout, and decoupling capacitor placement. Additional chapters explain mechanisms to mitigate unwanted emissions and to keep the overall noise floor to a low-level. This document is based on the ST25R200 device, but its content applies to ST25R100 as well.

Table 1. **Applicable products**

Type	Product
ST25 NFC / RFID Tags and Readers	ST25R200, ST25R100

1 Acronyms

Table 2. **Acronyms and abbreviations**

Acronyms	Definitions
AGND	Analog GND
DGND	Digital GND
EMC	Electro magnetic compatibility
EMI	Electro magnetic interference
EUT	Emitter under test
ESD	Electro static discharge
GND	Ground (reference) level for voltages
IC	Integrated circuit
PCB	Printed circuit board
RFI	Radio frequency input
RFO	Radio frequency output
USB	Universal serial bus
XTAL	Crystal oscillator

2 General recommendations

In PCB design there are guidelines to optimize EMC performance:

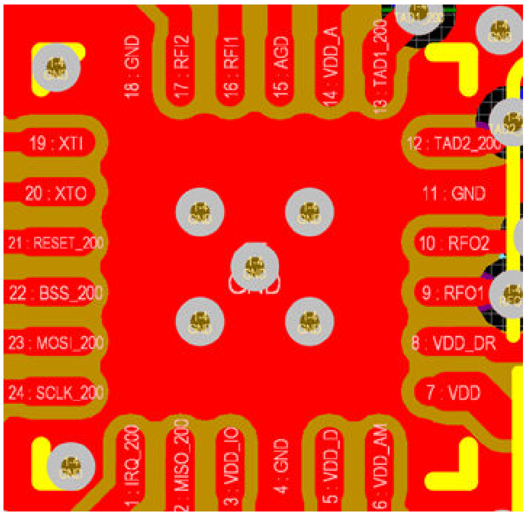
- Always consider and determine where and how the return currents are flowing.
- Do not route signals over ground gaps.
- Partition mixed-signal PCBs with separate analog and digital sections
- Do not split the current return plane; use one solid plane under both analog and digital sections of the board.
- Route digital signals only in the digital section of the board (for all digital related layers).
- Route analog signals only in the analog section of the board (for all analog related layers).
- In case ground or power planes are split for a specific reason (that is, mechanical and or electrical), do not run any traces across the split on an adjacent layer.
- Traces (analog or digital) that must go over a power plane split must be on a layer adjacent to a solid ground plane (analog or digital).
- A/D and D/A converters, as well as most other mixed-signal ICs, should be considered as analog devices with a digital section, not digital devices with an analog section.
- The AGND and DGND designation on the pins of a mixed signal IC refers to where the pins are connected internally, and it does not imply where or how they should be connected externally. On most mixed-signal ICs, both the AGND and DGND pins should be connected to the analog return plane.
- The digital decoupling capacitor should be connected directly to the digital ground pin.
- The decoupling capacitors are needed to supply, through a low-inductance path, some or all of the transient power supply current required when an IC logic gate switches.
- Decoupling capacitors are needed to short out, or at least reduce the noise injected back into the power ground system.
- Decoupling is not the process of placing a capacitor adjacent to an IC to supply the transient switching current; rather it is the process of placing an L-C network adjacent to the IC to supply the transient switching current.
- The value of the decoupling capacitor(s) is important for the low-frequency decoupling effectiveness.
- The value of the decoupling capacitor(s) is not important at high frequencies. At high frequencies, the most important criteria is to reduce the inductance in series with the decoupling capacitors.
- Effective high-frequency decoupling requires the use of a large number of capacitors.
- Place decoupling capacitors as close as possible to the device.
- Route RFI and RFO signals symmetrically, and avoid long signal traces for the matching network. Keep the traces between RFO1 and RFO2 close to each other, and do the same for RFI1 and RFI2.
- The matching components need be placed close to each other, and symmetrically.
- Care needs to be taken on the quartz crystal oscillator (XTAL) placement and startup behavior. Long connections to the XTAL may cause negative effects on the system by adding parasitic capacitances, be more prone to the influence of external signals/noise and impair the startup behavior.

3 ST25R200 device specific layout requirements

ST25R200 exposed pad

The exposed pad/thermal pad called VSS underneath the ST25R200 provides both a ground plane and a thermal heat sink. This pad must be connected to the PCB ground plane by multiple through-vias and must be plated to have good soldering results. The multiple vias keep the total parasitic inductance in this area low.

Figure 1. Exposed pad top view and recommended GND layout



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ST25R200 GND pins connection and routing

The ST25R200 device has 3 GND pins.

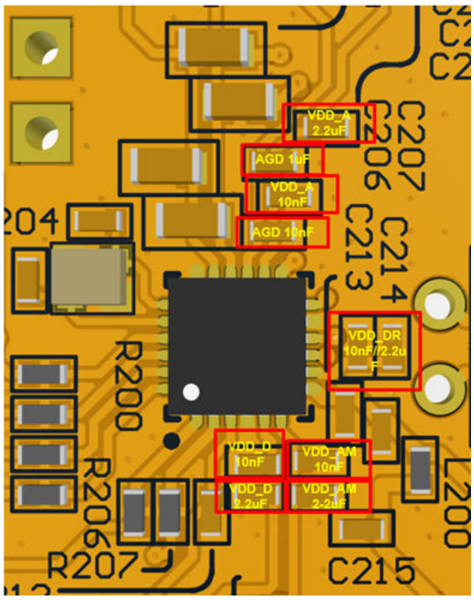
- GND_D (Pin4)
- GND_A (Pin18)
- GND_DR (Pin11)

All three GND pins must be directly connected to the exposed pad in the shortest way from the pad to the center. A PCB trace width of at least 0.2 mm connecting the GND pins must be regarded. A recommended layout example is shown in the figure above. Furthermore, the GND pins and the remaining corners of the exposed pad should be connected to a solid GND plane on the same layer.

Decoupling capacitors

All capacitors associated with the ST25R200 regulators and AGD voltage pins (VDD_D, VDD_AM, VDD_A, VDD_DR and AGD) must be positioned as close as possible to the device. A recommended distance of less than 3 mm for VDD_DR and VDD_AM between the ST25R200 pins and the capacitor should be regarded. An example placement of decoupling capacitors is depicted in the figure below.

Figure 2. **Decoupling capacitors placement example**

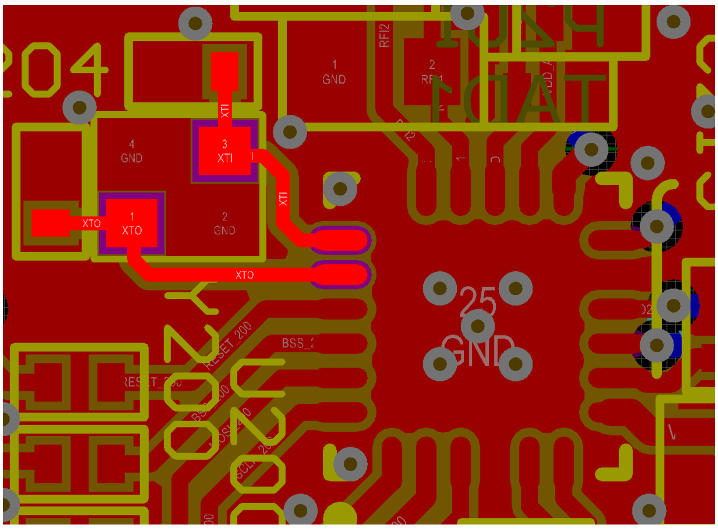


Crystal Placement

In a similar way to the decoupling capacitors, the XTAL must be positioned as close as possible to the XTI/XTO pins.

In order to avoid crosstalk from other other signals (for example, XTO <-> RESET), those PCB traces must be separated by a GND area.

Figure 3. **XTAL placement example**



4 Basic considerations

Most of the signals generated by ICs are in the form of periodic square wave signals (Figure 4), with a spectrum similar to the one shown in Figure 5.

Figure 4. Square wave

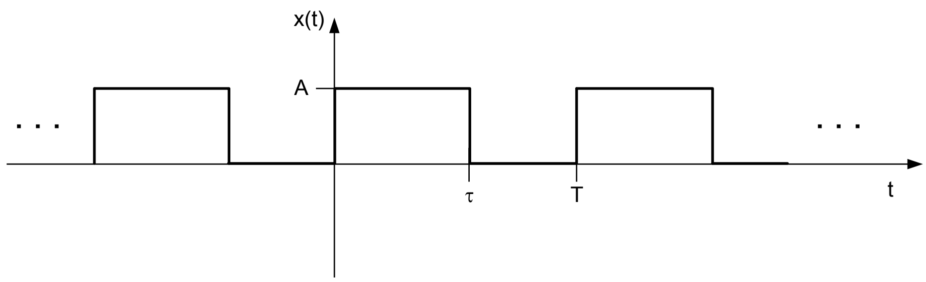
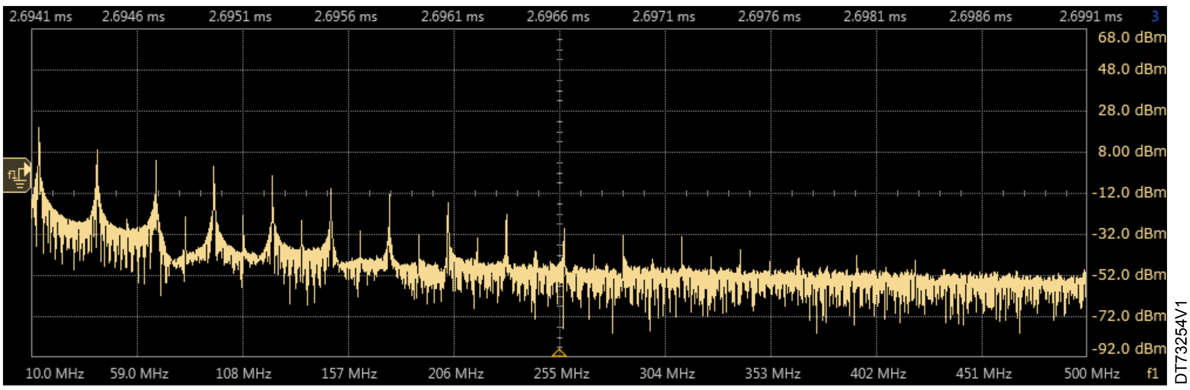
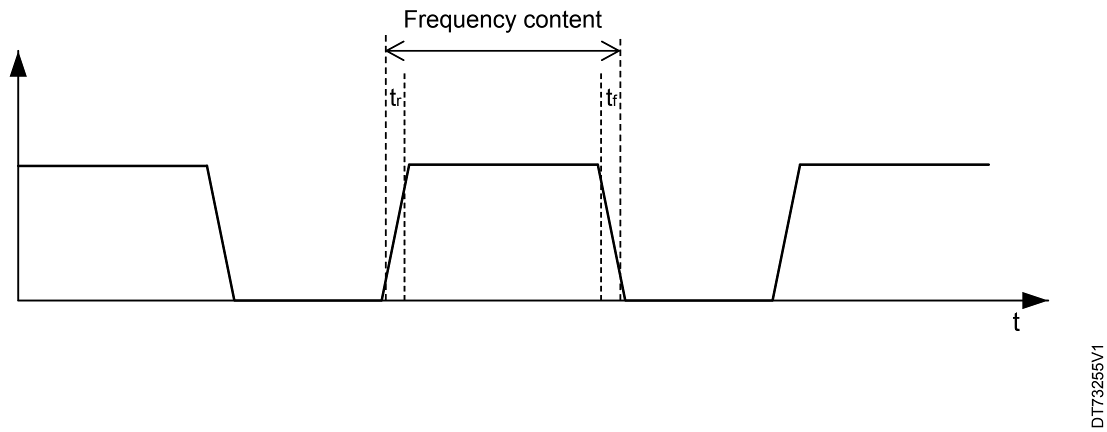


Figure 5. Spectrum of a square wave



As an ideal square wave cannot be generated in real devices, we have to deal with trapezoidal pulses from ICs or clocks, with finite slew rise and fall times (Figure 6). The amplitude of the higher frequency harmonics depends on the rise and fall times of the signal, dropping with longer rise times.

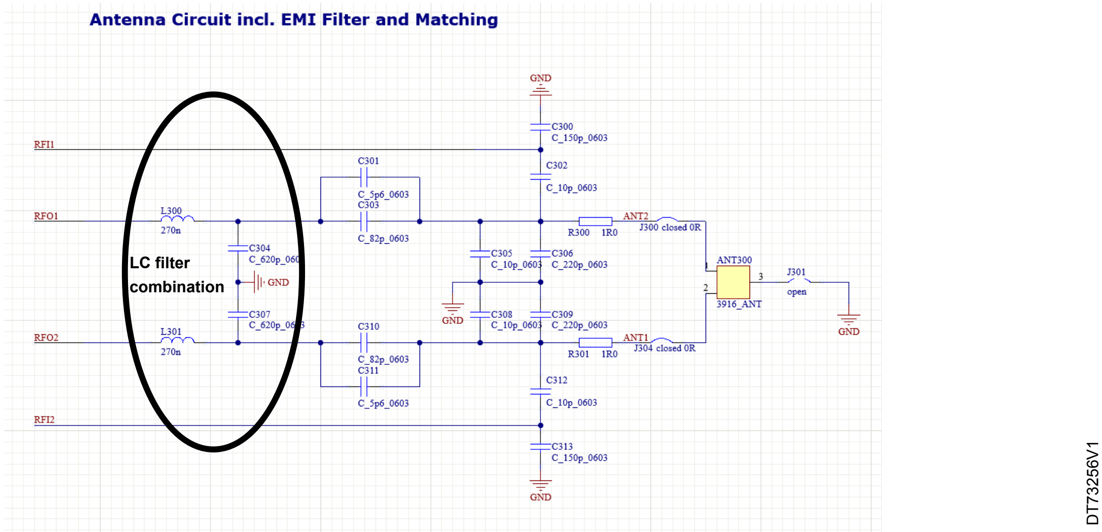
Figure 6. Trapezoidal wave



The generated RF signal at RFO1 and RFO2 is a rectangular shaped signal, which must be fed into an antenna matched LC tank for a proper RF communication. The RFOs are low pass filtered with an inductance/capacitance combination to reduce harmonics.

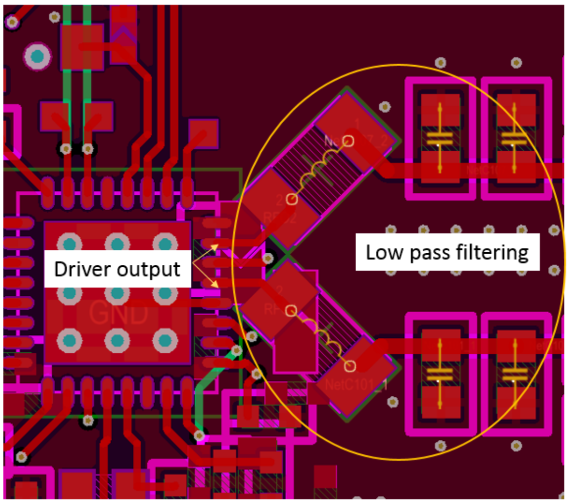
This is accomplished by an LC combination at the output of the RF drivers, as shown in the figure below.

Figure 7. Low-pass filtering



It is important to position the filter network as close as possible to the output stages (as in Figure 8), to avoid unwanted radiation over long traces.

Figure 8. Position of the low-pass filter on the PCB



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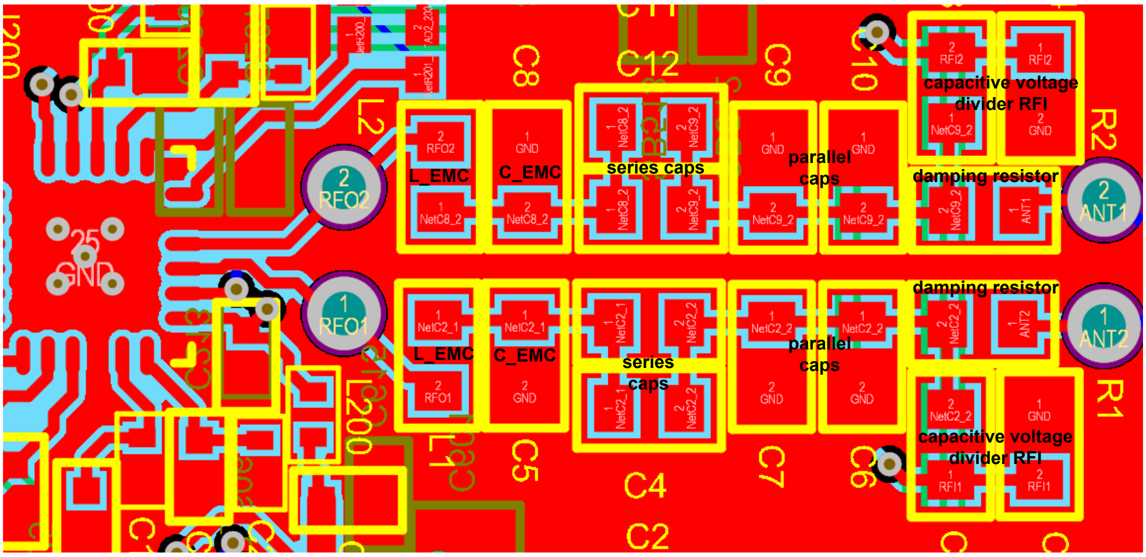
5 Radiation from traces

One of the sources of radiation can be identified in the exposed traces. To understand how traces radiate, the signals must be analyzed during their propagation. A signal propagating along traces can be divided into two main parts, namely a differential signal and a common mode signal.

5.1 Differential signals

The total radiated field from a differential signal propagating along two traces tends to cancel itself, and in ideal conditions is zero. The same effect applies to the output drivers of ST25R200, which are operating in differential mode. However, due to component tolerances and signal asymmetries along the traces, differences in the current flow may appear and consequently a non “quasi-zero” electric field is generated. Take care to lay out the matching topology in a symmetrical way.

Figure 9. ST25R200 with symmetrical matching layout



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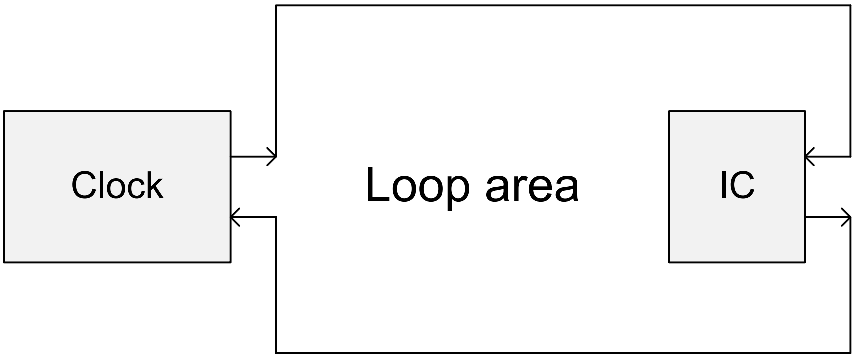
In addition, to control differential-mode radiated emission, it is important to minimize the loop areas (see Figure 10) formed by signal traces and their return current paths. Especially for clock signals, the length needs to be minimized, to form the smallest possible loop areas.

Figure 10. **Loop areas on a PCB**



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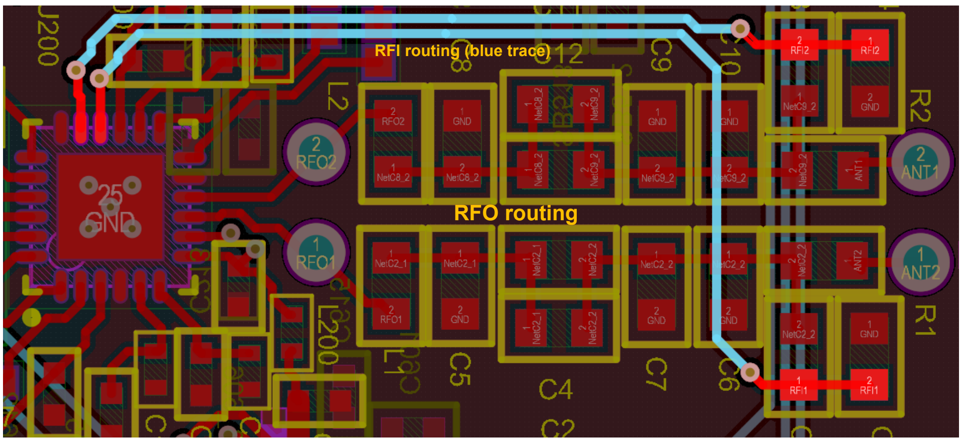
5.1.1 RFO and RFI routing

The transmit and receive stages of the ST25R200 are differential pairs and need to be treated carefully during the PCB layout to minimize unwanted signal coupling and radiated emissions. These signals should be routed in an internal layer, but to avoid a large number of vias interconnecting the traces with the matching components, the complete matching network is placed on one side (the top layer) of the PCB. The return current flows under the traces in the GND layer. It is important to have no cuts in the GND layer below the matching circuit.

Figure 11. **Routing of matching network**



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It is essential to avoid so called through-vias in the matching layout, because they only contribute to unwanted emissions. Note how the matching components are close to each other to reduce the trace length from RFO to the antenna feed. It is not advised to have long signal traces between the LC filter and the remaining matching components. The inductors after the RFO should be positioned side by side or in 45 degree relation to each other depending on the coil technology to minimize coupling effects.

The RFI lines are routed symmetrically, at a reasonable distance from the RFO lines. The receive signals are decoupled from the middle point of the matching network and crossing the series capacitance where the carrier signal is relatively low. Never route the RFI signals separated from each other, and do not use different signal lengths.

Alternatively, the RFI lines can be routed through the middle of the matching network back to the RFI pins.

Additionally, all the components (capacitors) to GND along the RFO path are connected to GND by using multiple vias to minimize inductance, and consequently avoid unwanted resonances.

5.2 Common-mode signals

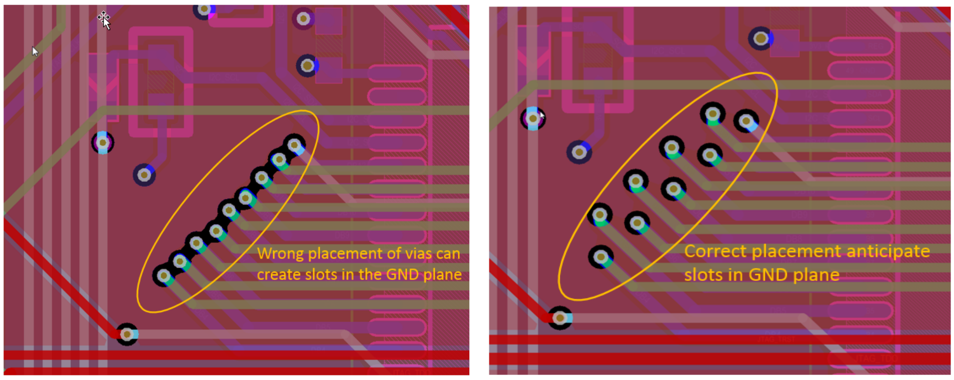
Common-mode radiation mainly emanates from the connected cables of a PCB system.

The PCB reference ground plane inductance (and consequently the ground voltage) is the major contributor to the common-mode radiation. Common-mode radiation is produced more effectively than differential mode radiation. Even a small amount of common-mode current can result in significant emission problems.

To reduce common-mode emissions:

- Keep the current supply path close to the current return path.
- Reduce the cable length.
- Minimize the common-mode voltage (usually the ground potential). Reducing the ground impedance can be done by using solid ground planes or ground grids, and by avoiding slots in the ground plane (see the differences in Figure 10).

Figure 12. Avoiding slots in the GND plane



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Take care of connected cables (if any), and shield them properly. This can be done, for instance, using common-mode impedance choke in series with the cable, with some isolation between connections from the enclosed cable to the PCB ground.

An integrated common-mode filter (ECMF02-4CMX8) for USB D+ and D- lines and ESD protection for all lines can be used, as exemplified in Figure 11 and Figure 12. Avoiding slots in the GND plane, showing, respectively, the position on the PCB and the schematic.

Figure 13. **Common mode filter - Position on the PCB**

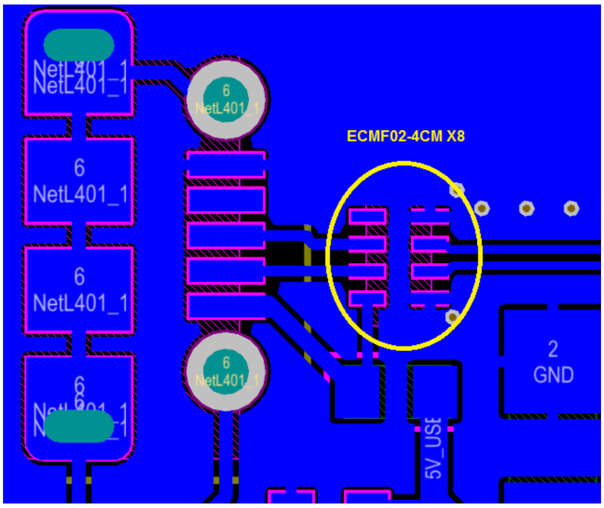

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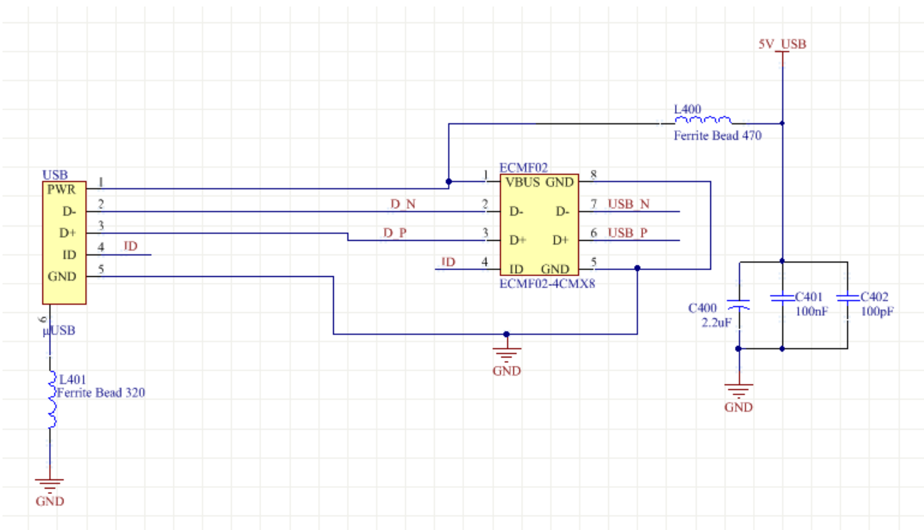
Figure 14. **Common mode filter - Schematic**



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5.2.1 SPI data signal routing

The SPI data signals from the ST25R200 to the MCU must be routed (as much as possible) with equal length and controlled impedance.

Keep the trace length of the SPI interface short and minimize the use of vias.

Avoid routing the SPI signals over crystal oscillators (such as those generating the 27.12 MHz or 13.56 MHz frequencies), to minimize crosstalk and signal distortion.

6 Parasitic components and current return paths

During the PCB design, attention must be paid to the selection of passive components and their parasitic contribution.

Most of the time component manufacturers provide measured values only at low frequency, or in a frequency range not compatible with the one used in the PCB being designed. It is then critical for a designer to know the exact value and the parasitics within the whole considered frequency range for each passive component used in the design to avoid undesired system resonance that may lead to unintentional radiating effects.

Together with the parasitic effect, the current return path on the PCB must be evaluated.

All currents return to their source: they flow in loops, and the return path has a large impact on radiated emissions. Note that currents returning to the source follow different paths, depending upon the frequency: the path with the lowest resistance is the preferred one at low frequencies, the path with the lowest inductance prevails in the high frequency range.

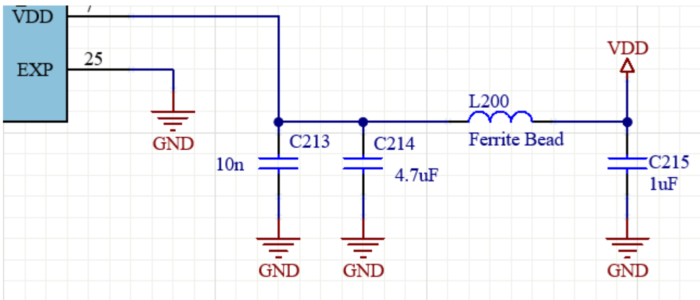
To understand return path resistance, it is important to calculate the impedance of a stripline and of a microstrip in the PCB, to identify paths with high and low impedance.

7 Power supply filtering

External noise may be injected into the system via the power supply, and, similarly, internal noise may be conducted off of the board on the DC power leads. It is advised to put in place filters in the PCB power supply system design to reduce the effect of noise and transients on the lines. Both common and differential mode filtering are applied on the PCB.

The power supply filter of the ST25R200 VDD pin can be formed by a PI filter. Typical values for capacitors range from 1 to 0.01 μF, and for the ferrite bead the typical resistance value varies from 50 to 1500 Ω in the frequency range of interest. Avoid saturation of ferrite bead by DC current.

Figure 15. Detail of power supply schematic



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8 Mixed signal PCB layout

When a designer faces the design of a mixed signal system, the main question that comes in the PCB layout definition is related to the separation of the analog and digital parts, and consequently on how to handle the separation of ground between the two subsystems.

The origin of the split GND approach comes from the need to keep separated return currents for analog and digital subsystems. The separation between the two subsystems can be achieved by a physical separation of the two grounds (real cut) or by a spatial separation of them. When using more than one mixed signal IC with common GND connections for analog and digital signal the approach of having separate grounds may cause more issues compared to a single GND configuration.

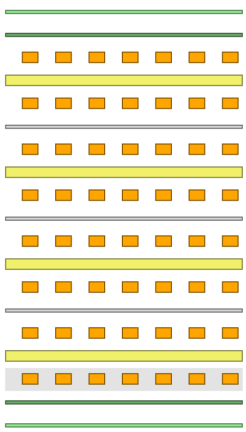
In this case it is recommended to use only one current return plane, paying attention to partition the PCB area into digital and analog sectors; route analog and digital signals only in the analog and digital sector, respectively, to keep the return current paths separated.

The use of a split GND plane can create other problems because of the presence of possible multiple return paths of the supply current, and consequently of possible current loops. The supply current must return through a common ground terminal to which both the analog and the digital sub subsystem are referenced. The presence of the current loop generates radiated emission, with the emission level being proportional to the loop area and to the current intensity.

A typical configuration of an 8-layer PCB implementing a full separation between analog and digital parts of the system is shown in Figure 16. In this configuration the analog components are placed on the top layer of the PCB, and the digital ones are located on the bottom layer.

Figure 17 shows a 4-layer PCB stack up configuration. Signals are routed on the top and bottom layer. The inner layers are composed of a separate GND and power supply layer.

Figure 16. Vertical separation between analog and digital signals



Layer Name	Type	Material
Top Overlay	Overlay	
Top Solder	Solder Mask/Coverl...	Surface Material
Component Side - ANALOG	Signal	Copper
Dielectric1	Dielectric	Core
Ground Plane 1 (GND) - ANALOG	Signal	Copper
Dielectric2	Dielectric	Prepreg
Inner Layer 1 - ANALOG	Signal	Copper
Dielectric 6	Dielectric	Core
Power Plane (VRF) - ANALOG POWER	Signal	Copper
Dielectric5	Dielectric	Prepreg
Power Plane (VCC) - DIGITAL POWER	Signal	Copper
Dielectric 7	Dielectric	Core
Inner Layer 3 - DIGITAL	Signal	Copper
Dielectric4	Dielectric	Prepreg
Ground Plane 2 (GND) - DIGITAL	Signal	Copper
Dielectric3	Dielectric	Core
Solder Side - DIGITIAL	Signal	Copper
Bottom Solder	Solder Mask/Coverl...	Surface Material
Bottom Overlay	Overlay	

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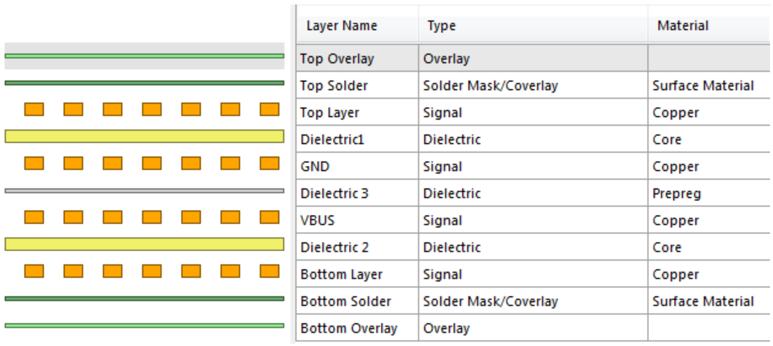
Figure 17. **4-layer PCB configuration**



Layer Name	Type	Material
Top Overlay	Overlay	
Top Solder	Solder Mask/Coverlay	Surface Material
Top Layer	Signal	Copper
Dielectric1	Dielectric	Core
GND	Signal	Copper
Dielectric 3	Dielectric	Prepreg
VBUS	Signal	Copper
Dielectric 2	Dielectric	Core
Bottom Layer	Signal	Copper
Bottom Solder	Solder Mask/Coverlay	Surface Material
Bottom Overlay	Overlay	

DT73265V1

9 Conclusion

Many of the EMC problems and operational pitfalls that impact the design of high power RF systems can be avoided following the guidelines illustrated in this document.

Care has to be taken especially on signal routing, and on which PCB layer the signals are placed.

PCB stack-up, placement of components, handling of multiple DC voltages, current return path and via placement must always be an integral part of the board design. The achievement of the required performance is often linked to an optimized PCB layout.

Revision history

Table 3. **Document revision history**

Date	Version	Changes
4-Sep-2023	1	Initial release.
17-Nov-2023	2	Updated the following information: part number, reference documents.
05-Apr-2024	3	First public release. Information about XTAL added.
30-May-2024	4	ST25R200 added to the document.

Contents

List of tables

List of figures