Data rate and consumption advantages with MIPI I3C interface example using TSC1641

Introduction

MIPI I3C is a standardized bus managed by the MIPI alliance. The MIPI I3C bus offers many advantages and is backwards compatible with legacy I2C:

Table 1. Comparison between I3C and I2C

Feature	I3C	I2C
Number of wires	2 (Data & Clock)	2 (Data & Clock)
Communication speed	12.5 MHz in SDR mode	3.4 MHz in Hs-mode
Bidirectional	Yes	Yes
Pull-up resistors needed	No	Yes
Dynamic addresses	Yes	No
Broadcast communication	Yes	No
In-Band interrupts	Yes	No

This application note compares the consumption and data rates of MIPI I3C and I2C. The analysis is also applied on the TSC1641 AFE (voltage, current, and power monitoring).

Main features of TSC1641:

- 16-bit resolution dual-channel sigma-delta ADC
- MIPI I3C up to 12.5 MHz
- I2C bus interface up to 1 MHz
- 2.7-3.6 V power supply voltage
- 0-60 V load voltage sensing
- Bi-directional current, high-side, or low-side sensing
- Temperature sensor

Note: For detailed information on I3C implementation in the TSC1641 device, refer to application note AN5988 on st.com.

Glossary and acronyms

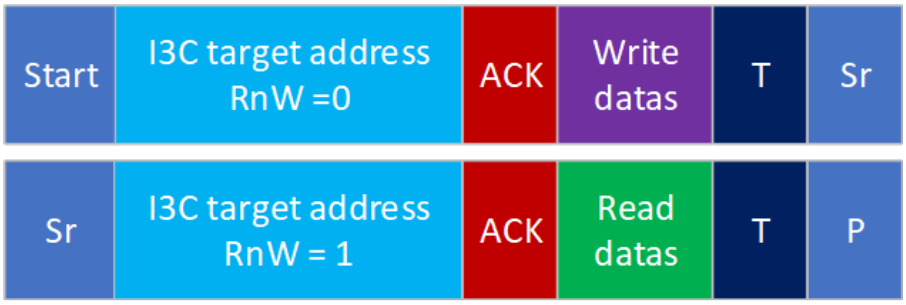
- I3C: MIPI improved inter-integrated circuit interface
- I2C: inter-integrated circuit. Two-wire communication protocol for connecting multiple devices, allowing data exchange and control in electronic systems
- SCL: Clock line
- SDA: Data line

1 Data rate comparison between I3C and I2C

1.1 I3C and I2C frame widths

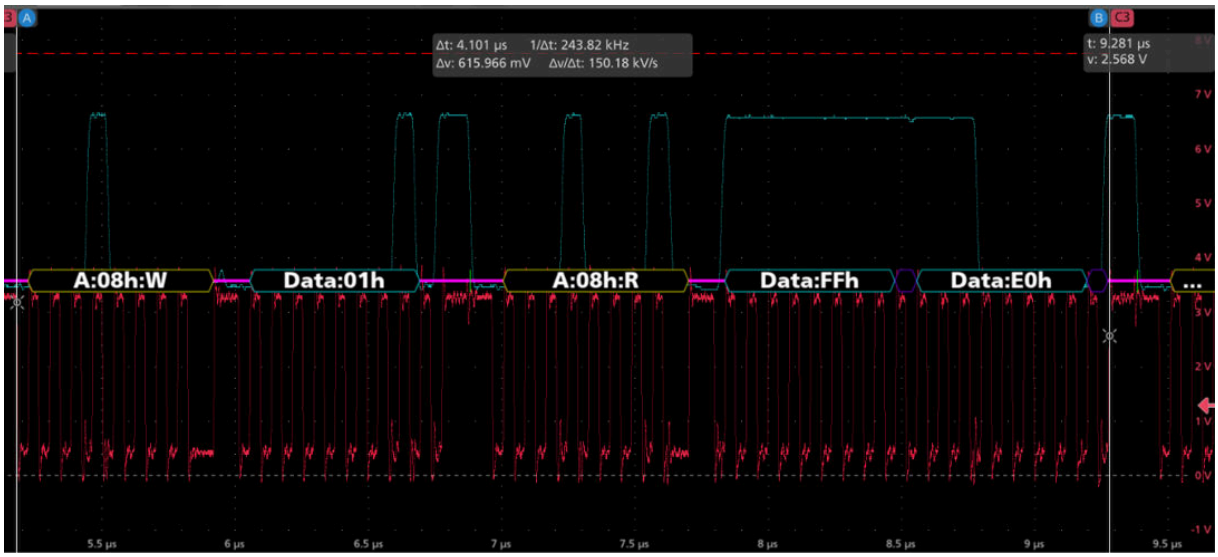
Figure 1. Example of a read transfer in I3C without the 7'h7E Address

ACK: Acknowledge
Sr: Repeated start
T: Transition Bit (end-of-data for read data)
P: Stop condition



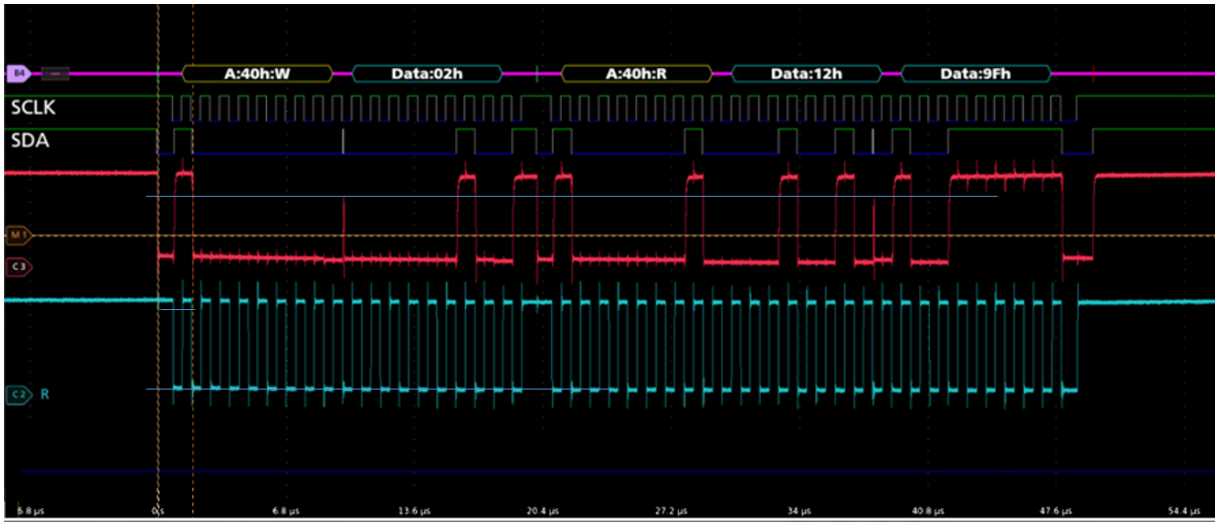
The frame width is only 4.101 µs @12.5 MHz for the detailed frame above.

Figure 2. Frame width for I3C



However, the frame width is about 49 µs in I2C @1 MHz for a read frame.

Figure 3. **Frame width for I2C**



1.2 I3C and I2C compatibility on the same bus

I2C spike filter and/or broadcast address 7E of devices allow making I3C traffic invisible for I2C devices.

- Only 2 wires allow communication in I3C and I2C on the same bus.

The spike filter consists of filtering SCL high times below 50 ns, used for I3C communication.

2 Consumption comparison between I3C and I2C

The main difference on consumption is that pull ups are not needed in I3C.

Table 2. TSC1641 consumption with continuous communication in I2C and its pull-up resistors consumption

Vs (V)	2.7	3.3	3.6
Current (mA)	2.33	2.614	2.824

Table 3. TSC1641 consumption with continuous communication in I3C, pull ups removed

Vs (V)	2.7	3.3	3.6
Current (mA)	1.006	1.076	1.113

We see that communicating in I2C double the consumption because of the pull ups.

2.1 Under 3.3V

If we consider a real case with TSC1641: the voltage and current are read every 128 µs.

Table 4. Consumption comparison in real case

Type of consumption	I3C	I2C
Consumption without communication (mA)	1.014	1.014
Consumption of TSC1641 with typical communication (mA)	1.018	2.264
Communication consumption (mA)	0.004	1.25

Communication consumption is decreased by 99.68% in I3C.

3 Conclusion

The frame length is about 49 µs in I2C, while this frame length could become 4.1µs in I3C. When I2C is working, the pull up consumption is higher than the chip consumption. In I3C, pull up can be removed to decrease the communication consumption by 99.68%.

Revision history

Table 5. **Document revision history**

Date	Version	Changes
09-Jan-2024	1	Initial release.

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