50 W converter using HVLED101 quasi-resonant HPF flyback controller with secondary side regulation

Introduction

The EVLHV101SSR50W is intended to provide a stable and insulated 60 V voltage supply for a maximum power of 50 W when a wide range of AC or DC input voltages is applied at its input.

It can be used as a standalone power supply or as a front-end stage in a dimmable (or non-dimmable) offline LED driver.

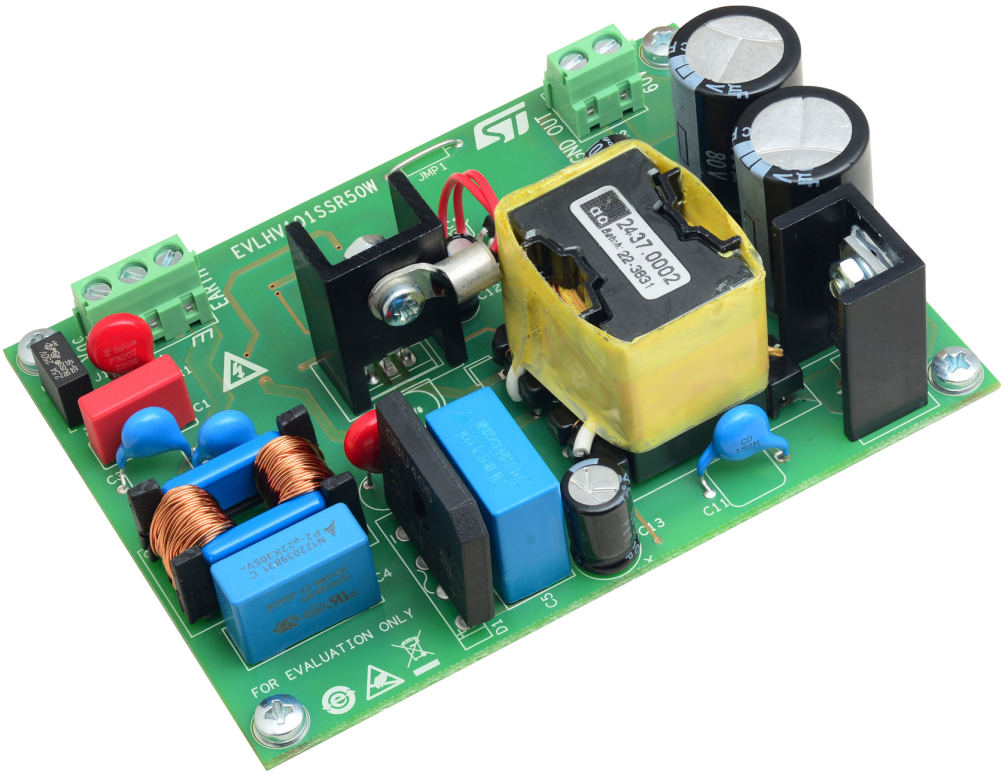
A very high power factor and low THD are achieved by this demonstration board thanks to HVLED101's features. It uses a patented THD optimizer and frequency foldback with a valley locking operation to reduce the switching losses and avoid acoustic noise.

Maximum input power is automatically limited by HVLED101's internal algorithm (MPC), which helps to increase system safety.

Input voltage variations, excessive input voltage (overvoltage like surge or bursts), and insufficient input voltage are managed by HVLED101's protections, which improve the reliability of the application.

Output short-circuit and overload protection with auto-restart behavior is implemented.

Figure 1. **EVLHV101SSR50W evaluation kit (75 x 100 mm)**



1 Main characteristics

- Input voltage: V_{IN}: 90 - 265 V_{RMS}, f: 45-66 Hz
- Output voltage: 60 V / 833 mA
- High power factor, low THD
- PF / THD:
- – >0.99 / < 3% at 115 V_{AC} and 230 V_{AC} @ full load
- – >0.99 / < 4% at 115 V_{AC}, > 0.97 / < 5% @ 230 V_{AC} @ half load
- – >0.99 / < 4% at 115 V_{AC}, > 0.92 / < 7% @ 230 V_{AC} @ 1/3 load
- 4 points (25%, 50%, 75%, and 100% load) average efficiency > 91%
- Efficiency > 50% in stand-by (Pout = 240 mW)
- Frequency foldback with valley locking for noise-free operation
- Startup time < 200 ms
- $T_{AMB-MAX}$ = 60 °C
- Open load voltage limiting (< 65 V)
- Short-circuit protection with auto-restart
- NTC overtemperature protection for switching MOSFET
- Safety Acc. to EN60065
- EMI Acc to EN55022 – conducted emissions
- RoHS compliant

Table 1. Main components

Main components	
HVLED101	Quasi-resonant flyback controller
STF14N80K5	N-channel 800V, 0.400Ohm typ., 12A MDmesh K5 Power MOSFET in a TO-220FP package
STTH16R04C	Ultrafast diode 400V, 4A in TO-220AB package
STTH108A	Ultrafast diode 800V, 1A in SMA package
TL432AIL3T	Adjustable 1% shunt voltage reference

Table 2. Description of connector signals

Con.	Pin	Signal name	Dir.	Description and use
J1	1	Vac	Input	First connection to AC Mains – Warning high voltage
	2	Vac	Input	Second connection to AC Mains – Warning high voltage
	3	EARTH	Earth	Earth connection
J2	1	GND OUT	Output	Ground
	2	60V	Output	60V output (isolated)

Figure 2. **Board connections**

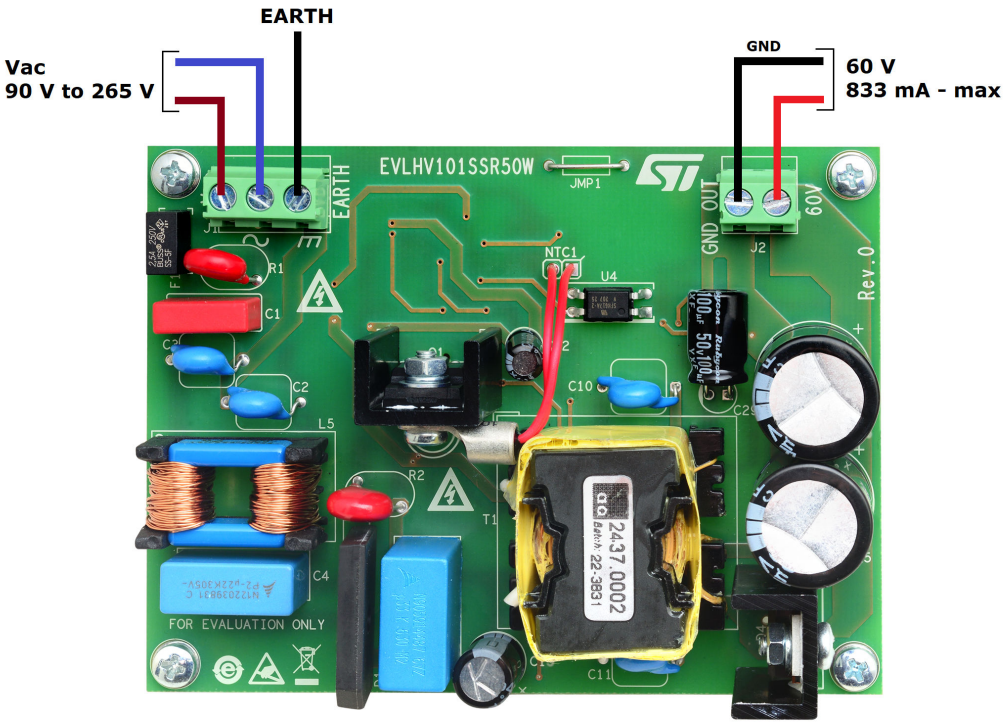


Figure 3. **Schematic diagram**

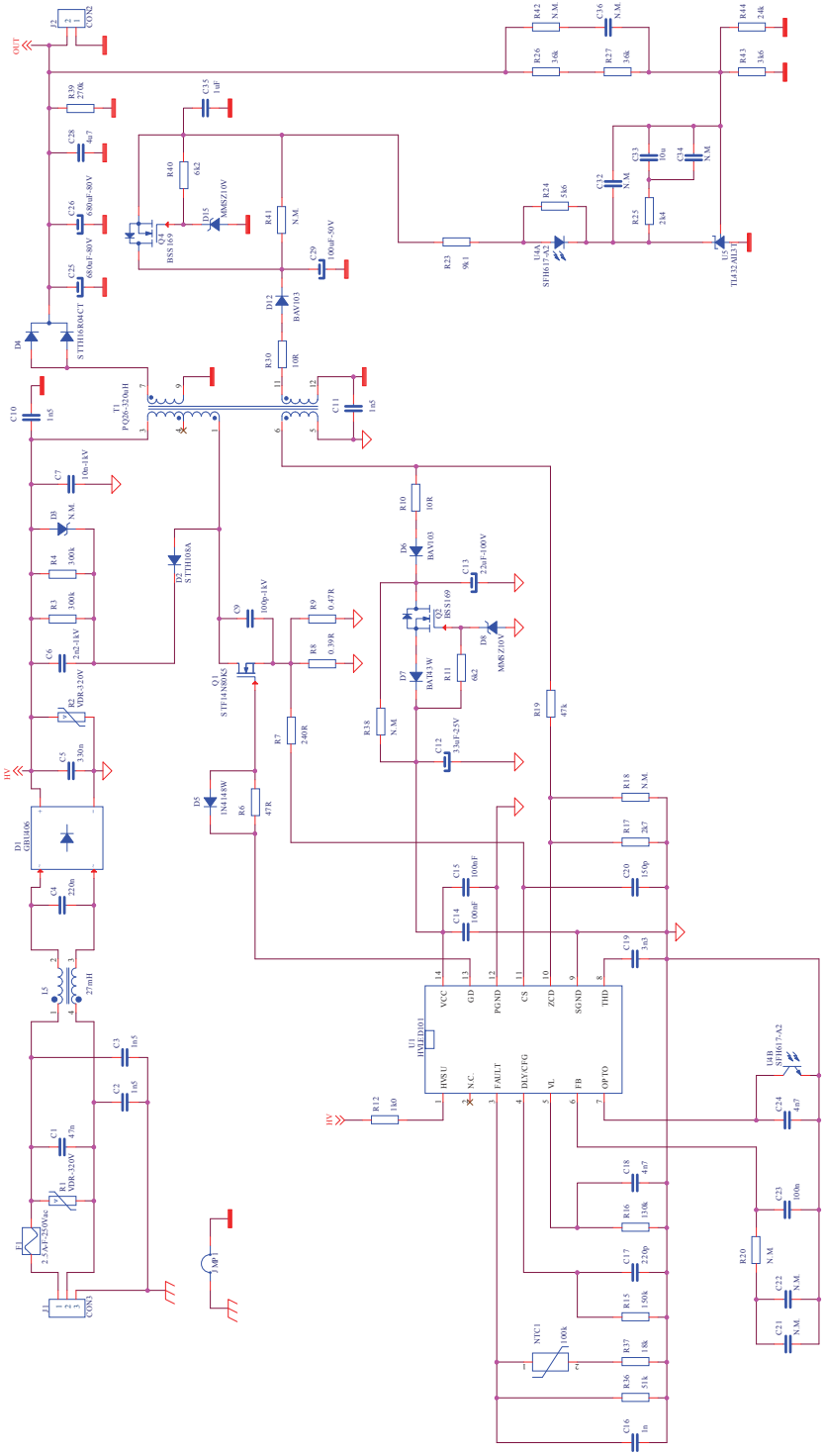


Table 3. List of parts

Item	Q.ty	Ref. Des.	Value - Rating	Description	Manufacturer	Part Number
1	1	C1	47n - 305VAC	X2 film capacitor 305VAC (MKP)	Wurth	890334023015CS
2	2	C2, C3	1n5	X1-Y2 ceramic capacitor 440-300VAC CS series	TDK	CS75ZU2GA152MANKA
3	1	C4	220n - 305VAC	X2 film capacitor 305VAC (MKP)	TDK	B32922C3224K
4	1	C5	330n	Polypropylene film capacitor 630VDC-310VAC	TDK	B32672Z6334K000
5	1	C6	2n2-1kV	Multilayer ceramic capacitor X7R 1kV	AVX	1206AC222KAT1A
6	1	C7	10n-1kV	Multilayer ceramic capacitor X7R 1kV	AVX	1812AC103KAT1A
7	1	C9	100p-1kV	Multilayer ceramic capacitor C0G 1kV	AVX	1206AA101JAT1A
8	2	C10, C11	1n5 - 400VAC	X1-Y1 ceramic capacitor 440-400VAC CD series	TDK	CD45-E2GA152M-NKA
9	1	C12	33uF – 25V	Aluminum ELCAP - YXF series- 105°C	Rubycon	25YXF33M5X11
10	1	C13	22u-100V	Aluminum ELCAP - YXF series- 105°C	Rubycon	100YXF22M8X11
11	1	C14	100n - 50V	Cercap P X7R - SMD-0805	---	---
12	1	C15	100n - 50V	Cercap X7R - SMD-1206	---	---
13	1	C16	1n – 50V	Cercap X7R - SMD-0805	---	---
14	1	C17	220p - 50V	Cercap C0G - SMD-0805	---	---
15	2	C18, C24	4n7 - 50V	Cercap X7R - SMD-0805	---	---
16	1	C19	3n3 - 50V	Cercap X7R - SMD-0805	---	---
17	1	C20	150p - 50V	Cercap C0G - SMD-0805	---	---
18	1	C23	100n – 50V	Cercap X7R - SMD-0805	---	---
19	2	C25, C26	680uF-80V	Aluminum ELECAP FS series 105°C	Panasonic	EEUFS1K681
20	1	C28	4u7 - 100V	Cercap X7R -	AVX	22201C475KAT2A

Item	Q.ty	Ref. Des.	Value - Rating	Description	Manufacturer	Part Number
				SMD-2020		
21	1	C29	100u – 50V	Aluminum ELCAP - YXF series- 105°C	Rubycon	50YXF100M8X11.5
22	1	C33	10u – 25V	Cercap X7R - SMD-1206	---	---
23	1	C35	1u – 25V	Cercap X7R - SMD-0805	---	---
24	1	D1	---	4A glass passivated bridge rectifier - GBU	Diodes Incorporated	GBU406
25	1	D2	---	High voltage ultrafast rectifier 800V - SMA	STMicroelectronics	STTH108A
26	1	D4	---	2X ultrafast recovery diode 400V - TO220AB	STMicroelectronics	STTH16R04CT
27	1	D5	---	Small signal switching diode- SOD-123	Vishay	1N4148W
28	1	D6, D12	---	Small signal switching diode - SOD80 (MiniMELF)	Vishay	BAV103-GS18
29	1	D7	---	Small signal Schottky diode – SOD-123-2	Vishay	BAT43W
30	1	D8, D15	---	Zener diode MMSZ series, 0.5W 5% - SOD123	Onsemi	MMSZ10T1G
33	1	F1	2.5A-250VAC	FUSE SS-5F series 2.5A-250VAC fast acting	Bussmann	SS-5F-2.5A
34	1	J1	---	PCB connector 3 PIN	Weidmuller	PM 5.08/03/90 3.5SN BK BX - 1760520000
35	1	J2	---	PCB connector 2 PIN	Weidmuller	PM 5.08/02/90 3.5SN BK BX - 1760510000
36	1	JMP1	---	Tinned copper wire jumper DIA 0.7mm	---	---
37	1	L5	27mH	27mH common-mode choke filter	Epcos	B82732F2901B001
38	1	NTC1	100k	NTC - 100k - 1% - wired thermostat with metallic ring	Vishay	NTCALUG01A104FA
39	1	Q1	---	N-channel power MOSFET 800V 0.4OHM	STMicroelectronics	STF14N80K5
40	2	Q2, Q4	---	Small signal N-channel depletion MOSFET 100V, SOT23	Infineon	BSS169
42	2	R1, R2	VDR-320V	Metal-oxide varistor LA series	Littelfuse	V320LA7P
43	2	R3, R4	300k - 200V	Stand. film RES - 1/4W	---	---

Item	Q.ty	Ref. Des.	Value - Rating	Description	Manufacturer	Part Number
				-5% - SMD-1206		
44	1	R6	47R - 150V	Stand. film RES - 1/8W -5% - SMD-0805	---	---
45	1	R7	240R - 200V	Stand. film RES - 1/4W -1% - SMD-1206	---	---
46	1	R8	0.39R - 200V	Stand. film RES - 1/4W -1% - SMD-1206	---	---
47	1	R9	0.47R - 200V	Stand. film RES - 1/4W -1% - SMD-1206	---	---
48	1	R10, R30	10R – 150V	Stand. film RES - 1/8W -5% - SMD-0805	---	---
49	2	R11, R40	6k2 – 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
50	1	R12	1k0 - 150V	Stand. film RES - 1/8W -5% - SMD-0805	---	---
51	1	R15	150k - 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
52	1	R16	130k - 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
53	1	R17	2k7 - 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
54	1	R19	47k - 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
55	1	R23	9k1 – 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
56	1	R24	5k6 – 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
57	1	R25	2k4 – 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
58	2	R26, R27	36k – 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
60	1	R36	51k - 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
61	1	R37	18k – 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
62	1	R39	270k – 200V	Stand. film RES - 1/4W -1% - SMD-1206	---	---
64	1	R43	3k6 – 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
65	1	R44	24k – 150V	Stand. film RES - 1/8W -1% - SMD-0805	---	---
66	1	T1	---	PQ26/22.5 flyback transformer 320uH	Magnetica	Custom

Item	Q.ty	Ref. Des.	Value - Rating	Description	Manufacturer	Part Number
67	1	U1	---	High power factor controller – HVLED101	STMicroelectronics	HVLED101
68	1	U4	---	HR optocoupler 400mil (OPT 6)	Vishay	SFH617-A2
69	1	U5	---	Adjustable 1% shunt voltage reference – SOT23-3L	STMicroelectronics	TL432AIL3T

Figure 4. EVLHV101SSR50W top side

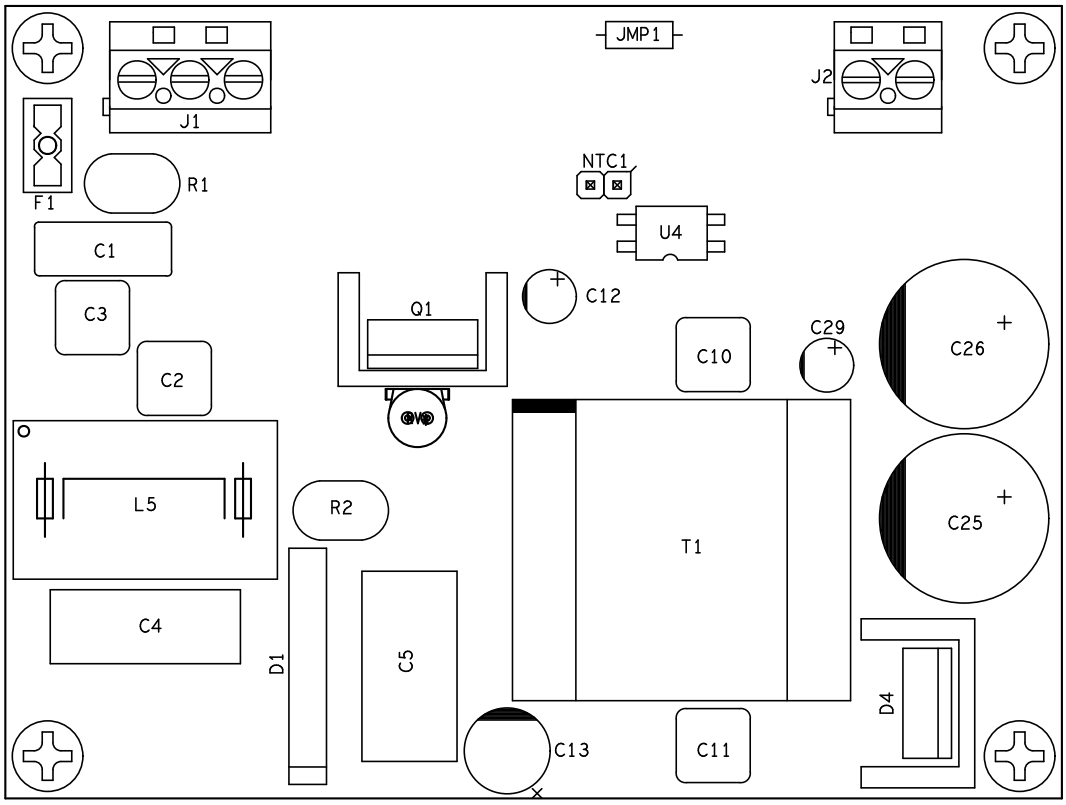
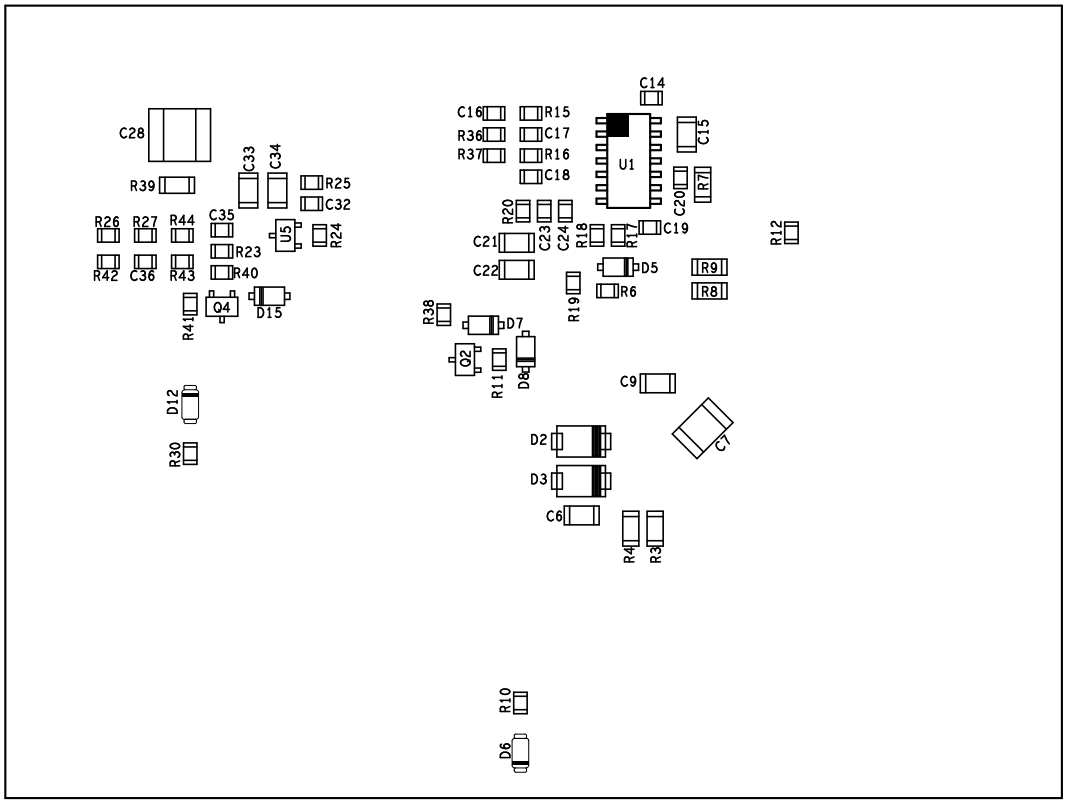


Figure 5. **EVLHV101SSR50W bottom side**



2 Flyback transformer specifications

Figure 6. **Flyback transformer – electrical diagram**

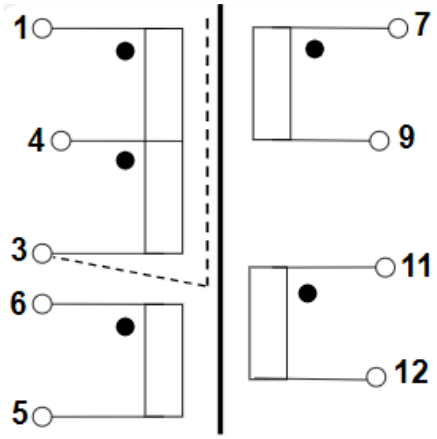


Table 4. **Flyback transformer – pin description**

No.	Description	Note
1	Primary drain	
2	Not connected	
3	Primary + VB & shield	
4	Primary center tap	
5	Auxiliary ground	41V - 25mA
6	Auxiliary	
7	Secondary	60V - 1.7A
8	Not connected	
9	Secondary ground	
10	Not connected	
11	Secondary auxiliary	26V – 25mA
12	Secondary auxiliary ground	

Note: Pins with the same subscript must be short-circuited on the PCB.

Table 5. Flyback transformer – windings technical data

Parameter	Pin	Min.	Typ.	Max.	Um	Note
Inductance	1 - 3	272	320	368	µH	Measure 1kHz, T_A 20°C
	6 - 5	3.57	4.20	4.83	µH	
	7 - 9	56.33	66.27	76.21	µH	
	11 - 12	10.70	12.59	14.48	µH	
Resistance	1 - 3	148	175	201	mΩ	Measure DC, T_A 20°C
	6 - 5	317	373	429	mΩ	
	7 - 9	87	102	117	mΩ	
	11 - 12	201	236	272	mΩ	
Transformer ratio	1 - 3 → 6 - 5		3.27		-	Measure 10kHz, T_A 20°C
	1 - 3 → 7 - 9		2.22		-	
	1 - 3 → 11 - 12		5.16		-	

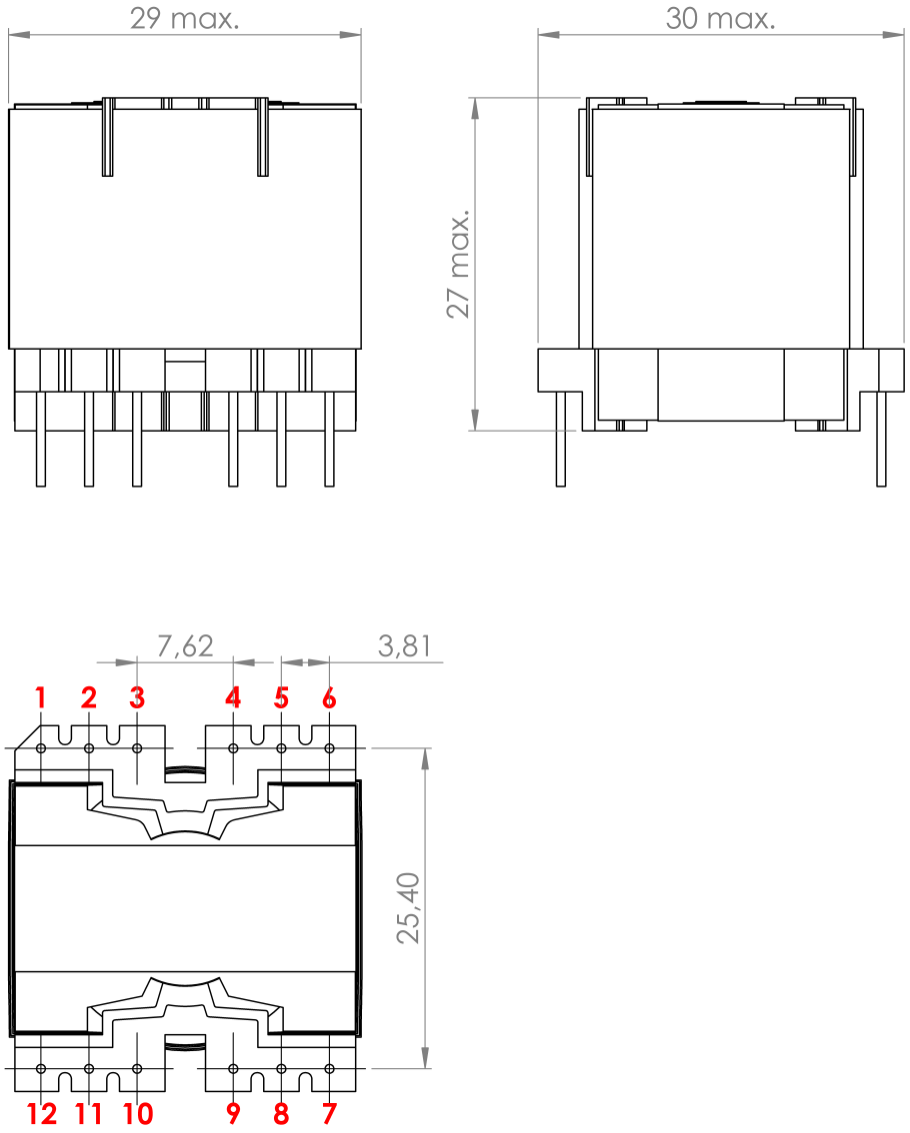
Table 6. Flyback transformer – electrical parameters

Parameter	Value	Um	Note
Leakage inductance	2.81	µH	Measure 1-3, all other pins in S.C., F 10kHz, T_A 20°C
Parasitic capacitance	16.1	pF	Measure 1-3, F_{RES} 2.20MHz, T_A 20°C
Operating current	3.7	Ap	Maximum peak current
Saturation current	6.2	A	Measure DC, L≥50% NOM, T_A 20°C
Operating frequency	60	kHz	Minimum frequency
Insulation	2.5	kVac	F 50Hz, test duration 2", T_A 20°C

Table 7. Flyback transformer – physical parameters

Parameter	\Value	Um	Note
Thermal class	B	-	
Ambient temp. range	-20 ÷ +85	°C	PMAX 50W with max self T_{rise} 45°C
Storage temp. range	-20 ÷ +85	°C	
Maximum dimensions	30 x 29 x H 27	mm	
Weight	45.4	g	

Figure 7. **Flyback transformer – mechanical aspect**



3 Circuit description and components selection

EVLHV101SSR50W is a quasi-resonant High Power Factor (HPF) flyback converter that works with secondary side regulation (SSR). The opto-isolated feedback allows for a very accurate voltage regulation.

The board uses the new HVLED101 quasi-resonant HPF flyback controller (U1), which enables the converter to draw a theoretically sinusoidal input current from the power line and adopt frequency foldback with valley locking operation to reduce the switching losses and minimize acoustic noise.

Following is a description of the new features of the HVLED101, and an explanation of the calculation of the relevant components.

For the design and selection of power components, refer to a standard high power factor flyback (see, for example, AN4932). Using HVLED101 allows more freedom in the selection of transformer primary inductance and reflected voltage with respect to HVLED001A and B because of reduced ZCD blanking time and the integrated THD optimizer.

HVLED101 supply management and line voltage monitoring function

The HVLED101 is supplied by applying a DC voltage source between the VCC pin and the PGND.

This voltage is obtained during normal operation, by the primary auxiliary winding of the transformer (T1) through R10, D6, and C13.

A linear regulator circuit using a Depletion MOSFET (Q2) and a Zener diode (D8) provides a voltage limited supply (about 12 V) to the VCC pin, which prevents the overage of the absolute maximum voltage rating of HVLED101 (VCC-max = 19 V).

At start-up and during low consumption mode, the IC is powered by the input voltage of the board that is applied to the HVSU pin using a low value resistor (R12 = 1 kΩ typ). The pin is internally connected to the high-voltage start-up generator that starts its operation when the applied voltage is higher than 20 V (typ.). The charging current ensures a quick start-up independent from the voltage applied to the HVSU pin.

During operational mode, the input voltage is read through an internal resistor divider connected to the HVSU pin to obtain a high power factor and to detect both input overvoltage and undervoltage, according to the protection configuration, selected on the DLY/CFG pin. (see the “Configuration programming and parameters selection” section).

Secondary side regulation

The HVLED101 is able to operate with primary side regulation (PSR) and secondary side regulation (SSR) independently, using the lower signal between FB and OPTO.

On EVLHV101SSR50W, the SSR feature is used to regulate the Vout, while the PSR is set to provide the secondary overvoltage protection.

The secondary control loop circuitry is mainly composed of the voltage resistor divider (R26, R27, R43, and R44) and by the TL432 reference (U5) in a standard configuration.

The opto-coupler collector (U4) is directly connected to the OPTO pin to close the loop.

A linear regulator circuit using a Depletion MOSFET (Q4) and a Zener diode (D15) provides a fixed voltage rail to the TL432, to prevent the overage of the maximum cathode to anode voltage (Vka-max = 37 V).

Resistor R23=9k1 limits the current in the diode of the opto-coupler (U4) and guarantees the minimum cathode current for regulation to the TL432.

The voltage resistor divider applied to the TL432 determines the Vout.

The Rhigh = R36 + R37 is set to 72 kΩ, a value that allows to have a low power dissipation but not too high to impact the regulation voltage Vka of the TL432.

The lower part of the divider is selected according to the following equation:

$$R_{low} = R43//R44 = \frac{V_{REF\_TL432}}{V_{OUT} - V_{REF\_TL432}} * R_{high} = \frac{2.5V}{60 - 2.5V} * 72k\Omega = 3.13k\Omega$$

Selected values are:

R43 = 3k6

R44 = 24 kΩ

The type 2 compensation network consists of the C33 + R25 series.

The pole is placed at a very low frequency so that the gain at twice line frequency is substantially less than unity, while the zero boosts the phase in the neighborhood of the open-loop crossover frequency to provide a good phase margin.

The capacitor C24 introduces a further pole at high frequency.

The voltage present on the OPTO pin is applied to a “MIN selection” block together with the FB pin voltage and MPC internal signal (see the “Maximum power control” section).

The FB pin is normally set to a high level by the internal OTA due to the dimensioning of the voltage divider (R17 and R19), as described later, and it intervenes on the regulation only in case of overvoltage on the Vout (OVP protection).

A small filter capacitor (C23 = 100 nF) is placed between the FB pin and the GND to prevent possible noise pickup.

The output of the “MIN selection” block (basically the OPTO signal) is multiplied by the input voltage, suitably scaled by the internal resistor divider connected to the HVSU pin and normalized to unity. The output of the multiplier passes through the THD optimizer, and its output is used as the threshold for the PWM comparator that turns off the power MOSFET (Q1) when the voltage across the primary current sense resistor (R8//R9) reaches that reference.

The THD optimization unit is placed between the multiplier output and the current sense threshold limiter to minimize the distortion of the absorbed AC current (THD) and to maximize the Power Factor (PF).

This unit uses the external capacitor C19, connected between the THD pin and the GND, to filter the switching frequency from the VCS threshold. The value of this capacitor must be selected accordingly to the following relationship:

$$C19 = \frac{4}{R_{THD} \cdot f_{SW.min}}$$

Where:

R_{THD} is the THD optimizer internal resistor and $f_{SW.min}$ is the minimum switching frequency.

For the EVLHV101SSR50W, the calculation is the following:

$$C19 = \frac{4}{22k\Omega * 70kHz} = 2.597nF \rightarrow 3n3F$$

As previously mentioned, the PSR feature of HVLED101 is used as secondary overvoltage protection due to its ability to read the Vout by means of the voltage developed across the primary auxiliary winding during the off-time of the MOSFET.

R19 must be selected in order not to exceed the maximum ZCD pin current (I_{ZCDmax} from datasheet recommended operating conditions) during MOSFET on-time.

$$R19_{min} = \frac{V_{PKmax}}{I_{ZCDmax}} \cdot \frac{Naux}{Nprim} = \frac{\sqrt{2} \cdot 264V}{3mA} \cdot \frac{11}{36} = 38.03k\Omega$$

The selected R19 is 47 kΩ.

The lower part of the divider is selected based on output overvoltage chosen according to the following equation:

$$R_{ZCDlow-max} = \frac{R19 * V_{REF\_PSR}}{V_{OVP} \cdot \frac{N_{aux}}{N_{sec}} - V_{REF\_PSR}} = \frac{47k\Omega * 2.6V}{69V \cdot \frac{11}{16} - 2.6V} = 2.725k\Omega$$

Where V_{OVP} = 69 V is the value of overvoltage chosen.

The selected R17 is 2.7 kΩ.

Maximum power control (MPC)

Maximum input power is automatically limited by the HVLED101 internal algorithm (MPC), which helps in increasing system safety.

The MPC defines the value of the primary current sense resistor R8//R9 according to the following equation:

$$R8//R9 = \frac{K_M \cdot K_{MPC}}{4 \cdot P_{in-lim}}$$

Where:

KM is the multiplier gain = 0.176 V/V.

KMPC is the scaling factor = 270 V^2.

$P_{in\text{-}lim}$ is the required limiting input power.

$P_{in\text{-}lim}$ can be calculated by considering the maximum output power and an efficiency of 0.9.

The MPC block automatically detects if the input voltage is AC or DC and applies the correct gain to have the required power limitation in both cases.

For the EVLHV101SSR50W, the calculation for the primary current sense resistor is the following:

$$R8//R9 = \frac{0.176\frac{V}{V} \cdot 270V^2}{4 \cdot \frac{50W}{0.9}} = 0.213\Omega$$

Selected values are:

R8 = 0.39 Ω

R9 = 0.47 Ω

Frequency foldback with valley locking operation

HVLED101 adopts frequency foldback with valley locking operation to reduce the switching losses and avoid acoustic noise. The level of the frequency foldback depth is determined by the voltage on the VL pin (proportional to the control voltage) which is compared to the VL1-VL6 internal thresholds, defining the number of valleys skipped.

The resistor R16 allows the tuning of VL voltage, and consequently the number of valleys skipped is determined according to the following relationship:

$$R16_{max} = \frac{VL_x}{K_{LV1}\left(\frac{4}{\sqrt{2}*V_{IN}}*\frac{P_{out}}{\eta}*\frac{R8//R9}{K_M} + V_{OS}\right)}$$

Where:

VLx is the valley threshold, internal to the IC, which is compared to the voltage on the VL pin.

K_{LV1} is the valley lock block gain (10 uA/V, it can be derived from the datasheet parameter $I_{VL\text{-}P\text{-}UP}$: if V_{OPTO} changes from 1 V to 2 V, the VL current changes from 10 uA to 20 uA).

K_M is the multiplier gain = 0.176 V/V.

V_{OS} is the FB and OPTO pin internal offset.

V_{IN} is the AC mains voltage at the input of the board.

Pout is the output power.

η is the expected efficiency.

R8//R9 are the primary sensing resistors.

A fine tuning of the R16 resistor may be required.

EVLHV101SSR50W has been designed to skip one valley at full load and V_{IN} = 230 V_{AC}.

The relevant VLx threshold is, therefore, VL1 and so the calculation is the following:

$$R16_{max} = \frac{1.75V}{10\mu A/V*\left(\frac{4}{\sqrt{2}*230V}*\frac{50W}{0.9}*\frac{0.213\Omega}{0.176V/V} + 0.5V\right)} = 131894\Omega \rightarrow 130\text{k}\Omega$$

As the load decreases, the voltage on the VL pin (proportional to control voltage) drops, and the HVLED101 increases the number of valleys skipped.

The controller stays locked in a valley until the load changes significantly.

After skipping 6 valleys, the system operates in discontinuous conduction mode (DCM) and when the output power is very low, the flyback converter enters burst mode operation to maintain the output regulation.

If the Vin changes, the HVLED101 accordingly adjusts the frequency foldback depth.

At V_{IN} = 115 V_{AC} with full load, the system operates in transition mode and starts to skip the valleys when the load decreases.

SSR burst mode operation

When the load is very light, the OPTO pin voltage decreases below the V_{BM} threshold, and the HVLED101 stops switching and it enters into burst-mode operation (deep low-consumption mode).

In the idle state, with the converter stopped, no energy is delivered to the output, so the output voltage starts decaying. The feedback circuit reacts to this drop and, as a consequence, the voltage on the OPTO pin increases; as it exceeds V_{BM}+V_{BM_HYST}, the IC restarts switching soon after.

With this operating mode the duration of each burst and the idle time are automatically adjusted according to the load conditions: as the load progressively decreases, the number of switching cycles in each burst becomes smaller and smaller, and the duration of the idle time becomes longer and longer.

If the load increases, then the number of switching cycles in each burst becomes larger and the duration of the idle time becomes shorter, until the operation becomes continuous again.

Configuration programming and parameter selection

MOSFET (Q1) always turns on when the demagnetization occurs, but in order to minimize the switching losses it is better to turn on the MOSFET at the minima of the oscillation (valley switching).

In HVLED101 this is achieved by programming the delay time (T_{DLY}) between ZCD detection and MOSFET turn-on by means of the R15 connected to the DLY/CFG pin.

The T_{DLY} required is calculated starting from the frequency ringing after demagnetization, as follows:

$$f_{ring} = \frac{1}{2\pi * \sqrt{L_P * C_{DRAIN}}}$$

Where:

Lp is the primary inductance of the transformer.

C_{DRAIN} is the estimated total drain node capacitance.

$$T_{ring} = 2\pi * \sqrt{L_P * C_{DRAIN}}$$

$$T_{dly} = \frac{T_{ring}}{4}$$

For EVLHV101SSR50W the calculations are the following:

$$f_{ring} = \frac{1}{2*3.14*\sqrt{320\mu H*200nF}} = 628.115kHz$$

$$T_{ring} = 2*3.14*\sqrt{320\mu H*200nF} = 1.59\mu s$$

$$T_{dly} = \frac{1.59\mu s}{4} = 397.384ns$$

The relationship between the T_{DLY} required and R15 is expressed by the following formula:

$$R15 = \frac{T_{dly} - T_{dly0}}{K_{dly}}$$

Where:

T_{DLY0} is the minimum delay time, 100 ns.

K_{DLY0} is ZCD to GD on gain, 2.13 ns/kΩ.

For the EVLHV101SSR50W the calculation is the following:

$$R15 = \frac{397.384ns - 100ns}{2.13ns/k\Omega} = 139.617k\Omega$$

Considering the standard resistor values, after a fine-tuning on the real board, 150 kΩ has been chosen.

The actual T_{DLY} programmed is:

$$T_{dly} = \left(K_{dly} * R15\right) + T_{dly0} = 419.5ns$$

The maximum waiting time (T_{WAIT}) is proportional to the programmed delay time (T_{DLY}) configured by R15 as per the following relationship:

$$T_{wait} = 8*\left(T_{dly} - T_{dly0}\right) + T_{dly0}$$

$$T_{wait} = 8*(419.5ns - 100ns) + 100ns = 2.656\mu s$$

The HVLED101 can be programmed with 5 different configurations of input range, brownout, and surge protections according to user needs (CFG1-CFG5).

The various configurations can be chosen by selecting the value of the time constant (Tau_{CFGn}) associated with the RC network placed between DLY/CFG and GND.

Table 8. Programming configurations

Tau_{CFGn} (µs)	CFG	iOVP	BrOut	K_{HV}	DC Det.	I_{BLEED} @ iOVP
30µs ... 45µs	CFG1	ON	Low	High	Low	ON
100µs ... 140µs	CFG2	OFF	OFF	Low	Low	N.A.

Tau_{CFGn} (µs)	CFG	iOVP	BrOut	K_{HV}	DC Det.	I_{BLEED} @ iOVP
300µs ... 410µs	CFG3	ON	High	High	High	ON
860µs ... 1.2ms	CFG4	OFF	Low	Low	Low	N.A.
> 2.05ms	CFG5	ON	Low	High	Low	OFF

Note that CFG2 has the brownout detection disabled. This is intended to be used mainly for debugging purposes because an input voltage lower than 80 V could lead to unpredictable Vout behavior.

The following table summarizes the suggested combination of R_{DLY} and C_{CFG} to obtain both delay time and configuration programming.

Table 9. Suggested R_{DLY}-C_{CFG} programming values

T_{DLY} (ns)	R_{DLY} (kΩ) (1%)	C_{DLY} (nF) (5% - >6.3V rated)				
		CFG1	CFG2	CFG3	CFG4	CFG5
163.9	30	1.2n	3.9n	12n	33n	82n
183.1	39	1n	2.7n	8.2n	27n	56n
219.3	56	680p	2.2n	6.2n	18n	39n
259.8	75	470p	1.5n	4.7n	12n	33n
355.6	120	270p	1n	2.7n	8.2n	18n
419.5	150	220p	680p	2.2n	6.8n	15n
483.4	180	180p	560p	1.8n	5.6n	12n
568.6	220	150p	470p	1.5n	4.7n	10n
675.1	270	120p	390p	1.2n	3.3n	8.2n
802.9	330	100p	330p	1n	2.7n	6.8n
1101.1	470	82p	220p	680p	2.2n	4.7n
1292.8	560	68p	180p	560p	1.8n	3.9n

For EVLHV101SSR50W, R_{DLY} = R15 is 150 kohm to fix T_{DLY} = 419.5 ns, and the C_{CFG} = C17 is 220 pF to select the CFG1 configuration, which is the one suggested for the universal input range (90 V_{AC} – 305 V_{AC}).

Protections

The HVLED101 provides a set of protections for a safe and reliable operation of the application during abnormal conditions.

The following protections are provided:

- 2^{nd} overcurrent protection (2^{nd} OCP)
- Input overvoltage protection (iOVP - against input voltage surge)
- Brownout protection (against insufficient input voltage)
- Output undervoltage protection

In the HVLED101, the information on the input voltage is read through the HVSU pin which is connected to the bridge diodes D1 through the series resistor R12.

When the voltage input (V_{IN}) decreases below the brownout threshold (V_{BO}) for a time longer than the brownout activation time (T_{BO}), the protection is entered: the IC stops switching and the high-voltage start-up current generator is activated periodically to charge VCC between V_{CC-OFF} and V_{CC-ON} to keep the IC alive, using the highest current level (I_{CHG-H}).

During the charging phase, the IC monitors the HVSU pin, whose voltage is the input reduced by the drop on the R12 resistor. If the measured voltage goes over the brownout threshold again, the device will restart when VCC reaches the V_{CC-ON} threshold.

The voltage drop on R12 represents, therefore, the hysteresis between the brownout and brown-in, and its value is chosen for having the proper amount of such hysteresis.

When the IC sources I_{CHG-H} to the VCC pin, it sinks about 7 mA from the HVSU pin.

In the EVLHV101SSR50W evaluation board, R12 = 1 kΩ provides about 7 V of hysteresis on the peak of Vin, i.e. about 5 V_{AC}.

This is usually acceptable for most of the applications. In case a different hysteresis is required, it is sufficient to modify the value of the HVSU series resistor, accordingly.

The HVLED101 also embeds the general-purpose FAULT pin, intended to disable the switching activity and to move the IC into low consumption if the voltage on this pin falls below the $V_{FLT-OFF}$ threshold or it is left floating.

The FAULT pin is mainly used to manage an NTC thermistor: in fact, the lower threshold has a well-defined hysteresis and the pin sources a precise current (50 uA) to create the desired thermal hysteresis for final application.

For EVLHV101SSR50W, the NTC1 is physically located on the dissipator of the switching MOSFET (Q1) and it is linearized using a resistor network consisting of one resistor in series (R37) and one in parallel (R38).

The design has been devised so that the value of the FAULT voltage is equal to $V_{FLT-OFF}$ (thermal protection activated) at about 100 °C.

If the NTC is not used, a fixed resistor (22 kΩ to 47 kΩ) should be connected to the GND.

The small capacitor C16 (1nF), which is connected from the pin to the ground, reduces switching noise pick-up, helping to achieve a clean operation.

4 Test results

In this section efficiency, THD, and power factor measurements under different line and load conditions are reported.

A voltmeter on connector J2 measured the output voltage, and an amperometer measured the current.

THD, PF, and the input power was measured using a digital power meter, while the output power was calculated as the product between V_{OUT} and I_{OUT}.

Table 10. Efficiency table (Vout = 60V)

Load [%]	I_{out} [mA]	V_{out} [V]	P_{out} [W]	P_{in} [W]	THD [%]	PF	η [%]
V_{IN} = 90V_{AC} / 50Hz							
10	83	59.84	4.97	5.89	5.25	0.9867	84.38
25	208	59.84	12.45	13.88	3.85	0.9980	89.70
33	278	59.84	16.64	18.42	4.16	0.9986	90.33
50	417	59.84	24.95	27.46	4.02	0.9990	90.88
75	625	59.84	37.40	41.05	3.21	0.9989	91.12
100	833	59.84	49.85	55.01	2.51	0.9983	90.62
4 points avg							90.58
V_{IN} = 115V_{AC} / 60Hz							
10	83	59.84	4.97	5.89	6.12	0.9448	84.28
25	208	59.84	12.45	13.89	4.60	0.9937	89.59
33	278	59.84	16.64	18.33	3.40	0.9972	90.74
50	417	59.84	24.95	27.28	3.35	0.9990	91.46
75	625	59.83	37.39	40.72	3.05	0.9993	91.82
100	833	59.83	49.85	54.37	2.70	0.9988	91.66
4 points avg							91.13
V_{IN} = 230V_{AC} / 50Hz							
10	83	59.84	4.93	6.034	20.55	0.6141	82.32
25	208	59.84	12.35	14.01	11.00	0.8490	88.82
33	278	59.84	16.50	18.40	6.40	0.9237	90.39
50	417	59.84	24.77	27.30	4.30	0.9683	91.39
75	625	59.84	37.13	40.62	3.20	0.9867	92.06
100	833	59.84	49.48	53.94	2.40	0.9948	92.41
4 points avg							91.17
V_{IN} = 265V_{AC} / 50Hz							
10	83	59.84	4.97	5.975	23.45	0.5175	83.13
25	208	59.84	12.45	14.13	15.21	0.7671	88.06
33	278	59.84	16.64	18.53	9.31	0.8616	89.75
50	417	59.84	24.95	27.40	6.18	0.9376	91.05
75	625	59.84	37.40	40.67	5.21	0.9713	91.95
100	833	59.84	49.85	53.98	2.98	0.9881	92.33
4 points avg							90.85

Figure 8. **Load regulation**

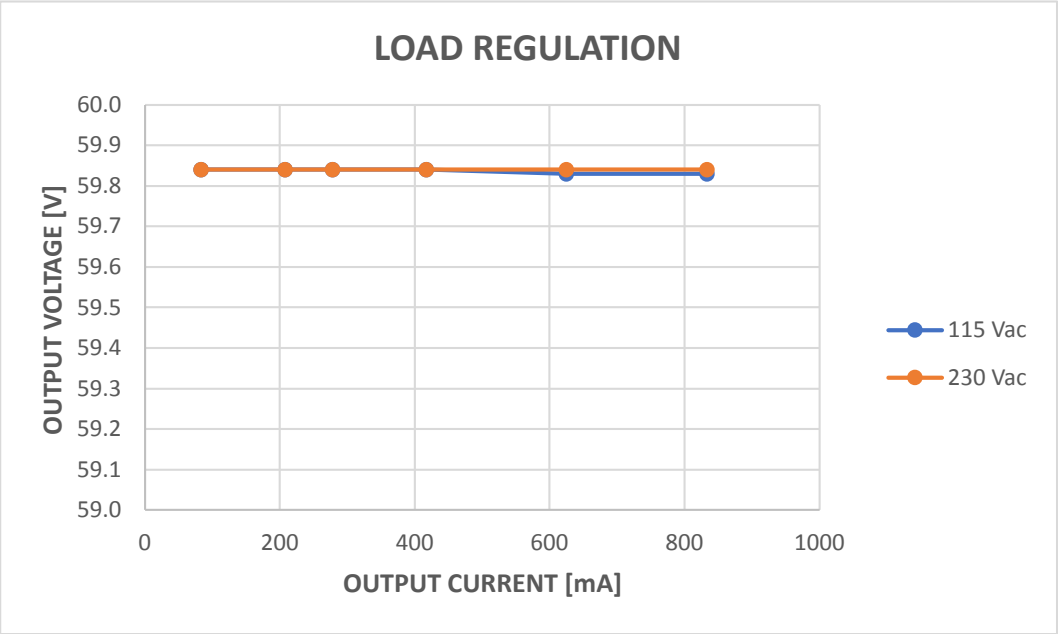


Figure 9. **Efficiency**

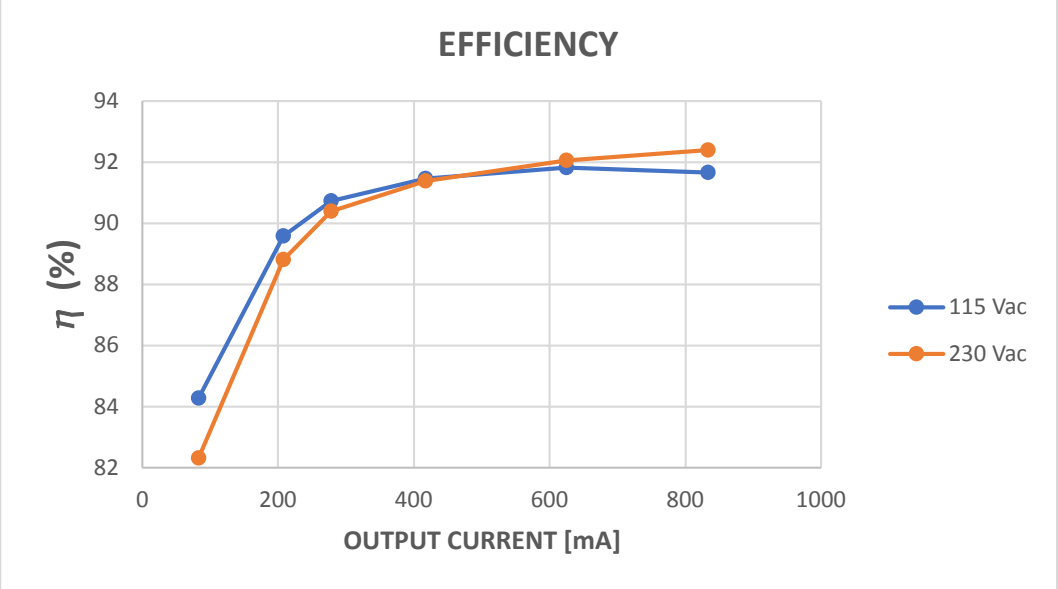


Figure 10. **THD**

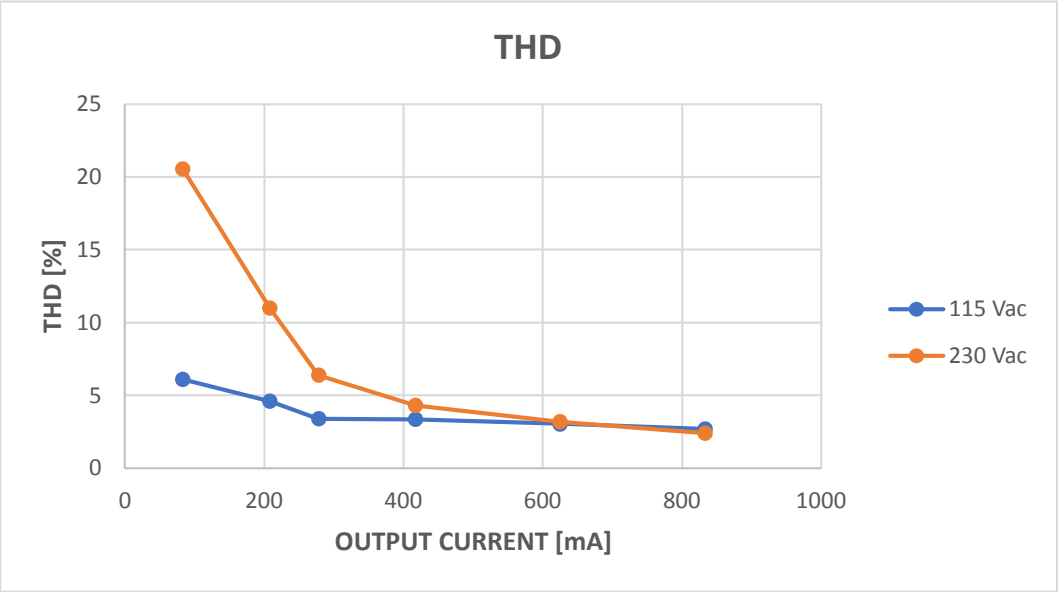


Figure 11. **Power factor**

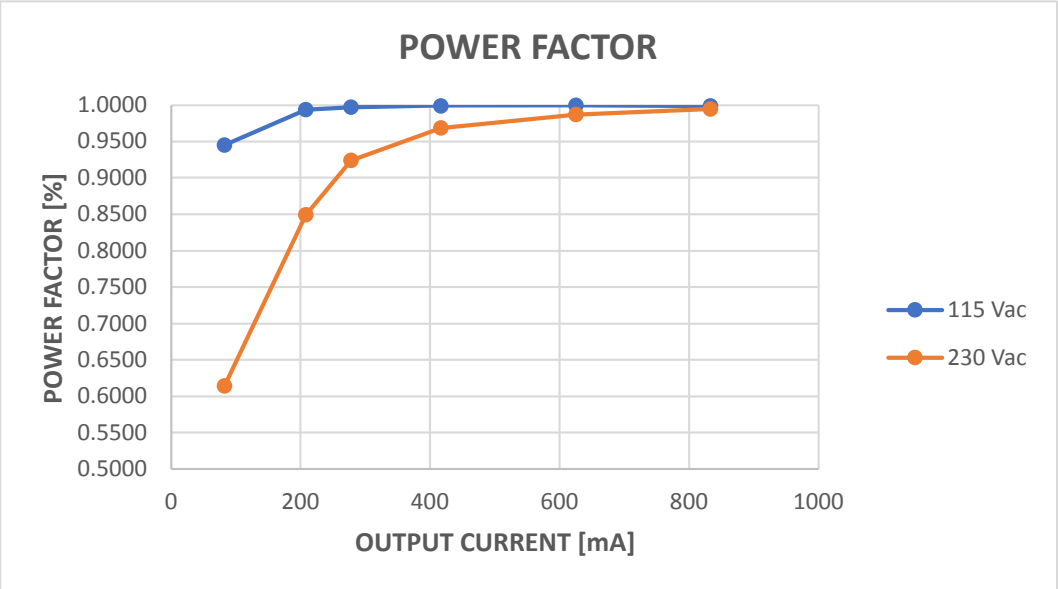


Figure 12. **THD vs Vin**

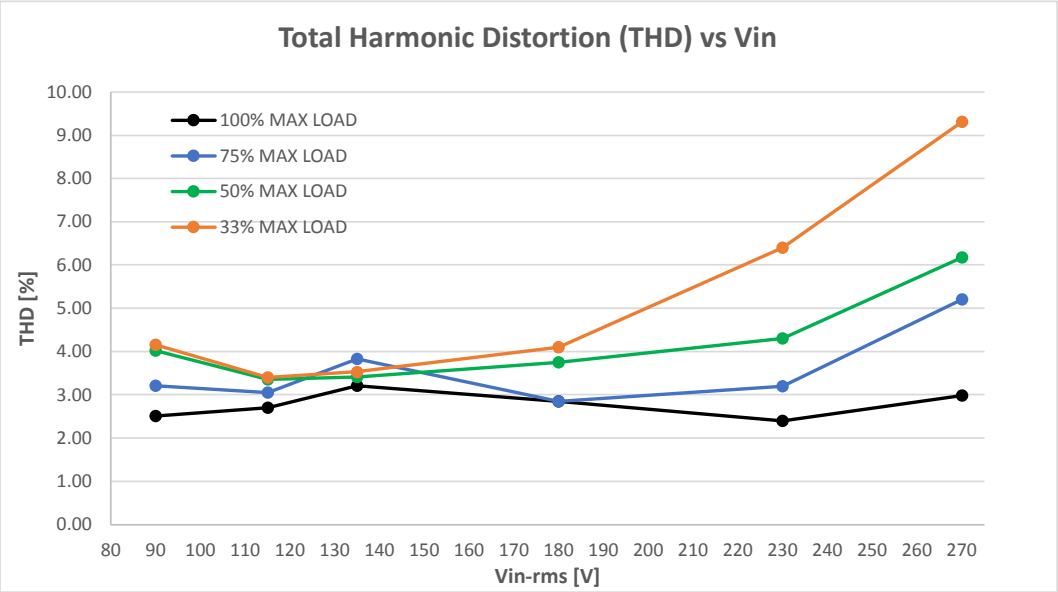


Figure 13. **Power Factor (PF) vs Vin**

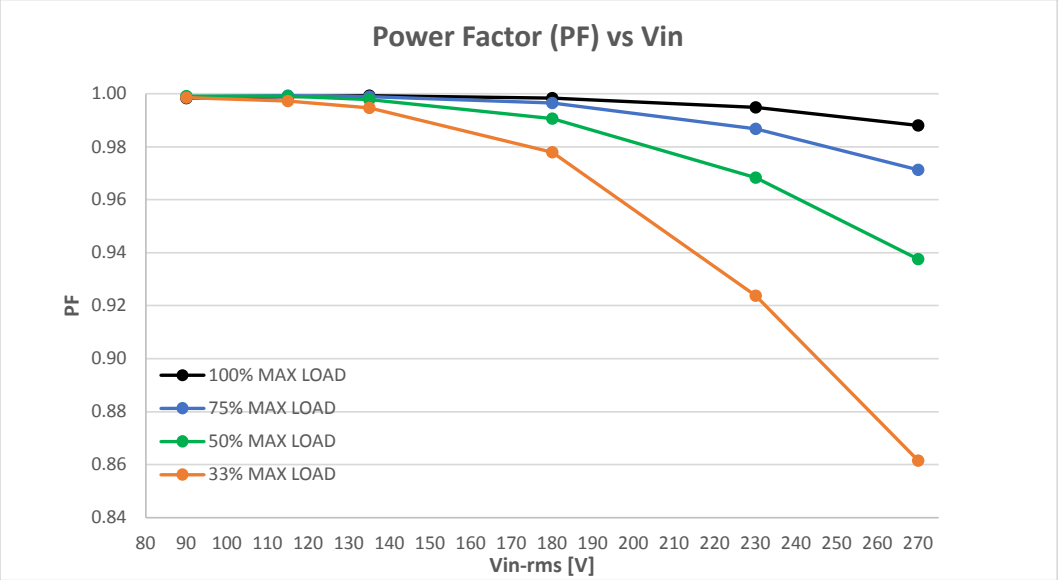
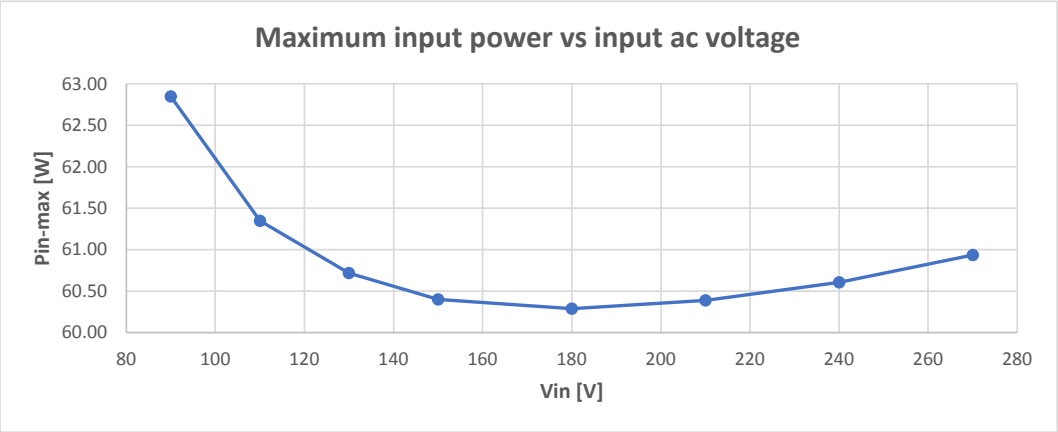


Figure 14. **Pin-max vs Vin**



5 No load & standby consumption

The consumption of EVLHV101SSR50W in no load & stand-by conditions at 115 V_{AC} and 230 V_{AC} are shown in table 11. The measurements were taken in the following conditions:

Consumption in a no load condition, nothing is connected to connector J2.

Consumption in stand-by, 4.6 mA current is drawn from the output connector J2 (POUT= 4.6 mA * 60 V = 270 mW).

Table 11. No load & stand-by consumption

Conditions	@ V_{IN} = 115V_{AC}	@ V_{IN} = 230V_{AC}
	P_{IN} [mW]	P_{IN} [mW]
No-load	135	140
Stand-by	450	440

6 Start-up and steady state

During the start-up phase, the HVLED101 is able to control the input current to reduce the stress placed on all the power components and provide a smooth rise of the output voltage.

The waveforms confirm that HVLED101 is able to achieve sinusoidal input current (extremely low THD).

Figure 15, Figure 16, Figure 17, and Figure 18 show the startup phase and steady state at full load with 115 V_{AC} and 230 V_{AC} input voltages.

In the following figures:

CH1 – yellow = CS current sense pin

CH2 – blue = V_{OUT}

CH3 – red = HVSU pin

CH4 – green = Input current

Figure 15. Start-up at 115V_{AC}, 100% load

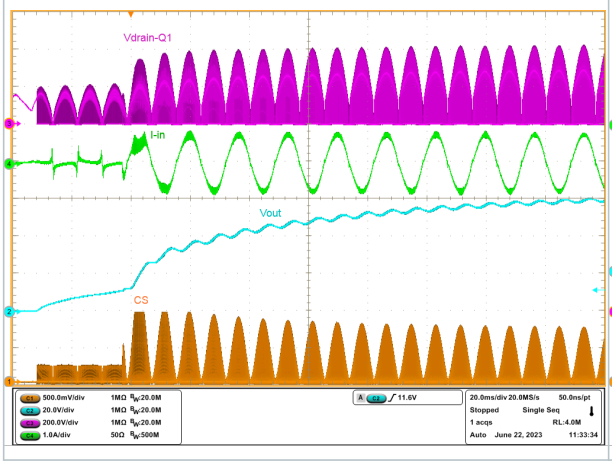


Figure 16. Steady state at 115V_{AC}, 100%

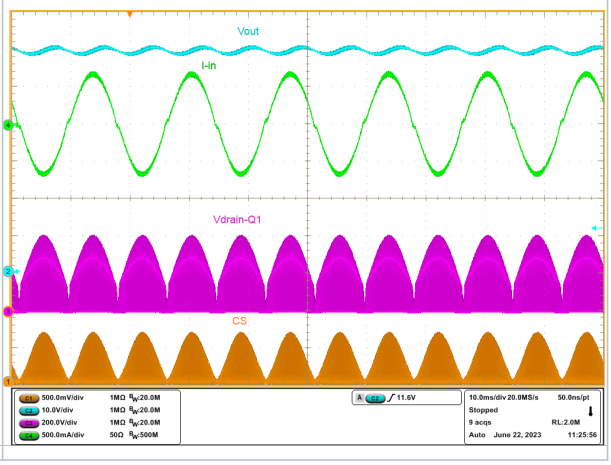


Figure 17. Start-up at 230V_{AC}, 100% load

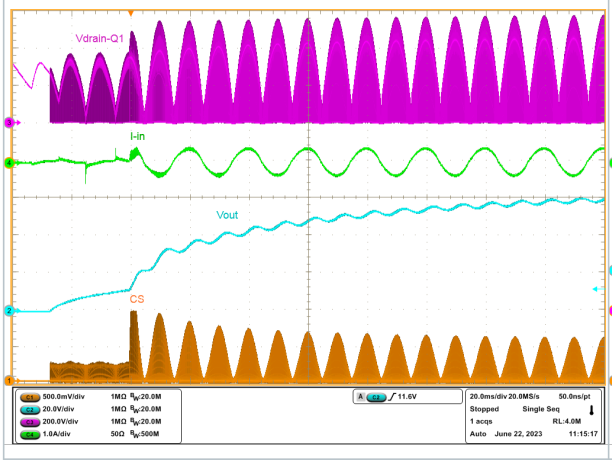
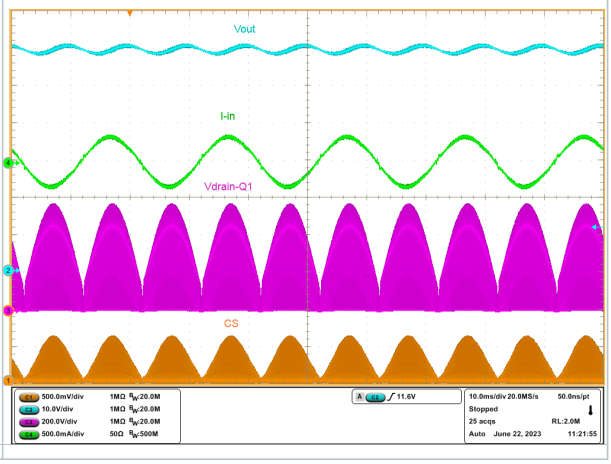


Figure 18. Steady state at 230V_{AC}, 100%



6.1 Start-up at 90 V_{AC} with different load conditions

HVLED101 embeds an 800 V start-up structure that allows for the fast start-up of the system.

On the EVLHV101SSR50W the start-up time is always lower than 200 ms in all V_{IN} and load conditions.

In the following figures:

CH1 – yellow = CS current sense pin

CH2 – blue = V_{OUT}

CH3 – red = VCC pin
CH4 – green = V_{AC} mains

Figure 19. Start-up at 90V_{AC}, 100% load

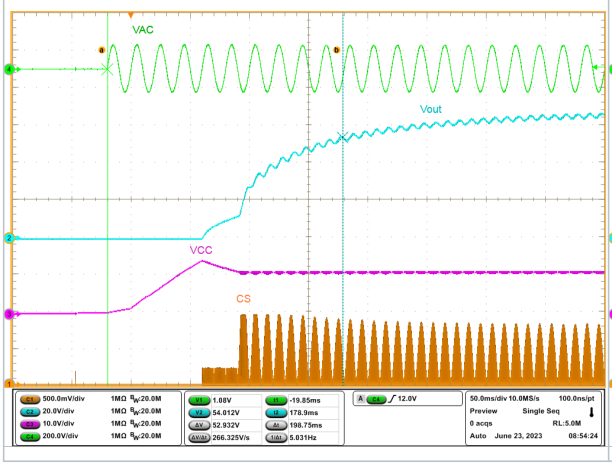


Figure 20. Start-up at 90V_{AC}, 75% load

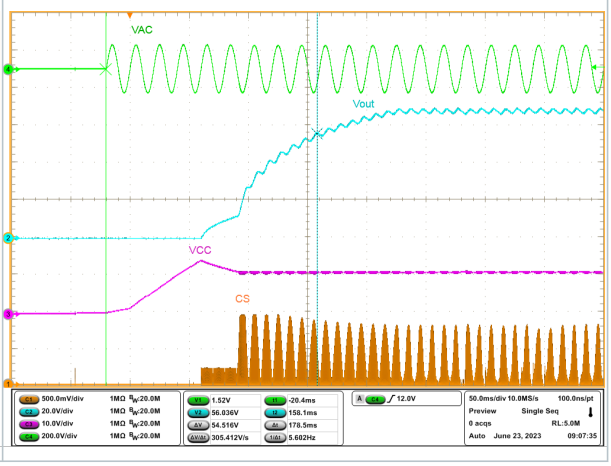


Figure 21. Start-up at 90V_{AC}, 50% load

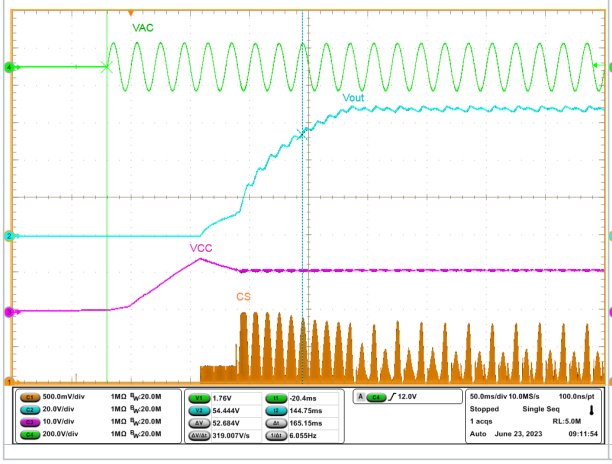


Figure 22. Start-up at 90V_{AC}, 25% load

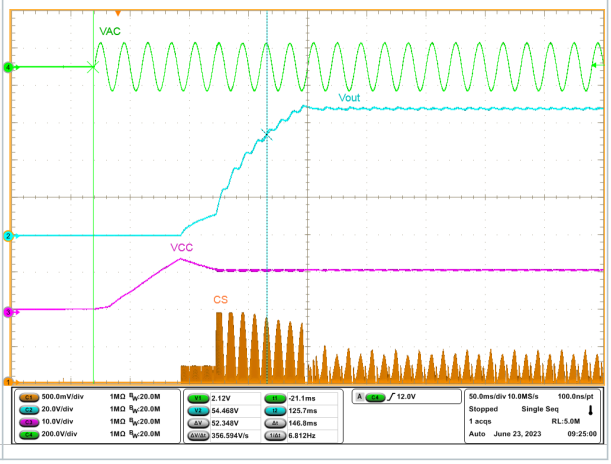


Figure 23. Start-up at 90V_{AC}, 270mW load

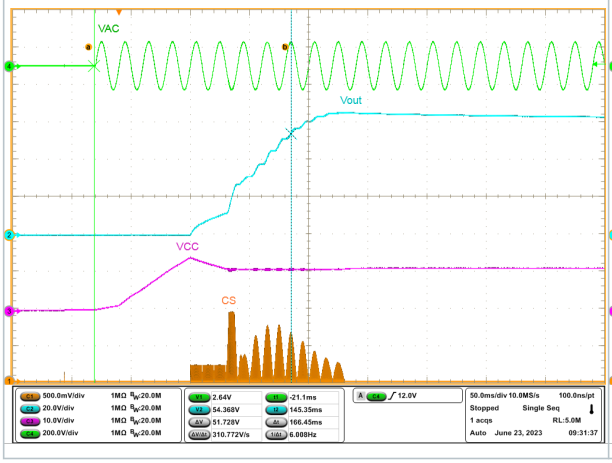
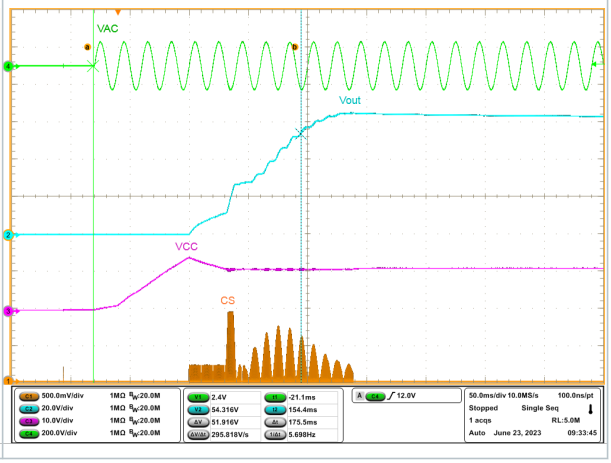


Figure 24. Start-up at 90V_{AC}, no load



6.2 Start-up at 115 V_{AC} with different load conditions

Figure 25. Start-up at 115V_{AC}, 100% load

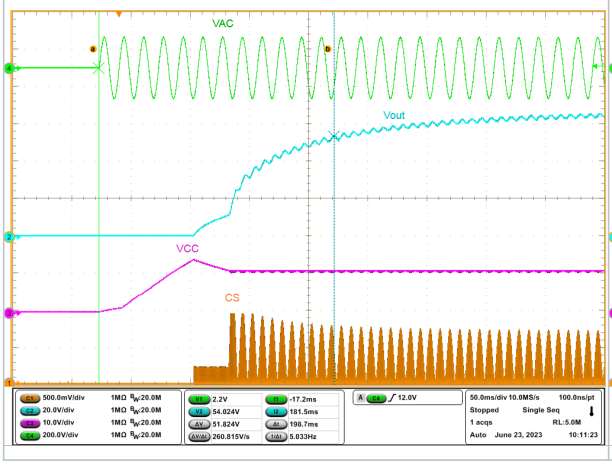


Figure 26. Start-up at 115V_{AC}, 75% load

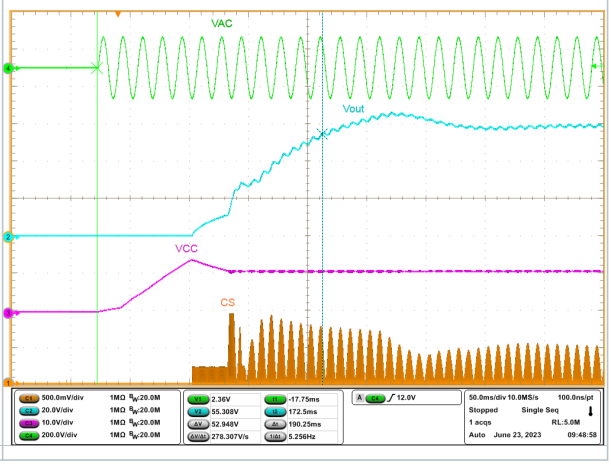


Figure 27. Start-up at 115V_{AC}, 50% load

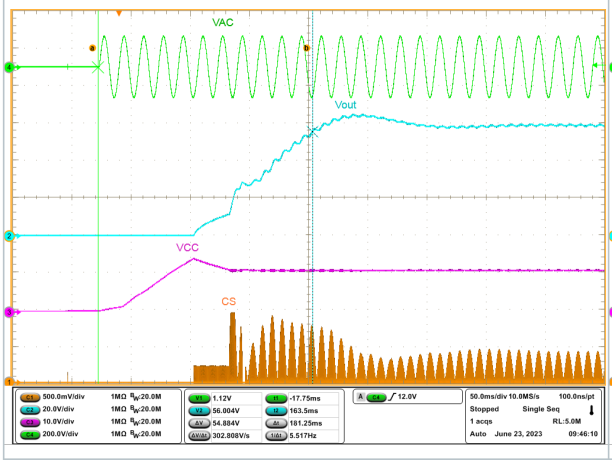


Figure 28. Start-up at 115V_{AC}, 25% load

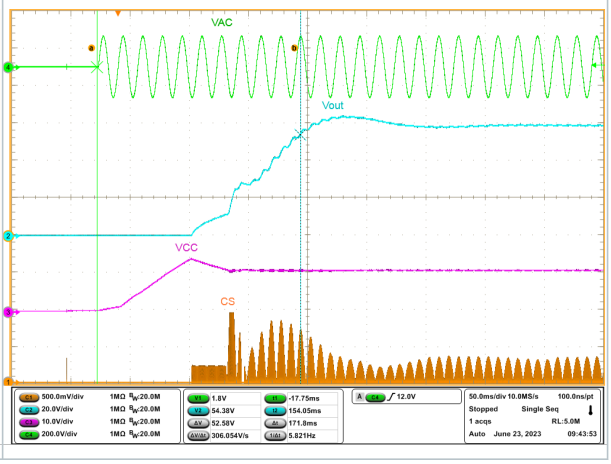


Figure 29. Start-up at 115V_{AC}, 270mW load

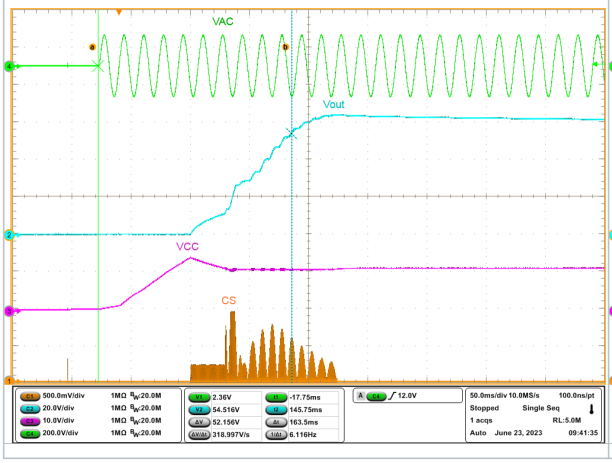
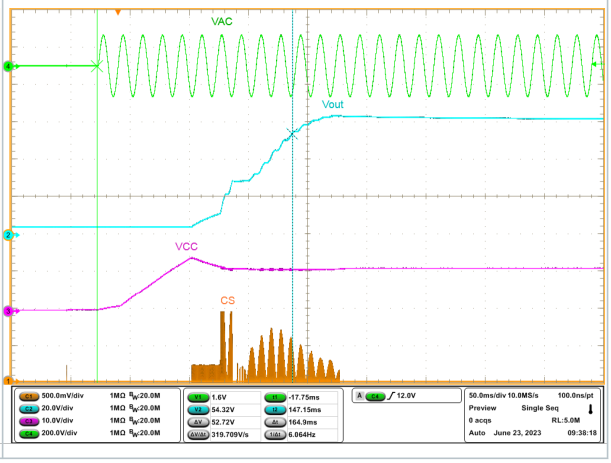


Figure 30. Start-up at 115V_{AC}, no load



6.3 Start-up at 230 V_{AC} with different load conditions

Figure 31. Start-up at 230V_{AC}, 100% load

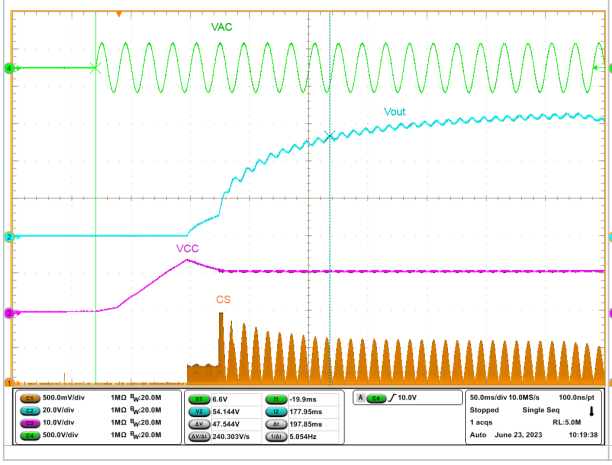


Figure 32. Start-up at 230V_{AC}, 75% load

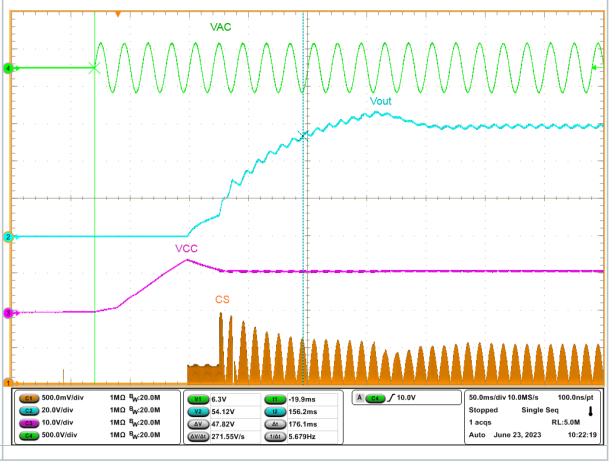


Figure 33. Start-up at 230V_{AC}, 50% load

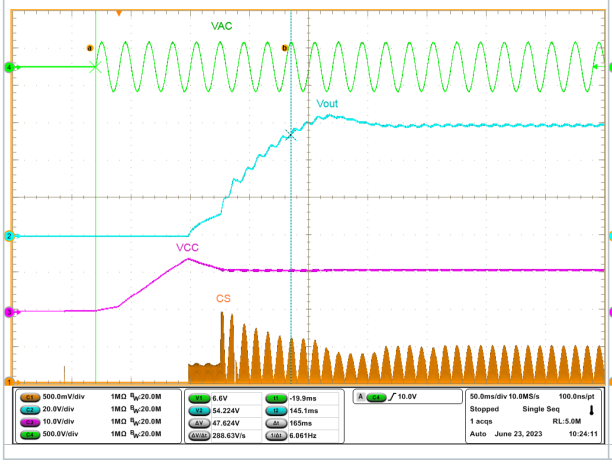


Figure 34. Start-up at 230V_{AC}, 25% load

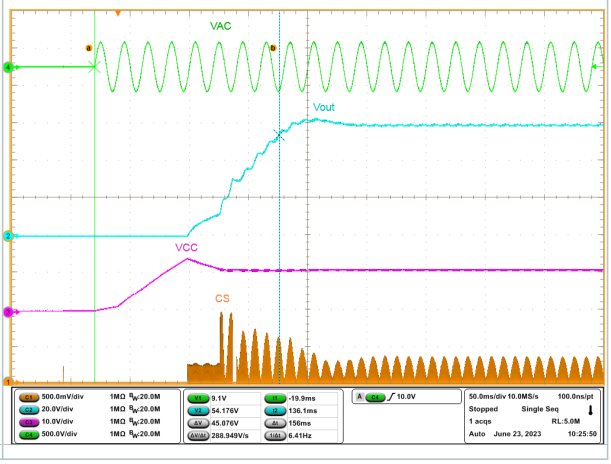


Figure 35. Start-up at 230V_{AC}, 270mW load

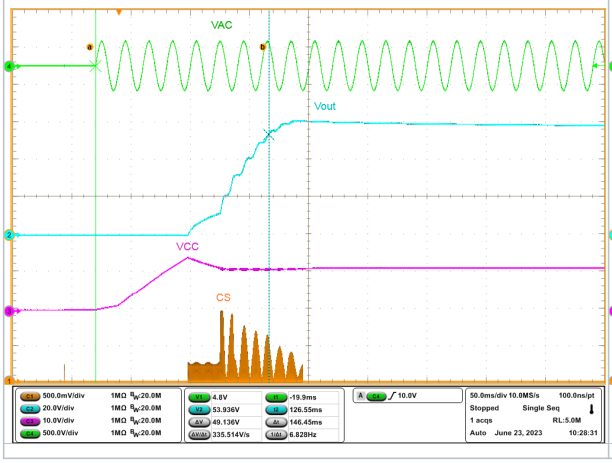
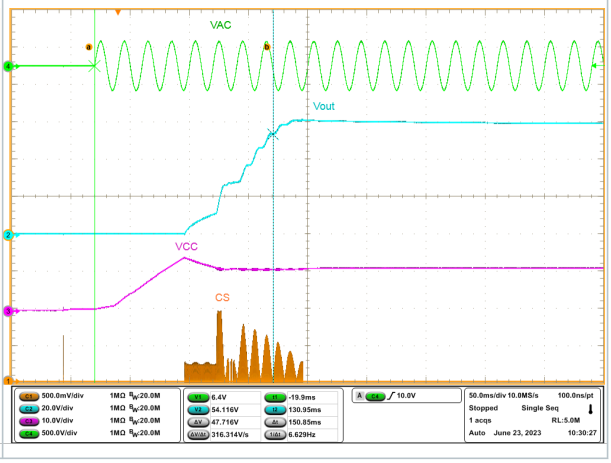


Figure 36. Start-up at 230V_{AC}, no load



6.4 Start-up at 265 V_{AC} with different load conditions

Figure 37. Start-up at 265V_{AC}, 100% load

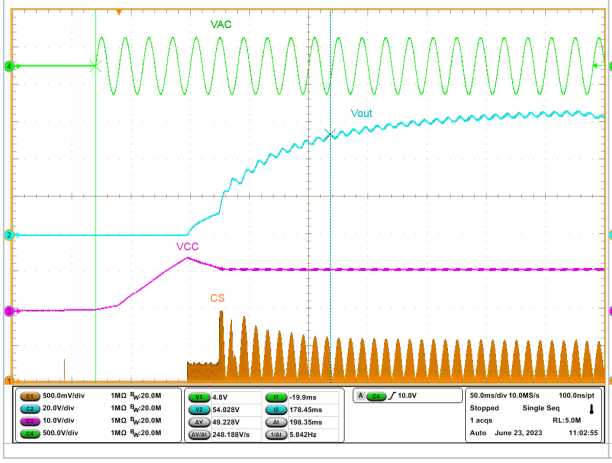


Figure 38. Start-up at 265V_{AC}, 75% load

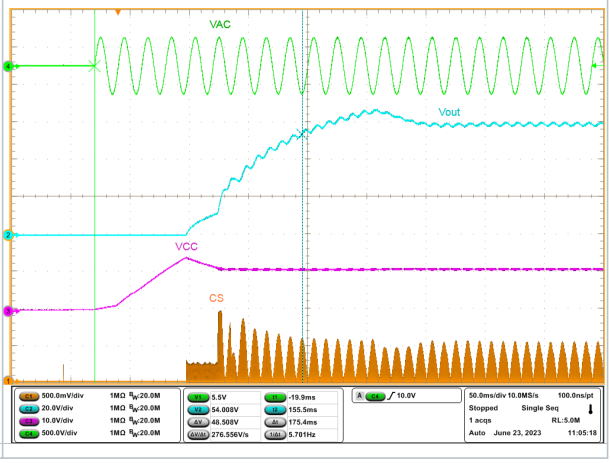


Figure 39. Start-up at 265V_{AC}, 50% load

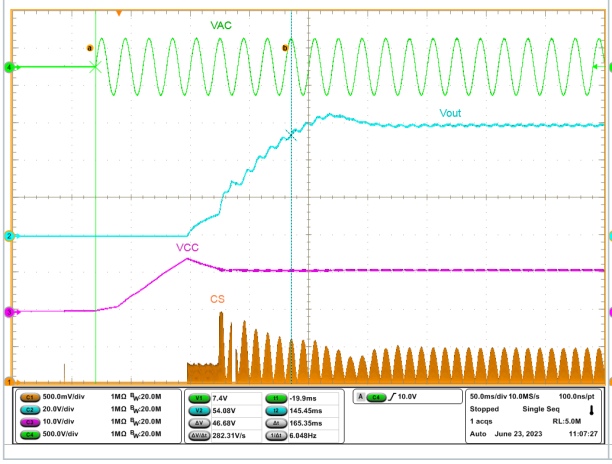


Figure 40. Start-up at 265V_{AC}, 25% load

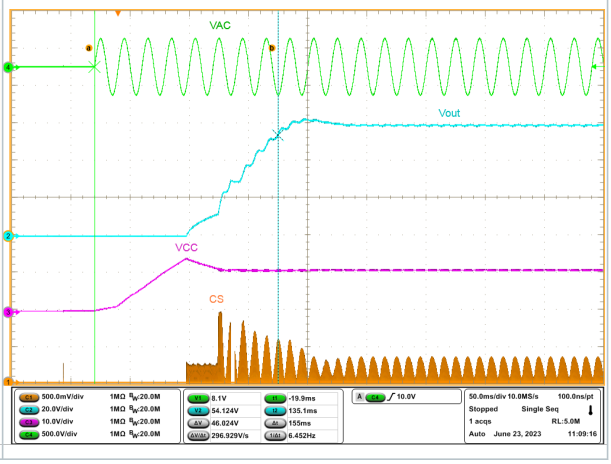


Figure 41. Start-up at 265V_{AC}, 270mW load

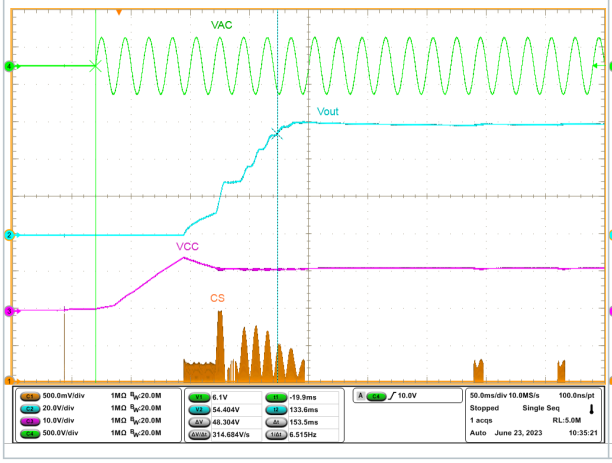
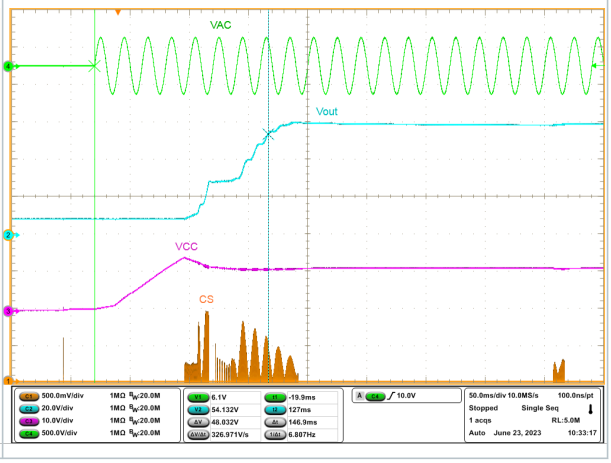


Figure 42. Start-up at 265V_{AC}, no load



7 Operation modes

The following figures show the operation modes of the HVLED101 under different conditions. The tests were performed with 115 V_{AC}/60 Hz and 230 V_{AC}/50 Hz as input voltages.

To change the mode of operation, the maximum load was slowly decreased until the minimum load value was reached (0 A), and vice versa.

Starting from the maximum load, with 115 V_{AC}, the QR mode may be observed. Then, decreasing the load, the system enters in valley skipping mode. Finally, at a very low load the device is in burst mode, and the reverse when the load is increased.

At 230 V_{AC}, the system is already in valley skipping mode (1 valley skipped) also at full load.

The number of valleys skipped is in accordance with the voltage on the VL pin.

7.1 Valley skipping mode at 115 V_{AC}

In the following figures:

CH1 – yellow = CS current sense pin

CH2 – blue = GD gate driver pin

CH3 – red = Q1 drain voltage

CH4 – green = VL pin

Figure 43. Steady state at 115V_{AC}, 100% load

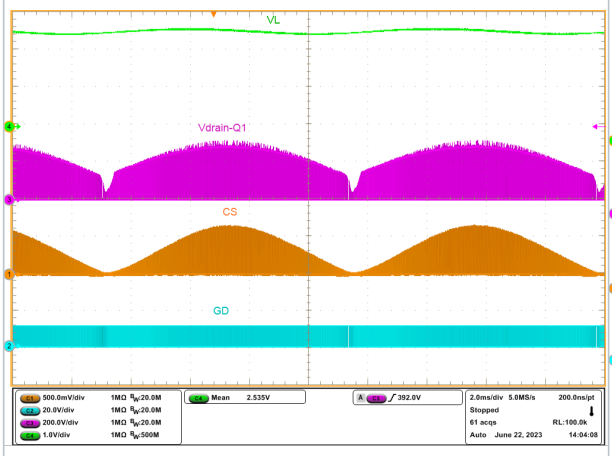


Figure 44. Steady state at 115V_{AC}, 100% load, AC peak – QR mode

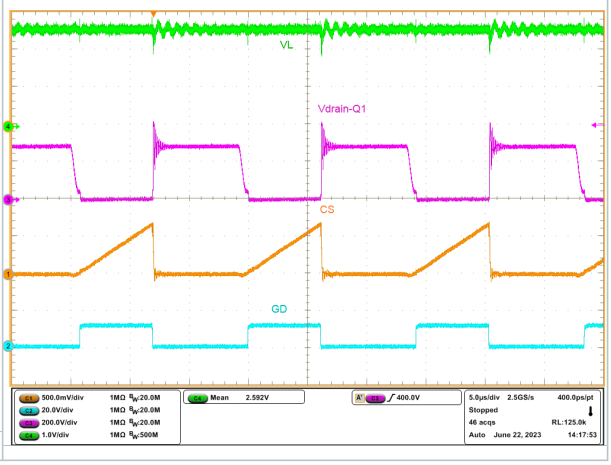


Figure 45. Steady state at 115V_{AC}, 50% load

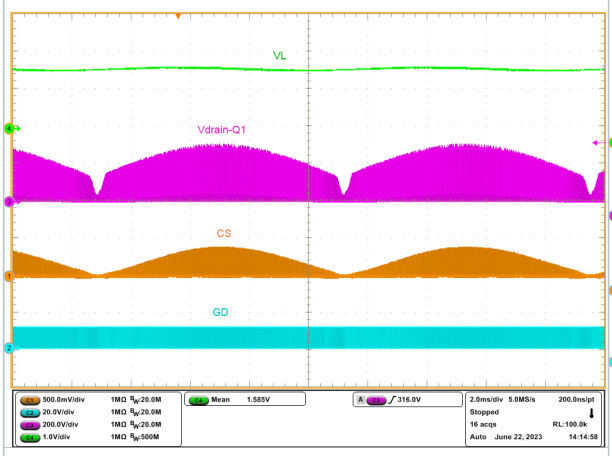


Figure 46. Steady state at 115V_{AC}, 50% load, AC peak – 1 valley skipped

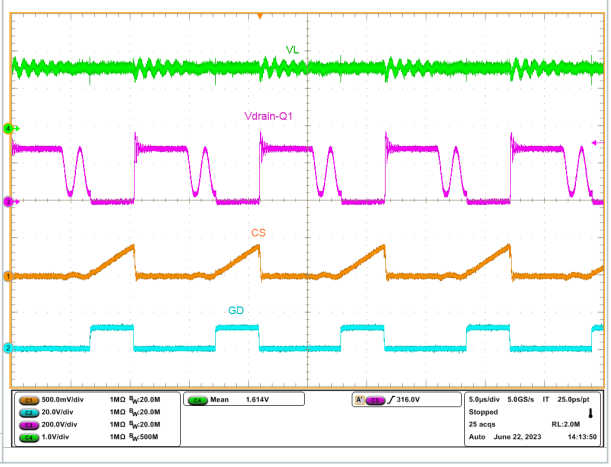


Figure 47. Steady state at $115V_{AC}$, 25% load

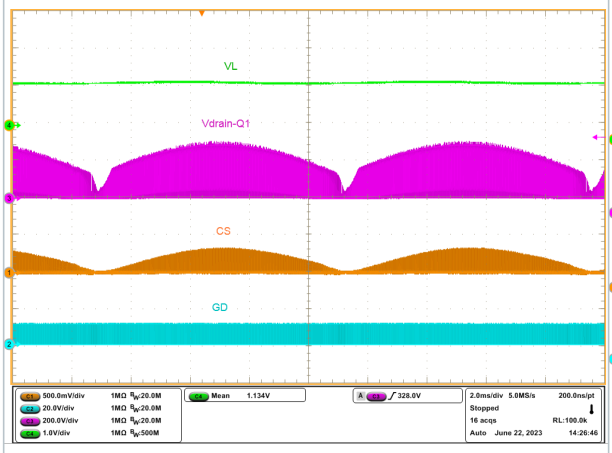


Figure 48. Steady state at $115V_{AC}$, 25% load, AC peak – 4 valleys skipped

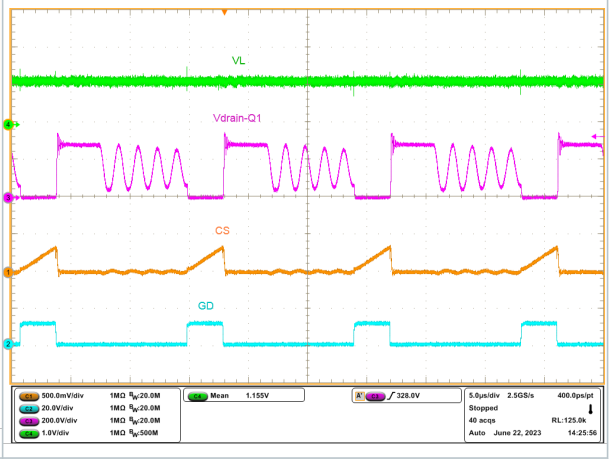


Figure 49. Steady state at $115V_{AC}$, light load (130mA)

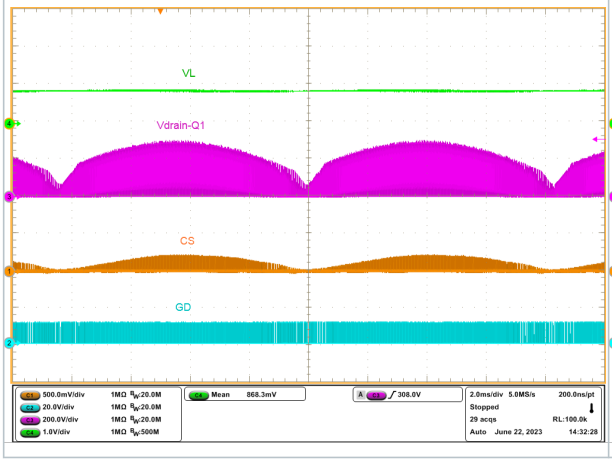


Figure 50. Steady state at $115V_{AC}$, light load (130mA), AC peak - DCM

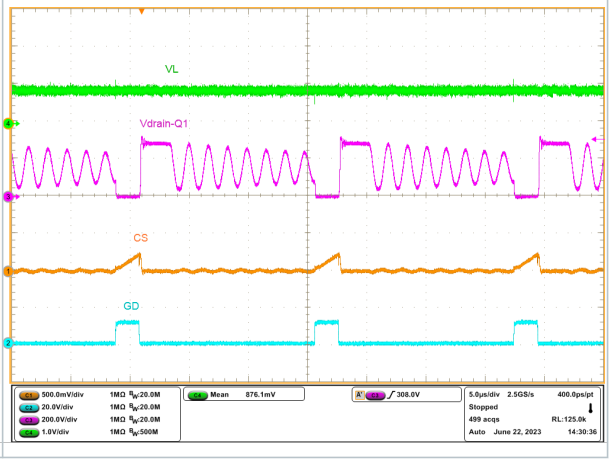


Figure 51. Burst mode at $115V_{AC}$ – 270mW

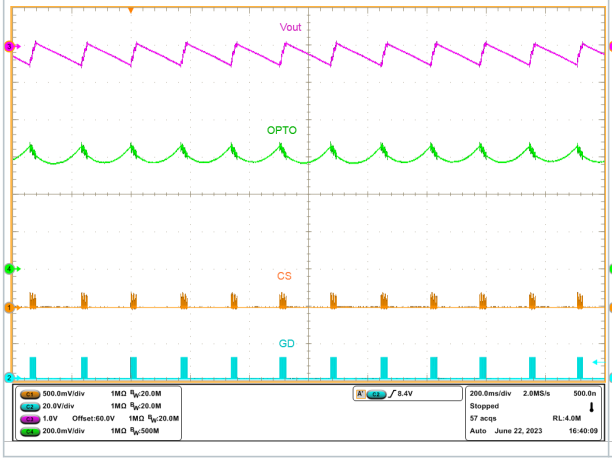
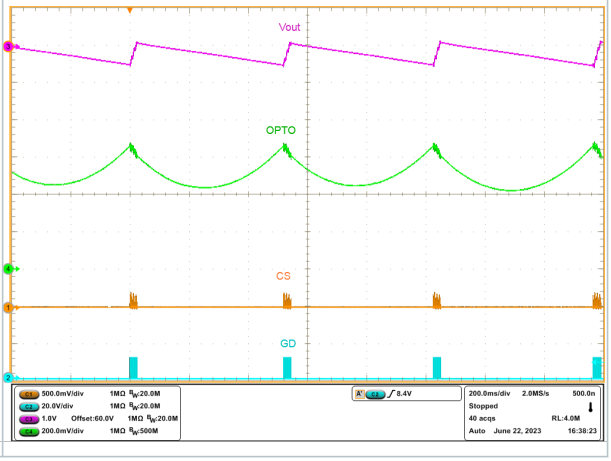


Figure 52. Burst mode at $115V_{AC}$, with no load



7.2 Valley skipping mode at 230 V_{AC}

Figure 53. Steady state at 230V_{AC}, 100% load

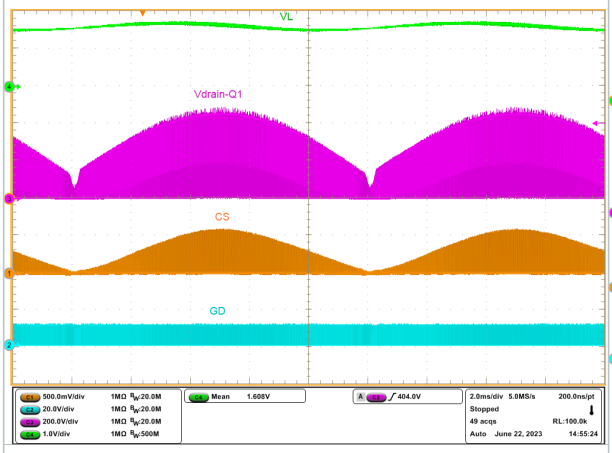


Figure 54. Steady state at 230V_{AC}, 100% load, AC peak – 1 valley skipped

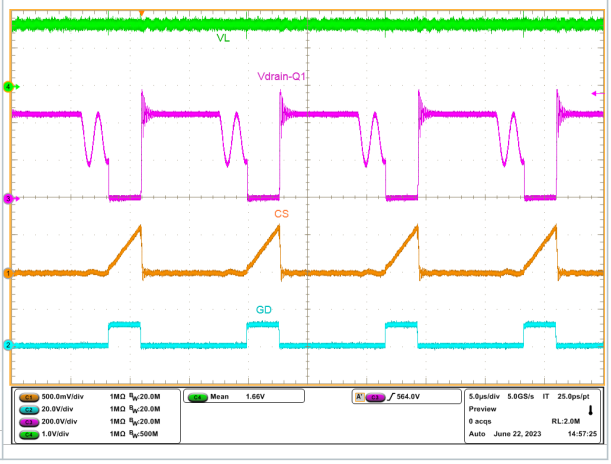


Figure 55. Steady state at 230V_{AC}, 50% load

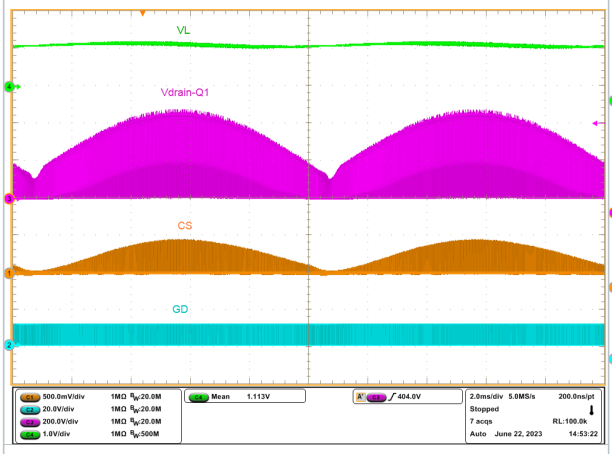


Figure 56. Steady state at 230V_{AC}, 50% load, AC peak – 4 valleys skipped

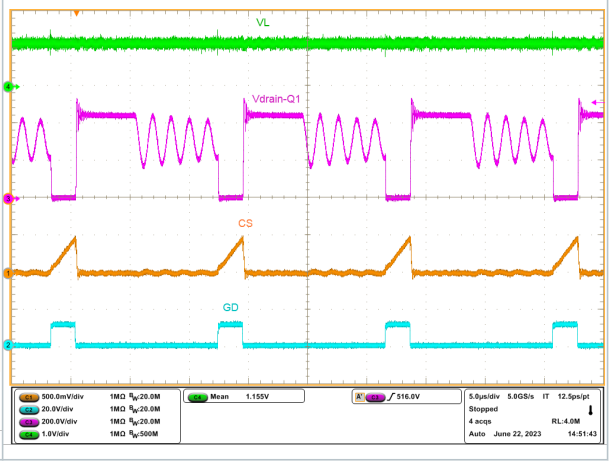


Figure 57. Steady state at 230V_{AC}, 25% load

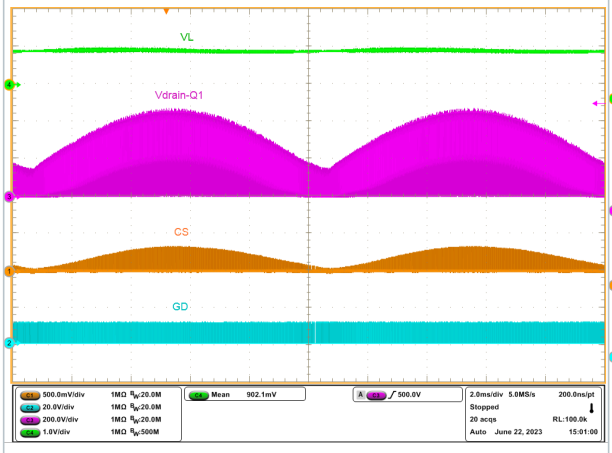


Figure 58. Steady state at 230V_{AC}, 25% load, AC peak – 5 valleys skipped

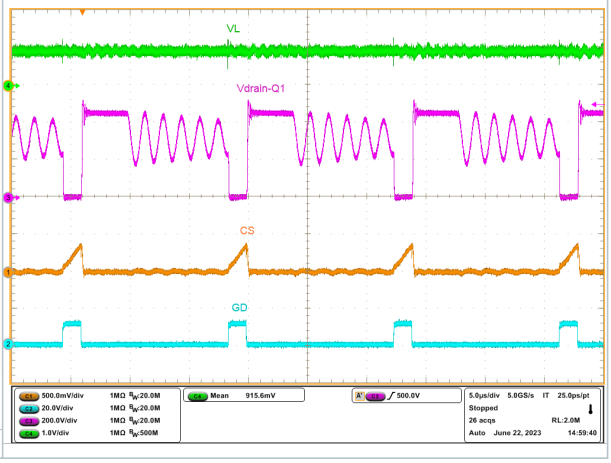


Figure 59. Steady state at 230V_{AC}, light load (100 mA)

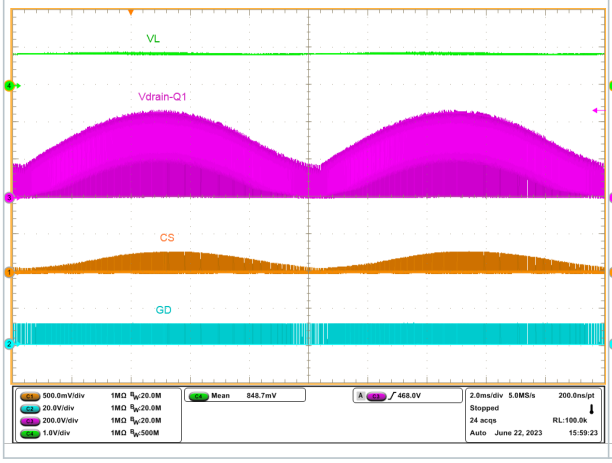


Figure 60. Steady state at 230V_{AC}, light load (100 mA), AC peak - DCM

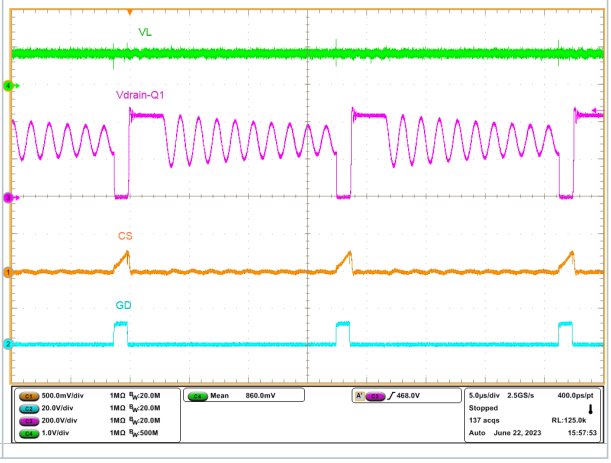


Figure 61. Burst mode at 230V_{AC} – 270mW

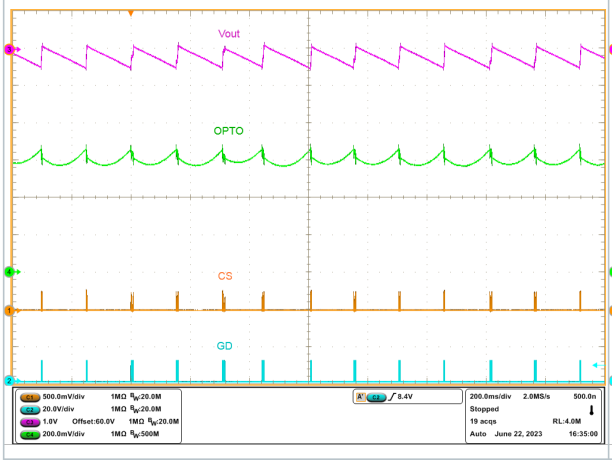
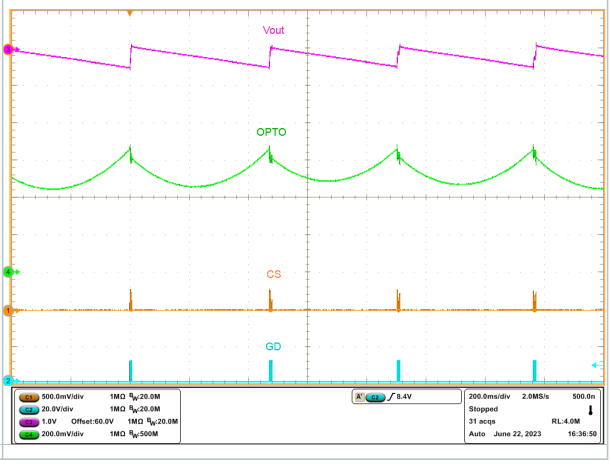


Figure 62. Burst mode at 230V_{AC}, with no load



8 Load transient 100%-10%-100%

The following figures show the load transient response waveforms of the EVLHV101SSR50W when subjected to repetitive dynamic load transitions from 100% to 10% of the load at 115 V_{AC}/60 Hz and 230 V_{AC}/50 Hz. The transition period is 1 s with a 50% duty cycle and a slew rate of 2.5 A/µs.

There are no abnormal oscillations in the output voltage, and the overshoot and undershoot are acceptable.

In the following figures:

CH3 – red = I_{OUT}

CH4 – green = V_{OUT}

Figure 63. Load transient 115V_{AC}, 100%-10%-100%

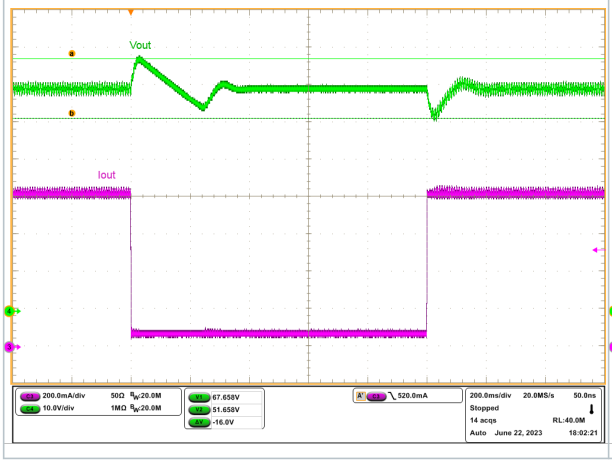
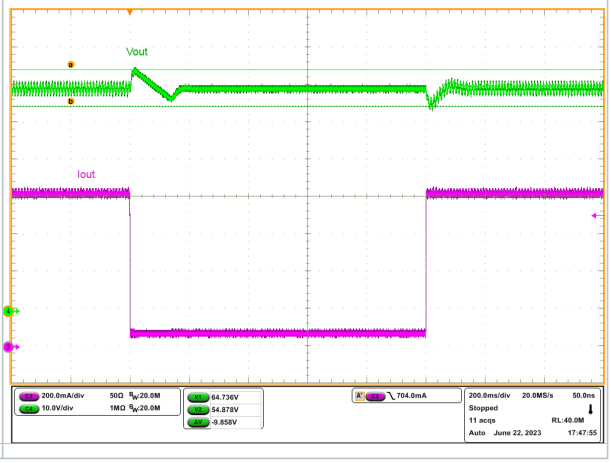


Figure 64. Load transient 230V_{AC}, 100%-10%-100%



9 Load transient 75%-25%-75%

The following figures show the load transient response waveforms of the EVLHV101SSR50W when subjected to repetitive dynamic load transitions from 75% to 25% of the load at 115 V_{AC}/60 Hz and 230 V_{AC}/50 Hz. The transition period is 1 s with a 50% duty cycle and a slew rate of 2.5 A/µs.

There are no abnormal oscillations in the output voltage and the overshoot and undershoot are acceptable.

In the following figures:

CH3 – red = I_{OUT}

CH4 – green = V_{OUT}

Figure 65. Load transient 115V_{AC}, 75%-25%-75%

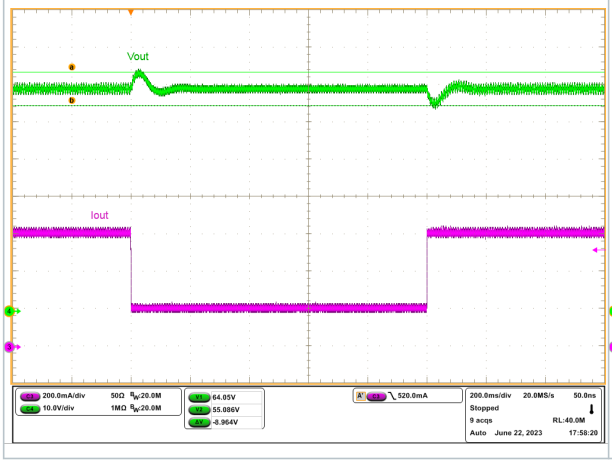
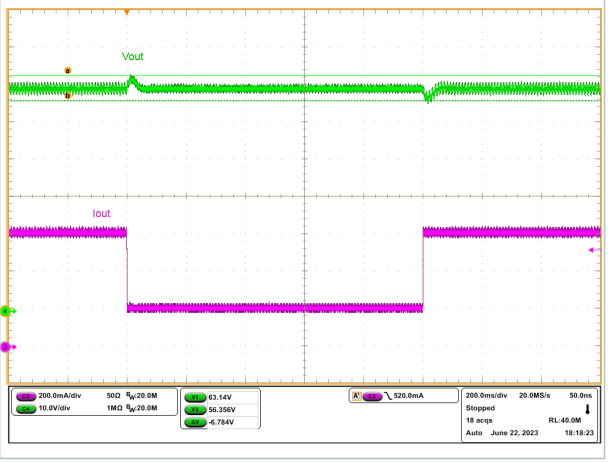


Figure 66. Load transient 230V_{AC}, 75%-25%-75%



10 Thermal measurements

A thermal analysis of the board was performed using an infrared thermal imaging camera. The test was performed at full load condition. The board underwent tests with 115 V_{AC} and 230 V_{AC} as inputs. The following figures show the thermal results 40 minutes after switching on the board.

The ambient temperature during the measurements was 25 °C.

Figure 67. Thermal map at 115V_{AC} - Top view

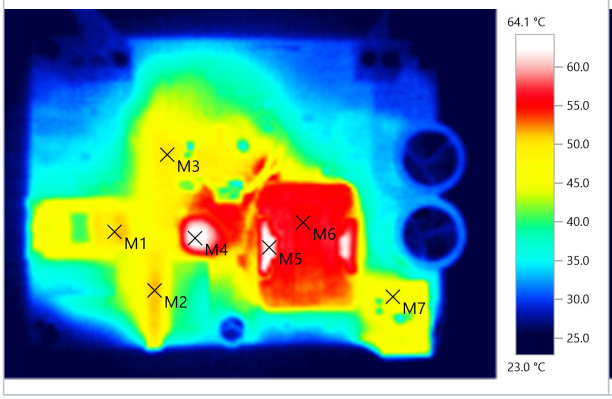


Figure 68. Thermal map at 115V_{AC} - Bottom view

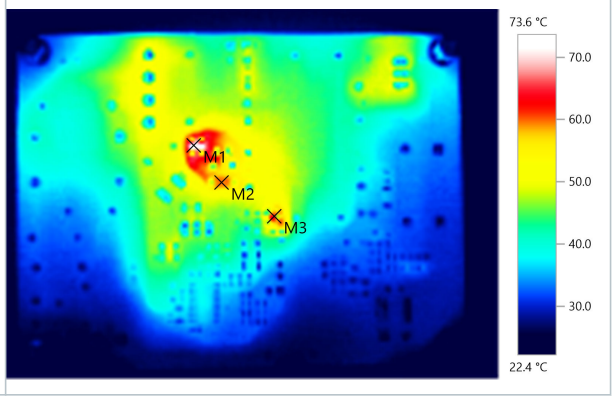


Table 12. Thermal map at 115V_{AC}

Point	Reference	Description	Temperature
Top view			
M1	L5	Common-mode choke filter	50.8°C
M2	D1	Bridge rectifier	51.4°C
M3	Q1	MOSFET	50.0°C
M4	R3 - R4	Top PCB area over R3 – R4 resistors	63.9°C
M5	T1	Transformer winding	63.4°C
M6	T1	Transformer ferrite	55.8°C
M7	D4	Diode	47.1°C
Bottom view			
M1	R3 – R4	Resistors	73.6°C
M2	D2	Diode	59.4°C
M3	D7	Diode	64.3°C

Figure 69. Thermal map at 230V$_{AC}$ - Top view

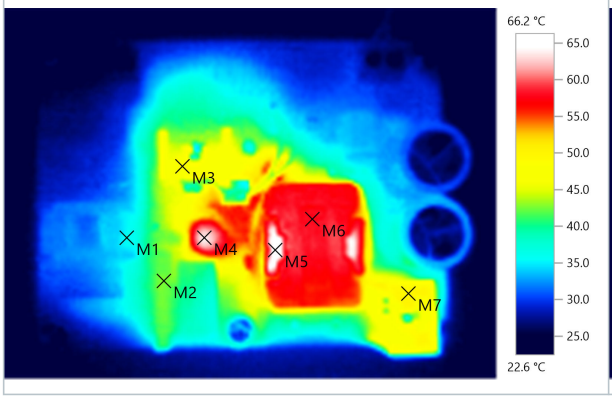


Figure 70. Thermal map at 230V$_{AC}$ - Bottom view

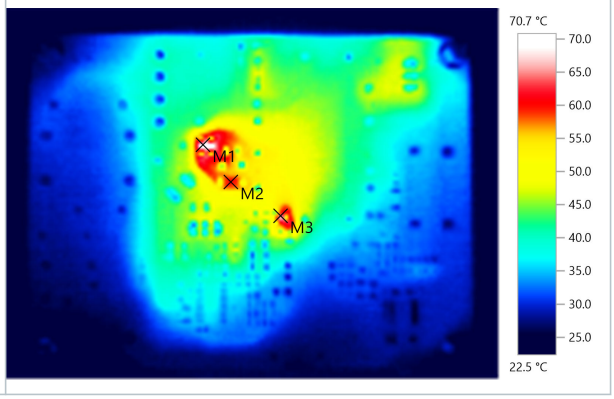


Table 13. Thermal map at 230V$_{AC}$

Point	Reference	Description	Temperature
Top view			
M1	L5	Common-mode choke filter	36.7°C
M2	D1	Bridge rectifier	42.6°C
M3	Q1	MOSFET	47.3°C
M4	R3 - R4	Top PCB area over R3 – R4 resistors	63.7°C
M5	T1	Transformer winding	65.8°C
M6	T1	Transformer ferrite	58.2°C
M7	D4	Diode	49.2°C
Bottom view			
M1	R3 – R4	Resistors	70.7°C
M2	D2	Diode	59.7°C
M3	D3	Diode	64.7°C

11 EMI measurement

The following figures show the measurements of the conducted emissions with an average mode detection with 115 V_{AC} and 230 V_{AC} as inputs.

Figure 71. EMI tests at 115V_{AC} (output: 60V - 833mA)

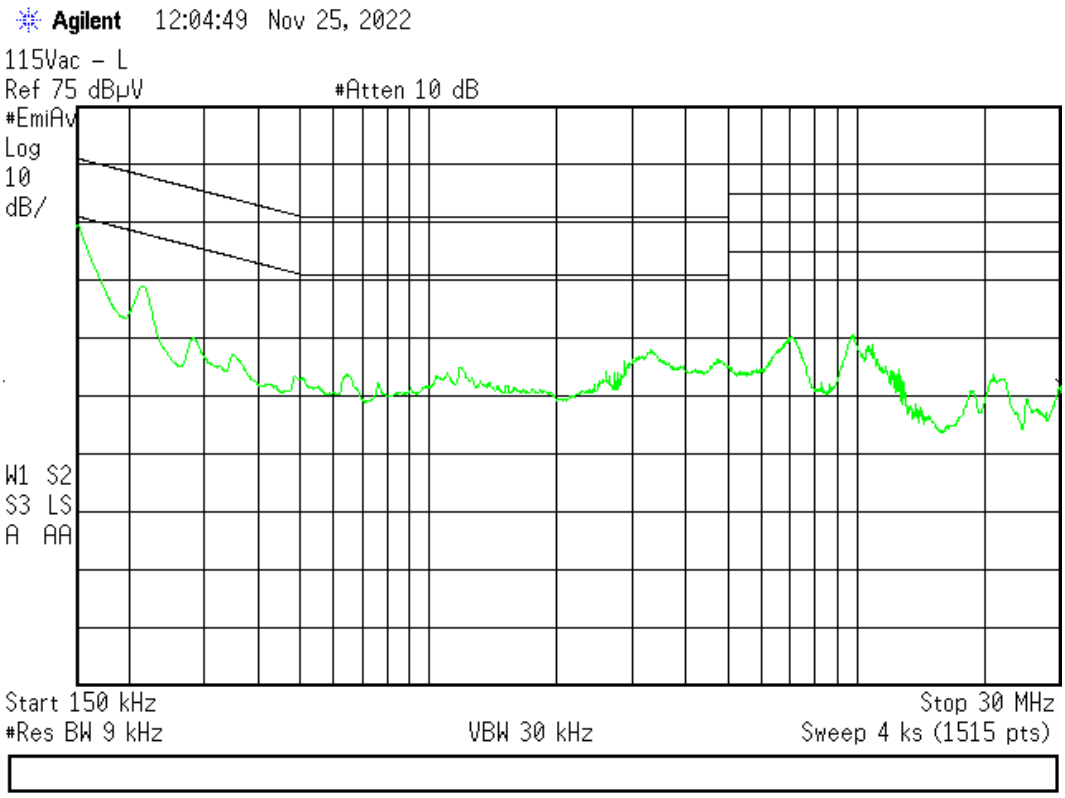
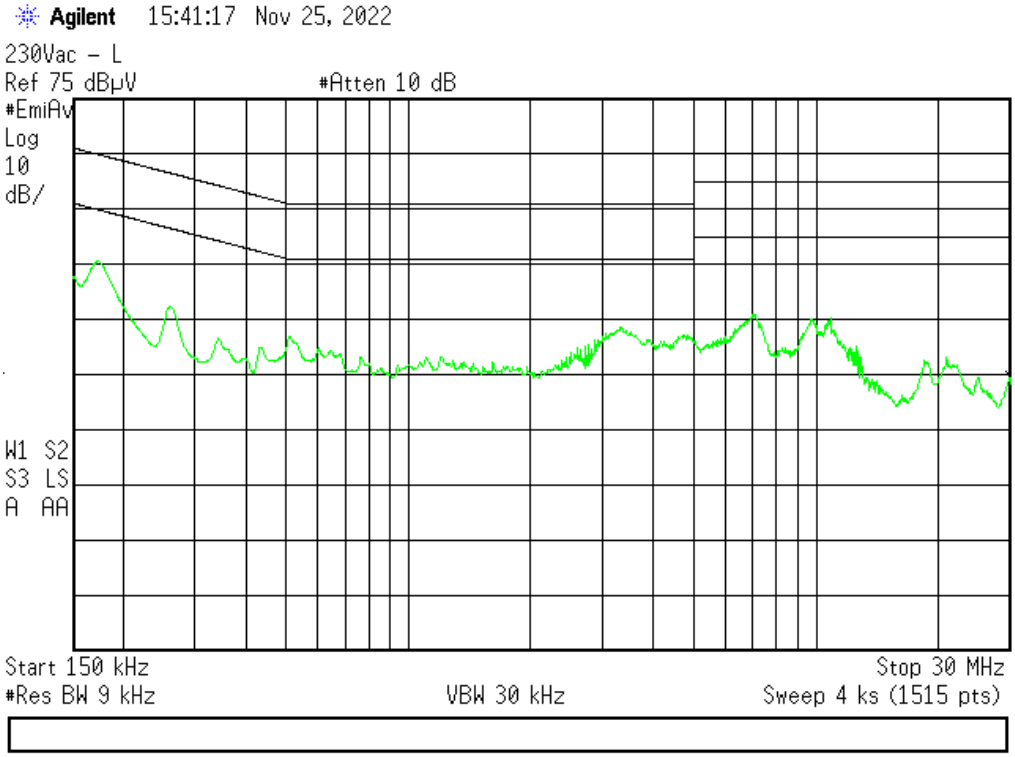


Figure 72. **EMI tests at 230V_{AC} (output: 60V - 833mA)**



12 References

1. HVLED101 Datasheet, see www.st.com
2. AN4932, HVLED001A - enhanced QR high power factor flyback controller for LED drivers, see www.st.com
3. AN5316, 35 W wide input range flyback converter using HVLED001B quasi-resonant flyback controller and STF10LN80K5 see www.st.com
4. AN1059, design equations of high-power-factor flyback converters based on the L6561, see www.st.com

Revision history

Table 14. **Document revision history**

Date	Version	Changes
10-Oct-2023	1	Initial release.

Contents

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