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Application note

Migrating from STM32L1 to STM32U0 MCUs

Introduction

For designers of STM32 microcontroller applications, being able to replace one microcontroller type with another from the same product family easily is an important asset. Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note analyzes the steps required to migrate an existing design from the STM32L1 series to the STM32U0 series. Three aspects need to be considered for the migration: hardware, peripherals, and firmware.

This document lists the full set of features available for the STM32L1 series and the equivalent features on the STM32U0 series (some products may have fewer features depending on their part number).

To benefit fully from this application note, the user must be familiar with the STM32 microcontroller documentation available on www.st.com, with a particular focus on the documents listed below:

- STM32L1 series datasheets.
- STM32U0 series datasheets.
- *STM32L100xx, STM32L151xx, STM32L152xx and STM32L162xx advanced Arm®-based 32-bit MCUs* reference manual (RM0038).
- STM32U0xxx reference manual (RM0503).

1 STM32U0 series overview

The STM32U0 series devices are a perfect fit in terms of ultra-low power, performance, memory size, and peripherals at a cost-effective price.

In particular, STM32U0 series devices offer higher frequency and performance operations than STM32L1 series devices. The STM32U0 series features an Arm® Cortex®-M0+ processor at 56 MHz, versus a Cortex®-M3 processor at 32 MHz featured on the STM32L1 series. STM32U0 devices also feature optimized flash memory access through the adaptive real-time memory accelerator (Chrom-ART Accelerator).

STM32U0 series MCUs increase the low-power efficiency in dynamic mode (µA/MHz), and reach a very low level of static power consumption on the various available low-power modes.

The detailed list of available features and packages for each product is available in the respective datasheets.

STM32U0 series devices include a larger set of peripherals with advanced features compared to the STM32L1 series, such as:

- Touch sensing controller (TSC).
- Low-power universal asynchronous receiver transmitter (LPUART)
- Infrared interface (IRTIM).
- Low-power timer (LPTIM).
- Voltage reference buffer (VREFBUF).
- DMA request multiplexer (DMAMUX).
- Clock recovery system (CRS) for USB.
- SRAM1 size is different on the various STM32U0 devices:
  - 32 Kbytes for STM32U0x3.
  - 8 Kbytes for STM32U0x1.
- Additional SRAM2 with data preservation in Standby mode:
  - 8 Kbytes for STM32U0x3.
  - 4 Kbytes for STM32U0x1.
- Optimized power consumption and an enriched set of low-power modes.

This migration guide covers only the migration from the STM32L1 series to the STM32U0 series, and as a consequence any new features present on the STM32U0 series but not already present on the STM32L1 series are not covered by this document. Refer to the STM32U0 reference manuals and datasheets for an exhaustive picture.

Table 1. STM32U0 memory availability

Part number	Flash memory size	SRAM1	SRAM2	Feature level
STM32U031x4	16 Kbytes	8 Kbytes	4 Kbytes	-
STM32U031x6	32 Kbytes			
STM32U031x8	64 Kbytes			
STM32U073x8	64 Kbytes	32 Kbytes	8 Kbytes	With LCD + USB.
STM32U083x8				STM32U073 with crypto.
STM32U073xB	128 Kbytes			With LCD + USB.
STM32U083xB				STM32U073 with crypto.
STM32U073xC	256 Kbytes			With LCD + USB.
STM32U083xC				STM32U073 with crypto.

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2 Hardware migration

2.1 Package availability

Some packages are available for both the STM32U0 and STM32L1 series, such as UFQFPN48 and LQFP64. The other packages available for the STM32L1 series are not available on the STM32U0 series. The STM32U0 series also brings new packages that are not available on the STM32L1 series.

Note that the WLCSP packages are not equivalent and have different die sizes for each product.

The table below lists the available packages for the STM32U0 series.

Table 2. Available packages for the STM32U0 series

Package	STM32U083xx	STM32U073xx	STM32U031xx	Size (mm x mm)
TSSOP20	-	-	X	6.5 x 4.4
UFQFPN32	X	X	X	5 x 5
LQFP48	X	X	X	7 x 7
LQFP64	X	X	X	10 x 10
UFQFPN48	X	X	X	7 x 7
UFBGA64	X	X	X	5 x 5
LQFP80	X	X	-	12 x 12
UFBGA81	X	X	-	5 x 5
WLCSP27	-	-	X	2.55 x 2.34
WLCSP42	X	X	-	2.82 x 2.93

2.2 Pin compatibility

The STM32U0 and STM32L1 series share a high level of pin compatibility. Most peripherals share the same pins in the two series, rendering the transition from an STM32L1 device to an STM32U0 device very straightforward. Due to the shared use of GPIOs using system pins, STM32U0 offers two additional GPIOs on the same package.

There are a few exceptions to take into consideration. The STM32U0 series TSC group assignment is different from that of the STM32L1 series, so applications using TSC require a PCB redesign. The STM32U0 ADC channels are connected to the same pins as for the STM32L1 series, but with different channel numbers. Refer to the product datasheet for more details.

Table 3. Pinout differences between STM32L1 and STM32U0 series (QFP)

STM32L1 series			STM32U0 series		
UFQFPN48/ LQFP48	LQFP64	Pinout	UFQFPN48/ LQFP48	LQFP64	Pinout
1	1	VLCD	1	1	VBAT
7	7	NRST	7	7	PF2-NRST(2)
9	13	VDDA	9	13	VDDA/VREF+
36	48	VDD	36	48	VDDUSB(1)
44	60	BOOT0	44	60	PF3-BOOT0(2)

1. *The VDDUSB pin can be connected externally to VDD.*
2. *System pins can also be used as GPIO.*

Table 4. Pinout differences between STM32L1 and STM32U0 series (BGA)

STM32L1 series		STM32U0 series	
UFBGA64	Pinout	UFBGA64	Pinout
B2	VLCD	B2	VBAT
G1	VREF+	G1	PC3
E5	VDD	E5	VDDUSB(1)
H1	VDDA	H1	VDDA/VREF+
B4	BOOT0	B4	PF3-BOOT0(2)
E1	NRST	E1	PF2-NRST(2)

1. *The VDDUSB pin can be connected externally to VDD.*
2. *System pins can also be used as GPIO.*

2.3 Recommendations for board migration

The VLCD pin in the STM32U0 series is now multiplexed on the PC3 GPIO through alternate function programming. The PC3 GPIO is located at pin 13 on LQFP80, pin 11 on LQFP64, and pin G1 on BGA64/BGA81.

This implies that any other function in the STM32U0 devices PC3 pins cannot be used on PC3 when the LCD is used by the application. It also implies that the related STM32L1 series PC3 alternate functions, if they are used by the application, must be mapped to other STM32U0 series pins.

The V_{BAT} or V_{DD} supply (if no specific V_{BAT} power is used), must now be connected to:

- Pin 1 (LQFP64/LQFP48)
- Pin B1 (BGA81)
- Pin B2 (BGA64)

On the BGA64 package, the G1 ball used for the VREF+ signal in the STM32L1 series is used as the PC3 GPIO (multiplexed with VLCD) in the STM32U0 series, and the VREF+ signal is bonded with VDDA on the H1 ball.

The boot pins are different in both families. The BOOT0 is multiplexed with the PF3 GPIO on the STM32U0. Refer to Section 3: Boot mode selection for details. Those changes do not impact the board design.

The NRST pin is multiplexed with the PF2 pin, referred to as PF2-NRST.

Note: The GPIOF port replaces the GPIOH port.

Note: New packages (LQFP80 and UFBGA81) have been introduced for the STM32U0 series.

3 Boot mode selection

Both the STM32L1 and STM32U0 series offer three different boot modes: boot from the main flash memory, boot from SRAM, or boot from the system memory. However, the way to select the boot mode differs between the products:

- On STM32L1 devices, the boot mode is selected using two pins: BOOT0 and BOOT1.
- On STM32U0 devices, the boot mode is selected using the nBOOT1 option bit with the BOOT0 pin or the nBOOT0 option bit, depending on the value of the nBOOT_SEL option bit in the FLASH_OPTR register. Additionaly, the BOOT_LOCK bit is available to increase application security. It forces the main flash memory as a boot memory area, and requires support in the firmware to connect the debug interface when the RDP level is not 0.

The tables below show the different configurations available for selecting the boot mode for STM32U0 and STM32L1 devices.

Table 5. Boot modes for STM32L1 devices

Boot mode selection		Boot mode	Aliasing
BOOT1 pin	BOOT2 pin		
X	0	Main flash memory	Main flash memory is selected as boot space.
0	1	System memory	System memory is selected as boot space.
1	1	Embedded SRAM	Embedded SRAM is selected as boot space.

Table 6. Boot modes for STM32U0 deivces

Boot mode configuration					Selected boot area
BOOT_LOCK bit	nBOOT1 bit	BOOT0 pin	nBOOT_SEL bit	nBOOT0_bit	
0	X	0	0	X	Main flash memory
0	1	1	0	X	System memory
0	0	1	0	X	Embedded SRAM
0	X	X	1	1	Main flash memory
0	1	X	1	0	System memory
0	0	X	1	0	Embedded SRAM
1	X	X	X	X	Main flash memory forced

3.1 Embedded bootloader

The embedded bootloader is located in the system memory, programmed by STMicroelectronics during production. This bootloader is used to reprogram the flash memory using one of the serial interfaces listed in the table below (where X = supported).

Table 7. Bootloader interfaces on the STM32L1 and STM32U0 series

Peripheral	Pin	STM32L1 series	STM32U0 series
DFU	USB_DM (PA11) USB_DP (PA12)	X	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	X	-
USART2	USART2_TX (PA2) USART2_RX (PA3)	-	X
USART3	USART3_TX (PC10) USART3_RX (PC11)	-	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	-	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	-	X
I2C3	I2C3_SCL (PB3) I2C3_SDA (PB4)	-	X
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	-	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	-	X

Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details on the bootloader.

For smaller packages, it is important to check the pin and peripheral availability.

4 Peripheral migration

4.1 STM32 product cross-compatibility

STM32 MCUs embed a set of peripherals that can be classified in three groups:

- The first group is for the peripherals that are common to all products. Those peripherals have the same structure, registers, and control bits. There is no need to perform any firmware changes to keep the same functionality at the application level after migration. Peripheral features and behavior remain the same across devices.
- The second group is for the peripherals that present minor differences from one product to another (usually due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third group is for peripherals that have been considerably modified from one product to another (new architecture or new features, for instance). For this group of peripherals, the migration requires a new development at application level.

The table below gives a general overview of this classification. The software compatibility mentioned in the table refers only to the register description for low-level drivers.

The STM32Cube hardware abstraction layer (HAL) is compatible between the STM32L1 series and the STM32U0 series.

Table 8. Peripheral compatibility analysis between STM32L1 series and STM32U0 series

Peripheral	Number of instances in STM32			Compatibility with STM32U0 series		
	STM32L1	STM32U073xx/83xx	STM32U031xx	Software	Pinout	Comments
SPI	3	3	2	Partial		• I2S is no longer supported by SPI on the STM32U0 series. • Some alternate functions are not mapped on the same GPIO for SPI1.
I2S (full duplex)	2	0				
WWDG	1	1		Full	NA	-
IWDG	1	1		Full		
DBGMCU	1	1		Full		
CRC	1	1		Partial		Additional features on the STM32U0 series.
EXTI	1	1			Full	-
USB FS	1	1	0			Additional features on the STM32U0 series.
DMA	1	2	1	Full	NA	• Same features. • DMA mapping request may differ (see Section 4.3: Direct memory access controller (DMA)).
TIM	-	-	-	Full	Partial	• Some pins are not mapped on the same GPIO. • Timer instance names may differ. • Internal connections may differ.
Basic	2	2	2			
General Purpose	7	4	4			
Advanced	0	1	1			
Low-power	0	3	2			
IRTIM	0	1	1			
SDIO	1	0		NA	NA	-
FSMC/FMC	1	0	0			-
PWR	1	1		Partial	NA	-

Peripheral	Number of instances in STM32			Compatibility with STM32U0 series		
	STM32L1	STM32U073xx/83xx	STM32U031xx	Software	Pinout	Comments
RCC	1	1			NA	-
USART **UART** **LPUART**	3 2 0	4 0 3	4 0 2	Partial		• Additional features on the STM32U0 series. • Additional LPUART on the STM32U0 series.
I2C	2	4	3	None	Full	Additional features on the STM32U0 series.
DAC channels	2	1		Partial		• Additional features on the STM32U0 series. • Software compatible except for output buffer management.
ADC	1	1		None	Partial	• Additional features on the STM32U0 series. • Different channels are mapped on the same GPIO.
RTC	1	1		Partial	Full	• Additional features on the STM32U0 series. • Can be powered by V_{BAT} on the STM32U0 series.
FLASH	1	1		None	NA	New peripheral.
GPIO	Up to 115 IOs	Up to 69 IOs	Up to 53 IOs	Full	Partial	• On reset, the STM32L1 series is configured in input-floating mode while the STM32U0 series is configured in analog mode to reduce consumption. • A few changes, mentioned in Section 2: Hardware migration.
LCD controller	1	1	0			• VLCD muxed on PC3 GPIO. • SEG21 mapped on a different GPIO. • Additional features on the STM32U0 series.
COMP	2	2	1	None		Some pins are mapped on different GPIOs.
SYSCFG	1	1		Partial	NA	-
AES	1	1 (on STM32U083xx only)	0	Full		-
OPAMP	3	1	1	None	Partial	Some pins are mapped on different GPIOs.

4.2 Memory mapping

The peripheral address mapping has been changed in the STM32U0 series compared to theSTM32L1 series.

The table below provides the peripheral address mapping differences between the STM32L1 and STM32U0 series.

Table 9. Peripheral address mapping differences between STM32L1 and STM32U0 series

Peripheral	STM32L1 series		STM32U0	
	Bus	Base address	Bus	Base address
FSMC/FMC	AHB	0xA0000000	AHB	NA
AES		0x50060000		0x40026000
DMAMUX		NA		0x40020800
DMA2		0x40026400		0x40020400
DMA1		0x40026000		0x40020000
Flash memory interface		0x40023C00		0x40022000
RCC		0x40023800		0x40021000
CRC		0x40023000		0x40023000
GPIOH		0x40021400		NA
GPIOG		0x40021C00		NA
GPIOF		0x40021800		0x50001400
GPIOE		0x40021000		0x50001000
GPIOD		0x40020C00		0x50000C00
GPIOC		0x40020800		0x50000800
GPIOB		0x40020400		0x50000400
GPIOA		0x40020000		0x50000000
USART1	APB2	0x40013800	APB	0x40013800
SPI1		0x40013000		0x40013000
SDIO		0x40012C00		NA
ADC1		0x40012400		0x40012400
TIM11		0x40011000		NA
TIM10		0x40010C00		
TIM9		0x40010800		
EXTI		0x40010400		0x40010400
SYSCFG		0x40010000		0x40010000
COMP	APB1	0x40007C00		0x40010200
RI		0x40007C04		NA
OPAMP		0x40007C5C		0x40007800
DAC		0x40007400		0x40007400
PWR		0x40007000		0x40007000
USB device FS SRAM		0x40006000		0x40009800
USB device FS		0x40005C00		0x40006800
I2C2		0x40005800		0x40005800
I2C1		0x40005400		0x40005400
USART5		0x40005000		NA
USART4		0x40004C00		0x40004C00
USART3		0x40004800		0x40004800
USART2		0x40004400		0x40004400
SPI3		0x40003C00		0x40003C00

Peripheral	STM32L1 series		STM32U0	
	Bus	Base address	Bus	Base address
SPI2	APB1	0x40003800	APB	0x40003800
IWDG		0x40003000		0x40003000
WWDG		0x40002C00		0x40002C00
RTC (inc. BKP registers)		0x40002800		0x40002800
LCD		0x40002400		0x40002400
TIM7		0x40001400		0x40001400
TIM6		0x40001000		0x40001000
TIM5		0x40000C00		NA
TIM4		0x40000800		NA
TIM3		0x40000400		0x40000400
TIM2		0x40000000		0x40000000
RNG	NA			0x50060800
USB				0x40005C00
TSC				0x40024000
TIM16				0x40014400
TIM15				0x40014000
TIM1				0x40012C00
VREF				0x40010030
LPTIM2				0x40009400
LPTIM3				0x40009000
LPUART3				0x40008C00
I2C3				0x40008800
LPUART2				0x40008400
LPUART1				0x40008000
LPTIM1				0x40007C00
CRS				0x40006C00

The system memory mapping has been updated between the STM32L1 series and STM32U0 series. Refer to the reference manuals and datasheets for more details.

The STM32U0 series features an additional SRAM (SRAM2) of the following size:

- 8 Kbytes on STM32U073xx/83xx devices.
- 4 Kbytes on STM32U031xx devices.

SRAM2 includes the additional features listed below:

- Maximum performance through I-Code bus access without physical remap.
- Parity check option (32-bit + 4-bit parity check).
- Write protection with 1 Kbyte granularity.
- Read protection (RDP).
- Erase by system reset (option byte) or by software.
- Content preserved in Low-power run, Low-power sleep, Stop 0, Stop 1, and Stop 2 modes.
- Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1).

Bit-banding

Both the STM32L1 and STM32U0 series support bit-banding on the lowest 1 Mbyte of the SRAM and on the peripheral memory region. However, the peripherals mapped in this bit-banding region are different for each series.

Detail of the peripherals that are accessible with bit-banding:

- STM32L1 series: all peripherals except AES and FSMC.
- STM32U0 series: all peripherals except GPIOx, ADC, AES, and RNG.

4.3 Direct memory access controller (DMA)

STM32U0 embeds DMAMUX, extending the capabilities of the regular DMA present in STM32L1 products. For the DMA in the STM32L1 series, each channel is dedicated to managing the memory access requests from one or more peripherals and has an arbiter for handling the priorities among the DMA requests.

For the STM32U0 series, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer, providing a high level of flexibility.

The DMAMUX request multiplexer allows a DMA request line to be routed between the peripherals and the DMA controllers of the product. The routing function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs.

The table below presents the differences between the DMA requests of the peripherals in the STM32L1 series and the peripherals in the STM32U0 series.

Table 10. DMA request differences between STM32L1 and STM32U0 series

Peripheral	DMA request	STM32L1 series	STM32U0 series
ADC	ADC1	DMA1_Channel1	DMAMUX request 5
DAC	DAC1_CH1	DMA1_Channel3	DMAMUX request 8
	DAC1_CH2	DMA1_Channel3	NA
SPI1	SPI1_RX	DMA1_Channel2	DMAMUX request 36
	SPI1_TX	DMA1_Channel3	DMAMUX request 37
SPI2	SPI2_RX	DMA1_Channel4	DMAMUX request 38
	SPI2_TX	DMA1_Channel5	DMAMUX request 38
SPI3	SPI3_RX	DMA2_Channel1	DMAMUX request 40
	SPI3_TX	DMA2_Channel2	DMAMUX request 41
USART1	USART1_RX	DMA1_Channel5	DMAMUX request 69
	USART1_TX	DMA1_Channel4	DMAMUX request 70
USART2	USART2_RX	DMA1_Channel6	DMAMUX request 71
	USART2_TX	DMA1_Channel7	DMAMUX request 72
USART3	USART3_RX	DMA1_Channel3	DMAMUX request 73
	USART3_TX	DMA1_Channel2	DMAMUX request 74
UART4	UART4_RX	DMA2_Channel3	DMAMUX request 75
	UART4_TX	DMA2_Channel5	DMAMUX request 76
UART5	UART5_RX	DMA2_Channel2	NA
	UART5_TX	DMA2_Channel1	
LPUART1	LPUART1_RX	NA	DMAMUX request 30
	LPUART1_TX		DMAMUX request 31
LPUART2	LPUART2_RX		DMAMUX request 32
	LPUART2_TX		DMAMUX request 33

Peripheral	DMA request	STM32L1 series	STM32U0 series
LPUART3	LPUART3_RX	NA	DMAMUX request 34
	LPUART3_TX		DMAMUX request 35
I2C1	I2C1_RX	DMA1_Channel7	DMAMUX request 9
	I2C1_TX	DMA1_Channel6	DMAMUX request 10
I2C2	I2C2_RX	DMA1_Channel5	DMAMUX request 11
	I2C2_TX	DMA1_Channel4	DMAMUX request 12
I2C3	I2C3_RX	NA	DMAMUX request 13
	I2C3_TX		DMAMUX request 14
I2C4	I2C4_RX		DMAMUX request 15
	I2C4_TX		DMAMUX request 16
SDIO SDMMC	SDIO	DMA2_Channel4	NA
TIM1	TIM1_CH1	NA	DMAMUX request 42
	TIM1_CH2		DMAMUX request 43
	TIM1_CH3		DMAMUX request 44
	TIM1_CH4		DMAMUX request 45
	TIM1_TRIG_UP		DMAMUX request 46
	TIM1_UP		DMAMUX request 47
TIM2	TIM2_CH1	DMA1_Channel5	DMAMUX request 48
	TIM2_CH2	DMA1_Channel7	DMAMUX request 49
	TIM2_CH3	DMA1_Channel1	DMAMUX request 50
	TIM2_CH4	DMA1_Channel7	DMAMUX request 51
	TIM2_TRIG	NA	DMAMUX request 52
	TIM2_UP	DMA1_Channel2	DMAMUX request 53
TIM3	TIM3_CH1	DMA1_Channel6	DMAMUX request 54
	TIM3_CH2	NA	DMAMUX request 55
	TIM3_CH3	DMA1_Channel2	DMAMUX request 56
	TIM3_CH4	DMA1_Channel3	DMAMUX request 57
	TIM3_TRIG	DMA1_Channel6	DMAMUX request 58
	TIM3_UP	DMA1_Channel3	DMAMUX request 59
TIM4	TIM4_UP	DMA1_Channel7	NA
	TIM4_CH1	DMA1_Channel1	
	TIM4_CH2	DMA1_Channel4	
	TIM4_CH3	DMA1_Channel5	
TIM5	TIM5_UP	DMA2_Channel2	
	TIM5_CH1	DMA2_Channel5	
	TIM5_CH2	DMA2_Channel4	
	TIM5_CH3	DMA2_Channel2	
	TIM5_CH4	DMA2_Channel1	
	TIM5_TRIG	DMA2_Channel1	
	TIM5_COM	DMA2_Channel1	

Peripheral	DMA request	STM32L1 series	STM32U0 series
TIM6	TIM6_UP	DMA1_Channel2	DMAMUX request 60
TIM15	TIM15_CH1	NA	TIM15_CH1 request 62
	TIM15_UP		TIM15_CH2 request 63
	TIM15_TRIG		TIM15_TRIG_COM request 64
	TIM15_COM		TIM15_UP request 65
TIM16	TIM16_CH1		TIM16_CH1 request 66
	TIM16_COM		TIM16_COM request 67
	TIM16_UP		TIM16_UP request 68
AES	AES_OUT	DMA2_Channel3	AES_OUT request 7
	AES_IN	DMA2_Channel5	AES_IN request 6

4.4 Interrupts

The table below presents the interrupt vectors on the STM32U0 series compared to the STM32L1 series.

Table 11. Interrupt vector differences between STM32L1 and STM32U0 series

Position	STM32L1 series			STM32U0 series
	Cat. 1 & 2	Cat. 3	Cat. 4 & 5	
0	WWDG			WWDG
1	PVD			PVD/PVM
2	TAMPER_ STAMP			TAMPER/RTC
3	RTC_WKUP			FLASH/WKUP
4	FLASH			RCC/CRS
5	RCC			EXTI0_1
6	EXTI0			EXT2_3
7	EXTI1			EXTI4
8	EXTI2			USB
9	EXTI3			DMA1_Channel1
10	EXTI4			DMA1_Channel2_3
11	DMA1_Channel1			DMA1_Channel4_5_6_7/ DMAMUX/ DMA2_Channel1_2_3_4_5
12	DMA1_Channel2			ADC_COMP
13	DMA1_Channel3			TIM1_BRK_UP_TRG_COM
14	DMA1_Channel4			TIM1_CC
15	DMA1_Channel5			TIM2
16	DMA1_Channel6			TIM3
17	DMA1_Channel7			TIM6_DAC/LPTIM1
18	ADC1			TIM7/LPTIM2
19	USB_HP			TIM15/LPTIM3
20	USB_LP			TIM16

Position	STM32L1 series			STM32U0 series
	Cat. 1 & 2	Cat. 3	Cat. 4 & 5	
21	DAC			TSC
22	COMP, TSC	COMP/CA		LCD
23	EXTI9_5			I2C1
24	LCD			I2C2/I2C3/I2C4
25	TIM9			SPI1
26	TIM10			SPI2/SPI3
27	TIM11			USART1
28	TIM2			USART2/LPUART2
29	TIM3			USART3/LPUART1
30	TIM4			USART4/LPUART3
31	I2C1_EV			AES/RNG
32	I2C1_ER			NA
33	I2C2_EV			
34	I2C2_ER			
35	SPI1			
36	SPI2			
37	USART1			
38	USART2			
39	USART3			
40	EXTI15_10			
41	RTC_Alarm			
42	USB_FS_WKUP			
43	TIM6			
44	TIM7			
45	NA	TIM5	SDIO	
46		SPI3	TIM5	
47		DMA2_Channel1	SPI3	
48		DMA2_Channel2	UART4	
49		DMA2_Channel3	UART5	
50		DMA2_Channel4	DMA2_Channel1	
51		DMA2_Channel5	DMA2_Channel2	
52		AES	DMA2_Channel3	
53		COMP_ACQ	DMA2_Channel4	
54	NA		DMA2_Channel5	
55			AES	
56			COMP_ACQ	

4.5 Reset and clock control (RCC)

The table below presents the differences related to the reset and clock controller (RCC) between the STM32L1 series and the peripherals in the STM32U0 series.

Table 12. RCC differences between STM32L1 and STM32U0 series

RCC	STM32L1 series	STM32U0 series
MSI	Multi speed RC factory and user trimmed (64 kHz, 128 kHz, 256 kHz, 512 kHz, 1.02 MHz, 2.05 MHz, 4.1 MHz)	• MSI is a low-power oscillator with programmable frequency up to 48 MHz. It can replace the PLL as system clock (faster wake-up, lower consumption). It can be used as a USB device clock (no need for an external high-speed crystal oscillator). • Multi-speed RC factory and user trimmed (100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz). • Auto calibration from LSE.
HSI16	16 MHz RC factory and user trimmed.	
LSI	37 kHz RC	• 32 kHz RC. • Lower consumption, higher accuracy (refer to product datasheet).
HSE	1 to 24 MHz	4 to 48 MHz
LSE	32.768 kHz	• 32.768 kHz • Configurable drive/consumption. • Available in backup domain (VBAT).
HSI48	NA	• 48 MHz RC forSTM32U0x3xx devices. • Can drive USB Full Speed and RNG.
PLL	• Main PLL for system. • PLL clock sources: HSI and HSE.	• Main PLL for system. • PLL for ADC, RNG, TIM1, TIM15, and USB FS clock. • PLL provides 3 independent outputs. • The PLL sources are MSI, HSI16, and HSE.
System clock source	MSI, HSI16, HSE, or PLL	MSI, HSI16, HSE, PLL, LSE, or LSI.
System clock frequency	• Up to 32 MHz. • 2 MHz after reset using MSI.	• Up to 56 MHz. • 4 MHz after reset using MSI.
AHB frequency	Up to 32 MHz.	Up to 56 MHz.
APB1 frequency	Up to 32 MHz.	Up to 56 MHz (APB).
APB2 frequency	Up to 32 MHz.	Up to 56 MHz (APB).
RTC clock source	LSI, LSE, or HSE clock divided by 2, 4, 8, or 16.	LSI, LSE, or HSE/32.
MCO clock source	MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI, or HSI48. With configurable prescaler, 1, 2, 4, 8 or 16 for each output	MCO pin (multiple pins): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI, HSI48, RTCCLK, RTCWAKEUP. MCO1 and MCO2 are available. With configurable prescaler, 1, 2, 4, 8 or 16 for each output
CSS	• CSS (clock security system). • CSS on LSE.	

RCC	STM32L1 series	STM32U0 series
Internal oscillator measurement/ calibration	• LSE connected to TIM9 or TIM10 CH1 IC: can measure HSI or MSI with respect to LSE clock high precision. • LSI connected to TIM10 CH1 IC: can measure LSI with respect to HSI or HSE clock precision. • HSE connected to TIM11 CH1 IC: can measure HSE with respect to LSE/HSI clock. • MSI connected to TIM11 CH1 IC: can measure MSI with respect to HSI/HSE clock.	• Mainly replacing TIM9/10/11 in the STM32L1 series by TIM15/16 in the STM32U0 series. • LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision. • LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision. • HSE/32 and MSI connected to TIM16 CH1 IC.
Interrupt	• CSS (linked to NMI IRQ). • LSECSS. • LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY (linked to RCC global IRQ).	• CSS (linked to NMI IRQ). • LSECSS. • LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, and PLLRDY (linked to RCC global IRQ).

In addition to the differences described in the table above, the following additional adaptation steps may be needed for the migration:

- Performance versus V_{CORE} ranges.
- Peripheral access configuration.
- Peripheral clock configuration.

4.5.1 Performance versus V_{CORE} ranges

On the STM32L1 series, the maximum CPU clock frequency and the flash memory wait state depend on the selected V_{CORE} voltage range and the selected V_{DD} range.

The tables below present the different clock source frequencies depending on different product voltage ranges.

Table 13. Performance versus V_{CORE} ranges for STM32L1 and STM32U0 series

W = wait state.

CPU performance	Power performance	V_{CORE} range	Typical Value (V)	Max frequency (MHz)				V_{DD} range
				3 WS	2 WS	1 WS	0 WS	
STM32L1 series								
High	Low	1	1.8	-	-	32	16	2.0 to 3.6
Medium	Medium	2	1.5	-	-	16	8	1.65 to 3.6
Low	High	3	1.2	-	-	4	2	
STM32U0 series								
High	Medium	1	1.2	-	56	48	24	1.71 to 3.6
Medium	High	2	1.0	-	18	16	8	1.71 to 3.6

4.5.2 Peripheral access configuration

The address mapping of several peripherals has changed for the STM32U0 series compared to the STM32L1 series, so different registers need to be used to enable/disable or enter/exit the peripheral clock or from Reset mode (see table below).

Table 14. RCC registers used for peripheral access configuration for STM32L1 and STM32U0 series

Bus	Register STM32L1 series	Register STM32U0 series	Comments
AHB	RCC_AHBRSTR	RCC_AHBRSTR	Used to enter/exit the AHB peripheral from reset.
	RCC_AHBENR	RCC_AHBENR	Used to enable/disable the AHB peripheral clock.
	RCC_AHBLPENR	RCC_AHBSMENR	Used to enable/disable the AHB peripheral clock in Sleep mode.
APB	RCC_APB1RSTR	RCC_APBRSTR1 RCC_APBRSTR2	Used to enter/exit the APB1 peripheral from reset.
	RCC_APB1ENR	RCC_APBENR1 RCC_APBENR2	Used to enable/disable the APB1 peripheral clock.
	RCC_APB1LPENR	RCC_APBSMENR1 RCC_APBSMENR2	Used to enable/disable the APB1 peripheral clock in Sleep mode.
APB2	RCC_APB2RSTR	NA	Used to enter/exit the APB2 peripheral from reset.
	RCC_APB2ENR		Used to enable/disable the APB2 peripheral clock.
	RCC_APB2LPENR		Used to enable/disable the APB2 peripheral clock in Sleep mode.

The configuration to access a given peripheral requires:

- Identifying the bus to which the peripheral is connected.
- Selecting the correct register, depending on the requested action.

For example, USART1 is connected to the APB bus. To enable the USART1 clock, the RCC_APBENR2 register needs to be configured as follows with the STM32Cube HAL driver RCC API:

```
__HAL_RCC_USART1_CLK_ENABLE();
```

To disable the USART1 clock during Sleep mode (to reduce power consumption), the RCC_APBSMENR2 register needs to be configured as follows with the STM32Cube HAL driver RCC API:

```
__HAL_RCC_USART1_CLK_SLEEP_ENABLE();
```

4.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source, independent from the system clock, which is used to generate the clock required for their operations:

- **USB:**
  - On STM32L1 devices, the USB 48 MHz clock is derived from the PLL VCO clock, which must be at 96 MHz.
  - On STM32U0 devices, the USB 48 MHz clock is derived from one of the following sources:
    - The main PLL VCO (PLLUSB1CLK).
    - The MSI clock.
    - The HSI48 internal oscillator.
- **SDIO/SDMMC:**
  - On STM32L1 devices, the SDIO clock (SDIOCLK) is derived from the PLL VCO clock and is equal to PLLVCO/2.
  - On STM32U0 devices, SDIO/SDMMC is not present.

- **RTC and LCD:**
  The RTC and the LCD glass clocks share the same clock source (RTCCLK).
  On STM32L1 devices, the RTC and LCD glass clocks are derived from one of the three following sources: LSE, LSI, or HSE divided by prescaler (/2, 4, 8, 16).
  On STM32U0 devices, the RTC and the LCD glass clocks are derived from one of the three following sources: LSE clock, LSI clock, or HSE clock divided by 32. The PCLK frequency must always be greater than or equal to the RTC clock frequency.
  RTC can also be set to ultra-low-power mode by enabling the LPCAL bit to further reduce consumption.
- **ADC:**
  - On STM32L1 devices, the ADC features two clock schemes:
    - The clock for the analog circuitry: ADCCLK. This clock is always the HSI oscillator clock. A divider by 1, 2, or 4 allows the adaptation of the clock frequency to the operating conditions of the device. This configuration is done using the ADC_CCR[ADCPRE] bits. The ADC clock also depends on the voltage range V_{CORE}. When the product voltage range 3 is selected (V_{CORE} = 1.2 V), the ADC is in low speed (ADCCLK = 4 MHz, 250 Ksps).
    - The clock for the digital interface (used for the read/write access of the register). This clock is the APB2 clock. The digital interface clock is enabled/disabled through the RCC_APB2ENR register (ADC1EN bit) and there is a bit to reset the ADC through the RCC_APB2RSTR[ADCRST] bit.
  - On STM32U0 devices, the input clock of the ADCs can be selected from two different clock sources:
    - Derived (selected by software) from the system clock (SYSCLK), PLLPCLK, or HSI16. In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to bits PREC[3:0]).
    - Derived from the APB clock of the ADC bus interface, divided by a programmable factor (1, 2, or 4). In this mode, a programmable divider factor can be selected (1, 2, or 4 according to bits CKMODE[1:0]). Refer to the STM32U0 series reference manual for more details.
- **DAC:**
  On STM32U0 devices, in addition to the PCLK clock, the LSI clock is used for the sample and hold operation.
- **U(S)ARTS:**
  - On STM32L1 devices, the U(S)ART clock is the APB1 or APB2 clock, depending on which APB bus is mapped to the U(S)ART.
  - On STM32U0 devices, the USART clock is derived from one of the four following sources: system clock (SYSCLK), HSI16, LSE, or APB.
    Using a source-clock independent from the system clock (like HSI16) allows an on-the-fly change of the system clock without reconfiguration of the USART peripheral baud rate prescalers.
- **I2Cs:**
  - On STM32L1 devices, the I2C clock is the APB1 clock (PCLK1).
  - On STM32U0 devices, the I2C clock is derived from one of the three following sources: system clock (SYSCLK), HSI16, or APB (PCLK).
    Using a source-clock independent from the system clock (like HSI16) allows an on-the-fly change of the system clock without reconfiguration of the I2C peripheral timing register.
- **I2S/SAI:**
  - On STM32L1 devices, the I2S clocks are derived from one of the three following sources: HSI16, HSE, or PLL.
  - On STM32U0 devices, I2S/SAI is not present.

4.6 Power control (PWR)

The PWR controller for STM32U0 devices presents some differences compared to the STM32L1 series, which are summarized in the table below.

Table 15. PWR differences between STM32L1 and STM32U0 series

PWR	STM32L1	STM32U0
Power supplies	• V_{DD} = 1.8 V at power-on, 1.65 V at power-down, and 3.6 V when BOR is available. • V_{DD} = 1.65 to 3.6 V when BOR is not available. • V_{DD} is the external power supply for I/Os and the internal regulator. • It is provided externally through VDD pins.	• V_{DD} = 1.71 to 3.6 V: external power supply for I/Os and internal regulator. • It is provided externally through VDD pins.
	• V_{CORE} = 1.2 to 1.8 V. • V_{CORE} is the power supply for the digital peripherals, SRAM, and flash memory. • It is generated by an internal voltage regulator. • Three V_{CORE} ranges can be selected by software depending on the V_{DD} and target frequency.	• V_{CORE} = 1.0 to 1.28 V. • V_{CORE} is the power supply for the digital peripherals, SRAM, and flash memory. • It is generated by an internal voltage regulator. • Two V_{CORE} ranges can be selected by software depending on the target frequency.
	NA	V_{BAT} = 1.55 to 3.6 V: the power supply for the RTC external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.
	V_{DD} and V_{DDA} must be at the same voltage value.	Independent power supplies (V_{DDA}, V_{DDUSB}) allow the improvement of power consumption by running the MCU at a lower supply voltage than analog and USB.
	• V_{SSA}, V_{DDA} = 1.8 V at power-on, 1.65 V at power-down, and 3.6 V when BOR is available. • V_{SSA}, V_{DDA} = 1.65 to 3.6 V when BOR is not available. • V_{DDA} is the external analog power supply for ADC, DAC, reset blocks, RC oscillators, and PLL. • The minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used • V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.	• V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DAC/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V • V_{DDA} is the external analog power supply for the A/D and D/A converters, voltage reference buffer, operational amplifiers, and comparators. • The V_{DDA} voltage level is independent from the V_{DD} voltage.
Power supplies (continued)	• V_{LCD} = 2.5 to 3.6 V • The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.	• V_{LCD} = 2.5 to 3.6 V. • The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.
	NA	• V_{DDUSB} = 3.0 to 3.6 V. • V_{DDUSB} is the external independent power supply for the USB transceivers. • The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
Battery backup domain		• RTC with backup registers (up to 9 bytes). • LSE. • PC13 to PC15 I/Os. • Up to 5 tamper pins.

PWR	STM32L1	STM32U0
Power supply supervisor	• Integrated POR/PDR circuitry. • Programmable voltage detector (PVD).	
	• Brownout reset (BOR). • BOR can be disabled after power-on.	• Brownout reset (BOR). • BOR is always enabled, except in Shutdown mode.
	NA	3 peripheral voltage monitoring (PVM): • PVM1 for V_{DDUSB}. • PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V).
Low-power modes	Sleep mode	
	• Low-power run mode (up to 128 kHz.) • Low-power sleep mode (up to 128 kHz.)	• Low-power run mode (up to 2 MHz.) • Low-power sleep mode (up to 2 MHz). • The system clock is limited to 2 MHz, but I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz.
	Stop mode.	• Stop 0, Stop 1, and Stop 2 mode. • Some additional functional peripherals (cf. wake-up source).
	Standby mode. (V_{CORE} domain powered off).	Standby mode (V_{CORE} domain powered off) with new features: • BOR is always ON. • SRAM2 content can be preserved. • Pull-up or pull-down can be applied to each I/O.
	NA	Shutdown mode (V_{CORE} domain powered off and power monitoring off).
Wake-up sources	Sleep mode Any peripheral interrupt/wakeup event.	
	Stop mode • Any EXTI line event/interrupt. • BOR, PVD, COMP, RTC, USB, IWDG.	Stop mode • Any EXTI line event/interrupt. • BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD.
	Standby mode • 3 WKUP pins rising edge. • RTC event. • External reset in NRST pin. • IWDG reset.	Standby mode • Up to 5 WKUP pins rising or falling edge. • RTC event. • External reset in NRST pin. • IWDG reset.
	NA	Shutdown mode • Up to 5 WKUP pins rising or falling edge. • RTC event; • External reset in NRST pin.
Wake-up clocks	Wake-up from Stop mode MSI (all ranges up to 4.1 MHz).	Wake-up from Stop mode HSI16 16 MHz or MSI (all ranges up to 48 MHz) allow a 5-µs wake-up at high speed without waiting for the PLL startup time.
	Wake-up from Standby mode MSI 2.097 MHz.	Wake-up from Standby mode MSI (ranges from 1 to 8 MHz)
	NA	Wake-up from Shutdown mode MSI 4 MHz.

PWR	STM32L1	STM32U0
Configuration	NA	• On STM32U0 devices, the registers are different: from 2 registers in the STM32L1 series to up to 25 registers in the STM32U0 series. – 4 control registers. – 2 status registers. – 1 status clear register. – 2 registers per GPIO port for controlling pull-up and pull-down. • Most configuration bits from the STM32L1 series can be found in the STM32U0 series (but some may have a different programming mode).

4.7 Real-time clock (RTC)

The STM32U0 and STM32L1 series implement almost identical RTC features. The table below summarizes the differences.

Table 16. PWR differences between STM32L1 and STM32U0 series

RTC	STM32L1 series	STM32U0 series
Features	• Coarse digital calibration (kept for compatibility only). • New developments must only use smooth calibration.	• Only smooth calibration available. • Ultra-low-power calibration saving further consumption is available when the LPCAL bit is set.
	1 tamper pin (available in VBAT).	5 tamper pins (available in VBAT).
	80-byte backup registers.	Up to 9 backup registers.
Configuration	-	• RTC_CR/DCE not available. • RTC_CALIB register not available. • RTC_TAFCR (L1) -> RTC_TAMPCR (U0) Except bit ALARMOUTTYPE available on RTC_OR/ RTC_ALARM_TYPE.

For more information about the RTC features of the STM32U0 series, refer to the RTC section of the STM32U0 series reference manual.

4.8 System configuration controller (SYSCFG) and RI

The STM32U0 and STM32L1 series implement almost identical SYSCFG features. The table below summarizes the differences.

Table 17. SYSCFG - RI differences between STM32L1 and STM32U0 series

SYSCFG - RI	STM32L1 series	STM32U0 series
RI features	TIM2/TIM3/TIM4 input captures 1, 2, 3, and four routing selections from selectable I/Os: • Routing of internal reference voltage VREFINT to selectable I/Os for all packages. • Up to 40 external I/Os + 3 internal nodes (internal reference voltage + temperature sensor + V_{DD} and $V_{DD}/2$ measurement by VCOMP) can be used for data acquisition purposes with the ADC interface. • Input and output routing of COMP1 and COMP2.	• The RI IO switch control used for the Touch Sense application has been replaced by a dedicated peripheral (TSC) in the STM32U0 series. • The remaining switch control (for ADC, COMP) and internal interconnects are managed within each specific peripheral in the STM32U0 series. The overall functionality is not equivalent.

SYSCFG - RI	STM32L1 series	STM32U0 series
SYSCFG features	• Remapping memory areas. • Managing the external interrupt line connection to the GPIOs. • Configuring the USB pull-up resistor.	• Remapping memory areas. • Managing the external interrupt line connection to the GPIOs. • Robustness management. • Configuring SRAM2 write protection and software erase. • Enabling /disabling I2C fast mode plus driving capability on some I/Os and voltage booster for I/Os analog switches.
Configuration	-	• Most registers from the STM32L1 series are identical in the STM32U0 series. • A few bits are different and EXTI configuration may differ (number of GPIOs is different depending on the product).

4.9 General-purpose I/O (GPIO) interface

The GPIO peripheral of the STM32U0 series embeds identical features compared to the one present on the STM32L1 series.

Minor adaptations of the code written for the the STM32L1 series using the GPIO may be required on the STM32U0 due to:

- The mapping of specific functions on different GPIOs (refer to the pinout differences in Section 2: Hardware migration).
- Alternate function selection differences (AFSELy[3:0] in the GPIOx_AFRL and GPIOx_AFRH registers).
- The additional mapping of GPIOs sharing pins with BOOT and NRST to provide more GPIOs in the same package.

The main GPIO features are:

- GPIO mapped on the AHB bus for better performance and accessibility by DMA.
- I/O pin multiplexer and mapping: the pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) to connect to an I/O pin at a time. In this way, no conflict can occur between peripherals sharing the same I/O pin.
- More possibilities and features for I/O configuration.

For more information on the STM32U0 series GPIO programming and usage, refer to the *I/O pin multiplexer and mapping* section in the GPIO chapter of the STM32U0 series reference manual. For a detailed description of the pinout and alternate function mapping, refer to the product datasheets.

4.10 Extended interrupt and event controller (EXTI) source selection

The external interrupt and event controller (EXTI) is very similar in the STM32U0 and STM32L1 series. The table below shows the main differences.

Table 18. EXTI differences between STM32L1 and STM32U0 series

EXTI	STM32L1 series	STM32U0 series
Number of event/interrupt lines	Up to 24 lines	Up to 37 lines: • 16 direct. • 22 configurable.
Configuration	-	The selection of the EXTI line source is performed through the EXTIx bits in the SYSCFG_EXTICRx registers (in the STM32L1 and STM32U0 series). However, the mapping of the EXTICRx registers has been changed.

4.11 Flash memory

The STM32U0 and STM32L1 series instantiate different flash memory modules, both in terms of architecture/technology and interface. Consequently, the STM32U0 series flash memory programming procedures and registers are different from those in the STM32L1 series, and any code written for the flash memory interface in the STM32L1 series needs to be rewritten to run on STM32U0 devices.

The table below presents the differences between the flash memory interface in the STM32L1 and STM32U0 series.

For more information on programming, erasing, and protection of the STM32U0 series flash memory, refer to the STM32U0 series reference manuals.

Table 19. Flash memory differences between STM32L1 and STM32U0 series

Flash	STM32L1 series	STM32U0 series
Main/program memory	0x0800 0000 to (up to) 0x0805 FFFF	0x0800 0000 to (up to) 0x0803 FFFF
	• Up to 512 Kbytes. • Split in 2 banks. • Each bank: up to 256 Kbytes. • Sector size = 4 Kbytes: 16 Pages of 256 bytes. • Programming granularity: 32-bit. • Read granularity: 64/32-bit.	• STM32U0x3xx: – Up to 256 Kbytes. – 1 bank. – 128 pages of 2 Kbytes. – Each page: 8 rows of 256 Kbytes. • STM32U031xx: – Up to 64 Kbytes. – 1 bank. – 32 pages of 2 Kbytes. – Each page: 8 rows of 256 Kbytes. • Programming and read granularity: 72-bit (incl 8 ECC bits).
Features	• Read while write (RWW). • Dual bank boot. • ECC (data EEPROM only).	• Read while write (RWW).
	NA	• ECC. • Flash empty check.
Wait state	Up to 1 (depending on the supply voltage and frequency).	Up to 1 (depending on the core voltage and frequency).
ART Accelerator™	NA	Allowing 0 wait state when executing from the cache.
Data EEPROM memory	• 4 Kbytes 0x0808 0000 to 0x0808 0FFF (Cat. 1, 2). • 8 Kbytes 0x0808 0000 to 0x0808 1FFF (Cat. 3). • 12 Kbytes 0x0808 0000 to 0x0808 2FFF (Cat. 4). • 16 Kbytes 0x0808 0000 to 0x0808 3FFF (Cat. 5).	N/A Can be emulated by software. For more details, refer to the application note *How to use EEPROM emulation on STM32 MCUs* (AN4894), available from http://www.st.com.
System memory	• 4 Kbytes 0x1FF0 0000 to 0x1FF0 0FFF (Cat. 1, 2). • 8 Kbytes 0x1FF0 0000 to 0x1FF0 1FFF (Cat. 3, 4, 5).	• 26 Kbytes 0x1FFF 0000 to 0x1FFF 67FF.
One time programmable (OTP)	NA	1 Kbyte 0x1FFF 6800 to 0x1FFF 6BFF.
Option bytes	• 0x1FF8 0000 to 0x1FF8001F (all Cat. x). • 0x1FF8 0080 to 0x1FF8 009F (Cat. 4, 5).	Improved programming method with no direct access to the option byte storage area.
Flash memory interface	0x4002 3C00 to 0x4002 3FFF.	0x4002 2000 to 0x4002 23FF.
	-	Different from STM32L1 series.
Erase granularity	• Program memory Mass/page (256 bytes).	Page erase (2 Kbytes), bank erase, and mass erase (all banks).

Flash	STM32L1 series	STM32U0 series
	• DATA EEPROM memory: Byte/half-word/word/double-word.	
Read protection (RDP)	• Level 0 no protection. • RDP = 0xAA.	• Level 0 no protection. • RDP = 0xAA.
	• Level 1 memory protection. • RDP ≠ (level 1 & level 0).	• Level 1 memory protection. • RDP ≠ (level 1 & level 0).
	• Level 2 RDP = 0xCC .	• Level 2 RDP = 0xCC .
	-	Improved protection scheme with OEM keys allowing the secure regression of protection levels.
Proprietary code readout protection (PCROP)	Granularity: 1 sector (4 Kbytes).	-
Write protection (WRP)	Granularity: 1 sector (4 Kbytes).	• Two write protection areas: • Granularity: 2 Kbytes.
User option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	NA	nRST_SHDW
	IWDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
		WWDG_SW
	NA	NOT_VBAT_VDD_OPT
		RAM_PARITY_CHECK
		BKPSRAM_HW_ERASE_DISABLE
		IRHEN, NRST_MODE[1:0]
	BOR_LEV[3:0]	BOR_LEV[2:0]
	nBFB2	BOOT_LOCK
	NA	nBOOT1
		nBOOT0
		nBOOT_SEL

4.12 Universal synchronous asynchronous receiver transmitter (U(S)ART)

The STM32U0 series implement several new features on USART compared to the STM32L1 series. The table below shows the differences.

Table 20. U(S)ART differences between STM32L1 and STM32U0 series

U(S)ART	STM32L1 series	STM32U0 series
Instances	• x3 USART • x2 UART	• x4 USART • x3 LPUART
Baud rate	Up to 4 Mbit/s when the clock frequency is 32 MHz and oversampling is by 8	Up to 6 Mbit/s when the clock frequency is 48 MHz and oversampling is by 8
Clock	Single clock domain	Dual clock domain allowing: • UART functionality and wake-up from Stop mode • Convenient baud rate programming independent from the PCLK reprogramming

U(S)ART	STM32L1 series	STM32U0 series
Data	Word length: programmable (8 or 9 bits)	• Word length: programmable (7, 8, or 9 bits) • Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	14 interrupt sources with flags
Features	• RS232 hardware flow control (CTS/RTS) • Continuous communication using DMA • Multiprocessor communication • Single-wire half-duplex communication • IrDA SIR ENDEC block • LIN mode • SPI master	
	• Smartcard mode T = 0 and T = 1 is to be implemented by software • Number of stop bits: 0.5, 1, 1.5, 2	Smartcard mode not supported
Features	NA	• Wake-up from Stop mode (start bit, received byte, address match) • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable Tx/Rx pin configuration • LPUART does not support synchronous mode (SPI master), smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt, or auto baud rate detection
Configuration	NA	L1 registers and associated bits are not identical in the STM32U0 series Refer to the STM32U0 series reference manuals for details

4.13 Inter-integrated circuit (I2C) interface

The STM32L1 series implement a different I2C peripheral, which allows for easier software management. The table below shows the differences.

Table 21. I2C differences between STM32L1 and STM32U0 series

I2C	STM32L1 series	STM32U0 series
Instances	x2 (I2C1, I2C2)	• x3 for STM32U0x3xx. • x2 for STM32U031xx.
Features	• 7-bit and 10-bit addressing mode. • Standard mode (Sm, up to 100 KHz). • Fast mode (Fm, up to 400 KHz).	
	NA	• Fast mode Plus (Fm+, up to 1 MHz). • Independent clock. • Wakeup from stop on address match.
	• SMBus	NA
Configuration	NA	Register configuration is very different in the STM32U0 series. Refer to the STM32U0 series reference manuals for details.

4.14 Serial peripheral interface (SPI)/Inter-IC sound (I2S)/serial audio interface (SAI)

The STM32U0 and STM32L1 series implement near-identical SPI features. The table below highlights the differences.

Table 22. SPI differences between STM32L1 and STM32U0 series

SPI	STM32L1 series	STM32U0 series
Instances	x3 (SPI1, SPI2, SPI3)	x3
Features	SPI + I2S	I2S is not supported by SPI on STM32U0 devices.
Data size	Fixed, configurable to 8 or 16 bits.	Programmable from 4 to 16 bits.
Data buffer	Tx & Rx 16-bit buffers (single data frame)	32-bit Tx & Rx FIFOs (up to 4 data frames)
Data packing	No (16-bit access only)	Yes (8-, 16-, or 32-bit data access, programmable FIFO data thresholds)
Mode	• SPI TI mode • SPI Motorola mode	• SPI TI mode • SPI Motorola mode • NSSP mode
Speed	16 MHz (core at 32 MHz)	24 MHz (core at 48 MHz)
Configuration	NA	The data size and Tx/Rx flow handling are different in the STM32L1 and STM32U0 series, requiring different software sequences.

Two serial audio interfaces (SAI) replace the the I^2S interface of the SPI on STM32U0 devices.

The table below shows the main differences between I^2S and SAI.

Table 23. Comparison of I2S and SAI features on STM32L1 and STM32U0 series

I2S/SAI	STM32L1 series	STM32U0 series
Instances	x2	NA
Features	Late frame synchronization signal detection in Slave mode	NA

4.15 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit is very similar in STM32L1 and STM32U0 devices.

The table below shows the differences.

Table 24. CRC differences between STM32L1 and STM32U0 series

CRC	STM32L1 series	STM32U0 series
Features	• Single input/output 32-bit data register. • CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size. • General-purpose 8-bit register (can be used for temporary storage).	
	• Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7. • Handles 32-bit data size.	• Fully programmable polynomial with programmable size (7, 8, 16, or 32 bits). • Handles 8-, 16-, and 32-bit data sizes. • Programmable CRC initial value. • Input buffer to avoid bus stall during calculation. • Reversibility option on I/O data.

CRC	STM32L1 series	STM32U0 series
Configuration	NA	Configuration registers in theSTM32L1 series are identical in the STM32U0 series. The STM32U0 series includes additional registers for new features. Refer to the reference manuals for details

4.16 Advanced encryption standard hardware accelerator (AES)

The STM32U0 series implement several new AES features compared to the STM32L1 series. The table below shows the differences.

Table 25. AES differences between STM32L1 and STM32U0 series

AES	STM32L1 series	STM32U0 series
Features	128-bit register for storing the encryption, or derivation key (4x 32-bit registers).	256-bit register for storing the encryption, decryption, or derivation key (8x 32-bit registers).
Mode	• Electronic codebook (ECB). • Cipher block chaining (CBC). • Counter mode (CTR).	• Electronic codebook (ECB). • Cipher block chaining (CBC). • Counter mode (CTR). • Galois counter mode (GCM). • Galois message authentication code mode (GMAC). • Cipher message authentication code mode (CMAC).
Key length	128-bit.	128-bit, 256-bit.
Configuration	NA	All registers and programming bits in the STM32L1 series can be found in the STM32U0 series.

4.17 Liquid-crystal display controller (LCD)

The LCD controller on the STM32U0 series implements the same features as the one on the STM32L1 series, except for an additional internal output buffer that allows for improved contrast. It is possible to use the output buffers instead of the high-drive resistive network.

All programmable registers and associated bits in the STM32L1 series are equivalent to the ones in the STM32U0 series. However, due to the fact that the VLCD pin is implemented as an alternate function in Sthe STM32U0 series (contrary to the STM32L1 series), a specific software sequence is required to configure the LCD controller when the step-up converter is used as the power source.

Refer to the STM32L1 and STM32U0 series reference manuals for more details.

Note: LCD is not available on STM32U031xx devices.

4.18 Universal serial bus interface (USB)

The STM32L1 and STM32U0 series implement similar USB peripherals: they both contain a USB FS device interface.

STM32U0x3xx devices include a clock recovery system (CRS). It provides a precise clock to the USB peripheral:

- When using USB device mode, the CRS allows crystal-less USB operation.
- When using USB host mode, the CRS allows low-frequency crystal (32.768 KHz) USB operations.

Most features supported by the STM32L1 series are also supported by the STM32U0 series. The table below highlights the key differences.

Table 26. USB differences between STM32L1 and STM32U0 series

USB	STM32L1 series	STM32U0 series
Features	Universal Serial Bus Revision 2.0.	Universal Serial Bus Revision 2.0, including link power management (LPM) support.
	FS mode: • 1 bidirectional control endpoint. • 7 IN endpoints. (Bulk, Interrupt, Isochronous.) • 7 OUT endpoints (Bulk, Interrupt, Isochronous.)	
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D+ (USB_DP) line.	
	NA	Independent V_{DDUSB} power supply, allowing a lower V_{DDCORE} while using USB.
Mapping	APB1	APB
Buffer memory	512 bytes (endpoint buffers and buffer descriptors structure.)	1024 bytes of dedicated packet buffer memory SRAM.
Low-power modes	USB suspend and resume.	• USB suspend and resume. • Link power management (LPM) support.
Configuration	NA	STM32U0 registers are different. Refer to the STM32U0 reference manuals for details.

4.19 Analog-to-digital converter (ADC)

The main ADC differences between the STM32L1 and STM32U0 series are a new digital interface and architecture. The table below presents the different features.

Table 27. ADC differences between STM32L1 and STM32U0 series

ADC	STM32L1 series		STM32U0 series	
ADC type	SAR structure			
Instances	ADC1		ADC	
Maximum sampling frequency	1 Msps		2.5 Msps	
Number of channels	Up to 42 channels.		Up to 19 channels.	
Resolution	12-bit		12-bit + digital oversampling up to 16-bit.	
Conversion modes	Single/continuous/scan/ discontinuous		Single/continuous/scan/discontinuous	
DMA	Yes			
External trigger	Yes			
	External event for regular group	External event for injected group	External event for regular group:	External event for injected group:
	TIM9_CC2	TIM9_CC1	TIM1_TRGO2	TIM1_TRGO2
	TIM9_TRGO	TIM9_TRGO	TIM1_CC4	TIM1_CC4
	TIM2_CC3	TIM2_TRGO	TIM2_TRGO	TIM2_TRGO
	TIM2_CC2	TIM2_CC1	TIM3_TRGO	TIM3_TRGO
	TIM3_TRGO	TIM3_CC4	TIM15_TRGO	TIM15_TRGO
	TIM4_CC4	TIM4_TRGO	TIM6_TRGO	TIM6_TRGO
	TIM2_TRGO	TIM4_CC1	EXTI11	EXTI11
	TIM3_CC1	TIM4_CC2		

ADC	STM32L1 series		STM32U0 series	
External trigger	TIM3_CC3 TIM4_TRGO TIM6_TRGO EXTI line11	TIM4_CC3 TIM10_CC1 TIM7_TRGO EXTI line15		
Supply requirement	1.8 V to 3.6 V.		• 1.62 V to 3.6 V. • Independent power supply (V_{DDA}).	
Reference voltage	External		Reference voltage for STM32U0 series external (2.0 V to V_{DDA}) or internal (2.048 V or 2.5 V).	
Electrical parameters	1.45 mA (max.), 1.0 mA (typ.).		Consumption proportional to conversion speed: 200 mA/Msps (Typ.).	
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$			

4.20 Digital-to-analog converter (DAC)

The STM32U0 series implement an enhanced DAC compared to the STM32L1 series. The table below shows the differences.

Table 28. DAC differences between STM32L1 and STM32U0 series

DAC	STM32L1 series	STM32U0 series
Number of channels	2	1
Resolution	12-bit	
Features	• Left or right data alignment in 12-bit mode. • Noise-wave and triangular-wave generation. • DAC with 2 channels for independent or simultaneous conversions.	
	NA	• Buffer offset calibration. • DAC1_OUTx can be disconnected from output pin. • Sample and hold mode for low-power operation in Stop mode.
DMA	Yes	
External trigger	Yes	
	• TIM6_TRGO • TIM7_TRGO • TIM9_TRGO • TIM2_TRGO • TIM4_TRGO • EXTI line9 • SW TRIG	• TIM1_TRGO_CKTIM • TIM2_TRGO_CKTIM • TIM3_TRGO_CKTIM • TIM6_TRGO_CKTIM • TIM7_TRGO_CKTIM • TIM15_TRGO_CKTIM • LPTIM1_OUT • LPTMI2_OUT • EXTI line9 • SW TRIG
Supply requirement	1.8 V to 3.6 V.	• 1.8 V to 3.6 V. • Independent power supply (V_{DDA}).
Reference voltage	External	Reference voltage for STM32U0 series external (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V).
Configuration	NA	Software compatible except for output buffer management.

4.21 Comparators (COMP)

The table below presents the differences in the COMP interface of the STM32L1 and STM32U0 series.

Table 29. COMP differences between STM32L1 and STM32U0 series

COMP	STM32L1 series	STM32U0 series
Type	• COMP1 fixed threshold • COMP2 rail-to-rail	• COMP1 • COMP2 rail-to-rail
Inputs	COMP1: • 25 (Cat. 1, 2: 24 ext IO + T sensor) • 32 (Cat. 3, 4, 5 : 29 ext IO + T sensor + OPAMP1/2)	COMP1: • Non inverting: 4 (PA6, PB2, PC5, PC6) • Inverting: 8 (PA0, PA1, PA4, PA5, PC4, PB1, DAC1_OUT1/2, V_{REFINT} x 1, ¾, ½, ¼)
	COMP2: • Non inverting: 2 (Cat. 1, 2: PB4, PB5) 4 (Cat. 3, 4, 5: PB4, PB5, PB6, PB7) • Inverting: 7 (PB3, DAC1_OUT1/2, V_{REFINT} x 1, ¾, ½, ¼)	COMP2: • Non inverting: 4 (PA3, PB4, PB6, PD10) • Inverting: 8 (PA2, PA4, PA5, PB3, PB7, DAC1_OUT1/2, V_{REFINT} x 1, ¾, ½, ¼)
Outputs	• Generation of input capture and OCREF clear signals for TIM2, TIM3, and TIM4, and input capture for TIM10. • Generation of wakeup interrupt or events (EXTI line).	• Generation of break input signals for timers through GPIO alternate function. • Generation of wakeup interrupt or events (EXTI line).
Features	Window comparator	
	NA	• Output with blanking source. • Programmable hysteresis.
	Programmable speed/consumption (COMP2).	Programmable speed/consumption (COMP1/ COMP2).
Supply requirement	1.65 V to 3.6 V.	1.62 V to 3.6 V.
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	

4.22 Operational amplifiers (OPAMP)

STM32U0 devices implement enhanced OPAMPs compared to the STM32L1 series. The table below shows the differences.

Table 30. OPAMP differences between STM32L1 and STM32U0 series

OPAMP	STM32L1 series	STM32U0 series
Instances	3	1
Features	• Rail-to-rail input and output voltage range. • Low input bias current. • Low input offset voltage. • Low-power mode. • Fast wakeup time. • Gain bandwidth of 1 MHz.	
	NA	Programmable gain amplifier (PGA).
Configuration	NA	The configuration registers are not organized in the same way on the STM32U0 series as on the STM32L1 series.

5 Software migration

5.1 Reference documents

- The Definitive Guide to Arm® Cortex®-M0 and Cortex®-M0+ processors.
- The Definitive Guide to Arm® Cortex®-M3 and Cortex®-M4 processors.
- *STM32F10xxx/20xxx/21xxx/L1xxxx Cortex®-M3 programming manual* (PM0056).
- *STM32 Cortex®-M0+ MCUs programming manual* (PM0223).
- Cortex®-M3 Technical Reference Manual, available from infocenter.arm.com.
- Cortex®-M0+ Technical Reference Manual, available from infocenter.arm.com.

5.2 Cortex®-M3 and Cortex®-M0+ overview

5.2.1 STM32 Cortex®-M3 processor and core peripherals

The Cortex®-M3 processor is built on a high-performance processor core, with a 3-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers an exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware, including single-cycle 32x32 multiplications and a dedicated hardware division.

Cortex®-M3 processor features and benefits summary

- Tight integration of system peripherals reducing the area and development costs.
- Thumb instruction set combining a high code density with 32-bit performance.
- Code-patch ability for ROM system update.
- Power control optimization of system components.
- Integrated sleep modes for low-power consumption.
- Fast code execution permitting a slower processor clock or increased Sleep-mode time.
- Hardware division and fast multiplier.
- Deterministic, high-performance interrupt handling for time-critical applications.
- Extensive debug and trace capabilities.

The figure below presents the STM32 Cortex®-M3 implementation.
ADD FIGURE

Cortex®-M3 key features

- Architecture 32 bits RISC Armv7-M.
- 3-stage pipeline with branch speculation.
- Instruction set:
  - Thumb, thumb-2.
  - Hardware multiply, hardware divide, saturated arithmetic.

5.2.2 STM32 Cortex®-M0+ processor and core peripherals

The Cortex®-M0+ processor is an entry-level 32-bit Arm® Cortex® processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- A simple architecture that is easy to learn and program.
- Ultra-low power, energy-efficient operation.
- Excellent code density.
- Deterministic, high-performance interrupt handling.
- Upward compatibility with Cortex®-M processor family.
- Platform security robustness, with optional integrated memory protection unit (MPU).

The Cortex®-M0+ processor is built on a 32-bit processor core that is highly optimized for area and power, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex®-M0+ processor implements the ARMv6-M architecture, which is based on the 16-bit Thumb® instruction set and includes Thumb-2 technology. This provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

The Cortex®-M0+ processor closely integrates a configurable nested vectored interrupt controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- Includes a non-maskable interrupt (NMI).
- Provides zero jitter interrupt option.
- Provides four interrupt priority levels.

The tight integration of the processor core and NVIC provides fast execution of interrupt service routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes that include a deep-sleep function that enables the entire device to be rapidly powered down.

5.3 Cortex mapping overview

Except for the floating point unit, the mapping is similar on the Cortex®-M3 and Cortex®-M0+ processors. The table below summarizes the differences.

Table 31. Cortex mapping overview for STM32L1 and STM32L0 series

Cortex		STM32L1 series	STM32U0 series
Core	Architecture	Cortex®-M3	Cortex®-M0+
	Nested vectored interrupt controller (NVIC)	57 maskable interrupt channels	32 maskable interrupt channels
	Extended interrupts and events controller (EXTI)	Up to 24 event/interrupt	Up to 38 event/interrupt
Mapping	System timer	0xE000 E010 to 0xE000 E01F	0xE000 E010 to 0xE000 E01F
	Nested vectored interrupt controller	0xE000 E100 to 0xE000 E4EF	0xE000E100 to 0xE000E4EF
	System control block	0xE000 ED00 to 0xE000 ED3F	0xE000 ED00 to 0xE000 ED3F
	Floating point unit coprocessor access control	NA	
	Memory protection unit	0xE000 ED90 to 0xE000 EDB8	0xE000 ED90 to 0xE000 EDB8
	Nested vectored interrupt controller	0xE000 EF00 to 0xE000 EF03	0xE000 EF00 to 0xE000 EF03
	Floating point unit	NA	

5.4 Security improvements

STM32U0 brings significant improvements in the security domain, like robust read-out protection (RDP) with three protections level states, password-based regression (128-bit PSWD), hardware protection feature (HDP), and more. The application note *Introduction to STM32 microcontrollers security* (AN5156) provides detailed descriptions of these features.

Revision history

Table 32. **Document revision history**

Date	Version	Changes
18-Mar-2024	1	Initial release.

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