# SR5 E1 line - design recommendations for the EMC reduction due to SMPS

## Introduction

STMicroelectronics SR5 E1 line uses a main 3.3 V operating supply, which is fed by all the high voltage pins (the ones named VDD_HV_*) and a low voltage supply (mainly digital supply) provided by an internal switched mode power supply (SMPS) regulator requiring external components and feed within device through dedicated pins.

*Note: External low voltage supply is not supported on SR5E1x device line.*

This application note will analyze the use of switched-mode regulators available in the SR5 E1 line and provide general recommendations for the component design.

SMPS is by far the biggest contributor to the electromagnetic emissions of a system, so most of the optimization aims at reducing the emissions at the expense of conversion efficiency. Some constraints to drive the choice of the components value will be presented, but the process of fine-tuning the electromagnetic compatibility (EMC) is largely an empiric one. The best approach is to leave on the printed circuit board some open spots where different components can be soldered, and then measure their impact on system performance.

# 1 Basic reference circuit

The figure below shows the minimal external network needed to have a working SMPS.

**Figure 1. Basic reference circuit**

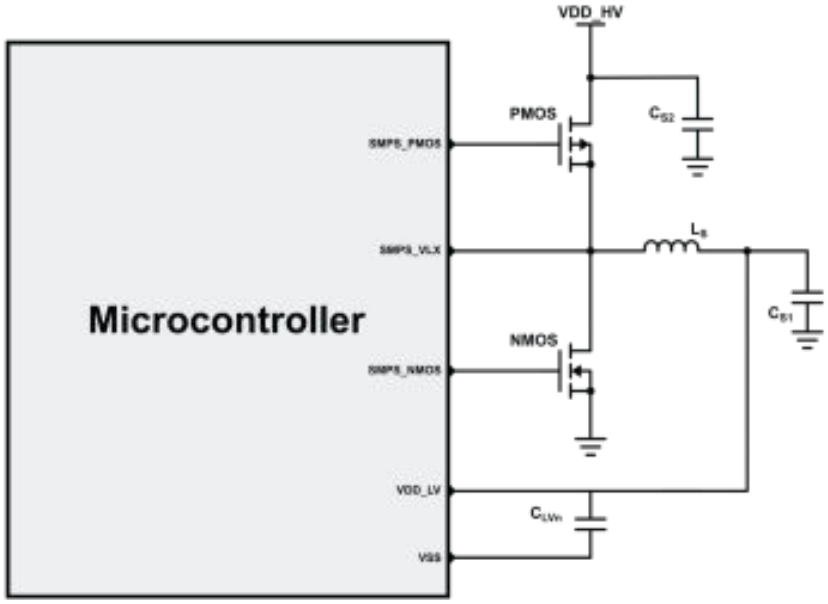


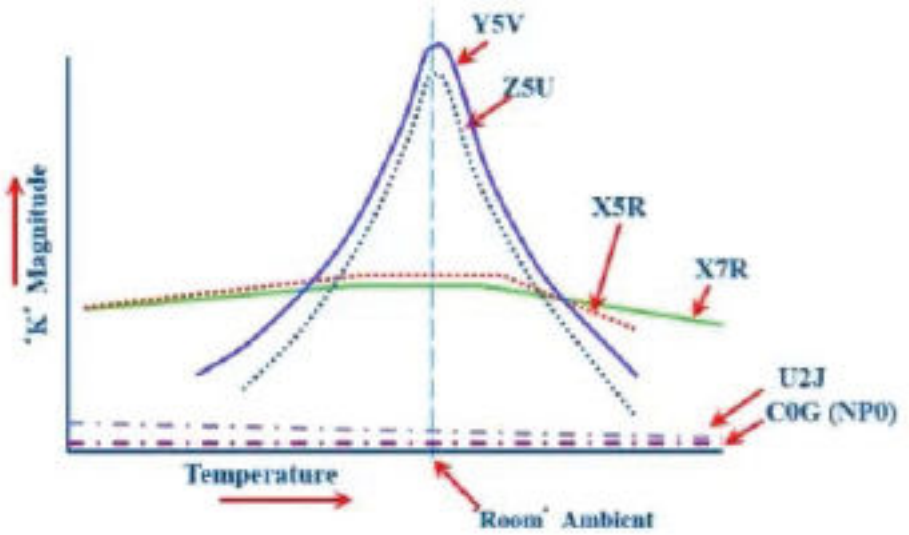

**Table 1. Recommended values**

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| PMOS | Recommended PMOS transistor | PMPB100XPEAX (1) | | | |
| NMOS | Recommended NMOS transistor | PMPB55XNEAX(2) | | | |
| $C_{S2}$ | SMPS external capacitance on HV supply | -50% | 47 | 35% | µF |
| $C_{S1}$ | SMPS external capacitance on LV supply | -50% | 20 | 35% | µF |
| $L_S$ | SMPS external inductance | -30% | 10 | 30% | µF |
| $D_S$ | Schottky diode (3) | PMEG3030EP(4) | | | |

1. *Alternative PMOS transistor for SMPS is BUK4D110-20P.*
2. *Alternative NMOS transistor for SMPS is BUK4D60-30.*
3. *Refer to Figure 5.*
4. *Recommended Schottky diode on NMOS transistor to reduce the emission.*

The figure below shows how the operating temperature affects the capacitance of some notable classes of components. The capacitors used for $C_{S1}$ and $C_{S2}$ should have a reasonably good stability over temperature, so a class 2 part (either an X7R or an X5R ceramic capacitor) is recommended.

**Figure 2. Variance overtemperature for several device classes**




The value given for $C_{S2}$ is a ballpark recommendation, and the application designer should tweak it basing on the external regulator and the EMC requirements.

# 2 General EMC considerations

The two external transistors in the Figure 1. Basic reference circuit continuously switch between saturation and cut-off states, where dissipation is low, and spend very little time in the high dissipation active state, which minimizes wasted energy. However, this constant switching causes voltage and current spikes, that provoke high electromagnetic emissions. To comply with EMC restrictions, it is usually necessary to make the transition between saturation and cut-off smoother, at the expense of reduced power efficiency.

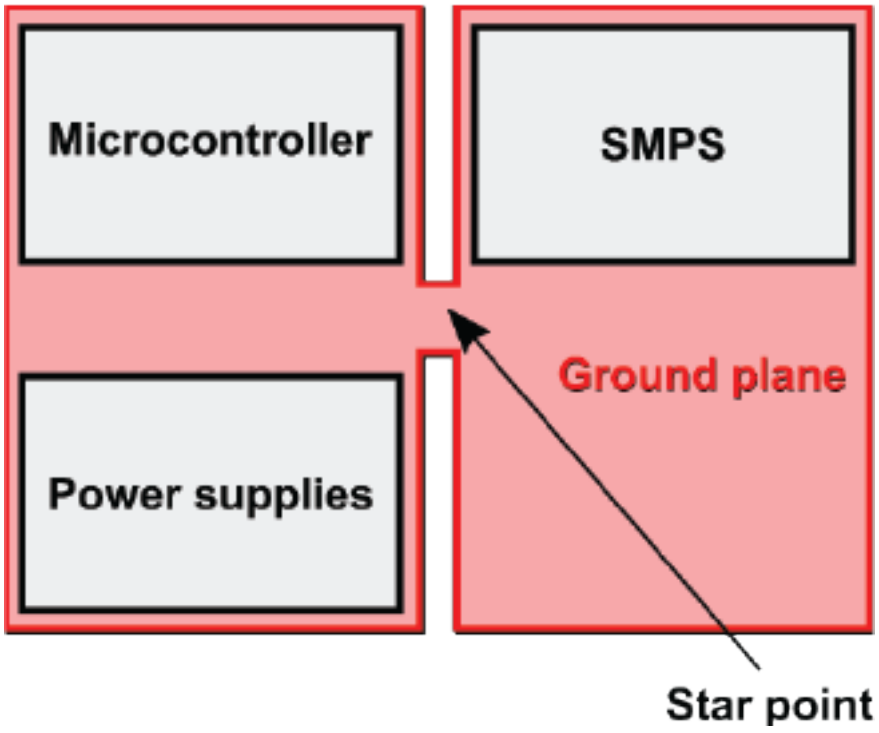
The SMPS circuit is by far the main source of electromagnetic emissions in a typical design, so special attention is necessary to minimize them. As a general note, connections should be kept as short as possible, in order to keep the parasitic impedance as low as possible. In particular, $C_{S2}$ should be as close as possible to the SoC.

## 2.1 Limiting injected noise

Circuit boards usually use a very large ground plane rather than thin strips among ground connections, as the latter can act as antennas and emit or receive an unacceptable amount of electromagnetic waves. A ground plane also offers a very low impedance, so that all ground pins are at a very close potential. However, a single ground plane will also allow the noise generated by constant SMPS switching to flow freely into other power sources.

To limit the amount of injected noise, it is recommended to use galvanic separation of the ground planes, joining them in a single point. This technique is known as star routing. The common ground or star point must be on the NMOS source.

**Figure 3. Using star routing to limit the noise injected by the SMPS**

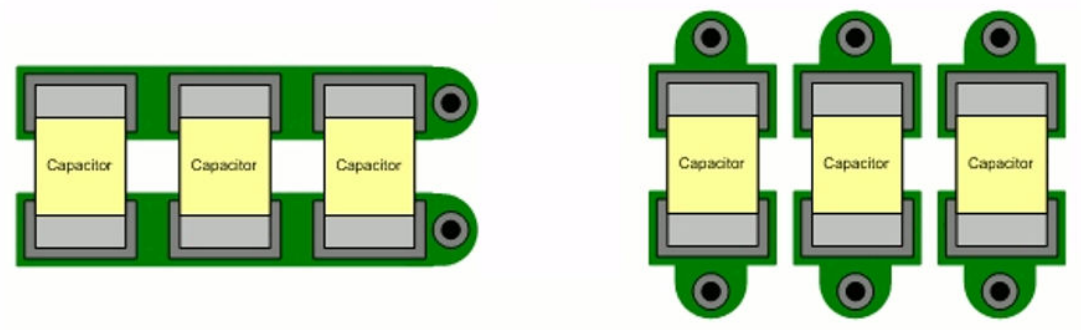


## 2.2 Some assembly required

All connections should be kept very short, in order to limit their parasitic impedance. In particular, $C_{S2}$ should be as close as possible to the SoC.

To reduce the assembly inductance of the capacitors, multi-vias connections should be preferred. The figure below shows a single-via connection on the left and a multi-vias one on the right:

**Figure 4. Single-via vs multi-vias connection**




The SMPS components should be surrounded by a guard ring extended on all the PCB layers, with frequent vias connecting the layers. This acts as a faraday cage to shield the rest of the coplanar conductors.

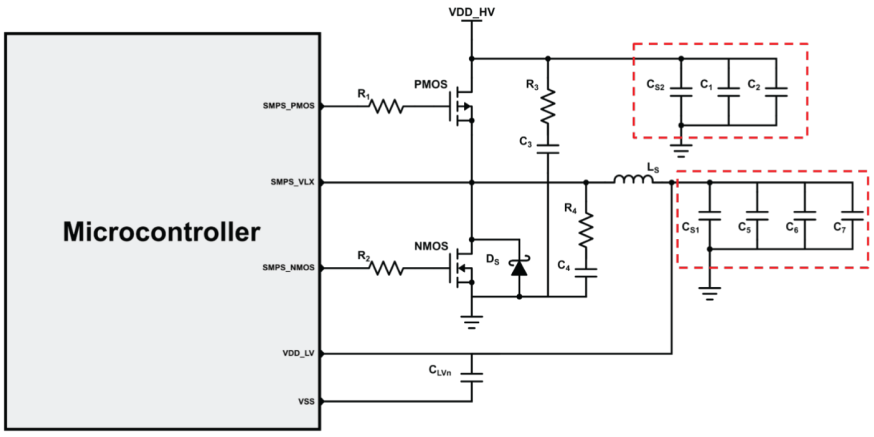
The VLX and the MOSFET gate traces should also be shielded. The topology of the board usually makes a full guard ring unfeasible, but placing some grounded traces that run in parallel can help.

# 3 Improving the circuit

To improve the EMC performance of an SMPS design, more components can be added to the board, so that noise is filtered, and spikes are limited. This causes increased cost and less efficiency, so the best approach is usually to try several combinations of components and measure the resulting emissions and the dissipated power. Then choose the cheapest solution that still meets the EMC targets. However, some guidelines are useful to have a starting point.

The figure below shows a reference circuit with a number of improvements that will be discussed in this chapter:

**Figure 5. Circuit with improvements for EMC**



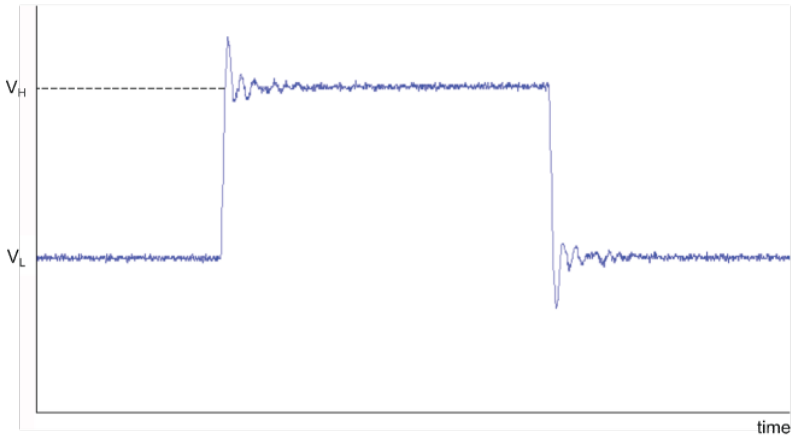

The value of the capacitance at the input and output of the regulator should still abide the one given in Table 1. Recommended values, so that the total value of the capacitors in the dashed boxes must be the same as the one given in the datasheet for $C_{S1}$ and $C_{S2}$.

## 3.1 Reactive components

The first problem to be faced is to prevent ground bouncing, which occurs when the rush of current on any change in state of the transistors causes the source voltage to rise.

This can briefly lower the VGS, causing some spurious state switches before the system settles down:

**Figure 6. Ground bounces can cause oscillations when transistors change state**

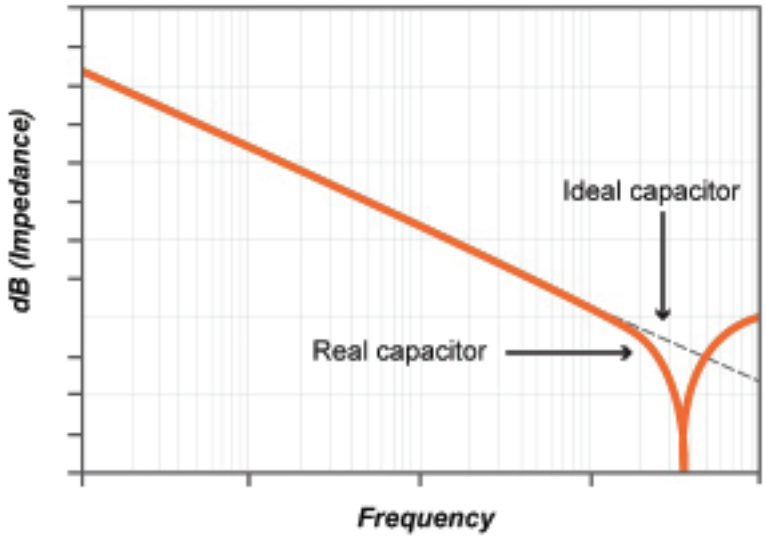



In order to reduce the ground bounces, the loops embracing the two transistors must have the same impedance, considering the parasitic effects as well. Each loop goes from the output of the SMPS circuit to the ground through the source terminal of each MOSFET:$C_{S2} + C_{PMOS} + C_L + C_{S1} = C_{NMOS} + C_L + C_{S1} \rightarrow C_{S2} + C_{PMOS} = C_{NMOS}$

In the previous equation, $C_{PMOS}$ and $C_{NMOS}$ are the parasitic capacitance between source and drain of the transistors, and $C_L$ is the parasitic capacitance of the inductor $L_S$.

The capacitors in parallel with $C_{S1}$ and $C_{S2}$ are used to filter out the high frequency components, so they need to have a self-resonance frequency as high as possible. Ideally, the impedance of a capacitor will decrease linearly as frequency increases, but at some point, the impedance due to the parasitic inductance of the component becomes prevalent, and the value starts rising again. The self-resonance frequency is the frequency where the total impedance of the component is the lowest.

**Figure 7. Impedance as a function of frequency in an ideal vs. real capacitor**



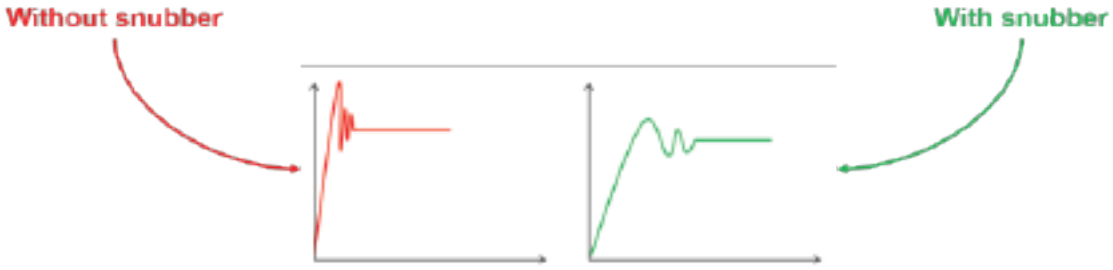
These capacitors usually have sizes in the range 1 nF - 100 nF and very low equivalent series resistance and inductance, possibly less than 5 mΩ and 600 pH, respectively.

## 3.2 Resistive components

The resistors $R_1$ and $R_2$ placed at the gate of each MOSFET form an RC filter with their own parasitic capacitance, which limits the slew rate of the voltage. This improves the EMC performance at the expense of an increased dissipation. The value of these resistors depends on the specifics of the board design, but it is usually in the range 10 Ω - 100 Ω.

The RC branches and the Schottky diode form a snubber circuit that lowers the amplitude and frequency of the voltage spike that occurs as the device turns on and off. The RC filters reduce the efficiency of the SMPS circuit but are usually necessary. The Schottky diode on NMOS transistor is recommended in SR5E1 applications so to reduce the emission.

**Figure 8. Impact of the snubber network on the slew rate at the drain of the MOSFETs**




The values of the snubber components depend on the parasitic values of the layout board and are often determined with an empiric trial-and-fix procedure.

Some reasonable values to start are respectively in the range:

- 10 Ω – 100 Ω for the resistors.
- 470 pF – 2.2 nF for the capacitors.

## Revision history

Table 2. **Document revision history**

| Date | Revision | Changes |
|---|---|---|
| 23-Oct-2023 | 1 | First release. |

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