AN6051

Application note

Migrating from STM32L4 and STM32L4+ to STM32U3 MCUs

Introduction

The designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another from the same product family or products from a different family. The reasons for migrating an application to a different microcontroller can be, for example:

- To fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os.
- To meet cost reduction constraints that require a switch to smaller components and shrinking the PCB area.

This document details the steps to migrate from an existing design based on the STM32L4 and STM32L4+ MCUs to an application based on one of the STM32U3 MCUs.

This document provides the full set of features available for STM32L4 and STM32L4+ MCUs, and the equivalent features of STM32U3 MCUs. This document also provides guidelines on both hardware and peripheral migration.

To better understand the information inside this application note, the user must be familiar with the STM32 microcontroller family.

This application note is a complement to the STM32L4, STM32L4+, and STM32U3 datasheets and reference manuals.

For additional information, refer to the product datasheets and reference manuals, available from www.st.com.

1 General information

This document applies to Arm®-based microcontrollers.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

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Referenced documents

Table 1. Referenced documents

Reference number	Document ID	Document title
[1]	RM0394	STM32L41xxx/42xxx/43xxx/44xxx/45xxx/46xxx Arm®-based 32-bit MCUs
[2]	RM0351	STM32L47xxx, STM32L48xxx, STM32L49xxx, and STM32L4Axxx Arm®-based 32-bit MCUs
[3]	RM0432	STM32L4+ series Arm®-based 32-bit MCUs
[4]	RM0487	STM32U3 series Arm®-based 32-bit MCUs
[5]	AN2606	STM32 microcontroller system memory boot mode
[6]	PM0264	STM32 Cortex®-M33 MCUs programming manual
[7]	PM0214	STM32 Cortex®-M4 MCUs and MPUs programming manual

2 STM32U3 series overview

Compared to the STM32L4 and STM32L4+ series, the STM32U3 series use a newer technology to achieve excellence in ultra-low power, increased security, enhanced efficiency, performance, and memory size, such as:

- Improved battery life owing to subtreshold voltage technology: active consumption down to 10 µA/MHz.
- Up to 1 Mbyte of flash memory.
- Up to 256 Kbytes of RAM.
- Ultra-low-power Arm®Cortex®-M33 32-bit core, with TrustZone® for Armv8-M.
- ST instruction cache (ICACHE), supporting both internal and external memories.
- Crypton peripheral embedding AES, SAES, PKA, HASH, and RNG peripherals and accelerators for increased security on the crypto line (available only on STM32U385).

2.1 Main features

The STM32U3 MCUs include a similar set of peripherals to the STM32L4 and STM32L4+ MCUs, but with advanced features, such as the ones listed below:

- **Security**
  - Arm® TrustZone® and securable I/Os, memories, and peripherals.
  - RDP and password-protected debug, secure firmware upgrade support, secure firmware installation, secure hide protection, and secure hide protection extension.
  - Up to eight configurable SAU regions.
  - Additional encryption accelerator engine (available only on STM32U385xx devices):
    - HASH hardware accelerator.
    - Two advanced encryption hardware accelerators (AES), including one with SCA resistance.
    - Public key accelerator (PKA), SCA-resistant.
    - Coupling and chaining bridge (CCB).
- **Power consumption**
  - Embedded regulator (LDO).
  - SMPS step-down converter:
    - Regulators are placed in parallel, making it possible to switch from one to another on the fly.
    - Both regulators can provide two different voltages (voltage scaling) and can operate in Stop modes.
  - Optimized RTC consumption.
- **Performance**
  - Frequency up to 96 MHz.
  - ICACHE for internal and external memories.
- **New peripherals**
  - Two ultra-low-power 12-bit ADCs with hardware oversampling up to 22 bits.
  - Audio digital filter.
  - Octo-SPI interface (OCTOSPI).
  - Two improved inter-integrated circuits (I3C).

Note: This document only compares the differences between common features in the STM32L4 and STM32L4+ MCUs and the STM32U3 MCUs. The new features of the STM32U3 series, mainly linked to TrustZone® support, are not covered. The detailed list of available features and packages for each product is available in the respective product datasheet.

2.2 System architecture

The STM32U3 series embed high-speed memories (up to 1 Mbyte of flash memory and up to 256 Kbytes of RAM), an Octo-SPI interface (on packages with less than 64 pins, only quad mode is supported), and an extensive range of enhanced I/Os and peripherals connected to a 32-bit multi-AHB bus matrix, three AHB buses, and three APB buses.

The following table illustrates the bus matrix differences between STM32L4, STM32L4+, and STM32U3 devices.

Table 2. Bus matrix on STM32L4, STM32L4+, and STM32U3 series

Bus type	STM32L4	STM32L4+	STM32U3
AHB bus matrix masters	5 masters: CPU, AHB system, DCode, ICode, DMA1 and DMA2(1).	Up to 9 masters: CPU, AHB system, DCode, ICode, DMA1 and DMA2, DMA2D, LCD-TFT controller DMA, SDMMC1, SDMMC2, GFXMMU(2).	Up to 7 masters: Fast C-bus, slow C-bus, CPU S-bus for SRAM1, CPU S-bus for other memories(3), GPDMA1, SDMMC1.
AHB bus matrix slaves	Up to 8 slaves: internal flash memory (on ICode and DCode bus), SRAM1, SRAM2, AHB1 (including APB1 and APB2), AHB2, FMC, and QUADSPI.	Up to 11 slaves: internal flash memory (on ICode and DCode bus), SRAM1, SRAM2, SRAM3, GFXMMU, AHB1 (including APB1 and APB2), AHB2, OCTOSPI1, OCTOSPI2, and FSMC.	Up to 6 slaves: Internal flash memory, SRAM1, SRAM2, AHB1, AHB2, peripherals (including APB1, APB2, and APB3), OCTOSPI1.

1. *Up to six masters with DMA2D only for STM32L496/4A6xx.*
2. *SDMMC2 and GFXMMU only available for STM32L4P5/L4Q5xx.*
3. *Two S-bus masters connected to two internal SRAMs without latency.*

The bus matrix provides access from a master to a slave, enabling concurrent access and efficient operation even when several high-speed peripherals work simultaneously.

The system architectures of STM32L4, STM32L4+, and STM32U375/385 are shown in the figures below.

Figure 1. STM32L4 series system architecture

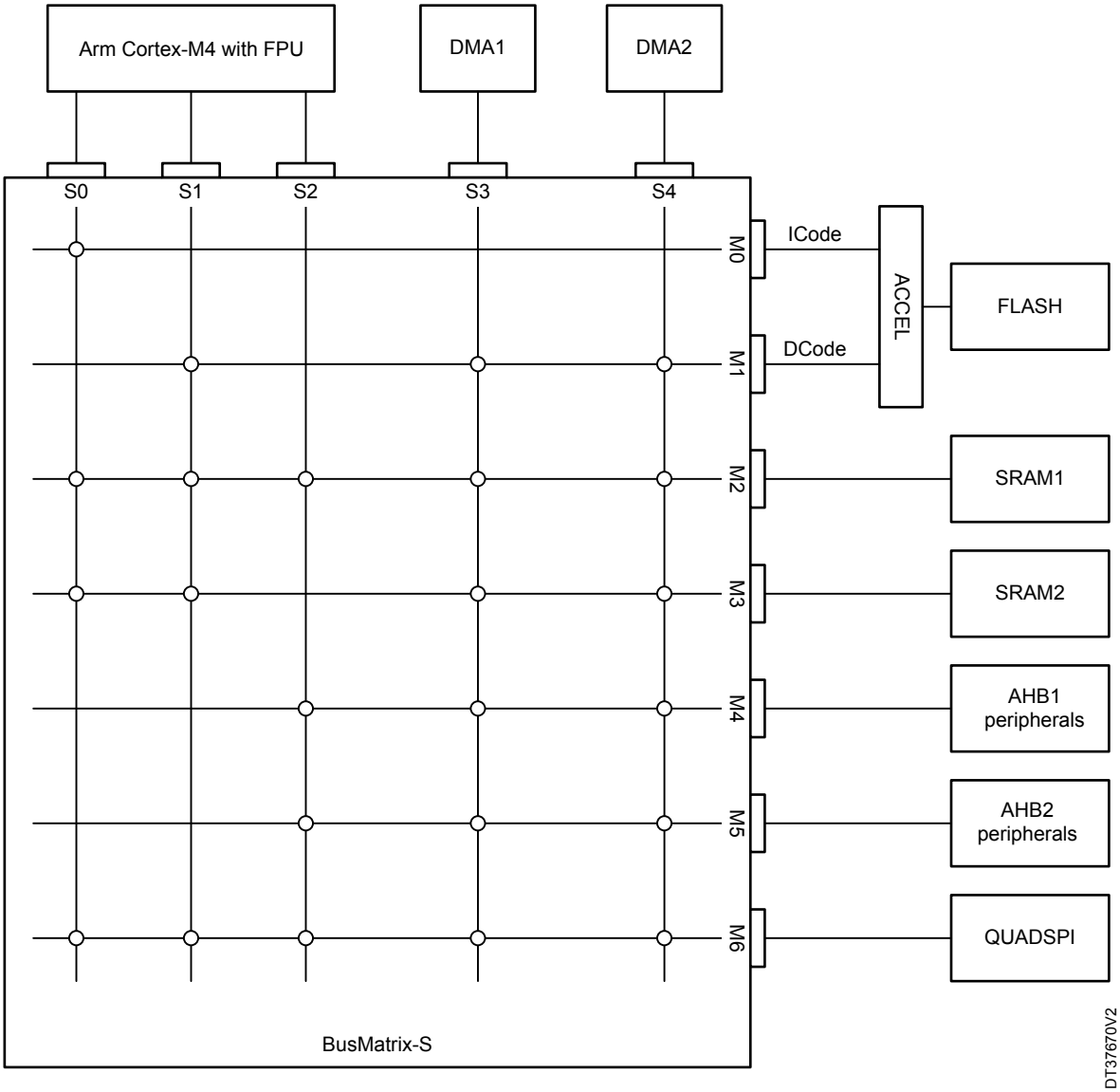


Figure 2. **STM32L4+ series system architecture**

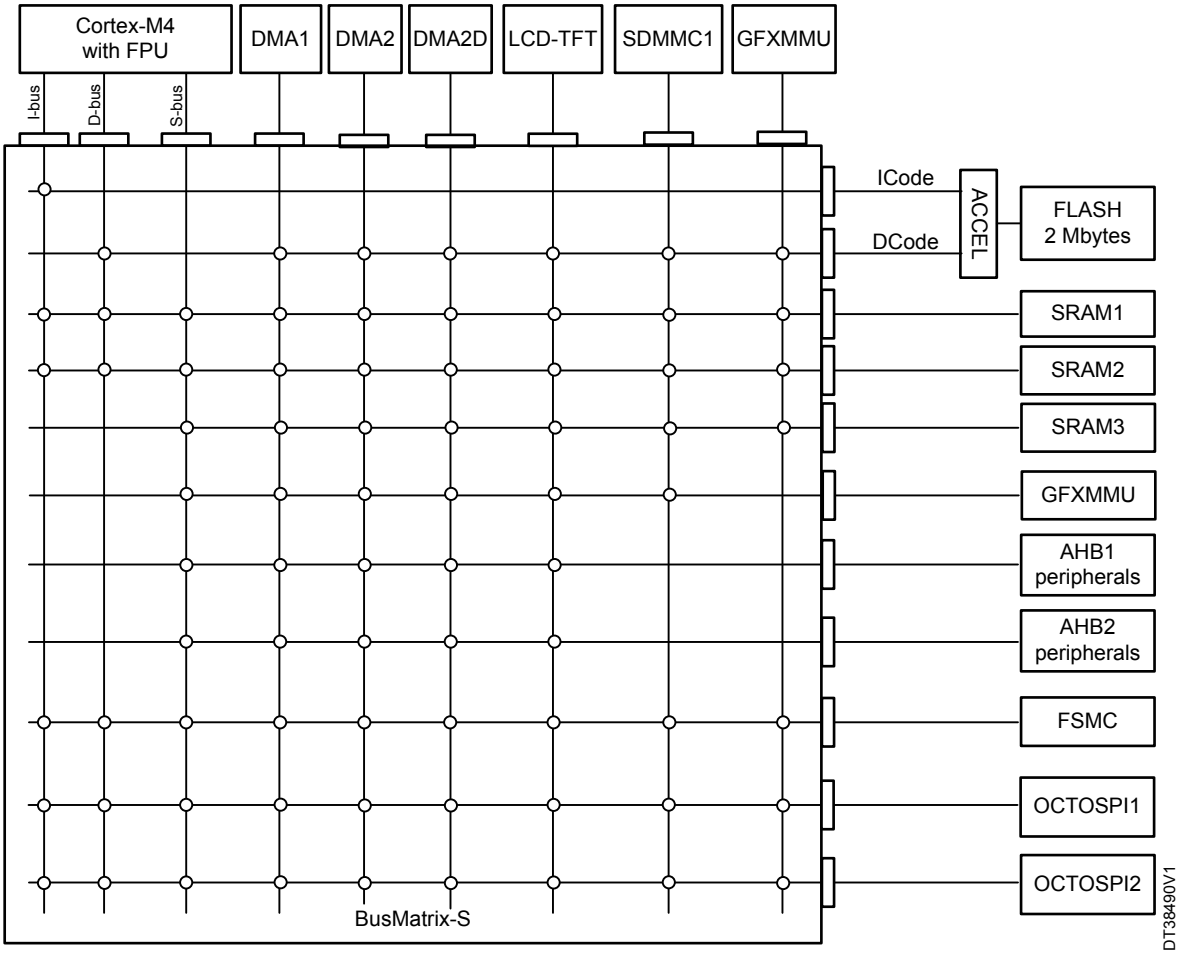
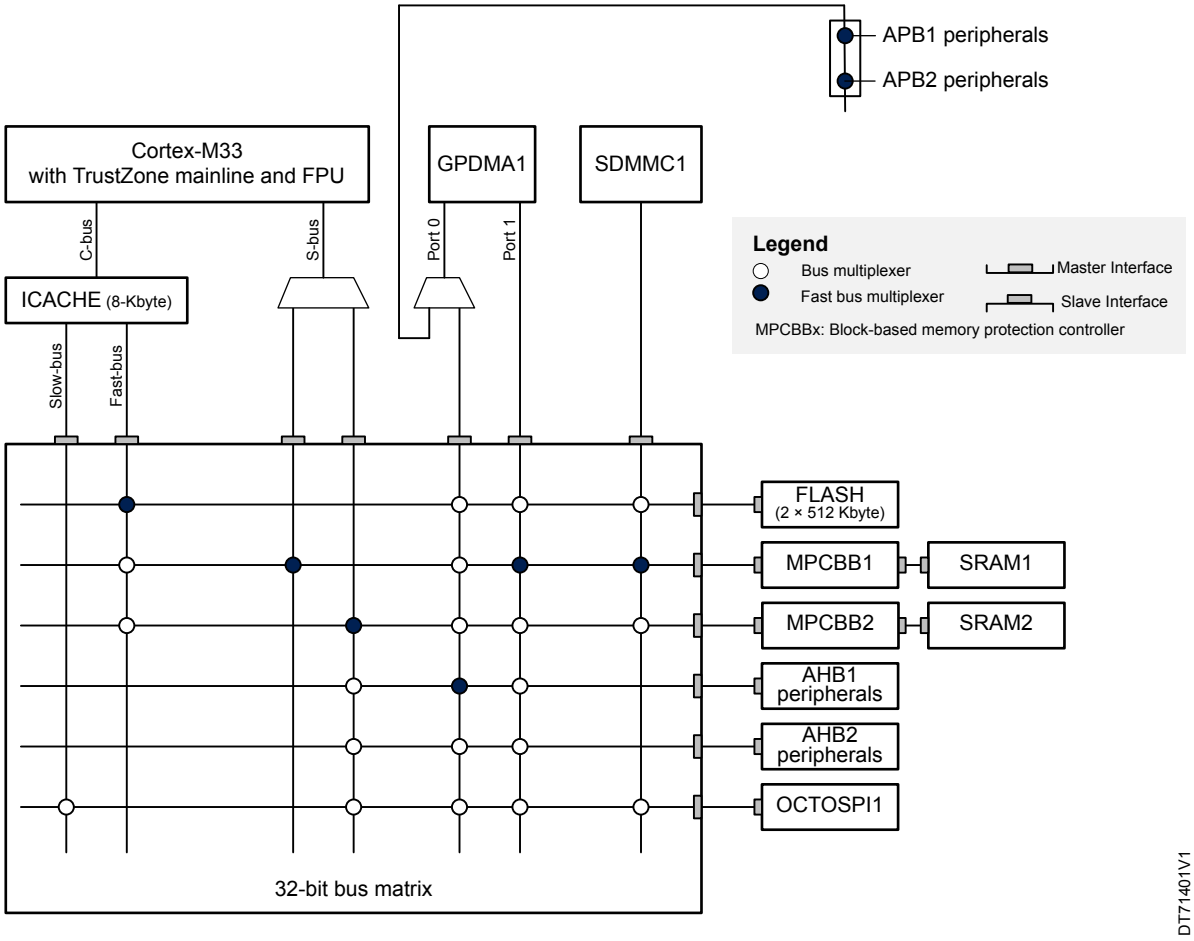


Figure 3. **STM32U3 series system architecture**



2.3 Memory availability

The table below summarizes the memory availability for STM32L4, STM32L4+, and STM32U3 MCUs.

Table 3. **Memory availability for STM32L4, STM32L4+, and STM32U3 MCUs**

Product	Flash memory		RAM size (Kbytes)			Comment
	Size	Bank	SRAM1	SRAM2	SRAM3	
STM32U375	512 Kbytes to 1 Mbyte	Dual	192 Kbytes	64 Kbytes	-	Without hardware crypto.
STM32U385	1 Mbyte					With hardware crypto.
STM32L41x/42x	128 Kbytes	-	32 Kbytes	8 Kbytes	-	-
STM32L43x/44x	256 Kbytes	-	48 Kbytes	16 Kbytes	-	-
STM32L45x/46x	512 Kbytes	-	128 Kbytes	32 Kbytes	-	-
STM32L47x/48x	1 Mbyte	-	96 Kbytes	32 Kbytes	-	-
STM32L49x/L4Ax	1 Mbyte	-	256 Kbytes	64 Kbytes	-	-
STM32L4P5x/L4Q5	1 Mbyte	-	128 Kbytes	64 Kbytes	128 Kbytes	-
STM32L4Rx/L4Sx	2 Mbytes	-	192 Kbytes	64 Kbytes	384 Kbytes	-

3 Hardware migration

The STM32U3 MCUs offer packages from 32 to 100 pins, and two pinout versions:

- Without internal SMPS: most packages are compatible with STM32L4 and STM32L4+ MCUs.
- With internal SMPS: brand new packages that are not compatible with STM32L4 and STM32L4+ MCUs. For this pinout version, the SMPS step-down converter and the LDO are embedded in parallel to provide the V_{CORE} supply.

For more details on the pinout, refer to the product datasheets.

The table below lists the available packages for STM32U3 MCUs compared to those available on STM32L4 and STM32L4+ MCUs, as well as their compatibility. Only the packages that are available in both series are shown. WLCSPxxx packages, which are not available for the STM32L4 and STM32L4+ MCUs, are not listed.

The table does not list the WLCSPx packages for STM32U3 MCUs, because they are dedicated to individual product lines. Refer to the product datasheets for more information.

Table 4. Packages on STM32U3 MCUs compared to STM32L4 and STM32L4+ MCUs

X = available, N/A = not available

Package (Size in mm x mm)	STM32L4(1)		STM32U3		
	STM32L4	STM32L4+	STM32U375/385	STM32U375/385 without SMPS compared toSTM32L4/L4+	STM32U375/385 with SMPS compared toSTM32L4/L4+
UFQFPN32 (5 x 5)	X(2)	N/A	X(4)	Compatible(5)	N/A
LQFP48 (7 x 7)	X(7)	X(3)	X	Compatible(6)	New pinout/ballout
UFQFPN48 (7 x 7)	X(7)	X(3)	X	Compatible(6)	
LQFP64 (10 x 10)	X	X(3)	X	Compatible(6)	
UFBGA64 (5 x 5)	X(7)	N/A	X	Compatible(6)	
LQFP100 (14 x 14)	X(9)	X	X	Compatible(6)	
UFBGA100 (7 x 7)	X(10)	N/A	X	Compatible(6)	

1. *For more details about the available packages for STM32L4 and STM32L4+, refer to the product datasheet.*
2. *Available only for STM32L47/48/49/4Axxx.*
3. *Available only for STM32L4Q5xx/4P5xx devices.*
4. *Available only for devices without internal SMPS.*
5. *Compatible, except pin PH3 becomes VCAP; BOOT0 functionality moved to PB7.*
6. *Compatible, except PB11 pin becomes VCAP.*
7. *Not available for STM32L47/48/49/4Axxx devices.*
8. *Available only for STM32L49/4Axxx.*
9. *Not available for STM32L41/42xxx devices.*
10. *Available only for STM32L43/44/45/46xxx devices.*

When SMPS is supported, a new, dedicated pinout supporting the SMPS step-down converter is available for the STM32U3 series.

When SMPS is not supported, the STM32U3 series devices are pin-to-pin compatible with the STM32L4 and STM32L4+ series devices, except:

- UFQFPN32 package: PH3-BOOT0 pin on STM32L4 is replaced by VCAP on STM32U3, and PB7 becomes PB7-BOOT0 on STM32U3.
- For other packages, the only incompatibility is in the PB11 pin on STM32L4 and STM32L4+, which is replaced by the VCAP pin on STM32U3.

Table 5. Different pins and their positions

Package (size in mm xmm)	Different pin/ball position	STM32L4 and STM32L4+	STM32U3
UFQFPN32 (5 x 5)	31	PH3-BOOT0	VCAP
	30	PB7	PB7-BOOT0
LQFP48 (7 x 7)	22	PB11	VCAP
UFQFPN48 (7 x 7)	22		
LQFP64 (10 x 10)	30		
UFBGA64 (5 x 5)	H7		
LQFP100 (14 x 14)	48		
UFBGA100 (7 x 7)	L11		

4 Boot mode compatibility

4.1 Boot mode selection

For STM32U3, the BOOT0 input pin may come from the PH3-BOOT0 pin or from an option bit, depending on the value of a user option bit to free the GPIO pad if necessary.

Table 6 and Table 7 below present the STM32U3 boot modes, when TrustZone® is disabled (Table 6) or enabled (Table 7).

Table 6. Boot modes for STM32U3 when TrustZone® is disabled (TZEN = 0)

NBOOT0 flash_OPTR[27]	BOOT0 pin PH3	NSWBOOT0 flash_ OPTR[26]	Boot address option-byte selection	Boot area	STMicroelectronics programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x0800 0000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	Bootloader: 0x0BF8 F000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash memory: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	Bootloader: 0x0BF8 F000

Table 7. Boot modes for STM32U3 when TrustZone® is enabled (TZEN = 1)

BOOT_LOCK	NBOOT0 flash_OPTR[27]	BOOT0 pin PH3	NSWBOOT0 flash_OPTR[26]	RSS command	Boot address option-byte selection	Boot area	STMicroelectronics programmed default value
0	-	0	1	0	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000
	-	1	1	0	N/A	RSS	RSS: 0x0FF80000
	1	-	0	0	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000
	0	-	0	0	N/A	RSS	RSS: 0x0FF80000
	-	-	-	≠ 0	N/A	RSS	RSS: 0x0FF80000
1	-	-	-	-	SECBOOTADD0 [24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash memory: 0x0C00 0000

On STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx, the boot mode is selected with the nBOOT1 option bit and the BOOT0 pin, or the nBOOT0 option bit, depending on the value of the nSWBOOT0 option bit in the flash_OPTR register (see Table 8 below).

Table 8. Boot modes for STM32L4+ and STM32L41/42/43/44/45/46/49/4Axxx

nBOOT1 flash_ OPTR[23]	nBOOT0 flash_ OPTR [27]	BOOT0 pin PH3	nSWBOOT0 flash_ OPTR [26]	Main flash empty (1)	Boot memory space alias
X	X	0	1	0	Main flash memory selected as boot area
X	X	0	1	1	System memory selected as boot area
X	1	X	0	X	Main flash memory selected as boot area
0	X	1	1	X	Embedded SRAM1 selected as boot area
0	0	X	0	X	Embedded SRAM1 selected as boot area
1	X	1	1	X	System memory selected as boot area
1	0	X	0	X	System memory selected as boot area

1. *For STM32L41/42/43/44/45/46xxx, a flash memory empty check mechanism is implemented to force the boot from system flash memory, if the first flash memory location is not programmed (0xFFFF FFFF), and if the boot selection was configured to boot from the main flash memory.*

On the other STM32L4 devices (STM32L47/48xxx), the boot mode is selected with one BOOT0 pin and the nBOOT1 option bit located in the user option bytes, at the memory address 0x1FFF 7800 (see Table 9 below).

Table 9. Boot modes for STM32L47/48xxx

Selected boot area	BOOT1	BOOT0
Main flash memory	X(1)	0
System flash memory	0	1
Embedded SRAM1	1	1

1. *X = equivalent to 0 or 1.*

4.2 Embedded bootloader

The embedded bootloader is located in the system memory and programmed by STMicroelectronics during production. It allows the flash memory to be reprogrammed, using the serial interfaces listed in the table below.

Table 10. Bootloader interface on STM32L4, STM32L4+, and STM32U3 MCUs

Peripheral	Pin	STM32L4 and STM32L4+	STM32U3
DFU	USB_DM (PA11)	X	X
	USB_DP (PA12)	X	X
USART1	USART1_TX (PA9)	X	X
	USART1_RX (PA10)	X	X
USART2	USART2_TX (PA2)	X	N/A
	USART2_RX (PA3)	X	N/A
USART3	USART3_TX (PC10)	X	X
	USART3_RX (PC11)	X	X
I2C1	I2C1_SCL (PB6)	X	X
	I2C1_SDA (PB7)	X	X
I2C2	I2C2_SCL (PB10)	X	X

Peripheral	Pin	STM32L4 and STM32L4+	STM32U3
I2C2	I2C2_SDA (PB11)	X	X
I2C3	I2C3_SCL (PC0)	X	X
	I2C3_SDA (PC1)	X	X
I2C4	I2C4_SCL (PD12)	X(1)	N/A
	I2C4_SDA (PD13)	X(1)	N/A
I3C1	I3C1_SCL (PB13)	N/A	X
	I3C1_SDA (PA1)	N/A	X
SPI1	SPI1_NSS (PA4)	X	X PG5 instead of PA4 for WLCSP68-G packages
	SPI1_SCK (PA5)	X	X PG2 instead of PA5 for WLCSP68-G packages
	SPI1_MISO (PA6)	X	X PG3 instead of PA6 for WLCSP68-G packages
	SPI1_MOSI (PA7)	X	X PG4 instead of PA7 for WLCSP68-G packages
SPI2	SPI2_NSS (PB12)	X	PD0
	SPI2_SCK (PB13)	X	PD1
	SPI2_MISO (PB14)	X	PD3
	SPI2_MOSI (PB15)	X	PD4
SPI3	SPI3_NSS (PA15)	N/A	X
	SPI3_SCK (PB3)	N/A	X
	SPI3_MISO (PB4)	N/A	X
	SPI3_MOSI (PB5)	N/A	X
CAN1	CAN1_RX (PB8)	X(2)	X(3)
	CAN1_TX (PB9)	X(2)	X(3)
CAN2	CAN2_RX (PB5)	X(4)	N/A
	CAN2_TX (PB6)	X(4)	N/A

1. *Available only for STM32L45/46/49/4Axxx.*
2. *Not available for STM32L41/42xxx.*
3. *FDCAN1 is available for STM32U3 series.*
4. *Available only for STM32L49/4Axxx.*

For more details on the bootloader, refer to the referenced document [5].

5 Peripheral migration

5.1 STM32 products cross-compatibility

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- **Group1**: peripherals common to all products by definition.
  These peripherals are identical, so they have the same structure, registers, and control bits. There is no need to perform any firmware changes to keep the same functionality at application level after migration. The behavior and features remain the same.
- **Group2**: peripherals shared by all products but with minor differences only. In general, they support new features.
  The migration from one product to another is very easy and does not require any significant new development efforts.
- **Group3**: peripherals that have considerable changes from one product to another (a new architecture or new features, for example).
  For this group of peripherals, the migration requires new developments at application level.

Each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, or small part of flash memory or SRAM can be configured as trusted or untrusted on STM32U3 MCUs.

The following table summarizes the available peripherals on the STM32L4, STM32L4+, and STM32U3 MCUs, as well as their compatibility.

Table 11. STM32 peripheral compatibility between STM32L4, STM32L4+, and STM32U3 MCUs

Peripheral		STM32L4		STM32U3
		STM32L4	STM32L4+	STM32U375/385
Core		Cortex®-M4		Cortex®-M33
Maximum CPU frequency		80 MHz	120 MHz	96 MHz
ICACHE		N/A		**8 Kbytes** 2-way associative or directly mapped.
PWR/regulators	Power supply	1.71 to 3.6 V		
	LDO	Available for all products/packages		
	LDO + internal DC-DC	N/A		STM32U3xxxxQ products **+ DC-DC/LDO on-the-fly selection**.
	LDO + external DC-DC	Available through VDD12 supply		N/A (no regulator bypass option).
Flash memory	Size	Up to 1 Mbyte	Up to 2 Mbytes	Up to 1 Mbyte **+ advanced features (such as secure hide protection)**.
	Bank	Dual bank		Dual bank **with TrustZone®**
SRAMs	SRAM1	Up to 256 Kbytes	192 Kbytes	192 Kbytes
	SRAM2	Up to 64 Kbytes	64 Kbytes	64 Kbytes with optional hardware parity
	SRAM3	N/A	384 Kbytes	N/A
DMA (not compatible)		DMA request line is connected directly to peripherals.	DMA request line is connected to peripherals through DMAMUX + DMA2D.	**GPDMA (12 channels) + advanced features (such as DMA peripheral control mode)**.

Peripheral		STM32L4		STM32U3
		STM32L4	STM32L4+	STM32U375/385
GTZC (global TrustZone® controller)		N/A		3 independent 32-bit AHB interface for TZSC, TZIC, and MPCBB. TZIC accessible only with secure transactions. Secure and nonsecure access supported for the privileged and unprivileged parts of TZSC. Set of registers to define product security settings. Privilege mode extended to internal memories.
Anti-tamper detection		Up to 3 tamper pins		Up to 5 tampers pins and 9 internal tamper events **+ new advanced features (such as GTZC and secure peripherals support)**.
CRC		1		1
FSMC (external memory controller for static memory LCD)		1		N/A
High-speed low-voltage mode (HSLV)		N/A		Some I/Os have the capability to increase their speed at low voltage by configuring them in HSLV mode.
Timers	Advanced control	Up to 2 (16-bit)	2 (16-bit)	1 (16-bit)
	General purpose	Up to 5 (16-bit) + up to 2 (32-bit)	5 (16-bit) + 2 (32-bit)	3 (16-bit) + 3 (32-bit)
	Basic	Up to 2 (16-bit)	2 (16-bit)	2 (16-bit)
	Low-power	2 (16-bit)		4 (16-bit) **+ autonomous mode**.
	Watchdogs	1 IWDG and 1 WWDG		1 IWDG and 1 WWDG + early interrupt feature.
	RTC	Yes		Yes **+ advanced features (TrustZone support)**.
	SysTick	1		2
Communication interfaces	SPI	Up to 3	3	3 **+ advanced features (such as more configurability) + autonomous mode registers not compatible**.
	I2C	Up to 4	4	3
	I3C	N/A		**2 + autonomous mode**.
	USART/UART	Up to 3/2	3/2	2/2 **+ autonomous mode**
	LPUART	1		1 **+ new features (such as input capture) + autonomous mode**
	SAI (audio interface)	2		1
	CAN	Up to 2 bxCAN	1 bxCAN	1 FDCAN
	USB	STM32L4x1 devices: no USB. For other STM32L41/42/43/45/46xxx devices: USB FS device. For otherSTM32L47/48/49/4Axxx devices: USB FS OTG.	USB FS OTG with clock recovery.	USB FS host/device with clock recovery.
	SDMMC	1[(1)]		1 + compliance with newer SD/MMC specifications.
	Camera interfaces	1 DCMI[(2)]	1 DCMI and 1 PSSI[(3)]	N/A

Peripheral		STM32L4		STM32U3
		STM32L4	STM32L4+	STM32U375/385
Communication interfaces	OCTOSPI	N/A (Quad-SPI only)	2 + Octo-SPI I/O manager	1
Analog peripherals	ADC	Up to 3 ADCs (12-bit)	2 ADCs (12-bit)	2 ADCs (12-bit) + new features (such as better oversampling).
	DAC	Up to 2 converters (12-bit)	2 converters (12-bit)	2 converters (12-bit)
	COMP	Up to 2	2	2 (**registers not compatible**)
	OPAMP	Up to 2	2	2 **+ new slew rate configuration**.
	Voltage reference buffer	Yes 2 voltage levels		Yes 4 voltage levels
Secure peripherals	AES	Yes(4)	Yes(5)	Yes(6)
	SAES (secure AES)	No		**Yes(6)**
	PKA (private key accelerator)	No	Yes(7)	Yes(6) **+ advanced features (such as SCA resistance)**.
	HASH	Yes(8)	Yes(9)	Yes **+ advanced features (such as support for SHA2-384/512)**.
	RNG	Yes	Yes	Yes **+ entropy enhancement + advanced features (such as connection with SAES/PKA)**.
	CCB (coupling and chaining bridge)	N/A		**Yes**
Signal-processing coprocessors	Digital filters	Up to 4 filters (DFSDM)(10)	4 filters (DFSDM)	1 ADF (1 audio digital filter)
	TSC (touch sensing control)	Up to 24 channels(11)		Up to 21 channels
	LTDC	N/A	1	N/A
	DSI	N/A	1	N/A

1. *Not available on STM32L41x/42x/432/442xx devices.*
2. *Available only for STM32L49/4Axxx devices.*
3. *PSSI available only for STM32L4P/4Qxxx devices.*
4. *Available only for STM32L42/44/46/48/4Axxx devices.*
5. *Available only for STM32L4S/4Qxxx devices.*
6. *Available only for STM32U385xx devices.*
7. *Available only for STM32L4Qxxx devices.*
8. *Available only for STM32L4Axxx devices.*
9. *Not available for STM32L4Rxxx devices.*
10. *Not available for STM32L41/42/43/44xxx devices.*
11. *Depending on the line: for instance, only 12 channels available for STM32L41/42xxx devices.*

5.2 Memory mapping

As shown in the table below, the peripheral address mapping has been changed in the STM32U3 MCUs, compared to the STM32L4, STM32L4+ MCUs. The secure boundary address is not disclosed in this table, as they cannot be compared to the STM32L4/STM32L4+ products. For further information, refer to the product reference manual.

Table 12. Peripheral address mapping of STM32L4, STM32L4+, and STM32U3 MCUs

Peripheral	STM32L4/STM32L4+	STM32U3
	Boundary address(1)	Nonsecure boundary address
HASH	0x5006 0400 - 0x5006 07FF	0x420C 0400 - 0x420C 07FF
AES	0x5006 0000 - 0x5006 03FF	0x420C 0000 - 0x420C 03FF
DCMI	0x5005 0000 - 0x5005 03FF	N/A
GPIOI	0x4800 2000 - 0x4800 23FF	N/A
OCTOSPIM	0x5006 1C00 - 0x5006 1FFF	N/A
DMA2D	0x4002 B000 - 0x4002 BBFF	N/A
GFXMMU	0x4002 C000 - 0x4002 EFFF (2)	N/A
DMAMUX1	0x4002 0800 - 0x4002 0BFF	N/A
I2C4	0x4000 8400 - 0x4000 87FF	N/A
OCTOSPI2	0xA000 1400 - 0xA000 17FF	N/A
OCTOSPI1	0xA000 1000 - 0xA000 13FF	0x420D 1400 - 0x420D 17FF
FSMC	0xA000 0000 - 0xA000 03FF	N/A
DSI	0x4001 6C00 - 0x4001 73FF	N/A
LTDC	0x4001 6800 - 0x4001 6BFF	N/A
USB_FS SRAM(3)	0x4000 6C00 - 0x4000 6FFF	0x4001 6400 - 0x4001 6BFF
USB_FS(3)	0x4000 6800 - 0x4000 6BFF	0x4001 6000 - 0x4001 63FF
OTG_FS	0x5000 0000 - 0x5003 FFFF	N/A
SDMMC1	• 0x4001 2800 - 0x4001 2BFF (APB2) on STM32L4 • 0x5006 2400 - 0x5006 27FF (AHB2) on STM32L4+	0x420C 8000 - 0x420C 83FF
SDMMC2	0x5006 2800 - 0x5006 2BFF(2)	N/A
CCB	N/A	0x420C 7C00 - 0x420C 7FFF
PKA	0x5005 E000 - 0x5005 FFFF(2)	0x420C 2000 - 0x420C 3FFF
PSSI	0x5005 0400 - 0x5005 07FF(2)	N/A
RNG	0x5006 0800 - 0x5006 0BFF	0x420C 0800 - 0x420C 0BFF
ADC	0x5004 0000 - 0x5004 03FF	0x4202 8000 - 0x4202 83FF
GPIOH	N/A	0x4202 1C00 - 0x4202 1FFF
GPIOG	0x4800 1800 - 0x4800 1BFF	0x4202 1800 - 0x4202 1BFF
GPIOF	0x4800 1400 - 0x4800 17FF	N/A
GPIOE	0x4800 1000 - 0x4800 13FF	0x4202 1000 - 0x4202 13FF
GPIOD	0x4800 0C00 - 0x4800 0FFF	0x4202 0C00 - 0x4202 0FFF
GPIOC	0x4800 0800 - 0x4800 0BFF	0x4202 0800 - 0x4202 0BFF
GPIOB	0x4800 0400 - 0x4800 07FF	0x4202 0400 - 0x4202 07FF
GPIOA	0x4800 0000 - 0x4800 03FF	0x4202 0000 - 0x4202 03FF

Peripheral	STM32L4/STM32L4+	STM32U3
	Boundary address(1)	Nonsecure boundary address
GTZC1_ TZSC	N/A	0x4003 2400 - 0x4003 27FF
GTZC1_ TZIC		0x4003 2800 - 0x4003 2BFF
GTZC1_ MPCBB1		0x4003 2C00 - 0x4003 2FFF
GTZC1_ MPCBB2		0x4003 3000 - 0x4003 33FF
TSC	0x4002 4000 - 0x4002 43FF	0x4002 4000 - 0x4002 43FF
CRC	0x4002 3000 - 0x4002 33FF	0x4002 3000 - 0x4002 33FF
Flash registers	0x4002 2000 - 0x4002 23FF	0x4002 2000 - 0x4002 23FF
RCC	0x4002 1000 - 0x4002 13FF	0x4003 0C00 - 0x4003 0FFF
DMA1	0x4002 0000 - 0x4002 03FF	N/A
DMA2	0x4002 0400 - 0x4002 07FF	N/A
GPDMA1	N/A	0x4002 0000 - 0x4002 0FFF
FIREWALL	0x4001 1C00 - 0x4001 1FFF	N/A
EXTI	0x4001 0400 - 0x4001 07FF	0x4003 2000 - 0x4003 23FF
DFSDM1	0x4001 6000 - 0x4001 67FF	N/A
SAI2	0x4001 5800 - 0x4001 5BFF	N/A
SAI1	0x4001 5400 - 0x4001 57FF	0x4001 5400 - 0x4001 57FF
TIM17	0x4001 4800 - 0x4001 4BFF	0x4001 4800 - 0x4001 4BFF
TIM16	0x4001 4400 - 0x4001 47FF	0x4001 4400 - 0x4001 47FF
TIM15	0x4001 4000 - 0x4001 43FF	0x4001 4000 - 0x4001 43FF
USART1	0x4001 3800 - 0x4001 3BFF	0x4001 3800 - 0x4001 3BFF
TIM8	0x4001 3400 - 0x4001 37FF	N/A
SPI1	0x4001 3000 - 0x4001 33FF	0x4001 3000 - 0x4001 33FF
TIM1	0x4001 2C00 - 0x4001 2FFF	0x4001 2C00 - 0x4001 2FFF
COMP	0x4001 0200 - 0x4001 03FF	0x4004 5400 - 0x4004 57FF
VREFBUF	0x4001 0030 - 0x4001 01FF	0x4000 7400 - 0x4000 77FF
SYSCFG	0x4001 0000 - 0x4001 002F	0x4004 0400 - 0x4004 07FF
FDCAN1 RAM	N/A	0x4000 AC00 - 0x4000 AFFF
LPTIM4		0x4004 4C00 - 0x4004 4FFF
LPTIM3		0x4004 4800 - 0x4004 4BFF
CAN1/FDCAN1(4)	0x4000 6400 - 0x4000 67FF	0x4000 A400 - 0x4000 A7FF
LPTIM2	0x4000 9400 - 0x4000 97FF	0x4000 9400 - 0x4000 97FF
LPUART1	0x4000 8000 - 0x4000 83FF	0x4004 2400 - 0x4004 27FF
LPTIM1	0x4000 7C00 - 0x4000 7FFF	0x4004 4400 - 0x4004 47FF
OPAMP	0x4000 7800 - 0x4000 7BFF	0x4000 7000 - 0x4000 73FF
DAC(5)	0x4000 7400 - 0x4000 77FF	0x4202 8400 - 0x4202 87FF
PWR	0x4000 7000 - 0x4000 73FF	0x4003 0800 - 0x4003 0BFF
CRS	0x4000 6000 - 0x4000 63FF	0x4000 6000 - 0x4000 63FF
I2C3	0x4000 5C00 - 0x4000 5FFF	0x4004 2800 - 0x4004 2BFF
I2C2	0x4000 5800 - 0x4000 5BFF	0x4000 5800 - 0x4000 5BFF
I2C1	0x4000 5400 - 0x4000 57FF	0x4000 5400 - 0x4000 57FF

Peripheral	STM32L4/STM32L4+	STM32U3
	Boundary address(1)	Nonsecure boundary address
UART5	0x4000 5000 - 0x4000 53FF	0x4000 5000 - 0x4000 53FF
UART4	0x4000 4C00 - 0x4000 4FFF	0x4000 4C00 - 0x4000 4FFF
USART3	0x4000 4800 - 0x4000 4BFF	0x4000 4800 - 0x4000 4BFF
USART2	0x4000 4400 - 0x4000 47FF	N/A
SPI3	0x4000 3C00 - 0x4000 3FFF	0x4000 2000 - 0x4000 23FF
SPI2	0x4000 3800 - 0x4000 3BFF	0x4000 3800 - 0x4000 3BFF
TAMPER and BKP registers(6)	0x4000 3400 - 0x4000 37FF(7)	0x4000 7C00 - 0x4000 7FFF
IWDG	0x4000 3000 - 0x4000 33FF	0x4000 3000 - 0x4000 33FF
WWDG	0x4000 2C00 - 0x4000 2FFF	0x4000 2C00 - 0x4000 2FFF
RTC	0x4000 2800 - 0x4000 2BFF	0x4000 7800 - 0x4000 7BFF
TIM7	0x4000 1400 - 0x4000 17FF	0x4000 1400 - 0x4000 17FF
TIM6	0x4000 1000 - 0x4000 13FF	0x4000 1000 - 0x4000 13FF
TIM5	0x4000 0C00 - 0x4000 0FFF	N/A
TIM4	0x4000 0800 - 0x4000 0BFF	0x4000 0800 - 0x4000 0BFF
TIM3	0x4000 0400 - 0x4000 07FF	0x4000 0400 - 0x4000 07FF
TIM2	0x4000 0000 - 0x4000 03FF	0x4000 0000 - 0x4000 03FF
ADF1	N/A	0x4003 4000 - 0x4003 4FFF
DLYBOS1		0x420C F400 - 0x420C F3FF
DLYBSD1		0x420C 8400 - 0x420C 87FF
SAES		0x420C 0C00 - 0x420C 0FFF
ICACHE		0x4003 0400 - 0x4003 07FF
RAMCFG		0x4002 6000 - 0x4002 6FFF

1. *If no boundary address, it means the peripheral is not available on all STM32L4/STM32L4+ devices.*
2. *Available only for STM32L4P5/4Q5xx.*
3. *USB for STM32U375/385.*
4. *FDCAN1 for STM32U375/385.*
5. *DAC1 for STM32L4+.*
6. *TAMP for STM32U375/385.*
7. *Available only for STM32L4+.*

6 Migration of system peripherals

6.1 System configuration controller (SYSCFG)

Table 13. SYSCFG features in STM32L4, STM32L4+, and STM32U3 MCUs

STM32L4 and STM32L4+	STM32U3
• Remapping memory areas. • Managing the external interrupt line connection to the GPIOs. • Managing robustness feature. • Setting SRAM2 write protection and software erase. • Configuring FPU interrupts. • Enabling the firewall. • Enabling/disabling the I^2C fast-mode plus driving capability on some I/Os.	• Managing robustness feature. • Configuring FPU interrupts. • Enabling/disabling the I^2C fast-mode plus driving capability on some I/Os and voltage booster for I/O analog switches. • Configuring TrustZone® security register access. • Tracking the PVT conditions to control the current slew-rate and output impedance in I/O buffer through compensations cells on V_{DD} and V_{DDIO2} GPIOs. • Configuration of IRTIM.

The remapping of memory areas was replaced by bank swapping, fixed mapping of SRAMs on C-bus (IBus for Cortex®-M4 devices), and a possibility to change the vector table offset in the VTOR of the system control block (part of the private peripheral bus). Refer to the referenced documents Introduction and Introduction for more information.

Configuration of SRAMs (including write protection and software erase settings) is ensured by the RAMCFG peripheral.

6.2 Embedded flash memory (FLASH)

Table 14. Flash memory features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature		STM32L4/STM32L4+	STM32U3
Page size		• 0x0800 0000 to up to 0x080F FFFF • 0x0810 0000 to up to 0x081F FFFF (only for STM32L4+)	• Bank1: 0x0800 0000 to 0x0807 FFFF • Bank2: 0x0808 0000 to 0x080F FFFF
Main/program memory		For **STM32L4+**: • Up to 2 Mbytes. • Split in two banks. • When dual bank is enabled: – Each bank = 256 pages of 4 Kbytes. – Each page = 8 rows of 512 bytes. • When dual bank is disabled: – Memory block contains 256 pages of 8 Kbytes. – Each page = 8 rows of 1024 bytes. For **STM32L47/48/49/4Axxx**: • Up to 1 Mbyte • Split in two banks: – Each bank = 256 pages of 2 Kbytes. – Each page = 8 rows of 256 bytes. For **STM32L45/46xxx**: • Up to 512 Kbytes. • One bank: – One bank = 256 pages of 2 Kbytes. – Each page = 8 rows of 256 bytes. For **STM32L43/44xxx**: • Up to 256 Kbytes. • One bank: – One bank = 128 pages of 2 Kbytes. – each page = 8 rows of 256 bytes. For **STM32L41/42xxx**: • Up to 128 Kbytes. • One bank = 64 pages of 2 Kbytes.	For STM32U375/385: • Up to 1 Mbyte: – Dual-bank architecture. – 512 Kbytes per bank for the main memory. – 4-Kbyte page size. • 68-Kbyte system memory. • 36-Kbyte immutable secure area containing the root security services. • 512 bytes of OTP (one-time programmable) bytes for user data (64 double words). • Option bytes for user configuration, accessible only through the flash register interface.
Specific features		• RWW (read-while-write). • Dual-bank boot (only for STM32L4+ and STM32L47/48/49/4Axxx). • ECC (single error correction and double error detection).	• RWW (read-while-write). • Dual-bank boot. • ECC (single error correction and double error detection).
Programming and read granularity		72 bits (including 8 ECC bits).	64 effective bits plus 8 ECC bits.
Wait states (WS)		Up to 4 WS (depending on the supply voltage and the frequency).	The number of wait states depends on the LPM value: • Up to 2 WS when LPM = 0 (depending on the supply voltage and the frequency). • Up to 4 WS when LPM = 1 (depending on the supply voltage and the frequency).
One time programmable (OTP)		1-Kbyte OTP bytes (bank1).	512-byte OTP for user data.
Read protection (RDP)	Level 0 (RDP = 0xAA)	No protection: no debug restriction.	Device open: • No debug restriction (secure and nonsecure). • Boot address must target a secure area when TrustZone® is enabled (secure SRAM, secure flash memory, RSS in system flash memory).

Feature		STM32L4/STM32L4+	STM32U3
Read protection (RDP)	Level 0.5 (RDP = 0x55)	N/A	Device partially closed (only when TrustZone® is enabled): • Nonsecure debug only. • NS-Flash access allowed (with debug connection). • Boot address must target a secure flash memory area (user or system). Boot from SRAMs is not allowed. • Regression from Level 1 to level 0.5 can be blocked by OEM2 key.
	Level 1 (RDP ≠ {0xAA, 0x55})	Memory readout protection	Device memories protected: flash memory, backup registers, and SRAM2 totally inaccessible: • Nonsecure debug only. • Boot address must target user flash memory (must be secure when TrustZone® is enabled). • Regression from Level 1 to level 0 can be blocked by OEM1 key.
	Level 2 (RDP = 0xCC)	Full protection: no debug(1)	Closed device (no JTAG): • No option byte change: – No debug (JTAG fuse). – Boot address in user flash memory (must be secure when TrustZone® is enabled). • RDP level 2 cannot be changed, unless OEM2 unlocking key is activated.
Write protection (WRP)		Two write protection areas per bank: 2-Kbyte granularity. For **STM32L4+** MCUs: dual bank with 2 areas per bank or single bank with 4 areas.	Two write protection areas per bank: 4-Kbyte granularity.
User option bytes	RDP option bytes	• 0xAA: Level 0 • 0xCC: Level 2 • Others: Level 1	• 0xAA: Level 0 • 0x55: Level 0.5 • 0xCC: Level 2 • Others: Level 1
	Reset option bytes	• BOR_LEV[2:0] • nRST_STOP • nRST_STDBY • nRST_SHDW • SRAM2_RST	• BOR_LEV[2:0] • BDRST_STOP • nRST_STOP • nRST_STDBY • nRST_SHDW • SRAM1_RST • SRAM2_RST
	Watchdog option bytes	• IWDG_SW • IWDG_STOP • IWDG_STDBY • WWDG_SW	
	FLASH banking option bytes	BFB2 (except for STM32L41/42/43/44/45/46xxx)	SWAP_BANK
		• DUALBANK (except for STM32L4+ and STM32L41/42/43/44/45/46xxx devices) • DB1M (for STM32L4+ devices) • DBANK (for STM32L4+ devices)	DUALBANK
	RAM and ECC enable option bits	SRAM2_PE	
	Secure and nonsecure boot option bytes	• nSWBOOT0 (except for STM32L47/48xxx devices). • nBOOT0 (except for STM32L47/48xxx devices).	• nSWBOOT0 • nBOOT0 • BOOT_LOCK

Feature		STM32L4/STM32L4+	STM32U3
User option bytes	Secure and nonsecure boot option bytes	• nBOOT1.	
		N/A	ADD[24:0] option bytes in FLASH_BOOT0R, FLASH_BOOT1R, and FLASH_SBOOT0R registers
	IO speed and pull-up selection option bits		• IO_VDD_HSLV • IO_VDDIO2_HSLV
	Global TrustZone® activation option bit		TZEN
	FLASH secure watermark option bytes	For **STM32L4** devices: • PCROPx_STRT[15:0] • PCROPx_END[15:0] For **STM32L4+** devices: • PCROPx_STRT[16:0] • PCROPx_END[16:0]	• SECWM1_STRT[6:0] • SECWM1_END[6:0] • HDP1_END[6:0] • HDP1EN • SECWM2_STRT[6:0] • SECWM2_END[6:0] • HDP2_END[6:0] • HDP2EN
	FLASH write protection (WRP) area option bytes	N/A	STRT[6:0], END[6:0], and UNLOCK option bytes in the WRP1AR, WRP1BR, WRP2AR, and WRP2BR registers.
	FLASH locking keys for level regression option bytes		• OEM1KEY[31:0] • OEM1KEY[63:32] • OEM1KEY[95:64] • OEM1KEY[127:96] • OEM2KEY[31:0] • OEM2KEY[63:32] • OEM2KEY[95:64] • OEM2KEY[127:96]
Protections		• Write protection: 2 areas per bank. • PCROP protection: one PCROP area per bank.	• 4 write protection areas: 2 per bank. • Configurable protection against unprivileged accesses with flash memory page granularity.
Security		N/A	• TrustZone® • 2 secure watermark-based areas (1 per bank). • 2 secure HDP (hide protection) and HDP extension areas are part of the secure areas (1 per bank).

1. *Memory read protection Level 2 is an irreversible operation. When Level 2 is activated, the level of protection cannot be decreased to Level 0 or Level 1.*

6.3 SRAMs

In STM32L4 and STM32L4+ MCUs, the control of SRAM1 and SRAM2 is integrated within the SYSCFG.

In STM32U3 MCUs, the new RAMCFG controller peripheral is dedicated to controlling SRAM1 and SRAM2.

Refer to the section "*RAM configuration controller*" in the product reference manual for more details.

Table 15. SRAM features in STM32L4 and STM32L4+, and STM32U375/385 MCUs

Feature		STM32L4STM32L4+		STM32U3
		STM32L4	STM32L4+	STM32U375/385
Size		For **STM32L49/4Axxx** devices: • 320 Kbytes – 256 Kbytes (SRAM1) – 64 Kbytes (SRAM2) For **STM32L47/48xxx** devices: • 128 Kbytes – 96 Kbytes (SRAM1) – 32 Kbytes (SRAM2) For **STM32L45/46xxx** devices: • 160 Kbytes – 128 Kbytes (SRAM1) – 32 Kbytes (SRAM2) For **STM32L43/44xxx** devices: • 64 Kbytes – 48 Kbytes (SRAM1) – 16 Kbytes (SRAM2) For **STM32L41/42xxx** devices: • 40 Kbytes – 32 Kbytes (SRAM1) – 8 Kbytes (SRAM2)	For **STM32L4R/4Sxxx** devices: • 640 Kbytes – 192 Kbytes (SRAM1) – 64 Kbytes (SRAM2) – 384 Kbytes (SRAM3) For **STM32L4P/4Qxxx** devices: • 320 Kbytes – 128 Kbytes (SRAM1) – 64 Kbytes (SRAM2) – 128 Kbytes (SRAM3)	• 256 Kbytes – 192 Kbytes (SRAM1): (2 x 16Kbytes + 5 x 32 Kbytes) – 64 Kbytes (SRAM2): (8 Kbytes + 24 Kbytes + 32 Kbytes)
Read/write granularity		Bytes, half words (16 bits) or full words (32 bits)		
Bus connectivity to CPU	System bus	SRAM1	SRAM1, SRAM2, SRAM3	SRAM1, SRAM2
	Other buses	IBus, DBus: SRAM1, SRAM2		Fast C-bus: SRAM1, SRAM2
Retention in low-power modes		SRAM1, SRAM2, SRAM3, and all register content fully retained in Stop 0/1/2 modes. Optional retention of SRAM2 in Standby mode.		Optional retention of inidividual subblocks of SRAM1 and SRAM2 in Stop 0/1/2/3 modes. Optional retention of individual SRAM2 sub-blocks in Standby mode.
Security		N/A		When TrustZone® security is enabled, all SRAMs are secure after reset. The SRAMs can be programmed as nonsecure using the MPCBB with a block granularity of 512 bytes.
Hardware erase conditions		N/A		All SRAMs are erased by hardware in case of RDP level regression to L0.5 or L0. SRAM2 is optionally protected by the tamper detection circuit and is blocked or erased by hardware in case of tamper detection.
Software erase conditions		The SRAM2 erase can be requested by software by configuring SRAM2ER in SYSCFG_SCSR.		The erase of individual SRAMs can be requested by execution of a specific software sequence on RAMCFG registers.
System reset erase		SRAM2 is optionally erased by hardware after a system reset (according to option bytes settings).		Both SRAM1 and SRAM2 are optionally erased by hardware after a system reset (according to option bytes settings).

Feature	STM32L4STM32L4+		STM32U3
	STM32L4	STM32L4+	STM32U375/385
Write protection	SRAM2 can be write-protected with a page granularity of 1 Kbyte. This configuration is done in the SYSCFG registers.		SRAM2 can be write-protected with a page granularity of 1 Kbyte. This configuration is done in the RAMCFG registers.
Error detection	Optional hardware parity check on SRAM2 (one bit per byte of data), configurable with user option bytes. In case of parity error an NMI is generated. The same error can also be linked to the BRK_IN break input of TIM1/TIM8/TIM15/TIM16/TIM17, with the SPL control bit.		Optional hardware parity check on SRAM2 (1 bit per byte of data), configurable in RAMCFG registers and/or with user option bytes. An interrupt or NMI is generated, if enabled in RAMCFG. The failing address can be optionally stored. The parity error triggers a system break event in TIM1/TIM15/TIM16/TIM17, if the SPL bit is set.

6.4 Instruction cache (ICACHE)

STM32U3 MCUs embed an 8-Kbyte instruction cache (ICACHE) that allows boosted code execution from the internal flash memory or external Octo-SPI memories. This cache can be configured in 2-way associative mode, or in the more power-efficient directly-mapped mode.

The STM32L4 and STM32L4+ MCUs do not embed any cache.

6.5 Direct memory access controller (DMA)

The STM32L4, STM32L4+, and STM32U3 MCUs have different DMA architectures and features. While each DMA channel of STM32L4/STM32L4+ can be configured only for a limited set of possible peripheral requests, any request can be assigned to every channel on STM32U3 devices.

These channels differ in FIFO size and type of addressing (linear or 2D addressing). Moreover, each channel can be configured in a linked-list manner, where individual list nodes represent a configuration of DMA registers enabling the execution of a sequence of multiple transfers between memories and peripherals. See Table 16 below for more information about the differences between STM32L4/STM32L4+ and STM32U3 DMAs.

All devices embed two DMA controllers:

- DMA1 (7 channels) and DMA2 (7 channels) for STM32L4 and STM32L4+ MCUs.
- GPDMA1 (12 channels) for STM32U3 MCUs.

STM32L49/4Axxx and STM32L4+ devices also embed a Chrom-ART Accelerator (DMA2D), which is a specialized DMA dedicated to image manipulation. The DMA2D peripheral is not present on STM32U3 devices.

Table 16. DMA features of STM32L4 and STM32L4+, and STM32U375/385 MCUs

Feature	STM32L4/STM32L4+		STM32U3
	DMA1	DMA2	GPDMA1
Architecture	Each instance of DMA controllers can access memory and peripherals.		
Number of instances	1	1	1
Number of masters	1 single bidirectional AHB master per instance.		Dual bidirectional AHB master.
Number of channels	7	7	12
Linked-List	N/A		• Separately programmed source and destination transfers. • Programmable data handling between source and destination (such as reordering, packing, padding, etc.). • Block-level (programmable number of data bytes).

Feature	STM32L4/STM32L4+		STM32U3
	DMA1	DMA2	GPDMA1
			• Linear source and destination addressing: either fixed or contiguously-incremented addressing, programmed at block level, between successive burst transfers.
Linked-List 2D addressing	N/A		• 2D source and destination addressing. • Scatter-gather (multi-buffer transfers), data interleaving and de-interleaving via 2D addressing.
Autonomous mode	N/A		Autonomous data transfers and wake-up during low-power Sleep mode.
TrustZone® security	N/A		Yes
Privileged/unprivileged DMA	N/A		Yes

6.6 Reset and clock control (RCC)

The STM32U3 MCUs implement the same RCC features as the STM32L4 and STM32L4+ MCUs, with some specification updates.

Table 17. RCC features of STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
MSI	• MSI is a low-power oscillator with programmable frequency up to 48 MHz. • It can replace PLLs as system clock (faster wake-up, lower consumption). • In PLL mode, it can be used as USB device clock (no need for an external high-speed crystal oscillator). • 12 frequency ranges are available: 100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz, and 48 MHz. • Auto-calibration from LSE (PLL-mode).	• MSI is made of two internal RC oscillators, clocked at 96 MHz and 24 MHz. Two output clocks are generated from these divided oscillators: MSIS and MSIK. • MSIS can be selected as system clock (selection from MSI, HSE, or HSI16). • MSIK can be selected by some peripherals as kernel clock. • In PLL mode, MSI can be used as USB device clock (no need for an external high-speed crystal oscillator). • 8 frequency ranges (6 unique frequencies): 3 MHz, 6 MHz, 12 MHz, 24 MHz, 48 MHz, 96 MHz. • Default value for MSIS and MSIK frequencies is 12 MHz, clocked from the 24 MHz (low-power) RC. • Auto-calibration from LSE or HSE (PLL-mode).
HSI16	16 MHz RC factory and user trimmed.	
LSI	• 32 kHz RC. • Kept running in Stop and Standby modes.	• 32 kHz RC (with higher accuracy), can be divided to 250 Hz for lower power consumption. • Kept running in Stop and Standby modes.
HSE	4 to 48 MHz	4 to 50 MHz
LSE	• 32.768 kHz. • Configurable drive/consumption. • Available in Backup domain (VBAT).	
HSI48	• 48 MHz RC (not available on STM32L47/48xxx devices). • Can drive USB (OTG) FS, SDMMC, and RNG.	• 48 MHz RC. • Can drive USB, SDMMC, and RNG.
PLL	• Main PLL for system: – x2 PLLs for SAI1/2, ADC, RNG, SDMMC, and OTG_FS clock (for STM32L4+ and STM32L47/48/49/4Axxx). – x1 PLL for SAI1, ADC, RNG, SDMMC, USB FS clock (forSTM32L43/44/45/46xxx).	N/A

Feature	STM32L4/STM32L4+	STM32U3
	• Each PLL provides up to three independent outputs. • The PLL sources are MSI, HSI16, and HSE.	
System clock frequency	• Up to 80 MHz (120 MHz for STM32L4+). • 4 MHz after reset using MSI.	• Up to 96 MHz. • 12 MHz after reset using MSI.
AHB, APB1, APB2 frequency	Up to 80 MHz (120 MHz for STM32L4+).	Up to 96 MHz.
RTC clock source	LSI, LSE, or HSE/32	
MCO clock source	• One MCO pin: PA8. • Selection from SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, or LSI (or HSI48, except for STM32L47/48xxx devices). • Configurable output prescaler 1, 2, 4, 8, or 16.	• Two MCO outputs available on pins: PA8, PA9, and PA10. • Selection from SYSCLK, HSI16, HSE, MSIS, MSIK, LSE, LSI, or HSI48. • Configurable prescaler for each output 1, 2, 4, 8, 16, 32, 64, or 128.
Clock security system (CSS)	CSS on HSE or CSS on LSE	
Internal oscillator measurement/calibration	• LSE connected to TIM15 or TIM16 CH1: can measure HSI16 or MSI with respect to LSE clock high precision. • LSI connected to TIM16 CH1: can measure LSI with respect to HSI16 or HSE clock precision. • HSE/32 connected to TIM17 CH1: can measure HSE with respect to LSE/HSI16 clock. • MSI connected to TIM17 CH1: can measure MSI with respect to HSI16/HSE clock. • OnSTM32L41/42/43/44/45/46xxx, the HSE/32 and MSI are connected to TIM16 CH1.	• The frequency of all on-board clock sources can be indirectly measured by means of the TIM15, TIM16, or TIM17 channel 1 input capture and LPTIM1 or LPTIM2 channel 2 input capture. • Calibration using LSE: HSI16 and MSI calibration using LSE, TIM15/TIM16/TIM17, and LPTIM2. • Calibration using HSE: – HSI16 and MSI calibration using HSE, TIM16/TIM17, and LPTIM2. – LSI calibration using HSE, TIM16/TIM17, and LPTIM1.
Interrupt	• CSS (linked to NMI IRQ). • LSECSS, LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY, PLLSAI1RDY, PLLSAI2RDY (only on STM32L4+ and STM32L47/48/49/4Axxx), HSI48RDY (not available on STM32L47/48xxx devices) (linked to RCC global IRQ).	• CSS (linked to NMI IRQ for HSE and Tamper for LSE): HSECSS, LSECSS. • HSERDY, LSERDY, HSIRDY, HSI48RDY, LSIRDY, MSISRDY, MSIKRDY, MSIPLL0RDY, MSIPLL1RDY (linked to global RCC IRQ). • MSIPLLUF, MSIPLLHSUF (linked to global RCC IRQ).
Autonomous mode	N/A	• Peripherals supporting autonomous mode are able to generate a kernel clock and AHB/APB bus clock requests when needed even in Stop modes 0/1/2. • Either MSIS or HSI16 are woken up for this purpose (can be selected in the RCC registers).

6.6.1 Performance versus V_{CORE} ranges

In the STM32U3 series, the maximum CPU clock frequency and the number of flash memory wait states depend on the selected voltage range V_{CORE}. The tables below present the different clock source frequencies depending on different product voltage range for STM32L4, STM32L4+, and STM32U3 MCUs.

Table 18. Flash memory wait states vs. maximum core frequency on STM32L4 and STM32L4+ series

CPU performance	Power performance (1)	V_{CORE} range	Typical value (V)	Max frequency (MHz)(2)					
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS
STM32L4 series									
High	Medium	1	1.2	-	80	64	48	32	16
Medium	High	2	1.0	-	26	26	18	12	6
STM32L4+ series									
High	Medium	1 (boost mode)	1.28	120	100	80	60	40	20
		1 (normal mode)	1.2	-	-	80	60	40	20
Medium	High	2	1.0	-	-	-	26	16	8

1. *When power performance increases, power consumption per MHz decreases.*
2. *WS = wait states.*

Table 19. Flash memory wait states vs. maximum core frequency on STM32U3 series

CPU performance	Power performance	V_{CORE} range	Typical voltage (V)(1)	Max frequency (MHz)											
				LPM = 0						LPM = 1					
				5 WS	4 WS	3 WS	2 WS	1 WS	0 WS	5 WS	4 WS	3 WS	2 WS	1 WS	0 WS
High	Medium	Range 1	~0.75	-	-	-	96	64	32	-	96	80	60	40	20
Medium	Low	Range 2	~0.9	-	-	-	48	32	16	-	-	-	48	32	16

1. *The actual value may differ due to AVS (adaptive voltage scaling).*

6.6.2 Peripheral access configuration

Since the address mapping of some peripherals has been changed in the STM32U3 MCUs, compared to STM32L4 and STM32L4+ MCUs, different registers must be used to control and configure peripheral clocks and reset mode. Table 20 below shows the RCC registers used for peripheral access configuration on STM32L4, STM32L4+, and STM32U3 MCUs.

Table 20. RCC registers for peripheral access configuration on STM32L4, STM32L4+, and STM32U3 MCUs

Bus	STM32L4/STM32L4+	STM32U3	Comments
AHB	• RCC_AHB1RSTR (AHB1) • RCC_AHB2RSTR (AHB2) • RCC_AHB3RSTR (AHB3)	• RCC_AHB1RSTR1 (AHB1) • RCC_AHB2RSTR1 (AHB2) • RCC_AHB2RSTR2 (AHB2)	Used to control/reset the AHB peripherals.
	• RCC_AHB1ENR (AHB1) • RCC_AHB2ENR (AHB2) • RCC_AHB3ENR (AHB3)	• RCC_AHB1ENR1 (AHB1) • RCC_AHB2ENR1 (AHB2) • RCC_AHB2ENR2 (AHB2)	Used to enable/disable the AHB peripherals clock.

Bus	STM32L4/STM32L4+	STM32U3	Comments
AHB	• RCC_AHB1SMENR (AHB1) • RCC_AHB2SMENR (AHB2) • RCC_AHB3SMENR (AHB3)	• RCC_AHB1SLPENR1 (AHB1 - Sleep mode only) • RCC_AHB1STPENR1 (AHB1 - Stop modes only) • RCC_AHB2SLPENR1 (AHB2 - Sleep mode only) • RCC_AHB2STPENR1 (AHB2 - Stop modes only) • RCC_AHB2SLPENR2 (AHB2 - Sleep mode only) • RCC_AHB2STPENR2 (AHB2 - Stop modes only)	Used to enable/disable the AHB peripheral clocks in Sleep and Stop modes.
APB1	• RCC_APB1RSTR1 • RCC_APB1RSTR2	• RCC_APB1RSTR1 • RCC_APB1RSTR2	Used to control/reset the APB1 peripherals.
	• RCC_APB1ENR1 • RCC_APB1ENR2	• RCC_APB1ENR1 • RCC_APB1ENR2	Used to enable/disable the APB1 peripherals clock.
	• RCC_APB1SMENR1 • RCC_APB1SMENR2	• RCC_APB1SLPENR1 (Sleep mode only) • RCC_APB1STPENR1 (Stop modes only) • RCC_APB1SLPENR2 (Sleep mode only) • RCC_APB1STPENR2 (Stop modes only)	Used to enable/disable the APB1 peripheral clocks in Sleep and Stop modes.
APB2	• RCC_APB2RSTR	• RCC_APB2RSTR	Used to control reset the APB2 peripherals
	• RCC_APB2ENR	• RCC_APB2ENR	Used to enable/disable the APB2 peripherals clock
	• RCC_APB2SMENR	• RCC_APB2SLPENR (Sleep mode only) • RCC_APB2STPENR (Stop modes only)	Used to enable/disable the APB2 peripheral clocks in Sleep and Stop modes.
APB3	N/A	• RCC_APB3RSTR	Used to control reset the APB3 peripherals.
		• RCC_APB3ENR	Used to enable/disable the APB3 peripherals clock.
		• RCC_APB3SLPENR (Sleep mode only) • RCC_APB3STPENR (Stop modes only)	Used to enable/disable the APB3 peripheral clocks in Sleep and Stop modes.
Peripherals independent clock	• RCC_CCIPR • RCC_CCIPR2 (not available on STM32L47/48xxx devices)	• RCC_CCIPR1 • RCC_CCIPR2 • RCC_CCIPR3	Used to select independent/kernel clock sources for individual peripherals (having corresponding input).

6.6.3 Peripheral clock configuration

The peripherals presented below have a dedicated clock source (independent from the system clock), that is used to generate the clock required for their operation. This section presents the differences between STM32L4, STM32L4+, and STM32U3 MCUs, for the peripherals with different clock sources.

SAI

- On STM32L4+ and STM32L47/48/49/4Axxx devices, the SAI clocks are derived from one of the following sources:
  - An external clock mapped on SAI1_EXTCLK or SAI2_EXTCLK.
  - PLLSAI1 VCO (PLLSAI1CLK).
  - PLLSAI2 VCO (PLLSAI2CLK).
  - Main PLL VCO (PLLSAI3CLK).
  - HSI16 clock.
- On STM32L43/44/45/46xxx devices, the SAI clocks are derived from one of the following sources:
  - An external clock mapped on SAI1_EXTCLK for SAI1.
  - PLLSAI1 (P) divider output (PLLSAI1CLK).
  - Main PLL (P) divider output (PLLSAI2CLK).
  - HSI16 clock.
- On STM32U3 devices, the SAI1 clock is derived from one of the following sources (selected by software):
  - An external clock mapped on AUDIOCLK.
  - MSIK clock.
  - HSE clock.

DFSDM/ADF/MDF

- On STM32L4 devices, the DFSDM clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK).
  - APB2 clock (PCLK2).
- On STM32L4+ devices, the DFSDM audio clock is derived from one of the following sources (selected by software):
  - SA1 clock.
  - HSI16 clock.
  - MSI clock.
- On STM32U3 devices, the ADF audio clock is derived from one of the following sources (selected by software):
  - HLCK clock.
  - SAI1 kernel.
  - MSIK clock.
  - An external clock mapped on AUDIOCLK.

OCTOSPI

- STM32L4 devices do not support the OCTOSPI peripheral.
- On STM32L4+ devices, the Octo-SPI clock is derived from one of the following sources (selected by software):
  - System clock.
  - PLL48M1CLK.
  - MSI clock.
- On STM32U3 devices, the OCTOSPI clock is derived from one of the following sources (selected by software):
  - System clock.
  - MSIK clock.

FDCAN

- On STM32U3 devices, the FDCAN clock is derived from one of the following sources (selected by software):
  - System clock.
  - MSIK clock.

Note: FDCAN is not available on STM32L4 and STM32L4++ devices and the available bxCAN has no peripheral/ kernel clock input.

USB

- On STM32L4 and STM32L4+ devices, the USB (OTG) FS clock is derived from one of the following sources (selected by software):
  - Main PLL VCO (PLL48M1CLK).
  - PLLSAI1 VCO (PLL48M2CLK).
  - MSI clock (only in PLL-mode with LSE).
  - HSI48 internal oscillator (not available on STM32L47/48xxx devices).
- On STM32U3 devices, the USB clock is derived from one of the following sources (selected by software), which can be divided by 2 optionally:
  - System clock.
  - HSE clock.
  - HSI48 clock.
  - MSIK clock (only in PLL-mode).

SDMMC

- On STM32L4 and STM32L4+ devices, the SDMMC clock is derived from one of the following sources (selected by software):
  - Main PLL VCO (PLL48M1CLK).
  - PLLSAI1 VCO (PLL48M2CLK).
  - MSI clock (only in PLL-mode with LSE).
  - HSI48 internal oscillator (not available on STM32L47/48xxx devices).
- On STM32U3 devices, the SDMMC clock is derived from one of the following sources (selected by software):
  - System clock.
  - HSE clock.
  - HSI48 clock.
  - MSIK clock (only in PLL-mode).

RNG

- On STM32L4 and STM32L4+ devices, the RNG clock is derived from one of the following sources (selected by software):
  - Main PLL VCO (PLL48M1CLK).
  - PLLSAI1 VCO (PLL48M2CLK).
  - MSI clock (only in PLL-mode with LSE).
  - HSI48 internal oscillator (not available on STM32L47/48xxx devices).
- On STM32U3 devices, the RNG clock is derived from one of the following sources (selected by software):
  - MSIK clock.
  - HSI48 internal oscillator.

ADC/DAC

- On STM32L4 and STM32L4+ devices, the ADC clock is derived from one of the following sources (selected by software):
  - System clock.
  - PLLSAI1 VCO (PLLADC1CLK): (not available on STM32L41/42xxx devices).
  - PLLSAI2 VCO (PLLADC2CLK): (available only on STM32L47/48/49/4Axxx devices).
- STM32L4 and STM32L4+ devices do not have a dedicated clock for DAC, independent from the system clock.
- On STM32U3 devices, the ADC and DAC clock is derived from one of the following sources (selected by software), which can be optionally divided by a factor up to 512:
  - HCLK clock.
  - HSE clock.
  - MSIK clock.
- Additionally, on STM32U3 devices, the DAC1 sample and hold clock is derived from one of the following sources (selected by software):
  - LSI.
  - LSE.

U(S)ART

- On STM32L4 and STM32L4+ devices, the U(S)ARTs clock is derived from one of the following sources (selected by software):
  - System clock (SYSCLK).
  - HSI16 clock.
  - LSE clock.
  - APB1 or APB2 clock (PCLK1 or PCLK2, depending on which APB U(S)ART is mapped).
- On STM32U3 devices, the U(S)ART clock is derived from one of the following sources (selected by software):
  - HSI16 clock.
  - APB1 or APB2 clock (PCLK1 or PCLK2, depending on which APB U(S)ART is mapped).

LPTIM

- On STM32L4 and STM32L4+ devices, the LPTIMx clock is derived from one of the following sources (selected by software):
  - LSI clock.
  - LSE clock.
  - HSI16 clock.
  - APB1 clock (PCLK1).
  - External clock mapped on LPTIMx_IN1.
- On STM32U3 devices, the LPTIM2 clock is derived from one of the following sources (selected by software):
  - APB1 clock (PCLK1)
  - LSI clock.
  - LSE clock.
  - HSI16 clock.
- On STM32U3 devices, the LPTIM1 clock and LPTIM34 clock are derived from one of the following sources (selected by software):
  - MSIK clock.
  - LSI clock.
  - LSE clock.
  - HSI16 clock.

LPUART

- On STM32L4 and STM32L4+ devices, the LPUART1 clock is derived from one of the following sources (selected by software):
  - System clock.
  - APB1 clock (PCLK1).
  - LSE clock.
  - HSI16 clock.
- On STM32U3 devices, the LPUART1 clock is derived from one of the following sources (selected by software):
  - PCLK3 clock.
  - MSIK clock.
  - LSE clock.
  - HSI16 clock.

SPI

- STM32L4 and STM32L4+ devices do not have a dedicated clock for SPI.
- On STM32U3 devices, the SPI clock is derived from one of the following sources (selected by software):
  - APB1 or APB2 clock (PCLK1 or PCLK2, depending on which APB the SPI is mapped).
  - MSIK clock.

I2C/I3C

- On STM32L4 and STM32L4+ devices, the I2C clocks are derived from one of the following sources (selected by software):
  - System clock.
  - HSI16 clock.
  - APB1 clock (PCLK1).
- On STM32U3 devices, the I2C and I3C clocks (one clock for each instance) are derived from one of the following sources:
  - APB1, APB2, or APB3 clock (PCLK1, PCLK2, or PCLK3, depending on which APB the instance is mapped).
  - MSIK clock

Note: The I3C peripheral is not available on STM32L4 and STM32L4+ devices.

SAES

On STM32U3 devices, the SAES clock is derived from the HCLK clock.

Note: SAES is not available on STM32L4 and STM32L4+ devices.

6.7 Power controller (PWR)

STM32U3 MCUs feature a similar PWR functionality to STM32L4 and STM32L4+ MCUs, with some specification updates and enhancements.

Like on STM32L4, STM32L4+ devices, on STM32U3 devices several peripherals are supplied through independent power domains: V_{DDA}, V_{DDIO2}, and V_{DDUSB}. These supplies must be provided with a valid operating supply on the VDD pin. Several other independent power domains, such as V_{LCD} and V_{DDDSI}, are not present on STM32U3 devices.

STM32L412/433/452/4x6xx and STM32L4P/4Q/4Rxx devices allow an the connection of an external SMPS (DC-DC) power converter. In contrast, some STM32U3 devices directly embed an internal SMPS DC-DC step-down converter. Therefore, no external SMPS is required. This internal SMPS is connected in parallel with the LDO, with on-the-fly selection for optimal power consumption and noise reduction.

On STM32U3 MCUs, the SMPS power supply pins are available only on specific packages embedding an SMPS step-down converter. If the SMPS converter is not going to be used in such a package, it is recommended to connect these supply pins as follows:

- VDDSMPS and VLXSMPS connected to VSS.
- VDD11 pins connected to VSS through two 2.2 µF capacitors, like in normal mode.

Table 21. PWR features of STM32L4, STM32L4+ and STM32U3 MCUs

Features	STM32L4 and STM32L4+	STM32U3
Power supplies	• V_{DD} = 1.71 to 3.6 V: External power supply for I/Os, flash memory and internal regulator. • It is provided externally through VDD pins.	• V_{DD} = 1.71 to 3.6 V: External power supply for I/Os, the internal regulator, and the system analog, such as reset, power management, and internal clocks. • It is provided externally through VDD pins.
	• V_{CORE} = 1.0 to 1.28 V: Power supply for digital peripherals, SRAM, and flash memory. • It is controlled by an internal voltage regulator and can be connected to an external SMPS. • Two V_{CORE} ranges can be selected by software, depending on the target frequency.	• V_{CORE} = 0.75 to 0.9 V: Power supply for digital peripherals, SRAM, and flash memory. • It is generated by an internal voltage regulator, LDO, or SMPS. • Two V_{CORE} power ranges can be programmed by software, depending on the target frequency. • The actual voltage may differ, due to AVS (Adaptive Voltage Scaling).
	V_{BAT} = 1.55 to 3.6 V: Power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.	V_{BAT} = 1.55 to 3.6 V: When V_{DD} is not present, V_{BAT} is the power supply for RTC, external clock 32 kHz oscillator and backup registers.
	Independent power supplies (V_{DDA}, V_{DDIO2}, V_{DDUSB}) allow a reduction of the power consumption by running the MCU at a lower supply voltage than analog and/or USB.	
	• V_{DDA} = 1.62 to 3.6 V (ADCs/COMPs) / 1.8 to 3.6 V (DAC/OPAMPs) / 2.4 to 3.6 V (VREFBUF) • V_{DDA} is the external analog power supply for ADCs and DACs, voltage reference buffer, operational amplifiers, and comparators. • The V_{DDA} voltage level is independent from the V_{DD} voltage.	• V_{DDA} = 1.58 V (COMPs) / 1.6 V (DACs, OPAMP) / 1.62 V (ADCs) / 1.8 to 3.6 V (VREFBUF) • V_{DDA} is the external analog power supply for ADCs and DACs, voltage reference buffer, operational amplifiers, and comparators. • The V_{DDA} voltage level is independent from the V_{DD} voltage.
	• V_{DDUSB} = 3.0 to 3.6 V: external independent power supply for USB transceivers. • The V_{DDUSB} voltage level is independent from the V_{DD} voltage.	
	• V_{DDIO2} = 1.08 to 3.6 V: external power supply for 14 I/Os (Port G[15:2]). • V_{DDIO2} voltage level is independent from the V_{DD} voltage (not applicable for STM32L41/42/43/44/45/46xxx).	

Features	STM32L4 and STM32L4+	STM32U3
Power supplies	• VDD12 = 1.05 to 1.32 V: An external SMPS can be connected to the VDD12 pins to supply V_{CORE}.	• V_{DDSMPS} = 1.71 to 3.6 V: External power supply for the SMPS step-down converter. It is provided externally through the VDDSMPS supply pin and must be connected to the same supply as the VDD pin. • V_{LXSMPS} is the SMPS step-down converter output. • An external coil with a typical value of 2.2 µH must be connected from the dedicated VLXSMPS pin to VSSSMPS, with a capacitor of 4.7 µF.
	V_{LCD} = 2.5 to 3.6 V	N/A
	Available only on STM32L4R9/4S9xx devices: • V_{DDDSI} is an independent DSI power supply dedicated to the DSI regulator and the MIPI DPHY. This supply must be connected to the global VDD. • V_{CAPDSI} pin is the output of the DSI regulator (1.2 V) which must be connected externally to $V_{DD12DSI}$. • $V_{DD12DSI}$ pin is used to supply the MIPI D-PHY, and to supply the clock and data lanes pins. An external capacitor of 2.2 uF must be connected to the $V_{DD12DSI}$ pin.	N/A
Battery backup domain	• RTC with tampers. • Backup registers. • LSE. • RCC_BDCR.	• RTC. • TAMP. • Backup registers. • LSE. • RCC_BDCR.
Power supply supervisor	• Integrated POR/PDR circuitry • Programmable voltage detector (PVD)	
	• Brownout reset (BOR) • BOR is always enabled, except in Shutdown mode.	
	Four peripheral voltage monitorings (PVM): • PVM1 for V_{DDUSB} (~1.2 V) (not available for STM32L431/451xx devices). • PVM2 for V_{DDIO2} (~0.9 V) (not available for STM32L41/42/43/44/45/46xxx devices). • PVM3/PVM4 for V_{DDA} (~1.65/ ~2.2 V).	Three peripheral voltage monitorings (PVM): • UVM for V_{DDUSB} (~1.2 V). • IO2VM for VDDIO2 (~0.9 V). • AVM1/AVM2 for V_{DDA} (~1.6/~1.8 V).
Wake-up sources	Stop 0, Stop 1, and Stop 2 modes: • any EXTI line event/interrupt • BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD	Stop 0, Stop 1, and Stop 2 modes: • any EXTI line event/interrupt • any PWR wake-up line • specific peripheral events/interrupts
	Standby mode: • 5 WKUP pins configurable rising or falling edge • RTC event • external reset in NRST pin • IWDG reset	Standby mode: • 24 WKUP pins configurable rising or falling edge • RTC event • external reset in NRST pin • IWDG reset • Tamper detection
System clock after wake-up	Wake-up from Stop: HSI16 (16 MHz) or MSI (all ranges up to 48 MHz) allowing 5 µs wake-up at high speed, without waiting for PLL startup time.	Wake-up from Stop: • HSI16 when STOPWUCK = 1 in RCC_CFGR1 • MSIS with the frequency before entering the Stop mode, limited to 48 MHz, when STOPWUCK = 0
	Wake-up from Standby: MSI (from 1 to 8 MHz)	Wake-up from Standby: MSIS (from 3 to 12 MHz)
	Wake-up from Shutdown: MSI (4 MHz)	Wake-up from Shutdown: MSIS (12 MHz)

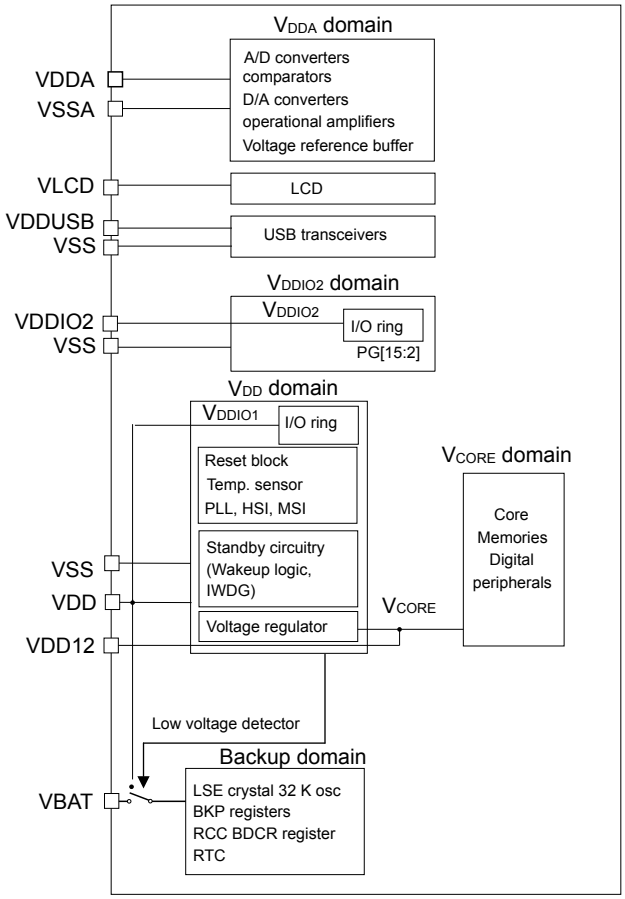
Table 22. Low-power modes of STM32L4, STM32L4+ and STM32U3 MCUs

Mode		STM32L4/STM32L4+	STM32U3
Low-power run	Description	Low-power mode of the internal regulator.	N/A (Range 2 - voltage scaling)
	Wake-up source	-	
	Wake-up system clock	No effect on system clock.	
Sleep	Description	• CPU clock OFF. • All peripherals remain ON, including the Cortex® Core peripherals and peripheral clocks.	• CPU clock OFF. • All peripherals remain ON, including the Cortex® Core peripherals and peripheral clocks.
	Wake-up source	Any interrupt/wake-up event.	Any interrupt/wake-up event.
	Wake-up system clock	Same as before entering.	Same as before entering.
Low-power sleep	Description	Sleep mode, when entered from the Low-power run mode.	N/A (Sleep with range 2 - voltage scaling).
	Wake-up source	Any interrupt/wake-up event.	
	Wake-up system clock	Same as before entering.	
Stop 0	Description	• SRAM content fully retained. • Main regulator ON. • LSI and LSE ON (RTC may be active), other clocks OFF (peripherals can turn HSI16 ON per request).	• Both SRAMs can be fully/partially powered OFF. • Main regulator ON (Range 1/2). • LSI and LSE ON (RTC may be active), other clocks OFF (peripherals can turn them ON per request). • Autonomous peripherals functional.
	Wake-up source	Any EXTI line and specific peripherals events.	Any EXTI line, any PWR wake-up line (WKUP pins and I3C reset pattern), specific peripherals events/interrupts.
	Wake-up system clock	HSI16 or MSI (with the same frequency as before entering).	HSI16 or MSI (with the same frequency as before entering, up to 48 MHz).
Stop 1	Description	• SRAM content fully retained. • Main regulator OFF, low-power regulator ON. • LSI and LSE ON (RTC may be active), other clocks OFF (peripherals can turn HSI16 ON per request).	• Both SRAMs can be fully/partially powered OFF. • Main regulator OFF, low-power regulator ON (SMPS or LDO). • LSI and LSE ON (RTC may be active), other clocks OFF (peripherals can turn them ON per request). • Autonomous peripherals functional.
	Wake-up source	Any EXTI line and specific peripherals events.	Any EXTI line, any PWR wake-up line (WKUP pins and I3C reset pattern), specific peripherals events/interrupts.
	Wake-up system clock	HSI16 or MSI (with the same frequency as before entering).	HSI16 or MSI (with the same frequency as before entering up to 48 MHz).
Stop 2	Description	• SRAM content fully retained (on STM32L4+ devices, SRAM3 might be switched OFF). • Main regulator OFF, low-power regulator ON. • LSI and LSE ON (RTC may be active), other clocks OFF (peripherals can turn HSI16 ON per request). • Most peripherals in V_{CORE} domain in lower leakage mode.	• Both SRAMs can be fully/partially powered OFF. • Main regulator OFF, low-power regulator ON (SMPS or LDO). • LSI and LSE ON (RTC may be active), other clocks OFF (peripherals can turn them ON per request). • Most peripherals in V_{CORE} domain in lower leakage mode, peripherals on APB3 functional.
	Wake-up source	HSI16 or MSI (with the same frequency as before entering).	Any EXTI line, any PWR wake-up line (WKUP pins and I3C reset pattern), specific peripherals events/interrupts.
	Wake-up system clock	HSI16 or MSI (with the same frequency as before entering).	HSI16 or MSI (with the same frequency as before entering up to 48 MHz).

Mode		STM32L4/STM32L4+	STM32U3
Stop 3	Description	N/A	• Both SRAMs can be fully/partially powered OFF; • Main regulator OFF, low-power regulator ON (SMPS or LDO). • LSI and LSE ON (RTC may be active), other clocks OFF (peripherals can turn them ON per request). • Most peripherals in lower leakage mode.
	Wake-up source		WKUP pin edge, RTC/TAMP events/ interrupts, external reset on NRST pin, IWDG events/interrupts or reset, I3C reset pattern.
	Wake-up system clock		HSI16 or MSI (with the same frequency as before entering up to 48 MHz).
Standby	Description	• SRAMs powered OFF (optional full/ partial retention of SRAM2). • V_{CORE} domain powered OFF. • Main regulator OFF, low-power regulator ON only in case of SRAM2 retention. • LSI and LSE ON (RTC may be active), other clocks OFF. • Optional I/O pull-up or pull-down configuration.	• SRAM1 powered OFF, full/partial retention of SRAM2. • V_{CORE} domain powered OFF. • Main regulator OFF, low-power regulator ON (SMPS or LDO) for SRAM2 full/partial retention. • LSI and LSE ON (RTC may be active), other clocks OFF. • Power supply monitoring might be switched to ultra-low-power mode. • Optional I/O pull-up or pull-down configuration.
	Wake-up source	WKUP pin edge, RTC event, external reset on NRST pin, IWDG reset.	WKUP pin edge, RTC/TAMP events/ interrupts, external reset on NRST pin, IWDG events/interrupts or reset, I3C reset pattern.
	Wake-up system clock	MSI from 1 MHz up to 8 MHz.	MSIS from 3 MHz up to 12 MHz.
Shutdown	Description	• SRAMs powered OFF. • V_{CORE} domain powered off. • LSE ON (RTC may be active), other clocks OFF. • Power supply monitoring and IWDG OFF.	• SRAMs powered OFF. • V_{CORE} domain powered off. • LSE ON (RTC may be active), other clocks OFF. • Power supply monitoring and IWDG OFF.
	Wake-up source	WKUP pin edge, RTC event, external reset on NRST pin.	WKUP pin edge, RTC/TAMP events/ interrupts, external reset on NRST pin, I3C reset pattern.
	Wake-up system clock	MSI 4 MHz.	MSIS 12 MHz.

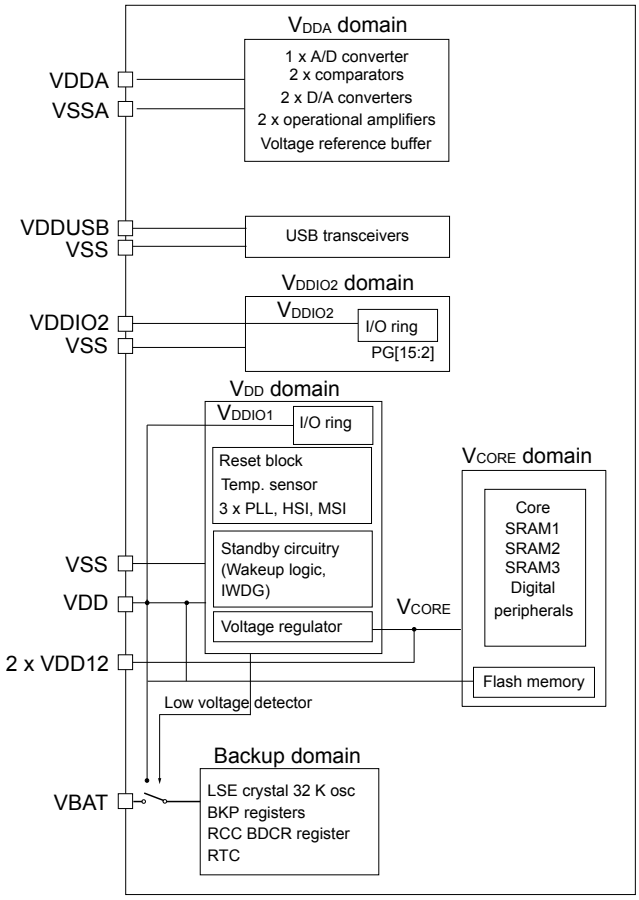
The following figures present the power supply for STM32L4, STM32L4+ and STM32U3 MCUs.

Figure 4. STM32L4 power supply overview



DT19671V6

Figure 5. STM32L4P5/4Q5/4S5/4R5/4S7/4R7xx power supply overview



DT43404V3

Figure 6. STM32L4R9/4S9xx power supply overview

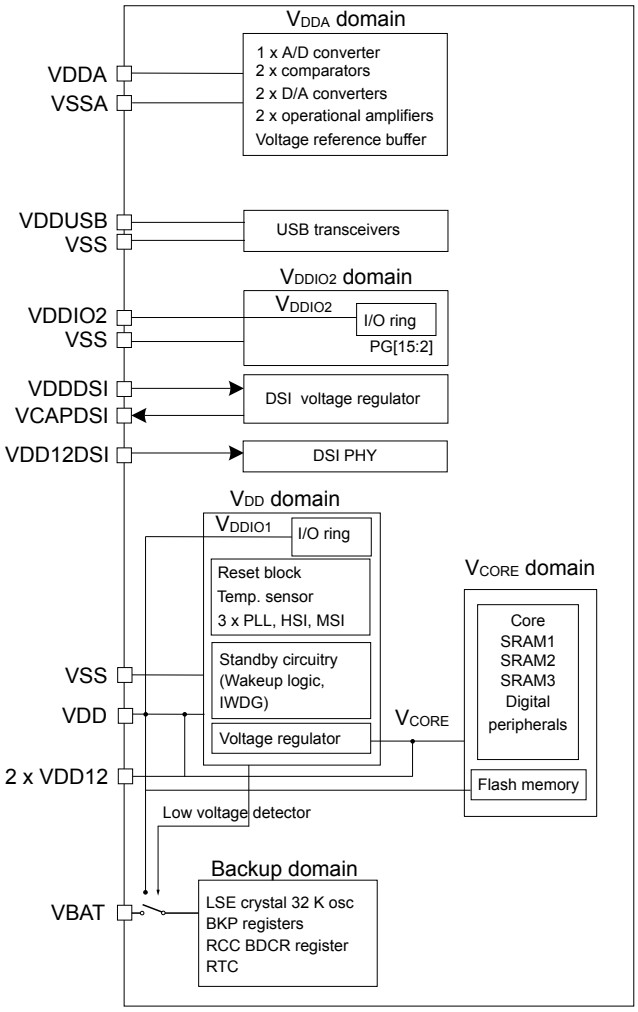


Figure 7. STM32U375xx/385xx power supply overview (without SMPS)

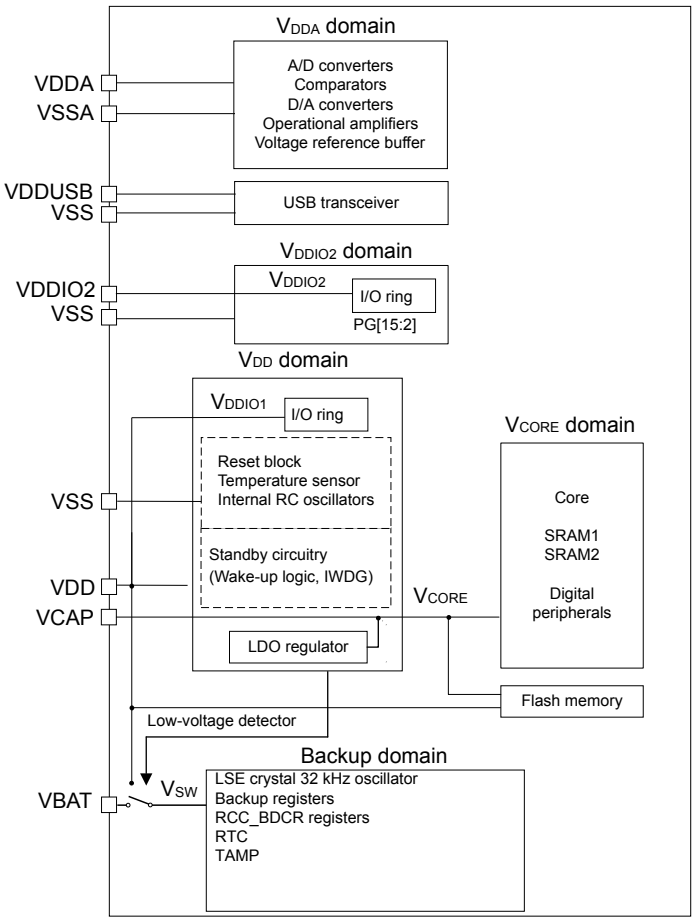
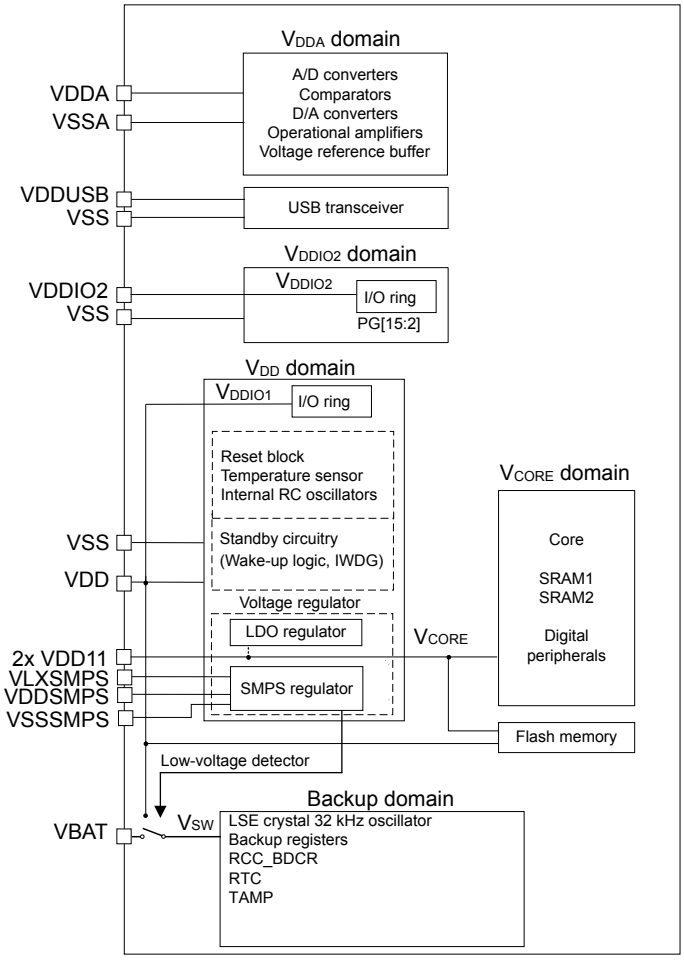


Figure 8. **STM32U375xxQ/385xxQ power supply overview (with SMPS)**



6.8 General-purpose I/Os (GPIO)

The STM32U3 devices implement the same GPIO features as STM32L4 and STM32L4+, but with additional TrustZone® security support.

For STM32U3 devices, each GPIO port has four 32-bit configuration registers (GPIOx_MODER, GPIOx_OTYPER, GPIOx_OSPEEDR, and GPIOx_PUPDR), two 32-bit data registers (GPIOx_IDR and GPIOx_ODR) and a 32-bit set/reset register (GPIOx_BSRR).

In addition, all GPIOs in the STM32U3 series have a 32-bit locking register (GPIOx_LCKR) and two 32-bit alternate function selection registers (GPIOx_AFRH and GPIOx_AFRL), a secure configuration register (GPIOx_SECCFGR), and a high-speed low-voltage register (GPIOx_HSLVR).

Each general-purpose I/O pin of a GPIO port in the STM32U3 series can be individually configured as secure or nonsecure in the GPIOx_SECCFGR register. After reset, all general-purpose I/O of GPIO ports are secure.

All GPIO registers can be read and written by privileged and unprivileged accesses, whatever the security state secure or non-secure.

For more information about TrustZone® security and GPIO programming and usage for STM32U3 devices, refer to the “General-purpose I/Os (GPIO)” section of the reference manual and to the product datasheet for detailed description of the pinout and alternate function mapping.

6.9 Extended interrupt and event controller (EXTI)

STM32U3 MCUs offer less EXTI lines (for example, no direct lines) with a slightly different assignment to event sources than STM32L4 and STM32L4+ MCUs. However, STM32U3 MCUs feature TrustZone® security support and privilege protection.

Table 23. EXTI features of STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
Number of event/interrupt lines	Up to 41 lines: • 13 direct, 26 configurable on STM32L4P/4Q/4R/4Sxxx. • 15 direct, 26 configurable on STM32L49/4Axxx. • 14 direct, 26 configurable on STM32L47/48xxx. • 12 direct, 25 configurable on STM32L41/42/43/44/45/46xxx.	23 lines: all lines are configurable.

The STM32U3 EXTI is able to protect event register bits from being modified by nonsecure and unprivileged access. The protection is activated individually per input event via register bits. At EXTI level, the protection consists in preventing the following unauthorized write access:

- Changing the settings of the secure and/or privileged configurable events.
- Changing the masking of the secure and/or privileged input events.
- Clearing the pending status of the secure and/or privileged input events.

The table below presents the EXTI line differences between the STM32L4, STM32L4+ and STM32U3 series.

Table 24. EXTI lines of STM32L4, STM32L4+ and STM32U3 MCUs

EXTI line	STM32L4/STM32L4+	STM32U3
0-15	GPIO	GPIO
16	PVD	PVD
17	USB (OTG) FS wake-up	COMP1
18	RTC alarms or SSRU(1)	COMP2
19	RTC tamper or timestamp or CSS_LSE	V_{DDUSB} voltage monitor
20	RTC wake-up timer	V_{DDIO2} voltage monitor
21	COMP1 output	V_{DDA} voltage monitor 1
22	COMP2 output	V_{DDA} voltage monitor 2
23	I2C1 wake-up	N/A
24	I2C2 wake-up	N/A
25	I2C3 wake-up	N/A
26	USART1 wake-up	N/A
27	USART2 wake-up	N/A
28	USART3 wake-up	N/A
29	UART4 wake-up	N/A
30	UART5 wake-up(2)	N/A
31	LPUART1 wake-up	N/A
32	LPTIM1	N/A
33	LPTIM2	N/A
34	SWPMI1 wake-up(3)	N/A
35	PVM1 wake-up	N/A

EXTI line	STM32L4/STM32L4+	STM32U3
36	PVM2 wake-up(2)	N/A
37	PVM3 wake-up	N/A
38	PVM4 wake-up	N/A
39	LCD wake-up(4)	N/A
40	I2C4 wake-up(5)	N/A

1. *SSRU available only on STM32L4P/4Qxxx devices.*
2. *Not available on STM32L41/42/43/44/45/46xxx devices.*
3. *Not available on STM32L4+ and STM32L41/42/45/46xxx devices.*
4. *Available only on STM32L433/443/476/486/496/4A6xx devices.*
5. *Available only on STM32L4+ and STM32L45/46/49/4Axxx devices.*

6.10 Cyclic redundancy check calculation unit (CRC)

The CRC architecture is the same in the STM32U3, STM32L4, and STM32L4+ series, supporting the same features, with a minor difference in CRC_IDR, which is extended from an 8-bit register in the STM32L4 and STM32L4+ series to a 32-bit register in the STM32U3 series.

7 Migration of security peripherals

7.1 Tamper and backup registers (TAMP)

The TAMP peripheral offers more functions on STM32U3 MCUs (such as internal events to protect against transient or environmental perturbation attacks) than on STM32L4 and STM32L4+ MCUs. The anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 backup registers, each of 32-bit size, are retained in all low-power modes and also in V_{BAT} mode.

The table below compares the tamper pins and internal events and lists the main differences between STM32U3, STM32L4, and STM32L4+ MCUs.

Table 25. Tamper pins and events of STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
Tamper pins	3 tamper pins: • PC13(RTC_TAMP1) • PA0(RTC_TAMP2) • PE6(RTC_TAMP3)	5 TAMP pins for 5 external tamper detection events: • PC13 (TAMP_IN1) • PA0 (TAMP_IN2) • PE6 (TAMP_IN3) • PC5 (TAMP_IN4) • PA1 (TAMP_IN5)
TAMP internal events	N/A	9 internal tamper events: • tamp_itamp3: LSE monitoring • tamp_itamp5: RTC calendar overflow • tamp_itamp6: JTAG/SWD access when RDP > 0 • tamp_itamp7: voltage monitoring through ADC analog watchdog 1 • tamp_itamp8: monotonic counter overflow • tamp_itamp9: cryptographic peripheral fault (SAES, AES, PKA, or RNG) • tamp_itamp11: IDWG reset when tamper flag is set • tamp_itamp12: voltage monitoring through ADC analog watchdog 2 • tamp_itamp13: voltage monitoring through ADC analog watchdog 3
TAMP functionality over V_{DD} mode	No effect on all features in all low-power modes when the external V_{DD} power supply is present.	
TAMP functionality over V_{BAT} mode	All tampers are functional in V_{BAT} mode.	
Potential tamper detection mode	N/A	X
Boot hardware key		• Stored in the first backup registers. • Written to secure AES during boot.
Tamper protected assets	Backup registers	• Backup registers • SRAM2 • ICACHE content • SAES, AES, CCB, and HASH peripherals • PKA SRAM • RHUK in system flash memory

7.2 Hash processor (HASH)

The STM32U3, STM32L4+, and STM32L49/4Axxx devices embed a HASH hardware accelerator, although the STM32U3 HASH accelerator offers more possibilities, such as suport of SHA2-384/512.

Both hash processors provide an interface to connect to the DMA controller. The STM32U3 HASH peripheral supports both single- and fixed-DMA burst transfers of four words. However, the HASH peripheral inSTM32L4+ and STM32L49/4Axxx devices only supports single-DMA transfers.

HASH registers are compatible, except for a minor difference in the ALGO bits in HASH_CR.

7.3 True random number generator (RNG)

The STM32U3, STM32L4, and STM32L4R/4Sxxx devices embed an RNG that delivers 32-bit random numbers generated by an integrated analog circuit, with the same features, except the minor differences detailed in the table below.

Table 26. RNG features of STM32L4, STM32L4+, and STM32U3 MCUs

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Feature	STM32L4 and STM32L4R/4Sxxx	STM32L4P/4Qxxx	STM32U3
Complexity/entropy	Entropy source for NIST-compliant DRBG(1)	Entropy source for NIST-compliant NRBG(1)	Entropy source for NIST-compliant NRBG (+ entropy enhancements)
Tested using German BSI statistical tests of AIS-31 (T0 to T8)	N/A	X	X
Can be disabled to reduce power consumption	X	X	X
Can be enabled with an automatic low-power mode	N/A	X	X
RNG internal tamper event signal to TAMP	N/A	N/A	X
Signals to provide random seeds to SCA/DPA-resistant IPs (AES, SAES, PKA)	N/A	N/A	X

1. *Deterministic random bit generator*

In STM32U3 MCUs, the RNG can be chained through CCB with SAES and PKA for SCA resistance. MOreover, when an unexpected error is found by the RNG, an internal tamper event is triggered in the TAMP peripheral, and the RNG stops delivering random data.

When this event occurs, a secure application needs to reset the RNG, either using central reset management, or the global SoC reset. Then a proper initialization of the RNG is required, again.

7.4 Public key accelerator (PKA)

The STM32U3 and STM32L4Q5xx devices embed one PKA peripheral intended for the computation of cryptographic public key primitives in the Montgomery domain. All necessary computations are performed within the accelerator, so no further hardware or software elaboration is needed to process the inputs or the outputs.

The STM32U3 and STM32L4Q5xx devices share almost the same PKA features. The STM32U3 devices embed two new features and three new computation operators. Registers are compatible, except for some new bits added in STM32U3 to map the new features.

The STM32L4 devices do not support a PKA peripheral.

Table 27. PKA features of STM32L4+ and STM32U3 MCUs

Feature	STM32L4Q5xx (in the STM32L4+ series)	STM32U3
RSA modular exponentiation, RSA Chinese remainder theorem (CRT) exponentiation	X	X
ECC scalar multiplication, point on curve check	X	X

Feature	STM32L4Q5xx (in the STM32L4+ series)	STM32U3
ECC complete addition, double-base ladder, projective to affine	N/A	X
ECDSA signature generation and verification	X	
Size of RSA/DH operands (in bits)	3136	4160
Size of ECC operands (in bits)	640	
Arithmetic and modular operations (such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication)	X	X
Built-in Montgomery domain inward and outward transformations	X	X
Protection against differential power analysis (DPA) and related side-channel attacks (SCA)	N/A	X

7.5 AES and SAES hardware accelerators

STM32U3 devices embed two AES accelerators: one secure AES (SAES) and a faster AES, while the STM32L4 and STM32L4 crypto devices embed only the faster one. The set of features of this AES is almost the same.

In the STM32U3 series, the SAES with hardware unique key embeds protection against differential power analysis (DPA) and related side channel attacks (SCA). It is certified SESIP and PSA security assurance level 3. When an unexpected hardware fault occurs, an output tamper event is triggered, and the AES automatically clears key registers. A reset is required for the AES to be usable again.

The AES can use the SAES as security coprocessor. In this case, the secure application prepares the key in robust SAES then, when ready, the AES can load this key through a dedicated hardware key bus. Recommended sequences are described in the sections "AES shared key usage" and "SAES operations with shared keys" of the product reference manual.

Refer to the table below for a comparison of AES and SAES features.

Table 28. AES/SAES features on STM32U3 MCUs

AES/SAES modes/features	AES(1)	SAES(1)
ECB, CBC chaining	X	X
CTR, CCM, GCM chaining	X	X
AES 128-bit ECB encryption in cycles(2)	51	528
DHUK and BHK key selection	-	X
Side-channel attacks resistance	-	X
Shared key between SAES and AES	X	

1. *X = supported.*
2. *With 128-bit cryptographic key*

7.6 Coupling and chaining bridge (CCB)

The coupling and chaining bridge (CCB) can be programmed to implement special coupling and chaining operations, which are required to protect private keys used in PKA-protected operations.

These coupling and chaining operations involve the PKA, SAES, and sometimes the RNG peripherals.

The CCB is a new peripheral, introduced on STM32U3 MCUs and it is therefore not present on STM32L4 or STM32L4+ devices. For more information, refer to the product reference manual.

7.7 Global TrustZone® controller (GTZC)

The security architecture of STM32U3 MCUs is based on Arm® TrustZone® with the Armv8-M mainline extension. Each GPIO or peripheral, DMA channel, clock configuration register, ICACHE, or small part of flash memory or SRAM can be configured as trusted or untrusted.

The GTZC embedded in STM32U3 devices is used to configure secure TrustZone® and privileged attributes within the full system. All details about GTZC are described in the product reference manual.

This controller is a new feature of the STM32U3 MCUs and is not present on STM32L4 or STM32L4+ MCUs.

8 Migration of timer peripherals

The STM32U3, STM32L4+, and STM32L4 devices include up to two advanced-control timers, up to seven general-purpose timers, up to two basic timers, up to four low-power timers (two for STM32L4 and STM32L4+ devices), two watchdog timers, and two SysTick timers (one for STM32L4 and STM32L4+ devices).

This section compares the features of the above-listed timers and RTC in STM32L4, STM32L4+, and STM32U375/385 devices.

8.1 Advanced-control timers (TIM1/8)

The STM32L47/48/49/4Axxx and STM32L4+ devices embed two advanced control timers (TIM1/8), while STM32L41/42/43/44/45/46xxx and STM32U3 devices contain one advanced control timer (TIM1). These have an identical set of features, which are detailed in the table below.

Table 29. Advanced-control timer (TIM1/8) features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
16-bit resolution	• For STM32L41/42/43/44/45/46xxx devices: – TIM1 • ForSTM32L47/48/49/4Axxx and STM32L4+ devices: – TIM1/TIM8	TIM1
Counter resolution and type	16-bit up, down, up/down auto-reload counter.	
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536.	
Channels	Up to six independent channels for: • Input capture (but channels 5 and 6). • Output compare. • PWM generation (edge and center-aligned mode). • One-pulse mode output.	
Complementary outputs	Complementary outputs with programmable dead-time.	
Synchronization with external signals and general-purpose timers	Synchronization circuit to control the timer with external signals and to interconnect several timers together. The advanced-control (TIM1/TIM8) and general-purpose (TIMx) timers are completely independent, and do not share any resources.	
Repetition counter	Repetition counter to update the timer registers only after a given number of counter cycles.	
Break inputs	Two break inputs to put the timer output signals in a safe user selectable configuration.	
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/ external trigger). • Trigger event (counter start, stop, initialization or count by internal/external trigger). • Input capture. • Output compare.	
Encoders and sensors	Support incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes.	
Trigger input	Trigger input for external clock or cycle-by-cycle current management.	
Application examples	• Measuring the pulse lengths of input signals (input capture). • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).	

8.2 GP timers with up, down, up-down auto-reload counter (TIM2/3/4/5)

The GP (general-purpose) timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler. The STM32U3, STM32L4+, and STM32L4 devices include GP timers with up, down or up-down auto-reload counter (TIM2, TIM3, TIM4, and TIM5), with identical features (TIM4/5 only available on STM32L4x1/47x/48x/49x/4Axxx, TIM3 only available on STM32L4x1/451/452/462/47x/48x/49x/4Axxx).

Table 30. GP timer (TIM2/3/4/5) features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
32-bit resolution	• For STM32L41/42/43/44/45/46xxx devices: – TIM2 • For STM32L47/48/49/4Axxx and STM32L4+ devices: – TIM2/TIM5	TIM2/TIM3/TIM4
16-bit resolution	• For STM32L41/42/43/44xxx devices: – NA • For STM32L45/46xxx devices: – TIM3 • For STM32L47/48/49/4Axxx and STM32L4+ devices: – TIM3/TIM4	-
Counter resolution and type	16- or 32-bit up, down, up/down auto-reload counter.	
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536.	
Channels	Up to four independent channels for: • Input capture. • Output compare. • PWM generation (edge and center-aligned mode). • One-pulse mode output.	
Synchronization with external circuits and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers.	
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger). • Trigger event (counter start, stop, initialization or count by internal/external trigger). • Input capture. • Output compare.	
Encoders and sensors	Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes.	
Trigger input	Trigger input for external clock or cycle-by-cycle current management.	
Application examples	• Measuring the pulse lengths of input signals (input capture). • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).	

8.3 GP timers with auto-reload up-counter (TIM15/16/17)

STM32U3, STM32L4+, and STM32L4 MCUs include up to three 16-bit resolution GP timers with a 16-bit auto-reload up-counter (TIM15, TIM16, and TIM17) with identical features.

Table 31. GP timer (TIM15/16/17) features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
16-bit resolution	• For STM32L41/42/43/44/45/46xxx devices: – TIM15/TIM16 • For STM32L47/48/49/4Axxx and STM32L4+ devices: – TIM15/TIM16/TIM17	TIM15/TIM16/TIM17
Counter resolution and type	16-bit auto-reload up-counter.	
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536.	
Channels	Up to two independent channels for: • Input capture. • Output compare. • PWM generation (edge mode). • One-pulse mode output.	
Complementary outputs	Complementary outputs with programmable dead-time (for channel 1 only).	
Synchronization with external circuits and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers.	
Repetition counter	Repetition counter to update the timer registers only after a given number of counter cycles.	
Break inputs	One break input to put the timer output signals in the reset state or a known state.	
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger). • Trigger event (counter start, stop, initialization, or count by internal/external trigger). • Input capture. • Output compare. • Break input (interrupt request).	
Application examples	• Measuring the pulse lengths of input signals (input capture). • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion).	

8.4 Basic timers (TIM6/7)

The basic timers TIM6 and TIM7 consist OF a 16-bit auto-reload counter driven by a programmable prescaler. These timers are completely independent and do not share any resources.

The STM32U3, STM32L4, and STM32L4+ devices contain one to two basic timers, which have the same basic timer features.

Table 32. Basic timer (TIM6/7) features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
16-bit resolution	• For STM32L412/422xx and STM32L45/46xxx devices: – TIM16 • For other STM32L4 and STM32L4+ devices: – TIM6/TIM7	TIM6/TIM7
Counter resolution and type	16-bit auto-reload up-counter.	

Feature	STM32L4/STM32L4+	STM32U3
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536.	
Synchronization signals	Synchronization circuit to trigger the DAC.	
Interrupt/DMA generation	Interrupt/DMA generation on the update event, counter overflow.	
Application examples	• Time-base generation. • Driving the DAC.	

8.5 Low-power timers (LPTIM1/2/3/4)

The LPTIMx is a 16-bit timer that benefits from the ultimate developments in power-consumption reduction. STM32U3 devices include four LPTIMs, whereas STM32L4 and STM32L4+ devices contain two. The LPTIMs share the same features in these series, but new features are added to the STM32U3 series, such as:

- Up to two independent channels per LPTIM.
- Input capture channels.
- DMA requests.
- Autonomous function in Stop modes.

Table 33. LP timer (LPTIMx) features of STM32L4, STM32L4+, and STM32U3 series

Feature	STM32L4 series	STM32L4+ series	STM32U3 series
LPTIMx	LPTIM1 and LPTIM2		LPTIM1, LPTIM2, LPTIM3, and LPTIM4
Counter resolution and type	16-bit up-counter.		
Prescaler factor	3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64, or 128).		
Selectable clock	• Internal clock sources: LSE, LSI, HSI or APB clock. • External clock source over LPTIMx input (working with no low-power oscillator running, used by pulse counter application).		
Auto-reload	16-bit ARR auto-reload register.		
Capture/compare	16 bit compare register.		16-bit capture/compare register.
Continuous mode	Continuous/one-shot mode.		
Trigger mode	Selectable software/hardware input trigger.		
Glitch filter	Programmable digital glitch filter.		
Configurable output	Configurable output: pulse, PWM.		
Polarity	Configurable I/O polarity.		
Encoder mode	X		
Repetition counter	X(1)	X(2)	X
Input capture, PWM, and one-pulse channels	One channel for: • PWM generation (edge aligned mode). • One-pulse mode output.		Up to two independent channels for: • Input capture. • PWM generation (edge aligned mode). • One-pulse mode output.
DMA requests	N/A		DMA request generation on the following events: • Update event. • Input capture.

1. *Only available on STM32L41/42xxx devices.*
2. *Only available on STM32L4P5/4Q5xx devices.*

Some of the above features are not similarly implemented on LPTIMx instances, as described in the table below.

Table 34. Implementation of LPTIMx features on various instances

Feature	STM32L4/STM32L4+ series		STM32U3 series			
	LPTIM1	LPTIM2	LPTIM1	LPTIM2	LPTIM3	LPTIM4
Encoder mode	X	N/A	X	X	N/A	N/A
PWM generation and one-pulse output mode	X	X	X	X	X	X
Input capture	N/A	N/A	X	X	X	N/A
Number of channels	1	1	2	2	2	1
Number of DMA requests	N/A	N/A	3	3	3	N/A
Autonomous mode	N/A	N/A	X	X	X	N/A

The STM32U3 LPTIM instances support the autonomous mode and can therefore be functional in Stop modes and perform DMA transfers. For all instances where this is valid for Stop 0 and Stop 1 modes, LPTIM3 might be functional in Stop 2 mode as well.

8.6 Watchdogs (WWDG/IWDG)

STM32L4, STM32L4+, and STM32U3 MCUs embed two watchdogs:

- A system window watchdog (WWDG) with the same features (only the position of the WDGTB bits in the WWDG registers has changed).
- An independent watchdog (IWDG) with the same features, except the STM32U3 IWDG , which has the capability to generate an early wake-up interrupt

Table 35. IDWG features of STM32L4, STM32L4+, and STM32U3 series

Feature	STM32L4/STM32L4+	STM32U3
LSI used as IWDG kernel clock	X	X
Window function	X	X
Early wake-up interrupt generation	N/A	X
Reset generation	X	X
Capability to work in system Stop	X	X
Capability to work in system Standby	N/A	X
Capability to generate an interrupt in system Stop		

8.7 Real-time clock (RTC)

STM32U3 MCUs implement similar RTC features to STM32L4 and STM32L4+ MCUs, adding some specification updates and enhancements. The main differences are listed in the table below.

Table 36. RTC features of STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L41/42xxx and STM32L4P/4Qxxx devices	STM32L43/44/45/46/47/48/49/4Axxx and STM32L4R/4Sxxx devices	STM32U3
Calendar with subsecond, seconds, minutes, hours (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format	X	X	X
Binary mode with 32-bit free-running counter	N/A	X	X
Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.	X	X	X
Programmable alarms	2	2	2
On-the-fly correction from 1 to 32767 RTC clock pulses	N/A	X	X
Reference clock detection	X	X	X
Digital calibration circuit with 0.95 ppm resolution	X	X	X
Time-stamp function for event saving	X	X	X
17-bit auto-reload wake-up timer (WUT)	X	X	X
TrustZone support - RTC fully securable, Alarm A, alarm B, wake-up Timer and timestamp individual secure or nonsecure configuration	N/A	N/A	X
Individual privilege protection	N/A	N/A	X

8.8 SysTick timer

The SysTick timer is dedicated to real-time operating systems, but can also be used as a standard down-counter.

The STM32U3 Cortex®-M33 device with TrustZone® embeds two SysTick timer instances, one secure and one nonsecure. Only the nonsecure SysTick is available when TrustZone® is disabled.

STM32L4 and STM32L4+ devices embed a Cortex®-M4 core with just one SysTick timer.

9 Migration of communication peripherals

9.1 Serial peripheral interface (SPI)

STM32U3 devices embed an enhanced version of the SPI peripheral, compared to STM32L4 and STM32L4+ devices. Refer to the table below for a comparison of the different features.

Note: The SPI peripheral registers of STM32U3 are entirely incompatible with the STM32L4/STM32L4+ SPI registers.

Table 37. SPI features on STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
Instances	SPI1, SPI2, and SPI3 (same features in the three instances)(1)	• SPI1, SPI2 (full feature set instances). • SPI3 (limited feature set instance).
Full-duplex synchronous transfer on three lines	X	X
Half-duplex synchronous transfer on two lines (with bidirectional data line)	X	X
Simplex synchronous transfer on two lines (with unidirectional data line)	X	X
Data size	• 4- to 16-bit data size selection.	• 4- to 32-bit data size selection on SPI1 and SPI2. • Fixed to 8- and 16-bit only on SPI3.
Multimaster or multislave mode capability	X	X
Clock inputs	One input: PCLK is the unique SPI clock source.	Two independent clock inputs: peripheral kernel clock (spi_ker_ck) is independent of PCLK.
Baudrate prescalers	Master/slave mode baudrate prescalers up to f_{PCLK} / 2.	Baudrate prescaler up to kernel frequency / 2.
	N/A	spi_ker_ck prescaler can be bypassed from RCC in master mode.
Protection of configuration and settings	N/A	X
Slave select (SS) management	NSS management by hardware or software for both master and slave: dynamic change of master/slave operations.	Hardware or software management of SS for both master and slave.
Adjustable minimum delays between data and between SS and data flow	N/A (fixed)	X
Configurable SS signal polarity and timing	N/A	Configurable SS signal polarity and timing, MISO x MOSI swap capability.
Programmable clock polarity and phase	X	X
Programmable data order with MSB-first or LSB-first shifting	X	X
Dedicated transmission and reception flags with interrupt capability	X	X
SPI Motorola and Texas Instrument formats support	X	X
Hardware CRC feature can secure communication at the end of transaction by: • adding CRC value in Tx mode • automatic CRC error checking for Rx mode	CRC fixed to 8- or 16-bit for all SPIs.	• CRC polynomial length configurable from 5 to 33 bits for SPI1 and SPI2. • CRC polynomial length 9 or 17 bits for SPI3.

Feature	STM32L4/STM32L4+	STM32U3
Interrupt events and error detection with interrupt capability	Interrupts: • Transmit TXFIFO ready to be loaded. • Data received in receive RXFIFO. • Master mode fault. • Overrun error. • TI frame format error. • CRC protocol error.	Interrupts: • TxFIFO ready to be loaded. • Data received in RxFIFO. • Both TXP and RXP active. • Transmission Transfer Filled. • Overrun error. • Underrun error. • TI frame format Error. • CRC error. • Mode fault. • End of transfer. • Master mode suspended. • TxFIFO transmission complete.
	N/A	All the interrupt events can wake up the system from Sleep mode at each instance, and some from Stop modes as well.
FIFO size	Two 32-bit embedded Rx and Tx FIFOs with DMA capability.	• Two 16x 8-bit embedded Rx and Tx FIFOs with DMA capability for SPI1 and SPI2. • Two 8x 8-bit embedded Rx and Tx FIFOs with DMA capability for SPI3.
Number of transferred data	Number defined by the counter for the SPI transmission DMA channel.	Programmable number of data in transaction: • Up to 65536 for SPI1 and SPI2. • Up to 1024 (no data counter) for SPI3.
FIFO thresholds	Fixed threshold to 1/2 FIFO or 1/4 FIFO level.	Configurable FIFO thresholds (data packing).
Configurable behavior at slave underrun condition	N/A	X (support of cascaded circular buffers.)
Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wake-up from Stop capability	N/A	Stop 0 and Stop 1 modes with wake-up capability.
RDY status pin	N/A	Optional status pin RDY signalizing the slave device ready to handle the data flow

1. *Only SPI1 and SPI2 available for STM32L41/42xxx devices.*

The three SPI peripherals in the STM32U3 series support autonomous operation in Stop 0 and Stop 1 modes, with the following main feature:

SPI can handle and initialize transactions autonomously, requiring no specific system execution interaction until the ongoing transaction ends.

9.2 Inter-integrated circuit (I2C)

The I2C peripherals share the same features in the STM32U3, STM32L4, and STM32L4+ MCUs. The differences are shown in the table below.

In addition, the STM32U3 MCUs embed the autonomous mode of I2C peripherals, allowing the I2C to be functional in Stop mode. The autonomous mode can also be used in Run, Sleep, or Stop mode.

Table 38. I2C features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4/STM32L4+	STM32U3
Instances	• For STM32L41/42/43/44/47/48xxx devices: – I2C1, I2C2, I2C3. • For STM32L49/4A/4R/4S/4P/4Qxxx devices: – I2C1, I2C2, I2C3, I2C4.	I2C1, I2C2, I2C3
7- and 10-bit addressing mode	X	X
Standard-mode (up to 100 Kbit/s)	X	X
Fast-mode (up to 400 Kbit/s)	X	X
Fast-mode Plus with 20 mA output drive	X	X
I/Os (up to 1 Mbit/s)	X	X
Independent clock	X	X
SMBus/PMBus	X	X
Wake-up from Stop 0 and Stop 1 modes	X	X
Wake-up from Stop 2 modes	I2C3 only	I2C3 only
Autonomous mode in Stop 0 and Stop 1 modes	N/A	X
Autonomous mode in Stop 2 mode	N/A	I2C3 only

9.3 Improved inter-integrated circuit (I3C)

The STM32U3 devices offer a new I3C peripheral, with two instances: I3C1 and I3C2. The I3C bus is a two-wire, serial single-ended, multidrop bus, intended to improve the legacy I²C bus.

The I3C SDR-only peripheral implements all the features required by the MIPI® I3C specification v1.1. It can control I3C bus-specific sequencing, protocol, arbitration, and timing, and can act as a controller (formerly known as master), or as a target (formerly known as slave).

When acting as a controller, the I3C peripheral improves the features of the I^2C interface while preserving some backward compatibility: it allows an I2C target to operate on an I3C bus in legacy I^2C fast-mode (Fm) or legacy I^2C fast-mode plus (Fm+), provided that the latter does not perform clock stretching.

The I3C peripheral can be used with DMA to off-load the CPU. It also offers an autonomous mode in Stop 0 and Stop 1 modes and can wake-up the device from all Stop modes, and even from Standby mode and Shutdown mode (through the I3C reset pattern).

Refer to the referenced document Introduction for more information.

9.4 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32U3 MCUs implement the same U(S)ART features as the STM32L4 and STM32L4+ MCUs, with some specification updates and enhancements. The main differences are stated in the table below.

Table 39. U(S)ART features of STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4 and STM32L4+	STM32U3
Instances	• For STM32L41/42xxx devices: – 3 USARTs – 1 LPUART	• 2 USARTs • 2 UARTs • 1 LPUART

Feature	STM32L4 and STM32L4+	STM32U3
	• For STM32L43/44/45/46xxx devices: – 3 USARTs – 1 UART – 1 LPUART • For STM32L47/48/49/4A/4P/4Q/4R/4Sxxx devices: – 3 USARTs – 2 UARTs – 1 LPUART	
Baud rate	Depends on the frequency (oversampling by 16 or 8).(1)	Depends on the frequency (oversampling by 16 or 8).(1)
Clock	Dual-clock domain allowing: • UART reception and wake-up from Stop mode (Stop 0/1 for U(S)ARTs, Stop 0/1/2 for LPUART). • Convenient baud rate programming independent from the PCLK reprogramming.	Dual-clock domain allowing: • UART autonomous mode and wake-up from Stop mode (Stop 0/1 for U(S)ARTs, Stop 0/1/2 for LPUART). • Convenient baud rate programming independent from the PCLK reprogramming.
Data	• Word length: programmable (7, 8, or 9 bits). • Programmable data order with MSB-first or LSB-first shifting.	• Word length: programmable (7, 8, or 9 bits). • Programmable data order with MSB-first or LSB-first shifting.
Interrupt	• 14 interrupt sources with flags for STM32L4. • 23 interrupt sources with flags for STM32L4+.	23 interrupt sources with flags
Autonomous mode	N/A	Autonomous functionality in Stop mode with wake-up from Stop capability (Stop 0/1 for U(S)ARTs, Stop 0/1/2 for LPUART1).
Other features	• Hardware flow control for modem and RS-485 transceiver. • Continuous communication using DMA. • Multiprocessor communication. • Single-wire half-duplex communication. • IrDA SIR ENDEC block. • LIN mode. • SPI master. • SPI slave (for STM32L4+ devices only).	• Hardware flow control for modem and RS-485 transceiver. • Continuous communication using DMA. • Multiprocessor communication. • Single-wire half-duplex communication. • IrDA SIR ENDEC block. • LIN mode. • SPI master/slave.
	• Wake-up from Stop mode (start bit, received byte, address match). • Support for ModBus communication: timeout feature, CR/LF character recognition. • Two internal FIFOs to transmit and receive data (for STM32L4+). • Receiver timeout interrupt. • Auto baud rate detection. • Driver enable. • Swappable TX/RX pin configuration. • Number of stop bits: 0.5, 1, 1.5, or 2. *Note: LPUART does not support Synchronous mode (SPI master), Smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt and auto baud rate detection.*	• Wake-up from Stop mode (start bit, received byte, address match). • Support for ModBus communication: timeout feature, CR/LF character recognition. • Two internal FIFOs to transmit and receive data. • Receiver timeout interrupt. • Auto baud rate detection. • Driver enable. • Swappable TX/RX pin configuration. • Number of stop bits: 0.5, 1, 1.5, or 2. *Note: LPUART does not support Synchronous mode (SPI master), Smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt and auto baud rate detection.*
	• Smartcard mode support, with both character and block mode (T = 0, T = 1). • Features are added to support T = 1 (such as receiver timeout, block length, end of block detection and binary data inversion).	• Smartcard mode support, with both character and block mode (T = 0, T = 1). • Features are added to support T = 1 (such as receiver timeout, block length, end of block detection and binary data inversion).

1. *Refer to the USART section in the reference manual.*

9.5 Serial audio interface (SAI)

STM32L4, STM32L4+, and STM32U3 devices offer up to two instances of SAI with the same features, as detailed in the table below. The SAI offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted (such as I2S standards, LSB- or MSB-justified, PCM/DSP, TDM, and AC'97 protocols). The SPDIF output is offered when the audio block is configured as a transmitter.

Table 40. SAI features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4	STM32L4+	STM32U3
Instances	• For STM32L41/42xxx devices: – N/A • For STM32L43/44/45/46xxx devices: – SAI1 • For STM32L47/48/49/4Axxx devices: – SAI1, SAI2	SA1, SAI2	SAI1
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X	X	X
Mute mode	X	X	X
Stereo/Mono audio frame capability	X	X	X
16 slots with configurable size	X	X	X
Configurable data size: 8-, 10-, 16-, 20-, 24-, 32-bit	X	X	X
SPDIF	X	X	X
FIFO size	8 words		
PDM	N/A	SA1 only	X

9.6 Controller area network (CAN)

The bxCAN peripheral of STM32L4 and STM32L4+ devices was replaced by an FDCAN peripheral on STM32U3. This peripheral offers compliance with newer standards and higher bit rates respectively. Refer to the table below for a comparison of these peripherals.

Table 41. CAN features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4	STM32L4+	STM32U3
Instances	• For STM32L41/42xxx devices: – N/A • For STM32L43/44/45/46/47/48xxx devices: – 1 bxCAN • For STM32L49/4Axxx devices: – 2 bxCAN	1 bxCAN	1 FDCAN
CAN 2.0 parts A, B active compliance	X		X
ISO 11898-1:2015 (FDCAN) compliance	N/A		X
AUTOSAR and J1939 compliance	N/A		X
CAN error logging	N/A		X
Maximum data size	8 bytes		64 bytes
Maximum bit rate	1 Mbit/s		5 Mbit/s
Transmission	Three transmit mailboxes with configurable priority.		Configurable transmit queue for up to 3 payloads (up to 64 bytes each) and transmit event FIFO.

Feature	STM32L4	STM32L4+	STM32U3
Reception	Two receive FIFOs with three stages.		Two receive FIFOs for three payloads each (up to 64 bytes per payload).
Acceptance filtering	• For STM32L43/44/45/46/47/48xxx devices: – 14 configurable filters; • For STM32L49/4Axxx devices: – 28 configurable filters.	28 configurable filters	28 configurable filters, improved
Other features	• Maskable interrupts. • Software-efficient mailbox mapping at a unique address space.		• Maskable module interrupts. • Separate signaling on reception of high priority messages. • Two clock domains: APB bus interface and CAN core kernel clock. • Power down support.

9.7 Secure digital input/output multimedia card interface (SDMMC)

STM32U3 devices contain an enhanced version of the SDMMC interface, also present on STM32L4 and STM32L4+ devices. This enhanced version offers compliance with newer standards as well as speed enhancements and IDMA support. Refer to the tabel below for a detailed comparison.

Table 42. SDMMC features of STM32L4, STM32L4+, and STM32U3 MCUs

Feature		STM32L4	STM32L4+	STM32U3
Instances		• For STM32L41/42xxx devices: – N/A • For other STM32L4 devices: – 1 SDMMC	• For STM32L4R/4Sxxx devices: – 1 SDMMC • For STM32L4P/4Qxxx devices: – 2 SDMMC	1 SDMMC
Compliance with embedded multimedia card system specification		• Full compliance with multimedia card system specification version 4.2. • Card support for three different databus modes: 1-bit (default), 4-bit, and 8-bit. • Full compatibility with previous versions of multimedia cards (backward compatibility).	• Full compliance with embedded multimedia card system specification version 5.1. • Card support for three different databus modes: 1-bit (default), 4-bit, and 8-bit. • Full compatibility with previous versions of multimedia cards (backward compatibility).	• Full compliance with embedded multimedia card system specification version 5.1. • Card support for three different databus modes: 1-bit (default), 4-bit, and 8-bit. • Full compatibility with previous versions of multimedia cards (backward compatibility).
Compliance with SD memory card specifications		• Full compliance with SD memory card specifications version 2.0.	• Full compliance with SD memory card specifications version 4.1. • SPI mode and UHS-II mode not supported.	• Full compliance with SD memory card specifications version 6.0. • SPI mode and UHS-II mode not supported.
Compliance with SDIO card specification		• Full compliance with SDIO card specification version 2.0. • Card support for two different databus modes: 1-bit (default) and 4-bit.	• Full compliance with SDIO card specification version 4.0. • Card support for two different databus modes: 1-bit (default) and 4-bit. • SPI mode and UHS-II mode not supported.	• Full compliance with SDIO card specification version 4.0. • Card support for two different databus modes: 1-bit (default) and 4-bit. • SPI mode and UHS-II mode not supported.
Data transfer speed		Up to 50 MHz	Up to 104 Mbytes/s	Up to 208 Mbytes/s
Features	Variable delay (SDR104, HS200)	N/A	N/A	X

Feature		STM32L4	STM32L4+	STM32U3
Features	SDMMC_CKIN	N/A	X	X
	SDMMC_CDIR, SDMMC_D0DIR	N/A	SDMMC1 only	X
	SDMMC_D123DIR	N/A	SDMMC1 only	X
Other features		N/A	N/A	• IDMA linked list support.

9.8 Universal serial-bus interface (USB)

The STM32L4, STM32L4+, and STM32U3 devices embed three different USB 2.0 full-speed peripherals. The main differences are summarized in the table below.

Table 43. USB features on STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4	STM32L4+	STM32U3
Instances	• For STM32L4x1xx devices: – N/A • For other STM32L41/42/43/44/45/46xxx devices: – USB 2.0 full-speed device with clock recovery. • For other STM32L47/48xxx devices: – USB 2.0 full-speed OTG without clock recovery. • For other STM32L49/4Axxx devices: – USB 2.0 full-speed OTG with clock recovery.	USB 2.0 full-speed OTG with clock recovery.	USB 2.0 full-speed host/ device with clock recovery.
Endpoints	• For USB 2.0 full-speed devices: – 8 configurable bidirectional endpoints. • For USB 2.0 full-speed OTG: – 1 bidirectional control endpoint. – 5 IN endpoints. – 5 OUT endpoints.		8 configurable bidirectional endpoints.
Size of dedicated SRAM	• For USB 2.0 full-speed devices: – 1 Kbyte • For USB 2.0 full-speed OTG: – 1.2 Kbytes		2 Kbytes
Link Power Management and Battery Charging Detection support	X		X
Other features	• For USB 2.0 full-speed devices: – Controllable embedded pull-up resistor on DP line. • For USB 2.0 full-speed OTG: – Attach detection protocol (ADP). – Other features that come with the OTG specification 2.0 compliance.		• Controllable embedded pull-up resistor on DP line.
Low-power modes	• For USB 2.0 full-speed devices: – USB Suspend/Resume operations. – Peripheral power-down mode. • For USB 2.0 full-speed OTG: – System stop during USB suspend. – Switch-off of clock domains internal to the digital core. – PHY and DFIFO power management.		• USB Suspend/ Resume operations. • Peripheral power-down mode.

On STM32U3, STM32L4+, and most STM32L4 (except STM32L47/48x lines) devices, an included clock recovery system (CRS) provides a precise clock to the USB peripheral:

- When using USB Device mode, the CRS allows crystal-less USB operation.
- When using USB Host mode, the CRS allows low frequency crystal (32.768 kHz) USB operation.

10 Migration of analog peripherals

10.1 Analog-to-digital converter (ADC)

All STM32U3, STM32L4, and STM32L4+ MCUs embed successive approximation ADC, which can be tightly coupled on some devices, and can operate in dual mode (ADC1 is master). Further information can be found in the table below.

Table 44. ADC features of STM32L4, STM32L4+, and STM32U3 MCUs

Feature		STM32L4	STM32L4+	STM32U3
Instances		• For STM32L41/42xxx devices: – 2x 12-bit ADC (ADC1, ADC2). • For STM32L43/44/45/46xxx devices: – 1x 12-bit ADC (ADC1). • For STM32L47/48/49/4Axxx devices: – 3x 12-bit ADC (ADC1, ADC2, ADC3).	• For STM32L4P/4Qxxx devices: – 1x 12-bit ADC (ADC1). • For STM32L4R/4Sxxx devices: – 2x 12-bit ADC (ADC1, ADC2).	2x 12-bit ADC (ADC1, ADC2).
Resolution		12, 10, 8, or 6 bits		12, 10, 8, or 6 bits
Channels		• ADC1: up to 16 external + 3 internal. • ADC2: up to 16 external + 2 internal (0 internal for STM32L41/42xxx devices). • ADC3: up to 12 external + 4 internal.		• ADC1: up to 15 external + 4 internal. • ADC2: up to 13 external + 6 internal.
Maximum sampling rate		5 Msps		2.5 Msps
Dual mode		STM32L41/42/47/48/49/4Axxx devices only	X	X
Injected channels		Up to 4		Up to 4
Differential inputs		X		N/A
Self-calibration (offset)		X		X
Independent clock		X		X
Oversampling	Maximum ratio	2-256x		2-1024x
	Register size	16 bits		32 bits
	Data shift	Up to 8-bit right shifting		Up to 10-bit right shifting
Programmable channel-wise sampling time		X		X
Offset compensation		X		X
Gain compensation		N/A		X
Analog watchdogs		3		3
DMA support		X		X

Feature	STM32L4	STM32L4+	STM32U3
Low-power features	• Speed adaptive low-power mode to reduce ADC consumption when operating at low frequency. • Allows slow bus frequency application while keeping optimum ADC performance. • Provides automatic control to avoid ADC overrun in low AHB bus clock frequency (auto-delayed mode).		• Speed adaptive low-power mode to reduce ADC consumption when operating at low frequency. • Allows slow bus frequency application while keeping optimum ADC performance. • Provides automatic control to avoid ADC overrun in low AHB bus clock frequency (auto-delayed mode).
Autonomous mode	N/A		X

10.2 Digital-to-analog converter (DAC)

All STM32U3 and STM32L4+, and most STM32L4 devices embed a DAC peripheral with up to two output channels. All instances offer the same features, except for autonomous mode double-data DMA support, enabling to send two data blocks (12- or 8-bit) simultaneously, on STM32U3 devices. This is summarized in the table below.

Table 45. DAC features in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4	STM32L4+	STM32U3
Instances/channels	• For STM32L41/42xxx devices: – N/A • For STM32L43/44xxx devices: – DAC1 with 2 channels. • For STM32L45/46xxx devices: – DAC1 with 1 channel	DAC1 with 2 channels	DAC1 with 2 channels
Resolution	8 or 12 bits		8 or 12 bits
Output buffer	X		X
Maximum sampling rate	1 Msps		1 Msps
DMA support	X		X
DMA Double-data mode	N/A		X
Autonomous mode	N/A		X
Other differences	N/A	• HFSEL bit when clock frequency >80 MHz	• 2 HFSEL bits when clock frequency >80 MHz

10.3 Comparator (COMP)

All STM32U3 and STM32L4+, and most STM32L4 devices (except for the STM32L41/42xx line) embed two ultra-low-power comparators, COMP1 and COMP2, with almost identical features. STM32L41/42xxx devices contain only COMP1. However, the structure of the control and status register is different among the series and the window mode interconnection was enhanced in STM32U3. Refer to the table below for more information.

Table 46. COMPx_CSR registers in STM32L4, STM32L4+, and STM32U3 MCUs

COMPx_CSR	STM32L41/42/43/44/45/46xxx	STM32L47/48/49/4Axxx and STM32L4+	STM32U3
Bit 0	EN	EN	EN
Bit 1	Reserved	Reserved	Reserved
Bit 2	PWRMODE[1:0]	PWRMODE[1:0]	

COMPx_CSR	STM32L41/42/43/44/45/46xxx	STM32L47/48/49/4Axxx and STM32L4+	STM32U3
Bit 3	PWRMODE[1:0]	PWRMODE[1:0]	Reserved
Bit 4	INMSEL[2:0]	INMSEL[2:0]	INMSEL[3:0]
Bit 5			
Bit 6			
Bit 7	INPSEL[1:0]	INPSEL	
Bit 8		Reserved	INPSEL[1:0]
Bit 9	WINMODE (footnote: Available in COMP2_CSR only.)	WINMODE (footnote: Available in COMP2_CSR only.)	
Bit 10	Reserved	Reserved	Reserved
Bit 11			WINMODE
Bit 12			Reserved
Bit 13			
Bit 14			WINOUT
Bit 15	POLARITY	POLARITY	POLARITY
Bit 16	HYST[1:0]	HYST[1:0]	HYST[1:0]
Bit 17			
Bit 18	BLANKING[2:0]	BLANKING[2:0]	PWRMODE[1:0]
Bit 19			
Bit 20			BLANKSEL[4:0]
Bit 21	Reserved	Reserved	
Bit 22	BRGEN	BRGEN	
Bit 23	SCALEN	SCALEN	
Bit 24	Reserved	Reserved	
Bit 25	INMESEL[1:0]		Reserved
Bit 26			
Bit 27			
Bit 28	Reserved		
Bit 29			
Bit 30	VALUE	VALUE	VALUE
Bit 31	LOCK	LOCK	LOCK

On STM32U3 devices, the blanking sources have changed as well: TIM3 OC3 was added to COMP1 and TIM3 OC4 replaced TIM15 OC1 for COMP2.

10.4 Voltage reference buffer (VREFBUF)

The internal VREFBUF is an operational amplifier, with programmable gain. The amplifier input is connected to the internal voltage reference V_{REFINT}.

The STM32U3, STM32L4, and STM32L4+ MCUs embed one VREFBUF that can be used as voltage reference for ADCs and DACs. VREFBUF can also be used as voltage reference for external components through the VREF+ pin.

The STM32U3 VREFBUF supports four voltages, whereas the STM32L4 and STM32L4+ MCUs support only two voltages.

Table 47. VREFBUF features in STM32L4, STM32L4+, and STM32U3 MCUs

STM32L4/STM32L4+(1)		STM32U3	
Symbol	Voltage (V)	Symbol	Voltage (V)
N/A		VREFUBUF0	1.5
		VREFUBUF1	1.8
VREF_OUT1	2.048	VREFUBUF2	2.048
VREF_OUT2	2.5	VREFUBUF3	2.5

1. *No VREFBUF in STM32L41/42xxx devices.*

10.5 Operational amplifier (OPAMP)

STM32L41/42/43/44/45/46xxx devices contain one OPAMP, whereas all other STM32L4, STM32L4+ and STM32U3 devices embed two amplifiers, with identical features and interconnections. Each OPAMP has two inputs and one output. The three I/Os can be connected to the external pins to enable any type of external interconnections.

Each OPAMP can be configured internally as a follower or as an amplifier with a non-inverting gain ranging from 2 to 16. The positive input can be connected to the internal DAC. The output can be connected to the internal ADC.

The only difference is that the STM32U3 OPAMPs support the high-speed mode and achieves a better slew rate.

11 Migration of signal/image processing accelerators

11.1 Digital filters

While the STM32L4 and STM32L4+ devices offer a digital filter for sigma-delta modulators (DFSDM), on STM32U3 this was replaced by a newer audio digital filter (ADF). The main benefits of ADF compared to DFSDM are the following:

- Support for autonomous mode in Stop modes.
- The kernel clock needs to be only twice the bitstream rate (four times the bitstream rate for DFSDM).
- Improved in-band droop thanks to the embedded CIC filter.
- Addition of a high-pass filter.
- Gain/attenuation steps of ~3 dB.
- Saturation blocks.
- Support of voice and sound activity detection.

Table 48. Digital filters in STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4	STM32L4+	STM32U3
Peripheral type	DFSDM	DFSDM	ADF
Number of channels	• For STM32L41/42/43/44/45/46xxx devices: – 4 • For STM32L47/48/49/4Axxx devices: – 8	• For STM32L4R/4Sxxx devices: – 8 • For STM32L4P/4Qxxx devices: – 4	1
Number of filters	• For STM32L41/42/43/44/45/46xxx devices: – 2 • For STM32L47/48/49/4Axxx devices: – 4	• For STM32L4R/4Sxxx devices: – 4 • For STM32L4P/4Qxxx devices: – 2	1
Input from internal ADC	STM32L49/4Axxx only	X	X
Supported trigger sources	• For STM32L41/42/43/44/45/46xxx devices: – 7 • For STM32L47/48/49/4Axxx devices: – 11	12	4
Pulses skipper/micro-delay control	N/A	X	X
Sound activity detection	N/A		X
Autonomous in Stop mode	N/A		X

11.2 Touch sensing controller (TSC)

STM32U3, STM32L4, and STM32L4+ MCUs embed a touch sensing controller (TSC) with the same features. The TSC provides a simple solution to add capacitive-sensing functionality to any application. A capacitive-sensing technology can detect a finger presence near an electrode that is protected from direct touch by a dielectric (such as glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. Refer to the product reference manual for more details on TSC features.

The number of capacitive-sensing channels is dependent on the size of the package and subject to I/O availability. The TSC input/output signals and their pin mapping are partially compatible between STM32L4, STM32L4+, and STM32U3 MCUs. The maximum number of available channels is 24 for STM32L47/48/49/4Axxx and STM32L4+ devices, while it is 21 for STM32L41/42/43/44/45/46xxx and STM32U3 devices.

12 Migration of external memory interface peripherals

12.1 Octo-SPI interface (OCTOSPI)

The OCTOSPI peripheral provides a serial interface that enables communication with external serial memories such as flash memory, PSRAM, HyperRAM™, HyperFlash™, and some specific ICs like FPGA or ASICs.

The Octo-SPI specialized communication interface targets single-, dual-, quad-, or octal-SPI memories, and can be configured in three modes: indirect, status-polling, and memory-mapped.

The OCTOSPI peripheral is available on STM32L4+ and STM32U3 MCUs, with several additional features. STM32L4 MCUs feature a QUADSPI peripheral.

Table 49. Quad-SPI and Octo-SPI features on STM32L4, STM32L4+, and STM32U3 MCUs

Feature	STM32L4	STM32L4+	STM32U3
Type	**QUADSPI**	**OCTOSPI**	**OCTOSPI**
Number of instances	1	2	1
OCTOSPI manager	N/A	X	N/A
Indirect, automatic status-polling and memory-mapped modes	X	X	X
HyperBus mode support	N/A	X	X
Xccela standard compliant	N/A	X	X
XSPI (JEDEC251ES) compliant	N/A	X	X
SDR and DTR modes	X	X	X
Dual AHB interface	N/A	N/A	X
Data strobe (DS, DQS)	N/A	X	X
Fully programable opcode, frame format	X	X	X
RX/TX FIFO	X	X	X
Refresh counter	N/A	STM32L4P/4Qxxx only	X
TrustZone security	N/A	N/A	X

13 Software migration

13.1 Reference documents

- Definitive guide to Cortex®-M33 and Cortex®-M4 processors
- *STM32 Cortex®-M4 MCUs and MPUs programming manual* (PM0214)
- *STM32 Cortex®-M33 MCUs programming manual* (PM0264)
- Cortex®-M4 processor Technical Reference Manual
- Cortex®-M33 processor Technical Reference Manual

13.2 Cortex®-M4 and Cortex®-M33 overview

13.2.1 STM32 Cortex®-M4 processor and core peripherals

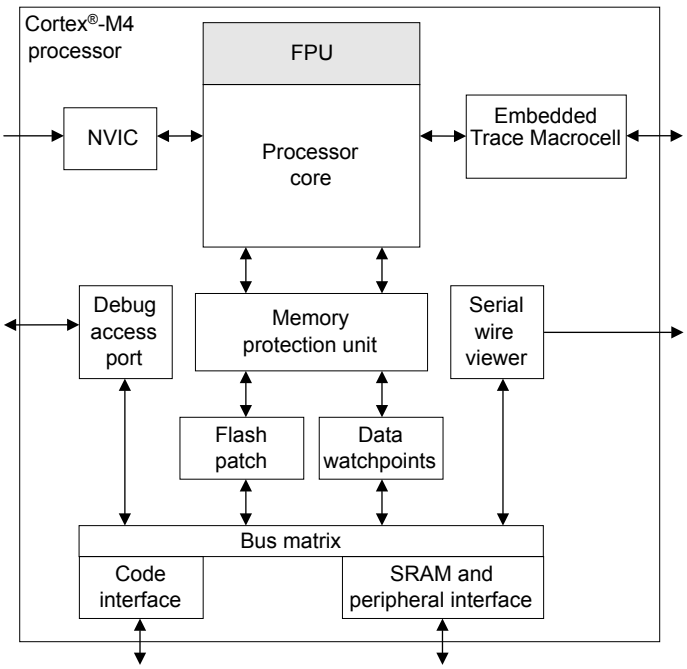
The Cortex®-M4 processor is a high-performance 32-bit processor designed for the microcontroller market. It offers significant benefits to the developers, including:

- Outstanding processing performance combined with fast interrupt handling.
- Enhanced system debug with extensive breakpoint and trace capabilities.
- Efficient processor core, system and memories.
- Ultra-low power consumption with integrated sleep modes.
- Platform security robustness, with integrated memory protection unit (MPU).

The Cortex®-M4 processor is built on a high-performance processor core, with a three-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers an exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, a saturating arithmetic, and dedicated hardware division.

The STM32 Cortex®-M4 implementation is illustrated in the figure below.

Figure 9. STM32 Cortex®-M4 implementation



Cortex®-M4 key features

- Architecture: 32 bits RISC Armv7E-M.
- Three-stage pipeline with branch speculation.
- Instruction set:
  - Thumb, Thumb-2.
  - Hardware multiply, hardware divide, saturated arithmetic.
  - DSP extensions:
    - Single-cycle 16/32-bit MAC.
    - Single-cycle dual 16-bit MAC.
    - 8/16-bit SIMD arithmetic.
- FPU (VFPv4-SP).

13.2.2 STM32 Cortex®-M33 processor and core peripherals

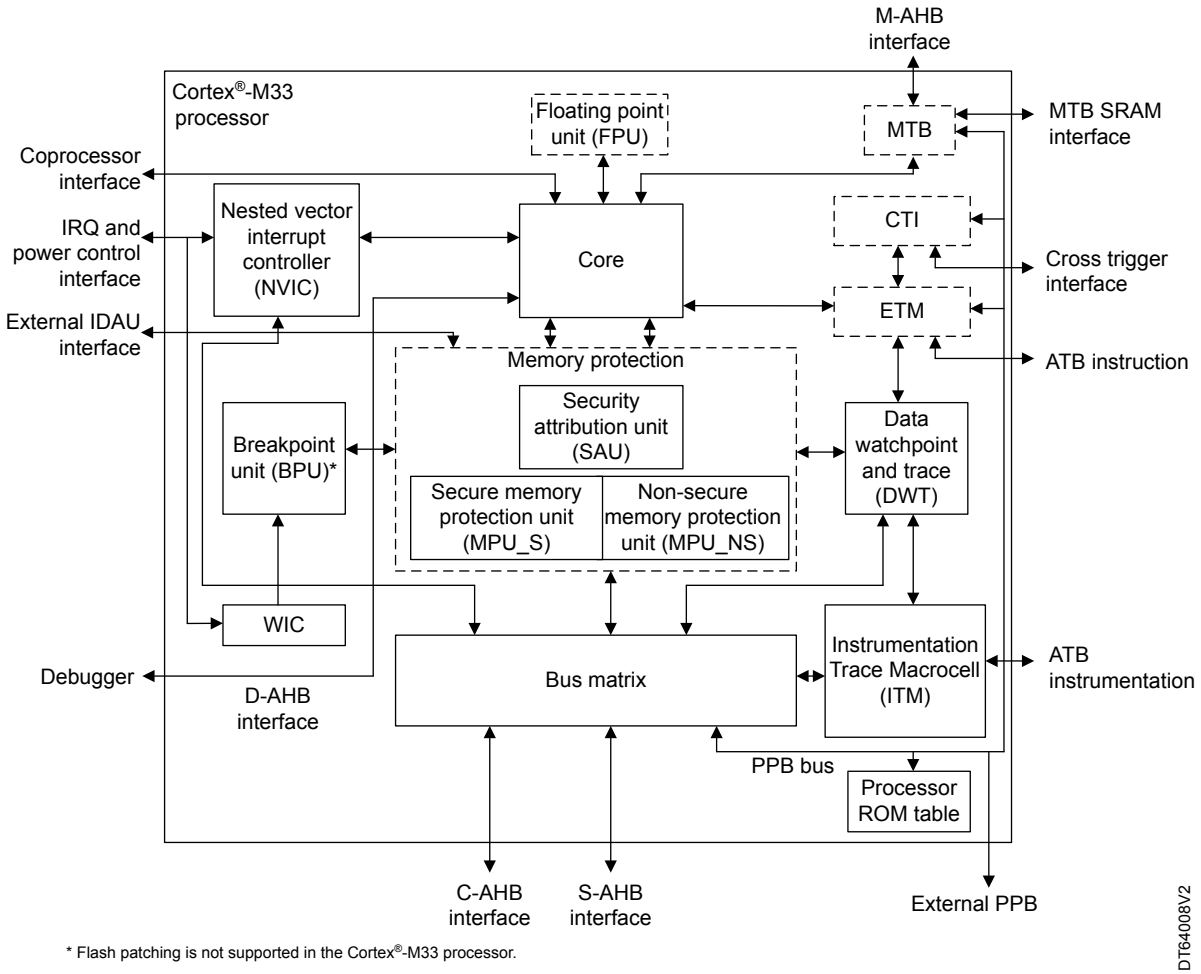
The Cortex®-M33 processor is excellent in ultra-low-power, performance and security.

This processor is based on the Armv8-M architecture for use in environments requiring more security implementation. The Cortex®-M33 core implements a full set of DSP (digital signal processing) instructions, TrustZone®-aware support and a memory protection unit (MPU) that enhances the application security.

The Cortex®-M33 core also features a single-precision floating-point unit (FPU) that supports all the Arm® single precision data-processing instructions and all the data types.

The STM32 Cortex®-M33 implementation is illustrated in the figure below.

Figure 10. STM32 Cortex®-M33 implementation



* Flash patching is not supported in the Cortex®-M33 processor.

Cortex®-M33 key features

- Arm-v8M architecture with 2/3-stage pipeline, Harvard, 1.5 DMIPS/MHz.
- Single-cycle branch, no branch prediction.
- Hardware divide instruction.
- Debug (CoreSight-compliant).
- Memory exclusive instructions.
- NVIC without interrupts increased up to 480 max (256 priority levels).
- Enhanced MPU, more flexible (32 bytes) up to 16 regions (for each one of the secure and non-secure states).
- New AMBA® 5 AHB interface, support of security state extension to the system.
- Support of external implementation defined attribution unit.
- Fully compatible with TrustZone® system.

Cortex®-M4 vs Cortex®-M33

The differences between Cortex®-M4 and Cortex®-M33 are presented in the table below.

Table 50. Cortex®-M4 versus Cortex®-M33

Feature	Cortex-M4	Cortex-M33
Instruction set architecture	Armv7-M	Armv8-M mainline
	Thumb, Thumb-2	
Pipeline	Three-stages	
Performance efficiency (CoreMark/MHz)	3.42	4.09
DMIPS/MHz	1.25	1.50
Memory protection	Yes	
Maximum MPU regions	8	8 secure and 8 non-secure
Trace (ETM or MTB)	ETMv3	MTB and/or ETMv4
DSP	Yes	
Floating point hardware		
Bus protocol	AHB Lite, APB	AHB5
Max. number of external interrupts	240	480
CMSIS support	Yes	
TrustZone for Armv8-M	No	Yes
Coprocessor interface		

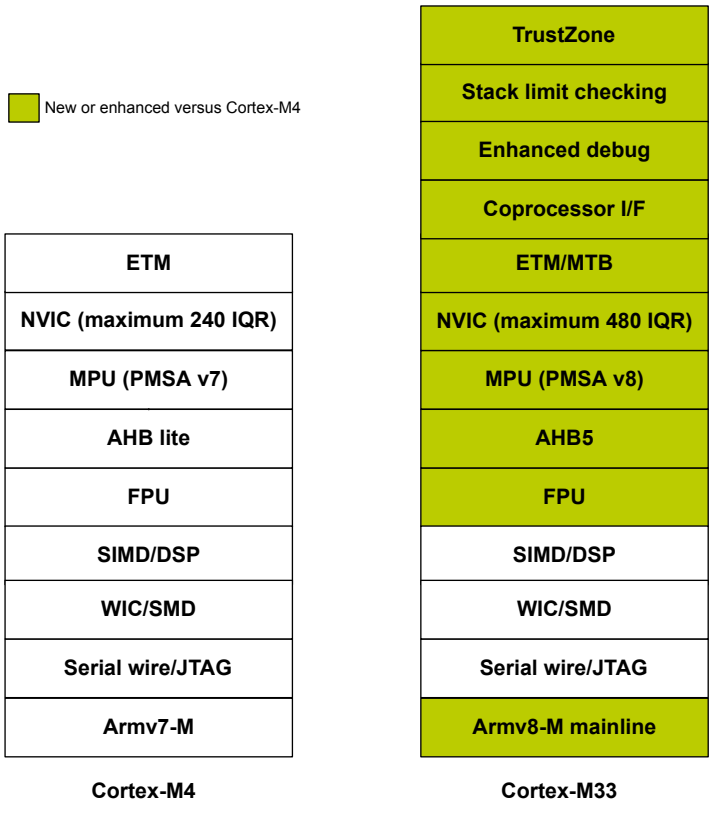
13.2.3 Software point of view

The Cortex®-M33 core has the same features as the Cortex®-M4 core, but also includes the following ones:

- Implementing Armv8-M architecture.
- Implementing the latest floating point unit FPU specification (based on Arm FPv5 architecture) that adds more instructions than the Cortex®-M4 has.
- AHB5 specification used for the system and memory interface, to extend security across the whole system.
- Latest version of the memory protection unit (MPU) specification used to simply the setup of regions.
- Extended number of maximum interrupts to 480.
- Optional execution trace using MTB or ETM.
- Enhanced debug components to make simplify usage.
- Coprocessor interface supporting up to 8 coprocessors units.
- Hardware stack limit checking.
- TrustZone® security features adding efficient security features.

The Cortex®-M33 enhancements compared to Cortex®-M4 are illustrated in the figure below.

Figure 11. Cortex®-M33 enhancements versus Cortex®-M4



13.3 Cortex® mapping overview

The mapping is different on the Cortex®-M4 and the Cortex®-M33 cores, as shown in the table below.

Table 51. Cortex® mapping for STM32L4, STM32L4+, and STM32U3 MCUs

Feature		STM32L4 and STM32L4+	STM32U3
Core	Architecture	Cortex®-M4	Cortex®-M33
	NVIC	Maskable interrupt channel: • 95 (STM32L4+) • 91 (STM32L49/4Axxx) • 82 (STM32L47/48xxx) • 67 (STM32L41/42/43/44/45/46xxx) (Not including the 16 Cortex®-M33 with FPU interrupt lines.)	96 maskable interrupt channels (not including the 16 Cortex®-M33 with FPU interrupt lines)
	EXTI	• Up to 39 events/interrupts (STM32L4+) • Up to 41 events/interrupts (STM32L49/4Axxx) • Up to 40 events/interrupts (STM32L47/48xxx) • Up to 37 events/interrupts (STM32L41/42/43/44/45/46xxx)	23 events/interrupts
Mapping	System timer	0xE000 E010 to 0xE000 E01F	0xE000 E010 to 0xE000 E0FF
	NVIC	0xE000 E100 to 0xE000 E4EF 0xE000 EF00 to 0xE000 EF03	0xE000 E100 to 0xE000 ECFF
	System control block	0xE000 ED00 to 0xE000 ED3F	0xE000 ED00 to 0xE000 ED8F
	Floating point unit	0xE000 ED88 to 0xE000 ED8B 0xE000 EF30 to 0xE000 EF44	0xE000 EF30 to 0xE000 EF44
	MPU (memory protection unit)	0xE000 ED90 to 0xE000 EDB8	0xE000 ED90 to 0xE000 EDB8
	Mapping (merged)/ security attribution unit	N/A	0xE000 ED00 to 0xE000 EDEF

Note: On Cortex®-M33 devices, there is a new section named "System control and ID registers", placed between `0xE000 E000` and `0xE000 EF8F`. This section contains:

- *Interrupt controller type and auxiliary control registers.*
- *System control block.*
- *Debug registers in the SCS.*
- *Software trigger interrupt register.*

Revision history

Table 52. **Document revision history**

Date	Version	Changes
12-Feb-2025	1	Initial release.

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