Migrating from STM32L0 to STM32U0 MCUs

Introduction

For designers of STM32 microcontroller applications, being able to replace one microcontroller type with another from the same product family easily is an important asset. Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note analyzes the steps required to migrate an existing design from the STM32L0 series to the STM32U0 series. Three aspects need to be considered for the migration: hardware, peripherals, and firmware.

This document lists the full set of features available for the STM32L0 series and the equivalent features on the STM32U0 series (some products may have fewer features depending on their part number).

To benefit fully from this application note, the user must be familiar with the STM32 microcontroller documentation available on www.st.com, with a particular focus on the documents listed below:

- STM32L0 series datasheets
- STM32U0 series datasheets:
  - STM32U031x4/6/8: *Ultra-low-power Arm® Cortex®-M0+ 32-bit MCU, up to 64-Kbyte flash memory, 12-Kbyte SRAM* (DS14581)
  - STM32U031x4/6/8: *Ultra-low-power Arm® Cortex®-M0+ 32-bit MCU, up to 64-Kbyte flash memory, 12-Kbyte SRAM* (DS14548)
  - STM32U083xC: *Ultra-low-power Arm® Cortex®-M0+ 32-bit MCU, 256-Kbyte flash memory, 40- Kbyte SRAM, USB, LCD, AES* (DS14463)
- STM32L0 series reference manuals:
  - *Ultra-low-power STM32L0x1 advanced Arm®-based 32-bit MCUs* (RM0377)
  - *Ultra-low-power STM32L0x2 advanced Arm®-based 32-bit MCUs* (RM0376)
  - *Ultra-low-power STM32L0x3 advanced Arm®-based 32-bit MCUs* (RM0367)
- STM32U0 reference manual: *STM32U0 series advanced Arm®-based 32-bit MCUs* (RM0503)

1 STM32U0 series overview

The STM32U0 series devices are a perfect fit in terms of ultra-low power, performance, memory size, and peripherals at a cost-effective price.

In particular, STM32U0 series devices offer higher frequency and performance operations than STM32L0 series devices. The STM32U0 series features an Arm® Cortex®-M0+ processor at 56 MHz, versus a Cortex®-M0+ processor at 32 MHz featured on the STM32L0 series. STM32U0 devices also feature optimized flash memory access through the adaptive real-time memory accelerator (ART accelerator).

STM32U0 series MCUs increase the low-power efficiency in dynamic mode (µA/MHz), and reach a very low level of static power consumption on the various available low-power modes.

The detailed list of available features and packages for each product is available in the respective datasheets.

STM32U0 series devices include a larger set of peripherals with advanced features compared to the STM32L0 series, such as:

- Touch sensing controller (TSC)
- Low-power universal asynchronous receiver transmitter (LPUART)
- Infrared interface (IRTIM)
- Low-power timer (LPTIM)
- Voltage reference buffer (VREFBUF)
- DMA request multiplexer (DMAMUX)
- Clock recovery system (CRS) for USB
- SRAM1 size is different on the various STM32U0 devices:
  - 32 Kbytes for STM32U0x3
  - 8 Kbytes for STM32U0x1
- Additional SRAM2 with data preservation in Standby mode:
  - 8 Kbytes for STM32U0x3
  - 4 Kbytes for STM32U0x1
- Optimized power consumption and an enriched set of low-power modes

This migration guide covers only the migration from the STM32L0 series to the STM32U0 series, and as a consequence any new features present on the STM32U0 series but not already present on the STM32L0 series are not covered by this document. Refer to the STM32U0 reference manuals and datasheets for an exhaustive picture.

Table 1. STM32U0 memory availability

Part number	Flash memory size	SRAM1	SRAM2	Feature level
STM32U031x4	16 Kbytes	8 Kbytes	4 Kbytes	-
STM32U031x6	32 Kbytes			
STM32U031x8	64 Kbytes			
STM32U073x8	64 Kbytes	32 Kbytes	8 Kbytes	With LCD + USB
STM32U083x8				STM32U073 + AES cryptography
STM32U073xB	128 Kbytes			With LCD + USB
STM32U083xB				STM32U073 + AES cryptography
STM32U073xC	256 Kbytes			With LCD + USB
STM32U083xC				STM32U073 with crypto

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

2 STM32L0 series overview

The exclusive combination of an Arm® Cortex®-M0+ core (max speed 32 MHz) and STM32 ultra-low-power features makes the STM32L0 series the best fit for applications operating on battery or supplied by energy harvesting and the world's lowest power consumption MCU at 125°C.

The STM32L0 series offer dynamic voltage scaling, an ultra-low-power clock oscillator, an LCD interface, comparators, DAC, and hardware encryption. Autonomous peripherals (including USART, I2C, and touch sense controller) reduce the load of the Arm® Cortex®-M0+ core, leading to fewer CPU wakeups and decreasing the processing time and power consumption.

The STM32L0 series devices are available with up to 192 Kbytes of flash memory, 20 Kbytes of RAM, and up to 6 Kbytes of embedded EEPROM (no emulation needed) in 14- to 100-pin packages.

Three feature levels (Table 2) and four categories (Table 3) cover a wide range of customer needs. Table 4 summarizes the memory availability of the STM32L0 series devices.

Table 2. STM32L0 series feature levels

Feature level	Additional features
1	• Access Line
2	• Crystal-less USB 2.0 FS (BCD, LPM-compliant) • 16 capacitive touch keys • True random number generator (TRNG)
3	• Crystal-less USB 2.0 FS • 16 capacitive touch keys • True random number generator (TRNG) • LCD driver (8x48)

Table 3. STM32L0 series product category overview

Type(1)	Part number
Category 1	STM32L01xxx, STM32L02xxx
Category 2	STM32L03xxx, STM32L04xxx
Category 3	STM32L05xxx, STM32L06xxx
Category 5	STM32L07xxx, STM32L08xxx

1. *Category X devices are referred to as "Cat. X" devices within this document.*

Table 4. STM32L0 memory availability and feature levels

Category	Part number	Flash memory size (Kbytes)	EEPROM size (Kbytes)(1)	RAM size (Kbytes)	Feature level
1	STM32L01xxx	8/16	0.5	2	1
	STM32L02xxx				1 + AES
2	STM32L03xxx	16/32	1	8	1, 2
	STM32L04xxx				1
3	STM32L05xxx	32/64	2	8	1, 2, 3
	STM32L06xxx				2, 3 + AES
5	STM32L07xxx	16/128/192	3/6	20	1, 2, 3
	STM32L08xxx				1, 2, 3 + AES

1. *Not available for all part numbers.*

3 Hardware migration

3.1 Package availability

Some packages are available for both the STM32U0 and STM32L0 series, as illustrated by Table 5 and Table 6. The other packages available for the STM32L0 series are not available on the STM32U0 series. The STM32U0 series also brings new packages that are not available on the STM32L0 series.

Note that the WLCSP packages are not equivalent and have different die sizes for each product.

The table below lists the available packages for the STM32U0 series.

Table 5. Available packages for the STM32U0 series

Package	STM32L0 series(1)	STM32U083xx	STM32U073xx	STM32U031xx	Size (mm x mm)
TSSOP20	X	-	-	X	6.5 x 4.4
UFQFPN32	X	X	X	X	5 x 5
UFQFPN48	X	X	X	X	7 x 7
LQFP48	X	X	X	X	7 x 7
LQFP64	X	X	X	X	10 x 10
LQFP80	-	X	X	-	12 x 12
UFBGA64	X	X	X	X	5 x 5
UFBGA81	-	X	X	-	5 x 5
WLCSP27	-	-	-	X	2.55 x 2.34
WLCSP42	-	X	X	-	2.82 x 2.93

1. *This column with a gray background represents the STM32L0 series to provide a comparison between both series.*

The table below lists the available packages for the STM32L0 series.

Table 6. Available packages for the STM32L0 series

Package	STM32U0 series(1)	STM32L0 series			
		Cat. 1 devices	Cat. 2 devices	Cat. 3 devices	Cat. 5 devices
		STM32L01xxx, STM32L02xxx	STM32L03xxx, STM32L04xxx	STM32L05xxx, STM32L06xxx	STM32L07xxx, STM32L08xxx
TSSOP14	-	X	-	-	-
TSSOP20	X	X	X	-	-
UFQFPN20	-	X	-	-	-
UFQFPN28	-	X	X	-	-
UFQFPN32	X	X	X	X	X
LQFP32	-	X	X	X	X
LQFP48	X	-	X	X	X
LQFP64	X	-	-	X	X
LQFP100	-	-	-	-	X
TFBGA64	X	-	-	X	X
UFBGA64	X	-	-	-	X
UFBGA100	-	-	-	-	X
WLCSP25	-	X	X	-	-
WLCSP36	-	-	-	X	-
WLCSP49	-	-	-	-	X

1. *This column with a gray background represents the STM32U0 series to provide a comparison between both series.*

3.2 Pin compatibility

The STM32U0 and STM32L0 series share a high level of pin compatibility. Most peripherals share the same pins in both series, rendering the transition from an STM32L0 device to an STM32U0 device very straightforward on most available packages, like UFBGA64, LQFP64/48/32, and UFQFPN48. The UFQFPN32 package requires a minor PCB redesign as STM32U0 does not have an exposed pad connected to VSS. STM32L0 Cat. 5 devices also need a PCB redesign, as the original pinout was already incompatible with the other devices in the same family. The TSSOP20 package brings better flexibility in the availability of GPIO and alternate functions, however it is not directly replacable either.

Due to the shared use of system pins as GPIOs, STM32U0 offers two additional GPIOs on the same package.

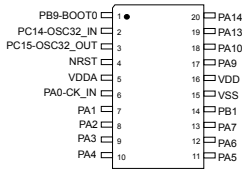
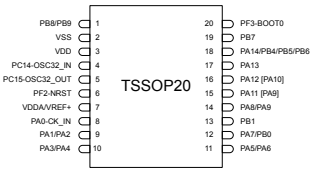
There are a few additional exceptions to take into consideration. The STM32U0 series TSC group assignment is different from that of the STM32L0 series, so applications using TSC require a PCB redesign. The STM32U0 ADC channels are connected to the same pins as for the STM32L0 series, but with different channel numbers.

Refer to the product datasheet for more details.

3.2.1 Pinout differences between STM32L0 and STM32U0 TSSOP packages

The pinout of the STM32U0 TSSOP20 package provides multiple bondings of the GPIO to offer an extended mix of alternate functions for user application as opposed to a fixed selection. Consequentially, it is different from the STM32L0 TSSOP20 pinout.

Table 7. Pinout comparison of STM32L0 and STM32U0 TSSOP20 packages

STM32L0 series	STM32U0 series
	

3.2.2 Pinout differences between STM32L0 and STM32U0 QFP packages

The table below shows the pinout differences in QFP packages for the STM32L0 and STM32U0 series.

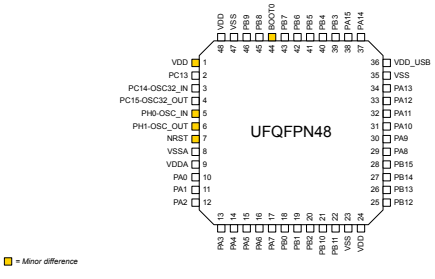
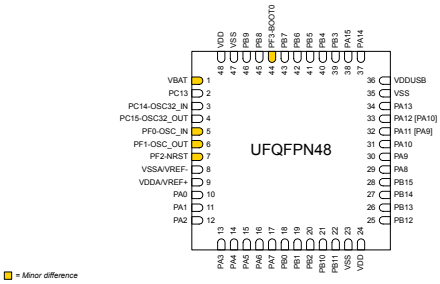
Table 8. Pinout differences between STM32L0 and STM32U0 QFP packages

STM32L0 series				STM32U0 series			
UFQFPN32[1]/LQFP32	UFQFPN48/ LQFP48	LQFP64	Pinout	UFQFPN32/ LQFP32	UFQFPN48/ LQFP48	LQFP64	Pinout
-	1	1	VLCD	-	1	1	VBAT
4	7	7	NRST	4	7	7	PF2-NRST[2]
5	9	13	VDDA	5	9	13	VDDA/VREF+
-	36	48	VDD	-	36	48	VDDUSB[3]
31	44	60	BOOT0	31	44	60	PF3-BOOT0[2]

1. *The pinout of STM32L0 Cat. 5 UFQFPN32 devices is not compatible with other STM32L0 devices. Refer to Table 11 for more details.*
2. *System pins can also be used as GPIO.*
3. *The VDDUSB pin can be connected externally to VDD.*

Table 9 below gives an example of the pinout differences between STM32L0 and STM32U0 UFQFPN48 packages.

Table 9. Example of pinout differences between STM32L0 and STM32U0 UFQFPN48 packages

STM32L052x6/8 UFQFPN48 pinout	STM32U0 UFQFPN48 pinout
	

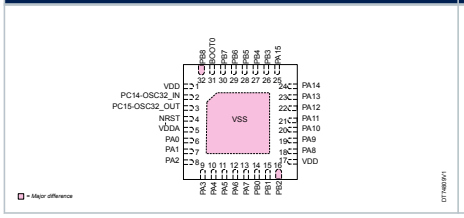
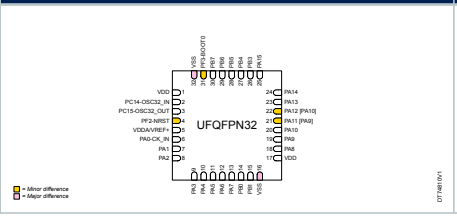
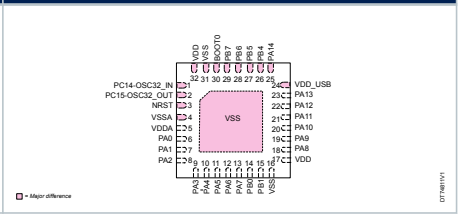
The UFQFPN packages used on STM32U0 devices does not support VSS on the exposed pad. On UFQFPN32, VSS is bonded to pins 16 and 32, and pins PB2 and PB8 are therefore not present on this package for the STM32U0 series.

Table 10. Additional pinout differences between STM32L0 UFQFPN packages with exposed pad and STM32U0 UFQPN packages

STM32L0			STM32U0		
UFQFPN32(1)	UFQFPN48	Pinout	UFQFPN32	UFQFPN48	Pinout
0	0	VSS	-	-	No exposed pad
16	X	PB2	16	X	VSS
32	X	PB8	32	X	VSS

Table 11 below gives an example of the pinout differences between STM32L0 and STM32U0 UFQFPN32 packages.

Table 11. Example of pinout differences between STM32L0 and STM32U0 UFQFPN32 packages

STM32L052x6/8 (Cat. 3)	STM32U031x4/6/8	STM32L072xx (Cat. 5)
		

3.2.3 Ballout differences between STM32L0 and STM32U0 BGA packages

Table 12 below shows the ballout differences in BGA packages for the STM32L0 and STM32U0 series.

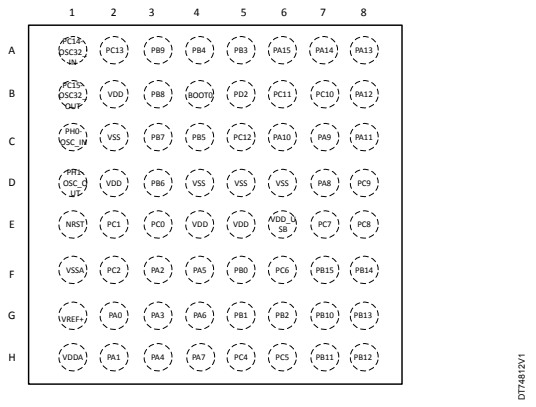
Table 12. Ballout differences between STM32L0 and STM32U0 BGA packages

STM32L0 series		STM32U0 series	
TFBGA64/UFBGA64	Ballout	UFBGA64	Ballout
B2	VDD	B2	VBAT
G1	VREF+	G1	PC3
E5	VDD	E5	VDDUSB(1)
H1	VDDA	H1	VDDA/VREF+
B4	BOOT0	B4	PF3-BOOT0(2)
E1	NRST	E1	PF2-NRST(2)
E6(3)	VDDIO2	E6	VDD

1. *The VDDUSB pin can be connected externally to VDD.*
2. *System pins can also be used as GPIO.*
3. *The STM32U0 series does not support independent VDDIO2.*

Table 13 below gives an example of the pinout differences between STM32L0 and STM32U0 UFBGA64 packages.

Table 13. Example of ballout differences between STM32L0 and STM32U0 UFBGA64 packages

STM32L072xx	STM32U073xx
	

3.3 Recommendations for board migration

The VLCD pin in the STM32U0 series is now multiplexed on the PC3 GPIO through alternate function programming. The PC3 GPIO is located at pin 13 on LQFP80, pin 11 on LQFP64, and pin G1 on BGA64/BGA81.

This implies that any other function in the STM32U0 devices PC3 pins cannot be used on PC3 when the LCD is used by the application. It also implies that the related STM32L0 series PC3 alternate functions, if they are used by the application, must be mapped to other STM32U0 series pins.

The V_{BAT} or V_{DD} supply (if no specific V_{BAT} power is used), must now be connected to the following pins, used as VDD on STM32L0:

- Pin 1 (LQFP64/LQFP48/UFQFPN48)
- Pin B1 (BGA81)
- Pin B2 (BGA64)

On the BGA64 package, the G1 ball used for the VREF+ signal in the STM32L0 series is used as the PC3 GPIO (multiplexed with VLCD) in the STM32U0 series, and the VREF+ signal is bonded with VDDA on the H1 ball.

The boot pins are different in both families. The BOOT0 is multiplexed with the PF3 GPIO on the STM32U0. Refer to Section 4: Boot mode selection for details. Those changes do not impact the board design.

The NRST pin is multiplexed with the PF2 pin, referred to as PF2-NRST.

Note: The GPIOF port replaces the GPIOH port.

Note: New packages (LQFP80, and UFBGA81) have been introduced for the STM32U0 series.

Note: Multiple GPIOs are bonded together to the same pin on TSSOP20.

The NRST pin is shared with GPIO in the STM32U0 series. Selection is available through the device option bytes, where the user could select legacy behavior, input only mode, or GPIO mode. This configuration is loaded from the option bytes after each power on, so the external circuitry must let the NRST pin cross VIH level after power on or exit from deep low-power modes.

4 Boot mode selection

Both the STM32L0 and STM32U0 series offer three different boot modes: boot from the main flash memory, boot from SRAM, or boot from the system memory. However, the way to select the boot mode differs between the products:

- On STM32L0 devices, the boot mode is selected using the nBOOT1 option bit with the BOOT0 pin. On Cat. 1 devices, the nBOOT0 and nBOOT_SEL option bits are available in the FLASH_OPTR register.
- On STM32U0 devices, the boot mode is selected using the nBOOT1 option bit with the BOOT0 pin or the nBOOT0 option bit, depending on the value of the nBOOT_SEL option bit in the FLASH_OPTR register. Additionally, the BOOT_LOCK bit is available to increase application security. It forces the main flash memory as a boot memory area, and requires support in the firmware to connect the debug interface when the RDP level is not 0.

The tables below show the different configurations available for selecting the boot mode for STM32U0 and STM32L0 devices.

Table 14. Boot modes for STM32L0

Boot mode configuration				Selected boot area
nBOOT1 bit	BOOT0 pin	nBOOT_SEL bit(1)	nBOOT0_bit(1)	
X	0	0	X	Main flash memory
1	1	0	X	System memory
0	1	0	X	Embedded SRAM
X	X	1	1	Main flash memory
1	X	1	0	System memory
0	X	1	0	Embedded SRAM

1. *Grayed options are available on Cat. 1 devices only.*

Table 15. Boot modes for STM32U0 devices

Boot mode configuration					Selected boot area
BOOT_LOCK bit	nBOOT1 bit	BOOT0 pin	nBOOT_SEL bit	nBOOT0_bit	
0	X	0	0	X	Main flash memory
0	1	1	0	X	System memory
0	0	1	0	X	Embedded SRAM
0	X	X	1	1	Main flash memory
0	1	X	1	0	System memory
0	0	X	1	0	Embedded SRAM
1	X	X	X	X	Main flash memory forced

4.1 Embedded bootloader

The embedded bootloader is located in the system memory, programmed by STMicroelectronics during production. This bootloader is used to reprogram the flash memory using one of the serial interfaces listed in the table below (where X = supported).

Table 16. Bootloader interfaces on the STM32L0 and STM32U0 series

Peripheral	Pin	STM32L0 series					STM32U0 series
		STM32L01xx STM32L02xx	STM32L03xx STM32L04xx	STM32L05xx STM32L06xx	STM32L071xx STM32L081xx	STM32L072xx STM32L082xx STM32L073xx STM32L083xx	
DFU	USB_DM (PA11) USB_DP (PA12)	-	-	-	-	X	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	-	-	X	X	X	X
USART2	USART2_TX (PD5) USART2_RX (PD6)	X	X	X	X	X	-
USART2	USART2_TX (PA2) USART2_RX (PA3)	-	-	-	-	-	X
USART3	USART3_TX (PC10) USART3_RX (PC11)	-	-	-	-	-	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	-	-	-	X	-	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	-	-	-	X	-	X
I2C3	I2C3_SCL (PB3) I2C3_SDA (PB4)	-	-	-	X	-	X
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	X	X	X	X	-	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	-	-	X	X	-	X

Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606) for more details on the bootloader.

For smaller packages, it is important to check the pin and peripheral availability.

5 Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. Several low-power modes are available to save power when the CPU does not need to be kept running, for example when waiting for an external event. It is up to the user to select the mode that gives the best compromise between low-power consumption, a short startup time, and available wake-up sources.

STM32L0 series and STM32U0 series share the same main low-power modes (Low-power run, Stop, Sleep, Low-power sleep, and Standby) with voltage ranges specific to each series. Additionnally, the STM32U0 series offer three stop modes (Stop 0 and Stop 1 with USB capabilities, and Stop 2) and a new shutdown mode.

Details on the low-power mode configuration in each series can be found in the device reference manual. The consumption figures are given in the device datasheets.

5.1 Low-power modes in the STM32L0 series

Low-power modes

The STM32L0 series devices have the following five low-power modes:

- **Low-power run** mode: regulator in low-power mode, limited clock frequency, limited number of peripherals running
- **Sleep** mode: CPU stopped, peripherals kept running
- **Low-power sleep** mode: CPU stopped, limited clock frequency, limited number of peripherals running, regulator in low-power mode, flash memory stopped
- **Stop** mode: SRAM and all registers content are retained. All clocks in the V_{CORE} domain are stopped, the PLL, MSI, HSI16, and HSE are disabled. LSI and LSE can be kept running
- **Standby** mode: V_{CORE} domain powered off.

Dynamic voltage scaling

The ultra-low-power STM32L0 series devices support the dynamic voltage scaling to optimize its power consumption in Run mode. The voltage from the internal low-drop regulator that supplies the logic can be adjusted according to the system's maximum operating frequency and the external voltage supply. There are three power consumption ranges:

- Range 1 (V_{Core} = 1.8 V), with the CPU running at up to 32 MHz
- Range 2 (V_{Core} = 1.5 V), with a maximum CPU frequency of 16 MHz
- Range 3 (V_{Core} = 1.2 V), with a maximum CPU frequency limited to 4.2 MHz

The global power consumption is reduced by using clock-gating on unused peripherals.

Table 17 presents a summary of the STM32L0 series low-power modes.

Table 17. STM32L0 series low-power modes

Mode	Reg.	CPU	Flash memory(1)	SRAM	Clocks	Peripherals(2)	Consumption (µA/MHz)	Wake-up time (µs)
Run	Range 1	On	On	On	Any	All peripherals available	200	N/A
	Range 2						160	
	Range 3						130	
Low-power run	LPR	On	On	On	MSI 131 kHz max	No USB, no ADC, no TSC Other peripherals available	200	3
Sleep	Range 1	Off	On	On	Any	All peripherals available	Down to 30	0.36
	Range 2							
	Range 3							
Low-power sleep	LPR	Off	On	On	MSI 131 kHz max	No USB, no ADC, no TSC Other peripherals available	200	3.2
Stop	LPR	Off	Off	On	LSI/LSE	RTC available	-	3.5
Standby	OFF	Down	Off	Off	LSI/LSE	RTC and IWDG available	-	50

1. *The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.*
2. *Can be clock-gated when unused.*

Wake-up sources

The STM32L0 series devices can get out of the low-power modes on the following events:

- Sleep mode:
  - Any peripheral interrupt/wake-up event
- Stop modes:
  - Any EXTI line event
  - BOR, PVD, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, LPTIM
- Standby mode:
  - WKUP pins rising or falling edge
  - RTC alarm
  - RTC wake-up
  - RTC tamper event
  - RTC timestamp event
  - External reset in NRST pin
  - IWDG reset

5.2 Low-power modes in the STM32U0 series

Low-power modes

The STM32U0 series devices offer more flexibility to reduce the global consumption, in addition to the low-power modes from the STM32L0 series devices. It offers the following new modes:

- Stop 0, Stop 1, and Stop 2 modes: SRAMs and all register content are retained. All clocks in the V_{CORE} domain are stopped; PLL, MSI, HSI16, and HSE are disabled. LSI and LSE can be kept running
- Shutdown mode: the V_{CORE} domain is powered off. All clocks in the V_{CORE} domain are stopped; PLL, MSI, HSI16, LSI, and HSE are disabled. LSE can be kept running

In the main Run mode, the power consumption can be reduced by one of the following means:

- Slowing down the system clocks
- Gating the clocks to the APB and AHB peripherals when they are unused

Low-power run and Sleep modes support a frequency up to 2 MHz, instead of 0.13 kHz on STM32L0.

Dynamic voltage scaling

The main regulator (MR) has two voltage ranges for dynamic voltage scaling (R1 and R2) used in the Run and Sleep modes:

- Range 1 (V_{Core} = 1.2 V), with the CPU running at up to 56 MHz
- Range 2 (V_{Core} = 1.0 V), with a maximum CPU frequency of 18 MHz. All peripheral clocks are also limited to 18 MHz

Compared to STM32L0, the V_{Core} supply is lower, allowing for higher speed at the same time and bringing better product consumption.

The low-power regulator (LPR) is for the Low-power run, Low-power sleep, Stop 1, and Stop 2 modes, as well as for the RAM retention in Standby mode.

Table 18 presents a summary of the STM32U0 series low-power modes. The consumption figures are given for the STM32U031xx devices as an indication. For the power consumption figures of other devices, refer to the dedicated datasheets.

Table 18. STM32U0 series low-power modes

(3)

Mode	Reg.	CPU	Flash memory (1)	SRAM	Clocks	Peripherals(2)	Consumption	Wake-up time (µs)
Run	Range 1	On	On	On	Any	All peripherals available	68 (uA/MHz)	N/A
	Range 2					All except USB, RNG	61 (uA/MHz)	
Low-power run	LPR	On	On	On	Any except PLL	All except USB, RNG	65 (uA/MHz)	Range 1: 4 µs to range 2: 64 µs
Sleep	Range 1	Off	On	On	Any	All peripherals available	24 (uA/MHz)	6 cycles
	Range 2					All except USB, RNG	26 (uA/MHz)	
Low-power sleep	LPR	Off	On	On	Any except PLL	All except USB, RNG	28 (uA/MHz)	6 cycles
Stop 0	MR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	100 uA	NC
Stop 1	LPR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	2.0 uA without RTC 2.2 uA with RTC	4 µs in SRAM 6 µs in flash memory
Stop 2	LPR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	515 nA without RTC 630 nA with RTC	5 µs in SRAM 7 µs in flash memory
Standby	LPR	Off	Off	SRAM2 On	LSI/LSE	BOR, RTC, IWDG All other peripherals are powered off I/O configuration can be floating, pull-up, or pull-down	121 nA without RTC 249 nA with RTC	14
	Off			Off			32.5 nA without RTC 160 nA with RTC	
Shutdown	Off	Off	Off	Off	LSE	RTC All other peripherals are powered off I/O configuration can be floating, pull-up, or pull-down	16 nA without RTC 195 nA with RTC	256

1. *The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.*
2. *All peripherals can be active or clock-gated to save power consumption. Values are provided with all clock-gated peripherals.*
3. *Typical current at V_{DD}=1.8 V, 25°C. The consumption values are provided when running from the SRAM, flash memory off: 48 MHz in range 1; 16 MHz in range 2; 2 MHz in Low-power run/Low-power sleep modes. The values differ for different products, refer to the dedicated product datasheets for the exact values.*

Wake-up sources

The STM32U0 series devices can get out of the low-power modes on the following events:

- Sleep mode:
  - Any peripheral interrupt/wake-up event
- Stop modes:
  - Any EXTI line event
  - BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
- Standby mode:
  - WKUP pins rising or falling edge
  - RTC event
  - External reset in NRST pin
  - IWDG reset
- Shutdown mode:
  - WKUP pins rising or falling edge
  - RTC event
  - External reset in NRST pin

5.3 Consumption and performance overview

Table 19 shows the comparison of power consumption between STM32L0 and STM32U0 devices for the main dynamic and static modes. The table represents the typical values for given devices at room temperature.

Note: On STM32L0 devices, consumption rises very slowly over the temperature, whereas on STM32U0 devices it increases significantly for the highest temperature range. Refer to the relevant device datasheet for the complete figures.

Table 19. Power consumtion comparison between STM32L0 and STM32U0 devices

Mode	STM32L08x/ STM32L07x	STM32L06x/ STM32L05x	STM32L04x/ STM32L03x	STM32L02x/ STM32L01x	STM32L08x/ 7x	STM32L03x	Unit
Run - while 1	93	88	76	76	52	52	uA/MHz
Run - CoreMark (Range 1)	216	197	161	153	78	78	uA/MHz
Run - CoreMark (Range 3/2)(1)	164	146	114	110	70	70	uA/MHz
Sleep (Range 3/2)(1)	33	33	27	27	28	26	uA/MHz
LP Run	202	168	141	137	80	80	uA/MHz
Stop 0	NA	NA	NA	NA	105	105	uA
Stop 1	NA	NA	NA	NA	3.3	2.1	uA
Stop 2	0.430	0.410	0.380	0.340	0.750	0.560	uA
Standby	0.290	0.290	0.255	0.230	0.075	0.068	uA
Shutdown	NA	NA	NA	NA	0.053	0.050	uA

1. *The lowest range has been used: Range 3 for STM32L0xx and Range 2 for STM32U0xx, with the highest frequency allowed for the given range.*

Table 20 shows a comparison of ULPMark scores, demonstrating better energy efficiency of STM32U0 in typical application use cases. For more information about ULPMark, go to https://www.eembc.org/ulpmark.

Table 20. ULPMark score comparison between STM32L0 and STM32U0 devices

ULPMark	STM32L06x/5x	STM32L02x/1x	STM32U08x/7x	STM32U03x
ULPMark-CP	207	244	407	430
ULPMark-PP	95	83	143	167
ULPMark-CM	-	-	19.7	20.3

6 Peripheral migration

6.1 STM32 product cross-compatibility

STM32 MCUs embed a set of peripherals that can be classified in three groups:

- The first group is for the peripherals that are common to all products. Those peripherals have the same structure, registers, and control bits. There is no need to perform any firmware changes to keep the same functionality at the application level after migration. Peripheral features and behavior remain the same across devices.
- The second group is for the peripherals that present minor differences from one product to another (usually due to the support of new features). Migrating from one product to another is very easy and does not require any significant new development effort.
- The third group is for peripherals that have been considerably modified from one product to another (new architecture or new features, for instance). For this group of peripherals, the migration requires a new development at application level.

The table below gives a general overview of this classification. The software compatibility mentioned in the table refers only to the register description for low-level drivers.

The STM32Cube hardware abstraction layer (HAL) is compatible between the STM32L0 series and the STM32U0 series.

Table 21. Peripheral compatibility analysis between STM32L0 series and STM32U0 series

<table>
<tr><th rowspan="2">Peripheral</th><th colspan="3">Number of instances in STM32</th><th colspan="3">Compatibility with STM32U0 series</th></tr>
<tr><th>STM32L0</th><th>STM32U073xx/83xx</th><th>STM32U031xx</th><th>Software</th><th>Pinout</th><th>Comments</th></tr>
<tr><td>SPI</td><td>2</td><td>3</td><td>2</td><td colspan="2" rowspan="2">Partial</td><td>• I2S is no longer supported by SPI on the STM32U0 series.
• Some alternate functions are not mapped on the same GPIO for SPI1.</td></tr>
<tr><td>I2S (full duplex)</td><td>2</td><td colspan="2">0</td></tr>
<tr><td>FIREWALL</td><td>1</td><td colspan="2">0</td><td colspan="2">NA</td><td>-</td></tr>
<tr><td>WWDG</td><td>1</td><td colspan="2">1</td><td rowspan="3">Full</td><td rowspan="4">NA</td><td rowspan="3">-</td></tr>
<tr><td>IWDG</td><td>1</td><td colspan="2">1</td></tr>
<tr><td>DBGMCU</td><td>1</td><td colspan="2">1</td></tr>
<tr><td>CRC</td><td>1</td><td colspan="2">1</td><td rowspan="4">Partial</td><td>Additional features on the STM32U0 series.</td></tr>
<tr><td>EXTI</td><td>1</td><td colspan="2">1</td><td rowspan="2">Full</td><td>-</td></tr>
<tr><td>USB FS</td><td>1</td><td>1</td><td>0</td><td>Additional features on the STM32U0 series.</td></tr>
<tr><td>DMA</td><td>1</td><td>2</td><td>1</td><td>NA</td><td>• Significant flexibility due to DMAMUX extension.
• DMA mapping request may differ (see Section 6.3: Direct memory access controller (DMA)).</td></tr>
<tr><td>TIM
Basic
General Purpose
Advanced
Low-power
IRTIM</td><td>-
2
4
0
1
0</td><td>-
2
4
1
3
1</td><td>-
2
4
1
2
1</td><td>Full</td><td>Partial</td><td>• STM32U0 brings one 32-bit timer.
• Some pins are not mapped on the same GPIO.
• Timer instance names may differ.
• Internal connections may differ.</td></tr>
<tr><td>PWR</td><td>1</td><td colspan="2">1</td><td rowspan="2">Partial</td><td rowspan="2">NA</td><td rowspan="2">-</td></tr>
<tr><td>RCC</td><td>1</td><td colspan="2">1</td></tr>
</table>

Peripheral	Number of instances in STM32			Compatibility with STM32U0 series		
	STM32L0	STM32U073xx/83xx	STM32U031xx	Software	Pinout	Comments
USART **UART** **LPUART**	Up to 4 0 1	4 0 3	4 0 2	Partial	Full	• Additional features on the STM32U0 series. • Additional LPUART on the STM32U0 series.
I2C	Up to 4	4	3	None		Additional features on the STM32U0 series.
DAC channels	2	1		Partial		• Additional features on the STM32U0 series. • Software compatible except for output buffer management.
ADC	1	1		None	Partial	• Additional features on the STM32U0 series. • Different channels are mapped on the same GPIO.
RTC	1	1		Partial	Full	• Additional features on the STM32U0 series. • Can be powered by V_{BAT} on the STM32U0 series.
FLASH	1	1		None	NA	New peripheral.
EEPROM	1	0				Emulated - refer to AN4894.
GPIO	Up to 115 IOs	Up to 69 IOs	Up to 53 IOs	Full	Partial	• Additional GPIO thanks to sharing with system pins. • A few changes, mentioned in Section 3: Hardware migration.
LCD controller	1	1	0			• VLCD muxed on PC3 GPIO. • SEG21 mapped on a different GPIO. • Integrated voltage output buffers for higher LCD driving capability
COMP	2	2	1	None		Some pins are mapped on different GPIOs.
SYSCFG	1	1		Partial	NA	-
AES	1	1 (on STM32U083xx only)	0	Full		-
OPAMP	0	1	1	None		-

6.2 Memory mapping

The peripheral address mapping has been changed in the STM32U0 series compared to theSTM32L0 series.

The table below provides the peripheral address mapping differences between the STM32L0 and STM32U0 series.

Table 22. Peripheral address mapping differences between STM32L0 and STM32U0 series

Peripheral	STM32L0 series		STM32U0	
	Bus	Base address	Bus	Base address
GPIOH	IOPORT	0x50001C00	AHB	NA
GPIOF		NA		0x50001400
GPIOE		0x50001000		0x50001000
GPIOD		0x50000C00		0x50000C00
GPIOC		0x50000800		0x50000800
GPIOB		0x50000400		0x50000400
GPIOA		0x50000000		0x50000000
CRC	AHB	0x40023000		0x40023000
FLASH		0x40022000		0x40022000
RCC		0x40021000		0x40021000
DMA1		0x40020000		0x40020000
DMA2		NA		0x40020400
DMAMUX		NA		0x40020800
AES		0x40026000	APB	0x40026000
RNG		0x40025000		0x50060800
TSC		0x40024000		0x40024000
USART1	APB2	0x40013800		0x40013800
SPI1		0x40013000		0x40013000
ADC1		0x40012400		0x40012400
EXTI		0x40010400		0x40010400
SYSCFG		0x40010000		0x40010000
COMP		0x40010000		0x40010200
OPAMP	APB1	NA		0x40007800
DAC		0x40007400		0x40007400
PWR		0x40007000		0x40007000
USB device FS SRAM		0x40006000		0x40009800
I2C3		0x40007800		0x40008800
I2C2		0x40005800		0x40005800
I2C1		0x40005400		0x40005400
USART5		0x40005000		NA
USART4		0x40004C00		0x40004C00
USART3		NA		0x40004800
USART2		0x40004400		0x40004400
LPUART1		0x40004800		0x40008000
SPI2		0x40003800		0x40003800
IWDG		0x40003000		0x40003000
WWDG		0x40002C00		0x40002C00
RTC (inc. BKP registers)		0x40002800		0x40002800
LCD		0x40002400		0x40002400

Peripheral	STM32L0 series		STM32U0	
	Bus	Base address	Bus	Base address
TIM7	APB1	0x40001400	APB	0x40001400
TIM6		0x40001000		0x40001000
TIM5		0x40000C00		NA
TIM3		0x40000400		0x40000400
TIM2		0x40000000		0x40000000
LPTIM1		0x40007C00		0x40007C00
TIM22		0x40011400		NA
TIM21		0x40010800		NA
TIM16	NA			0x40014400
TIM15				0x40014000
TIM1				0x40012C00
VREF				0x40010030
LPTIM2				0x40009400
LPTIM3				0x40009000
LPUART3				0x40008C00
LPUART2				0x40008400
CRS				0x40006C00

The system memory mapping has been updated between the STM32L0 series and STM32U0 series. Refer to the reference manuals and datasheets for more details.

The STM32U0 series features an additional SRAM (SRAM2) of the following size:

- 8 Kbytes on STM32U073xx/83xx devices.
- 4 Kbytes on STM32U031xx devices.

SRAM2 includes the additional features listed below:

- Maximum performance through I-Code bus access without physical remap.
- Parity check option (32-bit + 4-bit parity check).
- Write protection with 1 Kbyte granularity.
- Read protection (RDP).
- Erase by system reset (option byte) or by software.
- Content preserved in Low-power run, Low-power sleep, Stop 0, Stop 1, and Stop 2 modes.
- Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1).

Bit-banding

Both the STM32L0 and STM32U0 series support bit-banding on the lowest 1 Mbyte of the SRAM and on the peripheral memory region. However, the peripherals mapped in this bit-banding region are different for each series.

Detail of the peripherals that are accessible with bit-banding:

- STM32L0 series: all peripherals except AES and FSMC.
- STM32U0 series: all peripherals except GPIOx, ADC, AES, and RNG.

6.3 Direct memory access controller (DMA)

STM32U0 embeds DMAMUX, extending the capabilities of the regular DMA present in STM32L0 products. For the DMA in the STM32L0 series, each channel is dedicated by hardware connection to managing the memory access requests from one or more peripherals and has an arbiter for handling the priorities among the DMA requests.

For the STM32U0 series, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer, providing a high level of flexibility.

The DMAMUX request multiplexer allows a DMA request line to be routed between the peripherals and the DMA controllers of the product. The routing function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. Existing application software using DMA needs to be updated to integrate this new DMAMUX feature.

The table below presents the differences between the DMA requests of the peripherals in the STM32L0 series and the peripherals in the STM32U0 series.

Table 23. DMA request differences between STM32L0 and STM32U0 series

Peripheral	DMA request	STM32L0 series	STM32U0 series
ADC	ADC1	DMA1_Channel1	DMAMUX request 5
DAC	DAC1_CH1	DMA1_Channel2	DMAMUX request 8
	DAC1_CH2	DMA1_Channel4	NA
SPI1	SPI1_RX	DMA1_Channel2	DMAMUX request 36
	SPI1_TX	DMA1_Channel3	DMAMUX request 37
SPI2	SPI2_RX	DMA1_Channel4, DMA1_Channel6	DMAMUX request 38
	SPI2_TX	DMA1_Channel5, DMA1_Channel7	DMAMUX request 39
SPI3	SPI3_RX	NA	DMAMUX request 40
	SPI3_TX		DMAMUX request 41
USART1	USART1_RX	DMA1_Channel3, DMA1_Channel5	DMAMUX request 69
	USART1_TX	DMA1_Channel2, DMA1_Channel4	DMAMUX request 70
USART2	USART2_RX	DMA1_Channel5, DMA1_Channel6	DMAMUX request 71
	USART2_TX	DMA1_Channel4, DMA1_Channel7	DMAMUX request 72
USART3	USART3_RX	DMA1_Channel3	DMAMUX request 73
	USART3_TX	DMA1_Channel2	DMAMUX request 74
USART4	UART4_RX	DMA1_Channel4, DMA1_Channel6	DMAMUX request 75
	UART4_TX	DMA1_Channel3, DMA1_Channel7	DMAMUX request 76
USART5	UART5_RX	DMA1_Channel2, DMA1_Channel6	NA
	UART5_TX	DMA1_Channel3, DMA1_Channel7	
LPUART1	LPUART1_RX	DMA1_Channel3/DMA1_Channel6	DMAMUX request 30
	LPUART1_TX	DMA1_Channel2/DMA1_Channel7	DMAMUX request 31
LPUART2	LPUART2_RX	NA	DMAMUX request 32
	LPUART2_TX		DMAMUX request 33
LPUART3	LPUART3_RX		DMAMUX request 34
	LPUART3_TX		DMAMUX request 35
I2C1	I2C1_RX	DMA1_Channel3, DMA1_Channel7	DMAMUX request 9
	I2C1_TX	DMA1_Channel2, DMA1_Channel6	DMAMUX request 10
I2C2	I2C2_RX	DMA1_Channel5	DMAMUX request 11
	I2C2_TX	DMA1_Channel4	DMAMUX request 12
I2C3	I2C3_RX	DMA1_Channel3, DMA1_Channel5	DMAMUX request 13
	I2C3_TX	DMA1_Channel3, DMA1_Channel5	DMAMUX request 14
I2C4	I2C4_RX	NA	DMAMUX request 15
	I2C4_TX		DMAMUX request 16

Peripheral	DMA request	STM32L0 series	STM32U0 series
TIM1	TIM1_CH1	NA	DMAMUX request 42
	TIM1_CH2		DMAMUX request 43
	TIM1_CH3		DMAMUX request 44
	TIM1_CH4		DMAMUX request 45
	TIM1_TRIG_UP		DMAMUX request 46
	TIM1_UP		DMAMUX request 47
TIM2	TIM2_UP	DMA1_Channel2	DMAMUX request 48
	TIM2_CH1	DMA1_Channel5	DMAMUX request 49
	TIM2_CH2	DMA1_Channel3, DMA1_Channel7	DMAMUX request 50
	TIM2_CH3	DMA1_Channel1	DMAMUX request 51
	TIM2_CH4	DMA1_Channel4	DMAMUX request 52
			DMAMUX request 53
TIM3	TIM3_UP	DMA1_Channel3	DMAMUX request 54
	TIM3_CH1	DMA1_Channel5	DMAMUX request 55
	TIM3_TRIG	DMA1_Channel6	DMAMUX request 56
	TIM3_CH3	DMA1_Channel2	DMAMUX request 57
	TIM3_CH4	DMA1_Channel3	DMAMUX request 58
			DMAMUX request 59
TIM6	TIM6_UP	DMA1_Channel2	DMAMUX request 60
TIM7	TIM7_UP	DMA1_Channel4	DMAMUX request 61
TIM15	TIM15_CH1	NA	DMAMUX request 62
	TIM15_UP		DMAMUX request 63
	TIM15_TRIG		DMAMUX request 64
	TIM15_COM		DMAMUX request 65
TIM16	TIM16_CH1		
	TIM16_UP		DMAMUX request 66
	TIM16_CH1		DMAMUX request 67
	TIM16_UP		DMAMUX request 68
AES	AES_OUT	DMA2_Channel2, DMA2_Channel3	DMAMUX request 7
	AES_IN	DMA2_Channel1, DMA2_Channel5	DMAMUX request 6

6.4 Interrupts

The table below presents the interrupt vectors on the STM32U0 series compared to the STM32L0 series.

Table 24. Interrupt vector differences between STM32L0 and STM32U0 series

Position	STM32L0 series	STM32U0 series
0	WWDG	WWDG
1	PVD	PVD/PVM
2	RTC_WKUP	TAMPER/RTC
3	FLASH	FLASH/WKUP
4	RCC_CRS	RCC/CRS

Position	STM32L0 series	STM32U0 series
5	EXTI[1:0]	EXTI0_1
6	EXTI[3:2]	EXT2_3
7	EXTI[15:4]	EXTI4
8	TSC	USB
9	DMA1_Channel1	DMA1_Channel1
10	DMA1_Channel1[3:2]	DMA1_Channel2_3
11	DMA1_Channel[7:4]	DMA1_Channel4_5_6_7/ DMAMUX/DMA2_Channel1_2_3_4_5
12	ADC_COMP	ADC_COMP
13	LPTIM1	TIM1_BRK_UP_TRG_COM
14	USART4/USART5	TIM1_CC
15	TIM2	TIM2
16	TIM3	TIM3
17	TIM6_DAC	TIM6/DAC/LPTIM1
18	TIM7	TIM7/LPTIM2
19	-	TIM15/LPTIM3
20	TIM21	TIM16
21	I2C3	TSC
22	TIM22	LCD
23	I2C1	I2C1
24	I2C2	I2C2/I2C3/I2C4
25	SPI1	SPI1
26	SPI2	SPI2/SPI3
27	USART1	USART1
28	USART2	USART2/LPUART2
29	LPUART1/AES/RNG	USART3/LPUART1
30	NA	USART4/LPUART3
31	USB	AES/RNG

6.5 Reset and clock control (RCC)

The table below presents the differences related to the reset and clock controller (RCC) between the STM32L0 series and the peripherals in the STM32U0 series.

In addition to the differences described in the table above, the following additional adaptation steps may be needed for the migration:

- Performance versus V_{CORE} ranges.
- Peripheral access configuration.
- Peripheral clock configuration.

Table 25. RCC differences between STM32L0 and STM32U0 series

RCC	STM32L0 series	STM32U0 series
MSI	• Multi-speed internal RC oscillator • Frequency ranges: 65.536 kHz, 131.072 kHz, 262.144 kHz, 524.288 kHz, 1.048 MHz, 2.097 MHz (default value) and 4.194 MHz	• MSI is a low-power oscillator with programmable frequency up to 48 MHz. It can replace the PLL as system clock (faster wake-up, lower consumption). It can be used as a USB device clock (no need for an external high-speed crystal oscillator) • Multi-speed RC factory and user trimmed (100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz and 48 MHz) • Auto calibration from LSE
HSI16	• High speed internal 16 MHz RC oscillator • Factory and user trimmed	
HSI48	• High speed internal 48 MHz RC oscillator • High-precision clock for USB (CRS)	• 48 MHz RC forSTM32U0x3xx devices. • Can drive USB Full Speed and RNG.
LSI	• Low-speed internal clock • 32 Hz RC oscillator • Low-power clock	• 32 kHz RC. • Lower consumption, higher accuracy (refer to product datasheet).
HSE	• High-speed external clock • 1 to 24 MHz • From external clock or external crystal/ceramic resonator	4 to 48 MHz
LSE	• Low-speed external clock • Low-power • Configurable drive/consumption • High accuracy 32.768kHz	• 32.768 kHz • Configurable drive/consumption. • Available in backup domain (VBAT).
PLL	• One PLL with single output • PLL multiplication/division factors are different from STM32U0 series	• Main PLL for system • PLL for ADC, RNG, TIM1, TIM15, and USB FS clock • PLL provides 3 independent outputs • The PLL sources are MSI, HSI16, and HSE
System clock source	MSI, HSI16, HSE, or PLL	MSI, HSI16, HSE, PLL, LSE, or LSI.
System clock frequency	• Up to 32 MHz. • 2 MHz after reset using MSI.	• Up to 56 MHz. • 4 MHz after reset using MSI.
AHB frequency	Up to 32 MHz.	Up to 56 MHz.
APB1 frequency	Up to 32 MHz.	Up to 56 MHz (APB).
APB2 frequency	Up to 32 MHz.	Up to 56 MHz (APB).
RTC clock source	LSI, LSE, or HSE clock divided by 2, 4, 8, or 16.	LSI, LSE, or HSE/32.
MCO clock source	MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI, or HSI48. With configurable prescaler, 1, 2, 4, 8 or 16 for each output	MCO pin (multiple pins): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI, HSI48, RTCCLK, RTCWAKEUP. MCO1 and MCO2 are available. With configurable prescaler, 1, 2, 4, 8 or 16 for each output
CSS	• CSS (clock security system). • CSS on LSE.	
Internal oscillator measurement/ calibration	• LSE connected to TIM21 CH1 IC: can measure HSI or MSI with respect to LSE clock high precision.	• Mainly replacing TIM21 in the STM32L0 series by TIM15/16 in the STM32U0 series. • LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision.

RCC	STM32L0 series	STM32U0 series
		• LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision. • HSE/32 and MSI connected to TIM16 CH1 IC.
Interrupt	• CSS (linked to NMI IRQ). • LSECSS. • LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, PLLRDY (linked to RCC global IRQ).	• CSS (linked to NMI IRQ). • LSECSS. • LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, and PLLRDY (linked to RCC global IRQ).

6.5.1 Performance versus V_{CORE} ranges

On the STM32L0 series, the maximum CPU clock frequency and the flash memory wait state depend on the selected V_{CORE} voltage range and the selected V_{DD} range.

The tables below present the different clock source frequencies depending on different product voltage ranges.

Table 26. Performance versus V_{CORE} ranges for STM32L0 and STM32U0 series

WS = wait state.

CPU performance	Power performance	V_{CORE} range	Typical Value (V)	Max frequency (MHz)				V_{DD} range
				3 WS	2 WS	1 WS	0 WS	
STM32L0 series								
High	Low	1	1.8	-	-	32	16	1.71 to 3.6
Medium	Medium	2	1.5	-	-	16	8	1.65 to 3.6
Low	High	3	1.2	-	-	4.2	4.2	
STM32U0 series								
High	Medium	1	1.2	-	56	48	24	1.71 to 3.6
Medium	High	2	1.0	-	18	16	8	1.71 to 3.6

6.5.2 Peripheral access configuration

The address mapping of several peripherals has changed for the STM32U0 series compared to the STM32L0 series, so different registers need to be used to enable/disable or enter/exit the peripheral clock or from Reset mode (see table below).

Table 27. RCC registers used for peripheral access configuration for STM32L0 and STM32U0 series

Bus	Register STM32L0 series	Register STM32U0 series	Comments
AHB	RCC_AHBRSTR	RCC_AHBRSTR	Used to enter/exit the AHB peripheral from reset.
	RCC_AHBENR	RCC_AHBENR	Used to enable/disable the AHB peripheral clock.
	RCC_AHBLPENR	RCC_AHBSMENR	Used to enable/disable the AHB peripheral clock in Sleep mode.
APB	RCC_APB1RSTR	RCC_APBRSTR1 RCC_APBRSTR2	Used to enter/exit the APB1 peripheral from reset.
	RCC_APB1ENR	RCC_APBENR1 RCC_APBENR2	Used to enable/disable the APB1 peripheral clock.
	RCC_APB1LPENR	RCC_APBSMENR1 RCC_APBSMENR2	Used to enable/disable the APB1 peripheral clock in Sleep mode.

Bus	Register STM32L0 series	Register STM32U0 series	Comments
APB2	RCC_APB2RSTR	NA	Used to enter/exit the APB2 peripheral from reset.
	RCC_APB2ENR		Used to enable/disable the APB2 peripheral clock.
	RCC_APB2LPENR		Used to enable/disable the APB2 peripheral clock in Sleep mode.

The configuration to access a given peripheral requires:

- Identifying the bus to which the peripheral is connected.
- Selecting the correct register, depending on the requested action.

For example, USART1 is connected to the APB bus. To enable the USART1 clock, the RCC_APBENR2 register needs to be configured as follows with the STM32Cube HAL driver RCC API:

```
__HAL_RCC_USART1_CLK_ENABLE();
```

To disable the USART1 clock during Sleep mode (to reduce power consumption), the RCC_APBSMENR2 register needs to be configured as follows with the STM32Cube HAL driver RCC API:

```
__HAL_RCC_USART1_CLK_SLEEP_ENABLE();
```

6.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source, independent from the system clock, which is used to generate the clock required for their operations:

- **USB:**
  - On STM32L0 devices, the USB 48 MHz clock is derived from the PLL VCO clock, which must be at 96 MHz.
  - On STM32U0 devices, the USB 48 MHz clock is derived from one of the following sources:
    - The main PLL VCO (PLLUSB1CLK).
    - The MSI clock.
    - The HSI48 internal oscillator.
- **SDIO/SDMMC:**
  - On STM32L0 devices, the SDIO clock (SDIOCLK) is derived from the PLL VCO clock and is equal to PLLVCO/2.
  - On STM32U0 devices, SDIO/SDMMC is not present.
- **RTC and LCD:**
  The RTC and the LCD glass clocks share the same clock source (RTCCLK).
  On STM32L0 devices, the RTC and LCD glass clocks are derived from one of the three following sources: LSE, LSI, or HSE divided by prescaler (/2, 4, 8, 16).
  On STM32U0 devices, the RTC and the LCD glass clocks are derived from one of the three following sources: LSE clock, LSI clock, or HSE clock divided by 32. The PCLK frequency must always be greater than or equal to the RTC clock frequency.
  RTC can also be set to ultra-low-power mode by enabling the LPCAL bit to further reduce consumption.

- **ADC:**
  - On STM32L0 devices, the ADC features two clock schemes:
    - The clock for the analog circuitry: ADCCLK. This clock is always the HSI oscillator clock. A divider by 1, 2, or 4 allows the adaptation of the clock frequency to the operating conditions of the device. This configuration is done using the ADC_CCR[ADCPRE] bits. The ADC clock also depends on the voltage range V_{CORE}. When the product voltage range 3 is selected (V_{CORE} = 1.2 V), the ADC is in low speed (ADCCLK = 4 MHz, 250 Ksps).
    - The clock for the digital interface (used for the read/write access of the register). This clock is the APB2 clock. The digital interface clock is enabled/disabled through the RCC_APB2ENR register (ADC1EN bit) and there is a bit to reset the ADC through the RCC_APB2RSTR[ADCRST] bit.
  - On STM32U0 devices, the input clock of the ADCs can be selected from two different clock sources:
    - Derived (selected by software) from the system clock (SYSCLK), PLLPCLK, or HSI16. In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to bits PREC[3:0]).
    - Derived from the APB clock of the ADC bus interface, divided by a programmable factor (1, 2, or 4). In this mode, a programmable divider factor can be selected (1, 2, or 4 according to bits CKMODE[1:0]). Refer to the STM32U0 series reference manual for more details.
- **DAC:**
  On STM32U0 devices, in addition to the PCLK clock, the LSI clock is used for the sample and hold operation.
- **U(S)ARTS:**
  - On STM32L0 devices, the U(S)ART clock is the APB1 or APB2 clock, depending on which APB bus is mapped to the U(S)ART.
  - On STM32U0 devices, the USART clock is derived from one of the four following sources: system clock (SYSCLK), HSI16, LSE, or APB.
    Using a source-clock independent from the system clock (like HSI16) allows an on-the-fly change of the system clock without reconfiguration of the USART peripheral baud rate prescalers.
- **I2Cs:**
  - On STM32L0 devices, the I2C clock is the APB1 clock (PCLK1).
  - On STM32U0 devices, the I2C clock is derived from one of the three following sources: system clock (SYSCLK), HSI16, or APB (PCLK).
    Using a source-clock independent from the system clock (like HSI16) allows an on-the-fly change of the system clock without reconfiguration of the I²C peripheral timing register.
- **I2S:**
  - On STM32L0 devices, the I2S clocks are derived from one of the three following sources: HSI16, HSE, or PLL.
  - On STM32U0 devices, I2S is not present.

6.6 Power control (PWR)

The PWR controller for STM32U0 devices presents some differences compared to the STM32L0 series, which are summarized in the table below.

Table 28. PWR differences between STM32L0 and STM32U0 series

PWR	STM32L0	STM32U0
Power supplies	• V_{DD} = 1.8 V at power-on, 1.65 V at power-down, and 3.6 V when BOR is available. • V_{DD} = 1.65 to 3.6 V when BOR is not available. • V_{DD} is the external power supply for I/Os and the internal regulator. • It is provided externally through VDD pins.	• V_{DD} = 1.71 to 3.6 V: external power supply for I/Os and internal regulator. • It is provided externally through VDD pins.
	• V_{CORE} = 1.2 to 1.8 V.	• V_{CORE} = 1.0 to 1.28 V.

PWR	STM32L0	STM32U0
Power supplies	• V_{CORE} is the power supply for the digital peripherals, SRAM, and flash memory. • It is generated by an internal voltage regulator. • Three V_{CORE} ranges can be selected by software depending on the V_{DD} and target frequency.	• V_{CORE} is the power supply for the digital peripherals, SRAM, and flash memory. • It is generated by an internal voltage regulator. • Two V_{CORE} ranges can be selected by software depending on the target frequency.
	V_{DD} and V_{DDA} must be at the same voltage value.	Independent power supplies (V_{DDA}, V_{DDUSB}) allow the improvement of power consumption by running the MCU at a lower supply voltage than analog and USB.
	• V_{SSA}, V_{DDA} = 1.8 V at power-on, 1.65 V at power-down, and 3.6 V when BOR is available. • V_{SSA}, V_{DDA} = 1.65 to 3.6 V when BOR is not available. • V_{DDA} is the external analog power supply for ADC, DAC, reset blocks, RC oscillators, and PLL. • The minimum voltage to be applied to V_{DDA} is 1.8 V when the ADC is used • V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS} respectively.	• V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DAC/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V • V_{DDA} is the external analog power supply for the A/D and D/A converters, voltage reference buffer, operational amplifiers, and comparators. • The V_{DDA} voltage level is independent from the V_{DD} voltage.
	• V_{LCD} = 2.5 to 3.6 V • The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.	• V_{LCD} = 2.5 to 3.6 V. • The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.
	NA	• V_{DDUSB} = 3.0 to 3.6 V. • V_{DDUSB} is the external independent power supply for the USB transceivers. • The V_{DDUSB} voltage level is independent from the V_{DD} voltage.
Battery backup domain		• V_{BAT} = 1.55 to 3.6 V: the power supply for the RTC external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present. • RTC with backup registers (up to 9 bytes). • LSE. • PC13 to PC15 I/Os. • Up to 5 tamper pins.
Power supply supervisor	• Integrated POR/PDR circuitry. • Programmable voltage detector (PVD).	
	• Brownout reset (BOR). • BOR can be disabled after power-on.	• Brownout reset (BOR). • BOR is always enabled, except in Shutdown mode.
	NA	3 peripheral voltage monitoring (PVM): • PVM1 for V_{DDUSB}. • PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V).
Low-power modes	Sleep mode	
	• Low-power run mode (up to 131 kHz.) • Low-power sleep mode (up to 131 kHz.)	• Low-power run mode (up to 2 MHz.) • Low-power sleep mode (up to 2 MHz). • The system clock is limited to 2 MHz, but I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz.

PWR	STM32L0	STM32U0
Low-power modes	Stop mode.	• Stop 0, Stop 1, and Stop 2 mode. • Some additional functional peripherals (cf. wake-up source).
	Standby mode. (V_{CORE} domain powered off).	Standby mode (V_{CORE} domain powered off) with new features: • BOR is always ON. • SRAM2 content can be preserved. • Pull-up or pull-down can be applied to each I/O.
	NA	Shutdown mode (V_{CORE} domain powered off and power monitoring off).
Wake-up sources	Sleep mode Any peripheral interrupt/wakeup event.	
	Stop mode • Any EXTI line event/interrupt. • BOR, PVD, COMP, RTC, USB, IWDG.	Stop mode • Any EXTI line event/interrupt. • BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD.
	Standby mode • 3 WKUP pins rising edge. • RTC event. • External reset in NRST pin. • IWDG reset.	Standby mode • Up to 5 WKUP pins rising or falling edge. • RTC event. • External reset in NRST pin. • IWDG reset.
	NA	Shutdown mode • Up to 5 WKUP pins rising or falling edge. • RTC event; • External reset in NRST pin.
Wake-up clocks	Wake-up from Stop mode MSI (all ranges up to 4.1 MHz).	Wake-up from Stop mode HSI16 16 MHz or MSI (all ranges up to 48 MHz) allow a 5-µs wake-up at high speed without waiting for the PLL startup time.
	Wake-up from Standby mode MSI 2.097 MHz.	Wake-up from Standby mode MSI (ranges from 1 to 8 MHz)
	NA	Wake-up from Shutdown mode MSI 4 MHz.
Configuration	NA	• On STM32U0 devices, the registers are different: from 2 registers in the STM32L0 series to up to 25 registers in the STM32U0 series. – 4 control registers. – 2 status registers. – 1 status clear register. – 2 registers per GPIO port for controlling pull-up and pull-down. • Most configuration bits from the STM32L0 series can be found in the STM32U0 series (but some may have a different programming mode).

6.7 Real-time clock (RTC)

The STM32U0 and STM32L0 series implement almost identical RTC features. The table below summarizes the differences.

Table 29. RTC differences between STM32L0 and STM32U0 series

RTC	STM32L0 series	STM32U0 series
Features	• Coarse digital calibration (kept for compatibility only). • New developments must only use smooth calibration.	• Only smooth calibration available. • Ultra-low-power calibration saving further consumption is available when the LPCAL bit is set.
	-	5 tamper pins (available in VBAT).
	5 backup registers.	Up to 9 backup registers.
Configuration	-	• Additional bit LPCAL for drastic reduction of RTC consumption. • Backup domain reset as RTC is connected to VBAT. • Modified register memory map.

For more information about the RTC features of the STM32U0 series, refer to the RTC section of the STM32U0 series reference manual.

6.8 System configuration controller (SYSCFG)

The STM32U0 and STM32L0 series implement almost identical SYSCFG features. The table below summarizes the differences.

Table 30. SYSCFG differences between STM32L0 and STM32U0 series

SYSCFG	STM32L0 series	STM32U0 series
SYSCFG features	• Remapping memory areas. • Managing the external interrupt line connection to the GPIOs. • Configuring the USB pull-up resistor.	• Remapping memory areas. • Managing the external interrupt line connection to the GPIOs. • Robustness management. • Configuring SRAM2 write protection and software erase. • Enabling/disabling voltage booster for I/Os analog switches. • Enabling/disabling I2C fast mode plus driving capability is now controlled by I2C directly. Registers in SYSCFG have been kept for legacy reasons.
Configuration	-	• Most registers from the STM32L0 series are identical in the STM32U0 series. • A few bits are different and EXTI configuration may differ (number of GPIOs is different depending on the product).

6.9 General-purpose I/O (GPIO) interface

The GPIO peripheral of the STM32U0 series embeds identical features compared to the one present on the STM32L0 series.

Minor adaptations of the code written for the the STM32L0 series using the GPIO may be required on the STM32U0 due to:

- The mapping of specific functions on different GPIOs (see pinout differences in Section 3: Hardware migration.
- Alternate function selection differences (AFSELy[3:0] in the GPIOx_AFRL and GPIOx_AFRH registers).
- The additional mapping of GPIOs sharing pins with BOOT and NRST to provide more GPIOs in the same package.

The main GPIO features are:

- GPIO mapped on the AHB bus for better performance and accessibility by DMA.
- I/O pin multiplexer and mapping: the pins are connected to on-chip peripherals/modules through a multiplexer that allows only one peripheral alternate function (AF) to connect to an I/O pin at a time. In this way, no conflict can occur between peripherals sharing the same I/O pin.
- More possibilities and features for I/O configuration.

For more information on the STM32U0 series GPIO programming and usage, refer to the *I/O pin multiplexer and mapping* section in the GPIO chapter of the STM32U0 series reference manual. For a detailed description of the pinout and alternate function mapping, refer to the product datasheets.

6.10 Extended interrupt and event controller (EXTI) source selection

The external interrupt and event controller (EXTI) is very similar in the STM32U0 and STM32L0 series. The table below shows the main differences.

Table 31. EXTI differences between STM32L0 and STM32U0 series

EXTI	STM32L0 series	STM32U0 series
Number of event/interrupt lines	Up to 24 lines	Up to 37 lines: • 16 direct • 22 configurable
Configuration	-	The selection of the EXTI line source is performed through the EXTIx bits in the SYSCFG_EXTICRx registers (in the STM32L0 and STM32U0 series). However, the mapping of the EXTICRx registers has been changed.

6.11 Flash memory

The STM32U0 and STM32L0 series instantiate different flash memory modules, both in terms of architecture/ technology and interface. Consequently, the STM32U0 series flash memory programming procedures and registers are different from those in the STM32L0 series, and any code written for the flash memory interface in the STM32L0 series needs to be rewritten to run on STM32U0 devices.

An additional difference that might impact application porting is the opposite default memory state after erase: it is 0x00 for STM32L0, but STM32U0 returns 0xFF for erased memory.

The table below presents the differences between the flash memory interface in the STM32L0 and STM32U0 series.

For more information on programming, erasing, and protection of the STM32U0 series flash memory, refer to the STM32U0 series reference manuals.

Table 32. Flash memory differences between STM32L0 and STM32U0 series

Flash	STM32L0 series	STM32U0 series
Main/Program memory	0x0800 0000 to (up to) 0x0805 FFFF	0x0800 0000 to (up to) 0x0803 FFFF
	• Up to 192 Kbytes. • 1 or 2 banks. • Each bank: up to 256 Kbytes. • Sector size = 4 Kbytes: 32 pages of 128 bytes. • Programming granularity: 32-bit. • Read granularity: 64/32-bit.	• STM32U0x3xx: – Up to 256 Kbytes. – 1 bank. – 128 pages of 2 Kbytes. – Each page: 8 rows of 256 Kbytes. • STM32U031xx: – Up to 64 Kbytes. – 1 bank. – 32 pages of 2 Kbytes. – Each page: 8 rows of 256 bytes. • Programming and read granularity: 72-bit (incl 8 ECC bits).
Features	• Read while write (RWW). • Dual bank boot. • ECC (data EEPROM only).	• Read while write (RWW).
	NA	• ECC. • Flash empty check.
	Default memory value after erase: 0x00	Default memory value after erase: 0xFF
Wait state	Up to 1 (depending on the supply voltage and frequency).	Up to 2 (depending on the core voltage and frequency).
ART Accelerator™	NA	Allowing 0 wait state when executing from the cache.
Data EEPROM memory	Up to 6 Kbytes in 1 or 2 banks.	N/A Can be emulated by software. For more details, refer to the application note *How to use EEPROM emulation on STM32 MCUs* (AN4894), available from http://www.st.com.
System memory	Up to 8 Kbytes	• 26 Kbytes 0x1FFF 0000 to 0x1FFF 67FF.
One time programmable (OTP)	NA	1 Kbyte 0x1FFF 6800 to 0x1FFF 6BFF.
Option bytes	96 factory bytes + 32 user bytes	Improved programming method with no direct access to the option byte storage area.
Flash memory interface	0x4002 3C00 to 0x4002 3FFF.	0x4002 2000 to 0x4002 23FF.
	-	Different from STM32L0 series.
Erase granularity	• Program memory Mass/page (256 bytes). • DATA EEPROM memory: Byte/half-word/word/double-word.	Page erase (2 Kbytes), bank erase, and mass erase (all banks).
Read protection (RDP)	• Level 0 no protection. • RDP = 0xAA.	• Level 0 no protection. • RDP = 0xAA.
	• Level 1 memory protection. • RDP ≠ (level 2 & level 0).	• Level 1 memory protection. • RDP ≠ (level 2 & level 0).
	• Level 2 RDP = 0xCC.	• Level 2 RDP = 0xCC.
	-	Improved protection scheme with OEM keys allowing the secure regression of protection levels.
Proprietary code readout protection (PCROP)	Granularity: 1 sector (4 Kbytes).	-

Flash	STM32L0 series	STM32U0 series
Write protection (WRP)	Granularity: 1 sector (4 Kbytes).	• Two write protection areas: • Granularity: 2 Kbytes.
User option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	NA	nRST_SHDW
	IWDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
		WWDG_SW
	NA	NOT_VBAT_VDD_OPT
		RAM_PARITY_CHECK
		BKPSRAM_HW_ERASE_DISABLE
		IRHEN, NRST_MODE[1:0]
	BOR_LEV[3:0]	BOR_LEV[2:0]
	nBFB2	BOOT_LOCK
	NA	nBOOT1
		nBOOT0
		nBOOT_SEL

6.12 Universal synchronous asynchronous receiver transmitter (U(S)ART)

The STM32U0 series implement several new features on USART compared to the STM32L0 series. The table below shows the differences.

Table 33. U(S)ART differences between STM32L0 and STM32U0 series

U(S)ART	STM32L0 series	STM32U0 series
Instances	• x5 USART • x1 LPUART	• x4 USART • x3 LPUART
Baud rate	Up to 4 Mbit/s when the clock frequency is 32 MHz and oversampling is by 8	Up to 6 Mbit/s when the clock frequency is 48 MHz and oversampling is by 8
Clock	Single clock domain	Dual clock domain allowing: • UART functionality and wake-up from Stop mode • Convenient baud rate programming independent from the PCLK reprogramming
Data	Word length: programmable (8 or 9 bits)	• Word length: programmable (7, 8, or 9 bits) • Programmable data order with MSB-first or LSB-first shifting
Interrupt	10 interrupt sources with flags	14 interrupt sources with flags
Features	• RS232 hardware flow control (CTS/RTS) • Continuous communication using DMA • Multiprocessor communication • Single-wire half-duplex communication • IrDA SIR ENDEC block • LIN mode • SPI master	
	• Smartcard mode T = 0 and T = 1 is to be implemented by software	Smartcard mode not supported

U(S)ART	STM32L0 series	STM32U0 series
Features	• Number of stop bits: 0.5, 1, 1.5, 2	
Features	NA	• Wake-up from Stop mode (start bit, received byte, address match) • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable Tx/Rx pin configuration • LPUART does not support synchronous mode (SPI master), smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt, or auto baud rate detection
Configuration	NA	STM32L0 registers and associated bits are not identical in the STM32U0 series Refer to the STM32U0 series reference manuals for details

6.13 Inter-integrated circuit (I2C) interface

The STM32L0 series implement a different I2C peripheral, which allows for easier software management. The table below shows the differences.

Table 34. I2C differences between STM32L0 and STM32U0 series

I2C	STM32L0 series	STM32U0 series
Instances	x2 (I2C1, I2C2)	• x3 for STM32U0x3xx. • x2 for STM32U031xx.
Features	• 7-bit and 10-bit addressing mode. • Standard mode (Sm, up to 100 KHz). • Fast mode (Fm, up to 400 KHz).	
	NA	• Fast mode Plus (Fm+, up to 1 MHz). • Independent clock. • Wakeup from stop on address match.
	• SMBus	NA
Configuration	NA	Register configuration is very different in the STM32U0 series. Refer to the STM32U0 series reference manuals for details.

6.14 Serial peripheral interface (SPI)/Inter-IC sound (I2S)

The STM32U0 and STM32L0 series implement near-identical SPI features. The table below highlights the differences.

Table 35. SPI differences between STM32L0 and STM32U0 series

SPI	STM32L0 series	STM32U0 series
Instances	• SPI1 without I2S support • SPI2 with I2S support	3 without I2S support
Features	SPI + I2S	I2S is not supported by SPI on STM32U0 devices.
Data size	Fixed, configurable to 8 or 16 bits.	Programmable from 4 to 16 bits.
Data buffer	NA	32-bit Tx & Rx FIFOs (up to 4 data frames)

SPI	STM32L0 series	STM32U0 series
Data packing	NA	Yes (8-, 16-, or 32-bit data access, programmable FIFO data thresholds)
Mode	• SPI TI mode • SPI Motorola mode	• SPI TI mode • SPI Motorola mode • NSSP mode
Speed	16 MHz (core at 32 MHz)	24 MHz (core at 48 MHz)
Configuration	NA	The data size and Tx/Rx flow handling are different in the STM32L0 and STM32U0 series, requiring different software sequences.

As shown in Table 35. SPI differences between STM32L0 and STM32U0 series, no I2S is implemented on STM32U0.

6.15 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit is very similar in STM32L0 and STM32U0 devices.

The table below shows the differences.

Table 36. CRC differences between STM32L0 and STM32U0 series

CRC	STM32L0 series	STM32U0 series
Features	• Single input/output 32-bit data register. • CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size. • General-purpose 8-bit register (can be used for temporary storage).	
	• Uses CRC-32 (Ethernet) polynomial: 0x4C11DB7. • Handles 32-bit data size.	• Fully programmable polynomial with programmable size (7, 8, 16, or 32 bits). • Handles 8-, 16-, and 32-bit data sizes. • Programmable CRC initial value. • Input buffer to avoid bus stall during calculation. • Reversibility option on I/O data.
Configuration	NA	Configuration registers in theSTM32L0 series are identical in the STM32U0 series. The STM32U0 series includes additional registers for new features. Refer to the reference manuals for details

6.16 Advanced encryption standard hardware accelerator (AES)

The STM32U0 series implement several new AES features compared to the STM32L0 series. The table below shows the differences.

Table 37. AES differences between STM32L0 and STM32U0 series

AES	STM32L0 series	STM32U0 series
Features	128-bit register for storing the encryption, or derivation key (4x 32-bit registers).	256-bit register for storing the encryption, decryption, or derivation key (8x 32-bit registers).
Mode	• Electronic codebook (ECB). • Cipher block chaining (CBC). • Counter mode (CTR).	• Electronic codebook (ECB). • Cipher block chaining (CBC). • Counter mode (CTR). • Galois counter mode (GCM). • Galois message authentication code mode (GMAC). • Cipher message authentication code mode (CMAC).
Key length	128-bit	128-bit, 256-bit
Configuration	NA	All registers and programming bits in the STM32L0 series can be found in the STM32U0 series.

6.17 Liquid-crystal display controller (LCD)

The LCD controller on the STM32U0 series implements the same features as the one on the STM32L0 series, except for an additional internal output buffer that allows for improved contrast. It is possible to use the output buffers instead of the high-drive resistive network.

All programmable registers and associated bits in the STM32L0 series are equivalent to the ones in the STM32U0 series. However, due to the fact that the VLCD pin is implemented as an alternate function in Sthe STM32U0 series (contrary to the STM32L0 series), a specific software sequence is required to configure the LCD controller when the step-up converter is used as the power source.

Refer to the STM32L0 and STM32U0 series reference manuals for more details.

Note: LCD is not available on STM32U031xx devices.

6.18 Universal serial bus interface (USB)

The STM32L0 and STM32U0 series implement similar USB peripherals: they both contain a USB FS device interface.

STM32U0x3xx devices include a clock recovery system (CRS) as an additional feature. It provides a precise clock to the USB peripheral:

- When using USB device mode, the CRS allows crystal-less USB operation.
- When using USB host mode, the CRS allows low-frequency crystal (32.768 KHz) USB operations.

Most features supported by the STM32L0 series are also supported by STM32U0x3xx devices . The table below highlights the key differences.

Table 38. USB differences between STM32L0 and STM32U0 series

USB	STM32L0 series	STM32U0x3xx devices
Features	Universal Serial Bus Revision 2.0.	Universal Serial Bus Revision 2.0, including link power management (LPM) support.
	FS mode: • 1 bidirectional control endpoint. • 7 IN endpoints. (Bulk, Interrupt, Isochronous.) • 7 OUT endpoints (Bulk, Interrupt, Isochronous.)	

USB	STM32L0 series	STM32U0x3xx devices
Features	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D+ (USB_DP) line.	
	NA	CRS allows crystal-less USB operation. Independent V_{DDUSB} power supply, allowing a lower V_{DD} while using USB.
Mapping	APB1	APB
Buffer memory	1024 bytes (endpoint buffers and buffer descriptors structure.)	1024 bytes of dedicated packet buffer memory SRAM.
Low-power modes	USB suspend and resume.	• USB suspend and resume. • Link power management (LPM) support.
Configuration	NA	STM32U0 registers are different. Refer to the STM32U0 reference manuals for details.

6.19 Analog-to-digital converter (ADC)

The main ADC differences between the STM32L0 and STM32U0 series are a new digital interface and architecture. The table below presents the different features.

Table 39. ADC differences between STM32L0 and STM32U0 series

ADC	STM32L0 series		STM32U0 series	
ADC type	SAR structure			
Instances	ADC1		ADC	
Maximum sampling frequency	1.14 Msps		2.5 Msps	
Number of channels	Up to 19 channels		Up to 19 channels	
Resolution	12-bit		12-bit + digital oversampling up to 16-bit	
Conversion modes	Single/continuous/scan/ discontinuous/dual mode		Single/continuous/scan/discontinuous	
DMA	Yes			
External trigger	Yes			
	External event for regular group	External event for injected group	External event for regular group:	External event for injected group:
	TIM6_TRGO	TIM6_TRGO	TIM1_TRGO2	TIM1_TRGO2
	TIM21_CH2	TIM21_CH2	TIM1_CC4	TIM1_CC4
	TIM2_TRGO	TIM2_TRGO	TIM2_TRGO	TIM2_TRGO
	TIM2_CH4	TIM2_CH4	TIM3_TRGO	TIM3_TRGO
	TIM22_TRGO	TIM22_TRGO	TIM15_TRGO	TIM15_TRGO
	TIM2_CH3	TIM2_CH3	TIM6_TRGO	TIM6_TRGO
	TIM3_TRGO	TIM3_TRGO	EXTI11	EXTI11
	EXTI11	EXTI11		
Supply requirement	1.8 V to 3.6 V.		• 1.62 V to 3.6 V. • Independent power supply (V_{DDA}).	
Reference voltage	External		Reference voltage for STM32U0 series external (2.0 V to V_{DDA}) or internal (2.048 V or 2.5 V).	
Electrical parameters	1.45 mA (max.), 1.0 mA (typ.).		Consumption proportional to conversion speed: 200 uA/Msps (Typ.).	

ADC	STM32L0 series	STM32U0 series
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	

6.20 Digital-to-analog converter (DAC)

The STM32U0 series implement an enhanced DAC compared to the STM32L0 series. The table below shows the differences.

Table 40. DAC differences between STM32L0 and STM32U0 series

DAC	STM32L0 series	STM32U0 series
Number of channels	• 1 on STM32L05xx/STM32L06xx • 2 on STM32L07xx/STM32L08xx • No DAC for other devices.	1
Resolution	12-bit	
Features	• Left or right data alignment in 12-bit mode • Noise-wave and triangular-wave generation	
	• DAC with 2 channels for independent or simultaneous conversions	• DAC with 1 channel only • Buffer offset calibration • DAC1_OUTx can be disconnected from output pin • Sample and hold mode for low-power operation in Stop mode
DMA	Yes	
External trigger	Yes	
	• TIM6_TRGO event • TIM3_TRGO event • TIM3_CH3 event • TIM21_TRGO event • TIM2_TRGO event • TIM7_TRGO event • EXTI line9 • SWTRIG	• TIM1_TRGO_CKTIM • TIM2_TRGO_CKTIM • TIM3_TRGO_CKTIM • TIM6_TRGO_CKTIM • TIM7_TRGO_CKTIM • TIM15_TRGO_CKTIM • LPTIM1_OUT • LPTMI2_OUT • EXTI line9 • SW TRIG
Supply requirement	1.8 V to 3.6 V.	• 1.8 V to 3.6 V. • Independent power supply (V_{DDA}).
Reference voltage	External	Reference voltage for STM32U0 series external (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V).
Configuration	NA	Software compatible except for output buffer management.

6.21 Comparators (COMP)

The table below presents the differences in the COMP interface of the STM32L0 and STM32U0 series.

Table 41. COMP differences between STM32L0 and STM32U0 series

COMP	STM32L0 series	STM32U0 series
Type	• COMP1 • COMP2 rail-to-rail	• COMP1 • COMP2 rail-to-rail
Inputs	COMP1: • Non inverting: 6 (PA1, PA3, PB4, PA5 (DAC2), PB6, PB7) • Inverting: 4 (V_{REFINT}, PA0, DAC Channel1 (PA4), DAC Channel2 (PA5))	COMP1: • Non inverting: 4 (PA6, PB2, PC5, PC6) • Inverting: 8 (PA0, PA1, PA4, PA5, PC4, PB1, DAC1_OUT1/2, V_{REFINT} x 1, 3/4, 1/2, 1/4)
	COMP2: • Non inverting: 5 (PA3, PB4, PA5 (DAC2), PB6, PB7) • Inverting: PA2 , DAC Channel1 (PA4), DAC Channel2 (PA5), PB3, V_{REFINT} x 1, ¼, ¼ , ½, ¾	COMP2: • Non inverting: 4 (PA3, PB4, PB6, PD10) • Inverting: 8 (PA2, PA4, PA5, PB3, PB7, DAC1_OUT1/2, V_{REFINT} x 1, ¾, ½, ¼)
Outputs	• Generation of input capture and OCREF clear signals for timers. • Generation of wakeup interrupt or events (EXTI line).	• Generation of break input signals for timers through GPIO alternate function. • Generation of wakeup interrupt or events (EXTI line).
Features	Window comparator	
	NA	• Output with blanking source. • Programmable hysteresis.
	Programmable speed/consumption (COMP2).	Programmable speed/consumption (COMP1/ COMP2).
Supply requirement	1.65 V to 3.6 V.	1.62 V to 3.6 V.
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	

6.22 Operational amplifiers (OPAMP)

Contrary to the STM32L0 series, STM32U0 devices implement OPAMPs. The table below shows the available features.

Table 42. OPAMP features on series

OPAMP	STM32U0 series
Instances	1
Features	• Rail-to-rail input and output voltage range. • Low input bias current. • Low input offset voltage. • Low-power mode. • Fast wakeup time. • Gain bandwidth of 1 MHz. • Programmable gain amplifier (PGA).

7 Software migration

7.1 Reference documents

- The Definitive Guide to Arm® Cortex®-M0 and Cortex®-M0+ processors.
- *STM32 Cortex®-M0+ MCUs programming manual* (PM0223).
- Cortex®-M0+ Technical Reference Manual, available from infocenter.arm.com.

7.2 STM32 Cortex®-M0+ processor and core peripherals

The Cortex®-M0+ processor is an entry-level 32-bit Arm® Cortex® processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- A simple architecture that is easy to learn and program.
- Ultra-low power, energy-efficient operation.
- Excellent code density.
- Deterministic, high-performance interrupt handling.
- Upward compatibility with Cortex®-M processor family.
- Platform security robustness, with optional integrated memory protection unit (MPU).

The Cortex®-M0+ processor is built on a 32-bit processor core that is highly optimized for area and power, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex®-M0+ processor implements the ARMv6-M architecture, which is based on the 16-bit Thumb® instruction set and includes Thumb-2 technology. This provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

The Cortex®-M0+ processor closely integrates a configurable nested vectored interrupt controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- Includes a non-maskable interrupt (NMI).
- Provides zero jitter interrupt option.
- Provides four interrupt priority levels.

The tight integration of the processor core and NVIC provides fast execution of interrupt service routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes that include a deep-sleep function that enables the entire device to be rapidly powered down.

7.3 Cortex mapping overview

Except for the floating point unit, the mapping is similar on the Cortex®-M3 and Cortex®-M0+ processors. The table below summarizes the differences.

Table 43. Cortex mapping overview for STM32L0 and STM32U0 series

Cortex		STM32L0 series	STM32U0 series
Core	Architecture	Cortex®-M0+	
	Nested vectored interrupt controller (NVIC)	39 interrupt channels	32 maskable interrupt channels
	Extended interrupts and events controller (EXTI)	Up to 30 event/interrupt	Up to 38 event/interrupt
Mapping	System timer	0xE000 E010 to 0xE000 E01F	0xE000 E010 to 0xE000 E01F
	Nested vectored interrupt controller	0xE000E100 to 0xE000E4EF	0xE000E100 to 0xE000E4EF
	System control block	0xE000 ED00 to 0xE000 ED3F	0xE000 ED00 to 0xE000 ED3F
	Floating point unit coprocessor access control	NA	
	Memory protection unit	0xE000 ED90 to 0xE000 EDB8	0xE000 ED90 to 0xE000 EDB8
	Nested vectored interrupt controller	0xE000 EF00 to 0xE000 EF03	0xE000 EF00 to 0xE000 EF03
	Floating point unit	NA	

7.4 Security improvements

STM32U0 brings significant improvements in the security domain, like robust read-out protection (RDP) with three protections level states, password-based regression (128-bit PSWD), hardware protection feature (HDP), and more. The application note *Introduction to STM32 microcontrollers security* (AN5156) provides detailed descriptions of these features.

Revision history

Table 44. **Document revision history**

Date	Version	Changes
18-Mar-2024	1	Initial release.
22-Mar-2024	2	Updated: • Section Introduction • Section 1: STM32U0 series overview • Section 2: STM32L0 series overview • Table 6. Available packages for the STM32L0 series • Section 3.2: Pin compatibility • Table 7. Pinout comparison of STM32L0 and STM32U0 TSSOP20 packages • Section 3.2.2: Pinout differences between STM32L0 and STM32U0 QFP packages • Section 3.2.3: Ballout differences between STM32L0 and STM32U0 BGA packages • Section 3.3: Recommendations for board migration • Section 4: Boot mode selection • Section 5.2: Low-power modes in the STM32U0 series • Table 21. Peripheral compatibility analysis between STM32L0 series and STM32U0 series • Section 6.3: Direct memory access controller (DMA) • Section 6.5.3: Peripheral clock configuration • Section 6.6: Power control (PWR) • Table 29. RTC differences between STM32L0 and STM32U0 series • Section 6.8: System configuration controller (SYSCFG) • Section 6.11: Flash memory • Table 35. SPI differences between STM32L0 and STM32U0 series • Section 6.18: Universal serial bus interface (USB) • Table 39. ADC differences between STM32L0 and STM32U0 series • Table 41. COMP differences between STM32L0 and STM32U0 series • Table 42. OPAMP features on series Added Section 5.3: Consumption and performance overview

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