AN6099

Application note

Migrating from STM32L4 to STM32U0 MCUs

Introduction

For designers of STM32 microcontroller applications, being able to replace one microcontroller type with another from the same product family easily is an important asset. Migrating an application to a different microcontroller is often needed when product requirements grow, putting extra demands on memory size, or increasing the number of I/Os. The cost reduction objectives may also be an argument to switch to smaller components and shrink the PCB area.

This application note analyzes the steps required to migrate an existing design from the STM32L4 series to the STM32U0 series. Three aspects need to be considered for the migration: hardware, peripherals, and firmware.

This document lists the full set of features available for the STM32L4 series and the equivalent features on the STM32U0 series (some products may have fewer features depending on their part number).

To benefit fully from this application note, the user must be familiar with the STM32 microcontroller documentation available on www.st.com, with a particular focus on the documents listed in STM32L4 and STM32U0 documentation.

1 General information

This document applies to STM32L4 and STM32U0 devices, which are based on Arm® Cortex®-M cores.

Note: Arm and Cortex are registered trademarks of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

1.1 Reference documents

STM32L4 and STM32U0 documentation

- STM32L4 series datasheets
- STM32U0 series datasheets:
  - STM32U031x4/6/8: *Ultra-low-power Arm® Cortex®-M0+ 32-bit MCU, up to 64-Kbyte flash memory, 12-Kbyte SRAM* (DS14581)
  - STM32U073x8/B/C: *Ultra-low-power Arm® Cortex®-M0+ 32-bit MCU, up to 256-Kbyte flash memory, 40-Kbyte SRAM*, USB, LCD (DS14548)
  - STM32U083xC: *Ultra-low-power Arm® Cortex®-M0+ 32-bit MCU, 256-Kbyte flash memory, 40- Kbyte SRAM, USB, LCD, AES* (DS14463)
- STM32L4 series reference manuals:
  - *STM32L41xxx/42xxx/43xxx/44xxx/45xxx/46xxx advanced Arm®-based 32-bit MCUs* (RM0394)
  - *STM32L47xxx, STM32L48xxx, STM32L49xxx and STM32L4Axxx advanced Arm®-based 32-bit MCUs* (RM0351)
- STM32U0 reference manual: *STM32U0 series advanced Arm®-based 32-bit MCUs* (RM0503)

These documents are all available from www.st.com.

Arm® Cortex®-M0 and Cortex®-M4 documentation

- The Definitive Guide to Arm® Cortex®-M0 and Cortex®-M0+ processors
- The Definitive Guide to Arm® Cortex®-M3 and Cortex®-M4 processors
- *STM32 Cortex®-M4 MCUs and MPUs programming manual* (PM0214, available from www.st.com)
- *STM32 Cortex®-M0+ MCUs programming manual* (PM0223, available from www.st.com)
- Cortex®-M0+ Technical Reference Manual, available from infocenter.arm.com
- Cortex®-M4 Technical Reference Manual, available from infocenter.arm.com

2 STM32U0 series overview

The STM32U0 series devices are a perfect fit in terms of ultra-low power, performance, memory size, and peripherals at a cost-effective price.

In particular, STM32U0 series devices offer higher frequency and performance operations than STM32L4 series devices. The STM32U0 series features an Arm® Cortex®-M0+ processor at 56 MHz, versus a Cortex®-M0+ processor at 32 MHz featured on the STM32L4 series. STM32U0 devices also feature optimized flash memory access through the adaptive real-time memory accelerator (ART accelerator).

STM32U0 series MCUs increase the low-power efficiency in dynamic mode (µA/MHz), and reach a very low level of static power consumption on the various available low-power modes.

The detailed list of available features and packages for each product is available in the respective datasheets.

STM32U0 series devices include a larger set of peripherals with advanced features compared to the STM32L4 series, such as:

- Touch sensing controller (TSC)
- Low-power universal asynchronous receiver transmitter (LPUART)
- Infrared interface (IRTIM)
- Low-power timer (LPTIM)
- Voltage reference buffer (VREFBUF)
- DMA request multiplexer (DMAMUX)
- Clock recovery system (CRS) for USB
- SRAM1 size is different on the various STM32U0 devices:
  - 32 Kbytes for STM32U0x3
  - 8 Kbytes for STM32U0x1
- Additional SRAM2 with data preservation in Standby mode:
  - 8 Kbytes for STM32U0x3
  - 4 Kbytes for STM32U0x1
- Optimized power consumption and an enriched set of low-power modes

This migration guide covers only the migration from the STM32L4 series to the STM32U0 series, and as a consequence any new features present on the STM32U0 series but not already present on the STM32L4 series are not covered by this document. Refer to the STM32U0 reference manuals and datasheets for more details.

Table 1. STM32U0 memory availability

Part number	Flash memory size	SRAM1	SRAM2	Feature level
STM32U031x4	16 Kbytes	8 Kbytes	4 Kbytes	-
STM32U031x6	32 Kbytes			
STM32U031x8	64 Kbytes			
STM32U073x8	64 Kbytes	32 Kbytes	8 Kbytes	With LCD + USB
STM32U083x8				STM32U073 + AES cryptography
STM32U073xB	128 Kbytes			With LCD + USB
STM32U083xB				STM32U073 + AES cryptography
STM32U073xC	256 Kbytes			With LCD + USB
STM32U083xC				STM32U073 with crypto

3 STM32L4 series overview

The STM32L4 series is a perfect fit in terms of ultra-low power, performance, memory size, and peripherals at a cost-effective price.

In particular, the STM32L4 series enables a higher frequency and performance operation than theSTM32U0 series. STM32L4 devices feature an Arm® Cortex®-M4 processor at 80 MHz, whereas STM32U0 devices feature an Arm® Cortex®-M0+ processor at 56 MHz. Both STM32U0 and STM32L4 series also feature optimized flash memory access through the adaptive real-time memory accelerator (ART Accelerator).

The STM32L4 series MCUs increase the low-power efficiency in dynamic mode (µA/MHz), and reach a very low level of static power consumption in the various available low-power modes.

The STM32L4 series includes a large set of peripherals with advanced features, such as:

- Touch sensing controller (TSC)
- Controller area network (bxCAN)
- Single-wire protocol interface (SWPMI)
- Serial audio interface (SAI)
- Low-power universal asynchronous receiver transmitter (LPUART)
- Infrared interface (IRTIM)
- Low-power timer (LPTIM)
- Digital filter for sigma delta modulators (DFSDM) (for STM32L49xxx/4Axxx, STM32L47xxx/48xxx, and STM32L45xxx/46xxx devices)
- Voltage reference buffer (VREFBUF)
- Quad-SPI interface (QUADSPI)
- Firewall (FW)
- Clock recovery system (CRS) for USB (for STM32L49xxx/4Axxx, STM32L45xxx/46xx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx devices)
- Hash processor (HASH) (for STM32L49xxx/4Axxx devices)
- Digital camera interface (DCMI) (for STM32L49xxx/4Axxx devices)
- Chrom-ART Accelerator controller (DMA2D) (for STM32L49xxx/4Axxx) devices
- Different SRAM sizes:
  - 32 Kbytes for STM32L41xxx/44xxx
  - 48 Kbytes for STM32L43xxx/44xxx
  - 96 Kbytes for STM32L47xxx/48xxx
  - 128 Kbytes for STM32L45xxx/46xxx
  - 256 Kbytes for STM32L49xxx/4Axxx
- Additional SRAM2 with data preservation in Standby mode:
  - 8 Kbytes for STM32L41xxx/42xxx
  - 16 Kbytes for STM32L43xxx/44xxx
  - 32 Kbytes for STM32L47xxx/48xxx and STM32L45xxx/46xxx
- Optimized power consumption and enriched set of low-power modes

STM32L45xxx/46xxx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx devices implement USB Device only instead of an OTG FS. They also have a reduced flash memory size (512 Kbytes for STM32L45xxx/46xxx, 256 Kbytes for STM32L43xxx/44xxx and 128 Kbytes for STM32L41xxx/42xxx).

This application note covers the migration from the STM32L4 series to the STM32U0 series, and as a consequence, it does not cover any new features present on the STM32L4 series but not on the STM32U0.

Refer to the STM32L4 series reference manuals and datasheets for more details.

Table 2. **STM32L4 memory availability and feature levels**

Part number	Flash memory		RAM size		Feature level
	Size	Bank	SRAM1	SRAM2	
STM32L496xx	1 Mbyte	Dual	256 Kbytes	64 Kbytes	6
STM32L4A6xx					6 + AES cryptography
STM32L471xx			96 Kbytes	32 Kbytes	1
STM32L475xx					5
STM32L476xx					6
STM32L486xx					6 + AES cryptography
STM32L451xx	512 Kbytes		128 Kbytes	32 Kbytes	1
STM32L452xx					2
STM32L462xx					2 + AES cryptography
STM32L431xx	512 Kbytes	Single	48 Kbytes	16 Kbytes	1
STM32L432xx					3
STM32L442xx					2 + AES cryptography
STM32L433xx					3
STM32L443xx					3 + AES cryptography
STM32L412xx	128 Kbytes		32 Kbytes	8 Kbytes	2
STM32L422xx					2 + AES cryptography

4 Hardware migration

4.1 Package availability

Some packages are available for both the STM32U0 and STM32L4 series, as illustrated by Table 3 and Table 4. The other packages available for the STM32L4 series are not available on the STM32U0 series. The STM32U0 series also brings new packages that are not available on the STM32L4 series.

Note: WLCSP packages are not equivalent and have different die sizes for each product.

The current STM32U0 products do not support the SMPS option. Migration from SMPS products requires an application redesign, which is out of scope for this application note.

Table 3 lists the available packages for the STM32U0 series.

Table 3. Available packages for the STM32U0 series

Package	STM32L4 series	STM32U083xx	STM32U073xx	STM32U031xx	Size (mm x mm)
TSSOP20	-	-	-	X	6.5 x 4.4
UFQFPN32	X	X	X	X	5 x 5
UFQFPN48	X	X	X	X	7 x 7
LQFP48	X	X	X	X	7 x 7
LQFP64	X	X	X	X	10 x 10
LQFP80	-	X	X	-	12 x 12
UFBGA64	X	X	X	X	5 x 5
UFBGA81	-	X	X	-	5 x 5
WLCSP27	-	-	-	X	2.55 x 2.34
WLCSP42	-	X	X	-	2.82 x 2.93

Table 4 lists the available packages for the STM32L4 series.

Table 4. Available packages for the STM32L4 series

Package	STM32U0 series	STM32L4 series					Size (mm x mm)
		STM32L49xxx STM32L4Axxx	STM32L47xxx STM32L48xxx	STM32L45xxx STM32L46xxx	STM32L43xxx STM32L44xxx	STM32L41xxx STM32L42xxx	
UFQFPN32	X	-	-	-	X	X	5 x 5
UFQFPN48	X	-	-	X	X	X	7 x 7
LQFP32	X	-	-	-	-	X	5 x 5
LQFP48	X	-	-	-	X	X	7 x 7
LQFP64	X	X	X	X	X	X	10 x 10
LQFP100	-	X	X	X	X	-	14 x 14
LQFP144	-	X	X	-	-	-	20 x 20
UFBGA64	X	-	-	X	X	X	5 x 5
UFBGA100	-	-	X	X	X	-	7 x 7
UFBGA132	-	X	X	-	-	-	7 x 7
UFBGA169	-	X	-	-	-	-	7 x 7
WLCSP36	-	-	-	-	-	X	2.58 x 3.07
WLCSP49	-	-	-	-	X	-	3.141 x 3.127

Package	STM32U0 series	STM32L4 series					Size (mm x mm)
		STM32L49xxx STM32L4Axxx	STM32L47xxx STM32L48xxx	STM32L45xxx STM32L46xxx	STM32L43xxx STM32L44xxx	STM32L41xxx STM32L42xxx	
WLCSP64	-	-	-	-	X	-	3.141 x 3.127
WLCSP64	-	-	-	X	-	-	3.357 x 3.657
WLCSP72	-	-	X	-	-	-	4.408 x 3.759
WLCSP81	-	-	X	-	-	-	4.408 x 3.759
WLCSP100	-	X	-	-	-	-	4.618 x 4.142

4.2 Pin compatibility

The STM32U0 and STM32L4 series share a high level of pin compatibility. Most peripherals share the same pins in both series, rendering the transition from an STM32L4 device to an STM32U0 device very straightforward on available packages, like UFBGA64, LQFP64/48/32, and UFQFPN48/32.

Due to the shared use of system pins as GPIOs, STM32U0 offers up to two additional GPIOs on the same package.

JTAG is not supported on the STM32U0 series.

There are some additional exceptions to consider. The STM32U0 series TSC group assignment is different from that of the STM32L4 series, so applications using TSC require a PCB redesign. The STM32U0 ADC channels are connected to the same pins as for the STM32L4 series, but with different channel numbers, and the devices embed a single ADC without differential inputs.

GPIO port GPIOH has been replaced by GPIOF, keeping the same position and alternate functions.

Refer to the product datasheets for more details.

4.2.1 Pinout differences between STM32L4 and STM32U0 QFP packages

Table 5 shows the pinout differences in QFP packages for the STM32L4 and STM32U0 series.

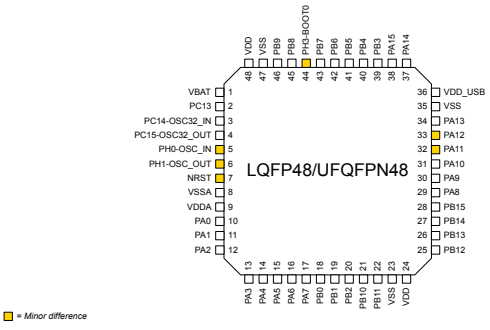
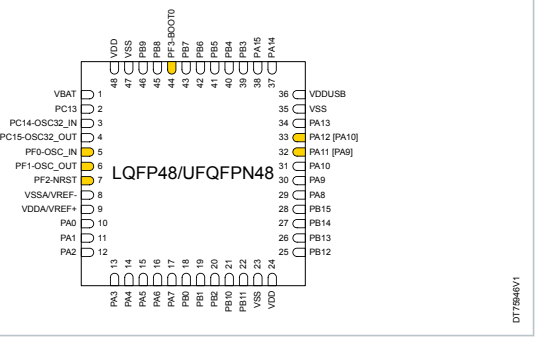
Table 5. Pinout differences between STM32L4 and STM32U0 QFP packages

STM32L4 series				STM32U0 series			
UFQFPN32/ LQFP32	UFQFPN48/ LQFP48	LQFP64	Pinout	UFQFPN32/ LQFP32	UFQFPN48/ LQFP48	LQFP64	Pinout
4	7	7	NRST	4	7	7	PF2-NRST(1)
31	44	60	PH3-BOOT0(2)	31	44	60	PF3-BOOT0(1)

1. *System pins can also be used as GPIO.*
2. *Only the dedicated BOOT0 pin is available on STM32L47xxx/STM32L48xxx devices.*

Table 6 gives an example of the pinout differences between STM32L4 and STM32U0 48-pin packages. These packages all have the same layout and migrating from an STM32L4 to an STM32U0 device does not require an extensive update.

Table 6. Example of pinout differences between STM32L4 and STM32U0 48-pin packages

STM32L452x6/8 LQFP48/UFQFPN48 pinout	STM32U0 LQFP48/UFQFPN48 pinout
	

4.2.2 Ballout differences between STM32L4 and STM32U0 BGA packages

Table 7 shows the ballout differences in BGA packages for the STM32L4 and STM32U0 series.

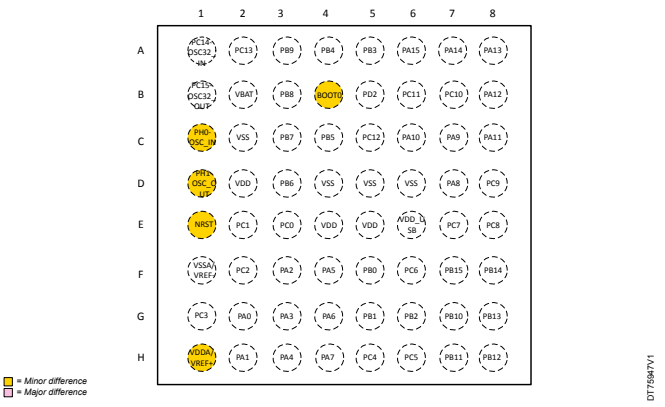
Table 7. Ballout differences between STM32L4 and STM32U0 BGA packages

STM32L4 series		STM32U0 series	
UFBGA64	Ballout	UFBGA64	Ballout
B4	BOOT0	B4	PF3-BOOT0(1)
E1	PH2-NRST(2)	E1	PF2-NRST(1)

1. *System pins can also be used as GPIO.*
2. *Only the dedicated BOOT0 pin is available on STM32L47xxx/STM32L48xxx devices.*

Table 8 gives an example of the pinout differences between STM32L4 and STM32U0 UFBGA64 packages.

Table 8. Example of ballout differences between STM32L4 and STM32U0 UFBGA64 packages

STM32L472xx	STM32U073xx
	

4.3 Recommendations for board migration

There is backward compatibility between the pinout of the STM32U0 and STM32L4 series, making PCB migration simple. As mentioned before, TSC and ADC assignment requires cautiousness.

The BOOT0 is multiplexed with the GPIO on the STM32U0 series and all STM32L4 devices except STM32L47xxx/48xxx. Refer to Section 5: Boot mode selection for details.

The NRST pin is multiplexed with the GPIO pin, referred to as PF2-NRST. It is shared with GPIO in the STM32U0 series. Selection is available through the device option bytes, where the user could select legacy behavior, reset, input-only mode, or GPIO mode. This configuration is loaded from the option bytes after each power on, so the external circuitry must let the NRST pin cross V_{IH} level after power-on or exit from deep low-power modes.

Note: The GPIOF port replaces the GPIOH port for packages available on the STM32U0 series. GPIOF, available on STM32L4 series devices with more than 100 pins, is not present on STM32U0 series devices.

New packages (LQFP80, and UFBGA81) have been introduced for the STM32U0 series.

Multiple GPIOs are bonded together to the same pin on TSSOP20.

STM32U0 devices do not support SMPS.

5 Boot mode selection

Both the STM32L4 and STM32U0 series offer three different boot modes: boot from the main flash memory, boot from SRAM, or boot from the system memory. However, the way to select the boot mode differs between the products:

- On STM32L4 devices, the boot mode is selected using the nBOOT1 option bit with the BOOT0 pin or the nBOOT0 option bit, depending on the value of the nSWBOOT0 option bit in the FLASH_OPTR register.
- On STM32U0 devices, the boot mode is selected using the nBOOT1 option bit with the BOOT0 pin or the nBOOT0 option bit, depending on the value of the nBOOT_SEL option bit in the FLASH_OPTR register. Additionally, the BOOT_LOCK bit is available to increase application security. It forces the main flash memory as a boot memory area, and requires support in the firmware to connect the debug interface when the RDP level is not 0.
- STM32U0 embeds the empty memory check feature, forcing the execution of the bootloader when the main flash memory is selected but the reset vector is not programmed in the memory. This feature is available only on selected STM32L4 devices.

Table 9 and Table 10 show the different configurations available for selecting the boot mode for STM32L4 and STM32U0 devices.

Table 9. Boot modes for STM32L4 devices

nBOOT1 FLASH_OPTR [23](1)	nBOOT0 FLASH_OPTR [27]	BOOT0 pin PH3(1)	nSWBOOT0 FLASH_OPTR [26]	Main flash memory empty	Boot memory space alias
X	X	0	1	0	Main flash memory is selected as boot area
X	X	0	1	1	System memory is selected as boot area
X	1	X	0	X	Main flash memory is selected as boot area
0	X	1	1	X	Embedded SRAM1 is selected as boot area
0	0	X	0	X	Embedded SRAM1 is selected as boot area
1	X	1	1	X	System memory is selected as boot area
1	0	X	0	X	System memory is selected as boot area

1. *Grey-shaded cells indicate options that are not available for STM32L47xxx/STM32L48xxx devices.*

Table 10. **Boot modes for STM32U0 devices**

Boot mode configuration					Selected boot area
BOOT_LOCK bit	nBOOT1 bit	BOOT0 pin	nBOOT_SEL bit	nBOOT0_bit	
0	X	0	0	X	Main flash memory
0	1	1	0	X	System memory
0	0	1	0	X	Embedded SRAM
0	X	X	1	1	Main flash memory
0	1	X	1	0	System memory
0	0	X	1	0	Embedded SRAM
1	X	X	X	X	Main flash memory forced

5.1 Embedded bootloader

The embedded bootloader is located in the system memory, programmed by STMicroelectronics during production. This bootloader is used to reprogram the flash memory using one of the serial interfaces listed in the table below (where X = supported).

Table 11. **Bootloader interfaces on the STM32L4 and STM32U0 series**

Peripheral	Pin	STM32L4 series	STM32U0 series
DFU	USB_DM (PA11) USB_DP (PA12)	X	X
USART1	USART1_TX (PA9) USART1_RX (PA10)	X	X
USART2	USART2_TX (PA2) USART2_RX (PA3)	X	X
USART3	USART3_TX (PC10) USART3_RX (PC11)	X	X
I2C1	I2C1_SCL (PB6) I2C1_SDA (PB7)	X	X
I2C2	I2C2_SCL (PB10) I2C2_SDA (PB11)	X	X
I2C3	I2C3_SCL (PB3) I2C3_SDA (PB4)	X	X
SPI1	SPI1_NSS (PA4) SPI1_SCK (PA5) SPI1_MISO (PA6) SPI1_MOSI (PA7)	X	X
SPI2	SPI2_NSS (PB12) SPI2_SCK (PB13) SPI2_MISO (PB14) SPI2_MOSI (PB15)	X	X
CAN1	CAN1_RX (PB8) CAN1_TX (PB9)	X	-

Refer to the application note *STM32 microcontroller system memory boot mode* (AN2606, available from www.st.com) for more details on the bootloader.

For smaller packages, it is important to check the pin and peripheral availability.

5.2 Debugging interface

JTAG and ETM are not supported by the STM32U0 series.

SWD is supported on both the STM32U0 and STM32L4 series.

6 Low-power modes

By default, the microcontroller is in Run mode after a system or a power reset. Several low-power modes are available to save power when it is not necessary to keep the CPU running, for example when waiting for an external event. It is up to the user to select the mode that gives the best compromise between low-power consumption, a short startup time, and available wake-up sources.

The STM32L4 and STM32U0 series share the same main low-power modes (Low-power run, Stop, Sleep, Low-power sleep, Standby, and Shutdown) with voltage ranges specific to each series.

Details on the low-power mode configuration in each series can be found in the device reference manual. The consumption figures are given in the device datasheets.

6.1 Low-power modes in the STM32U0 and STM32L4 series

Compared to the STM32L4 series, STM32U0 series devices offer similar flexibility to reduce general consumption by using the following modes:

- Stop 0, Stop 1, and Stop 2 modes: SRAMs and all register content are retained. All clocks in the VCORE domain are stopped; PLL, MSI, HSI16, and HSE are disabled. LSI and LSE can be kept running.
- Standby mode: the VCORE domain is powered off; SRAM2 retention can be enabled; RTC with LSE can be kept running.
- Shutdown mode: the VCORE domain is powered off. All clocks in the VCORE domain are stopped; PLL, MSI, HSI16, LSI, and HSE are disabled. LSE can be kept running

In the main Run mode, power consumption can be reduced by one of the following means:

- Slowing down the system clocks
- Gating the clocks to the APB and AHB peripherals when they are unused

Low-power run and Sleep modes support a frequency up to 2 MHz.

Dynamic voltage scaling

The main regulator (MR) has two voltage ranges for dynamic voltage scaling (Range 1 and Range 2) used in the Run and Sleep modes, as shown in Table 12.

Table 12. Voltage ranges for dynamic voltage scaling

MR range	V_{Core} supply	STM32U0	STM32L4
Range 1	1.2 V	56 MHz	80 MHz
Range 2	1.0 V	18 MHz	26 MHz

The low-power regulator (LPR) is for the Low-power run, Low-power sleep, Stop 1, and Stop 2 modes, as well as for the RAM retention in Standby mode.

Integration of new features

The following features, which decrease power consumption, have been tested on the smallest STM32L412xx/ STM32L422xx devices:

- Enabling sampling of the voltage reference for power monitoring (ENULP)
- Optimized design of RTC and clock distribution

All STM32U0 devices also integrate these features

Low-power mode overview

Table 13 presents a summary of the STM32U0 series low-power modes. The consumption figures are given for the STM32U031xx devices as an indication. For the power consumption figures of other devices, refer to the dedicated product datasheets.

Table 13. STM32U0 series low-power modes

Mode	Reg.	CPU	Flash memory(1)	SRAM	Clocks	Peripherals(2)	Consumption(3)	Wake-up time (µs)
Run	Range 1	On	On	On	Any	All peripherals available	68 (uA/MHz)	N/A
	Range 2					All except USB, RNG	61 (uA/MHz)	
Low-power run	LPR	On	On	On	Any except PLL	All except USB, RNG	65 (uA/MHz)	Range 1: 4 µs to range 2: 64 µs
Sleep	Range 1	Off	On	On	Any	All peripherals available	24 (uA/MHz)	6 cycles
	Range 2					All except USB, RNG	26 (uA/MHz)	
Low-power sleep	LPR	Off	On	On	Any except PLL	All except USB, RNG	28 (uA/MHz)	6 cycles
Stop 0	MR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	100 uA	NC
Stop 1	LPR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	2.0 uA without RTC 2.2 uA with RTC	4 µs in SRAM 6 µs in flash memory
Stop 2	LPR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	515 nA without RTC 630 nA with RTC	5 µs in SRAM 7 µs in flash memory
Standby	LPR	Off	Off	SRAM2 On	LSI/LSE	BOR, RTC, IWDG All other peripherals are powered off I/O configuration can be floating, pull-up, or pull-down	121 nA without RTC 249 nA with RTC	14
	Off			Off			32.5 nA without RTC 160 nA with RTC	
Shutdown	Off	Off	Off	Off	LSE	RTC All other peripherals are powered off I/O configuration can be floating, pull-up, or pull-down	16 nA without RTC 195 nA with RTC	256

1. *The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.*
2. *All peripherals can be active or clock-gated to save power consumption. Values are provided with all clock-gated peripherals.*
3. *Typical current at V_{DD} = 1.8 V, 25°C. The consumption values are provided when running from the SRAM, flash memory off: 48 MHz in range 1; 16 MHz in range 2; 2 MHz in Low-power run/Low-power sleep modes. The values differ for different products, refer to the dedicated product datasheets for the exact values.*

Table 14 presents a summary of the STM32L4 series low-power modes. The consumption figures are given for the STM32L476xx devices as an indication. For the power consumption figures of other references, refer to the dedicated product datasheets.

Table 14. STM32L4 series low-power modes

Mode	Reg.	CPU	Flash memory (1)	SRAM	Clocks	Peripherals(2)	Consumption(3)	Wake-up time (µs)
Run	Range 1	On	On	On	Any	All peripherals available	112 (uA/MHz)	N/A
	Range 2					All except USB, RNG	100 (uA/MHz)	
Low-power run	LPR	On	On	On	Any except PLL	All except USB, RNG	136 (uA/MHz)	Range 1: 4 µs to Range 2: 64 µs
Sleep	Range 1	Off	On	On	Any	All peripherals available	37 (uA/MHz)	6 cycles
	Range 2					All except USB, RNG	35 (uA/MHz)	
Low-power sleep	LPR	Off	On	On	Any except PLL	All except USB, RNG	40 (uA/MHz)	
Stop 0	MR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	NC	NC
Stop 1	LPR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	6.6 uA without RTC 6.9 uA with RTC	4 µs in SRAM 6 µs in flash memory
Stop 2	LPR	Off	Off	On	LSI/LSE	LCD, RTC, I/Os, BOR, PVD, PVM, COMPs, IWDG, LPUART, USB, UART, I2C	1.1 uA without RTC 1.4 uA with RTC	5 µs in SRAM 7 µs in flash memory
Standby	LPR	Off	Off	SRAM2 On	LSI/LSE	BOR, RTC, IWDG All other peripherals are powered off I/O configuration can be floating, pull-up, or pull-down	0.35 uA without RTC 0.65 uA with RTC	14
	Off			Off			0.12 uA without RTC 0.42 uA with RTC	
Shutdown	Off	Off	Off	Off	LSE	RTC All other peripherals are powered off I/O configuration can be floating, pull-up, or pull-down	0.03 uA without RTC 0.33 uA with RTC	256

1. *The flash memory can be put in power-down and its clock can be gated off when executing from SRAM.*
2. *All peripherals can be active or clock-gated to save power consumption. Values are provided with all clock-gated peripherals.*

3. *Typical current at V_{DD} = 1.8 V, 25°C. The consumption values are provided when running from the SRAM, flash memory off: 48 MHz in range 1; 16 MHz in range 2; 2 MHz in Low-power run/Low-power sleep modes. The values differ for different products, refer to the dedicated product datasheets for the exact values.*

Wake-up sources

STM32U0 and STM32L4 series devices can get out of the low-power modes on the following events:

- Sleep mode:
  - Any peripheral interrupt/wake-up event
- Stop modes:
  - Any EXTI line event
  - BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD
- Standby mode:
  - WKUP pins rising or falling edge
  - RTC event
  - External reset in NRST pin
  - IWDG reset
- Shutdown mode:
  - WKUP pins rising or falling edge
  - RTC event
  - External reset in NRST pin

6.2 Consumption and performance overview

Table 15 shows the comparison of power consumption between STM32L4 and STM32U0 devices for the main dynamic and static modes. The table represents the typical values for given devices with up to 256 Kbytes flash memory and at room temperature.

Table 15. Power consumtion comparison between STM32L4 and STM32U0 devices

Mode	STM32L4		STM32U0		Unit
	STM32L41xxx/ STM32L42xxx	STM32L43xxx/ STM32L44xxx	STM32U08xxx/ STM32U07xxx	STM32U03xxx	
Run - while(1)	75	88	52	52	uA/MHz
Run - CoreMark (Range 1)	102	121	78	78	uA/MHz
Run - CoreMark (Range 2) (1)	88	103	70	70	uA/MHz
Sleep (Range 2)(1)	20	26	28	26	uA/MHz
LP Run	103	126	80	80	uA/MHz
Stop 0	115	111	105	105	uA
Stop 1	4.0	4.41	3.3	2.1	uA
Stop 2	0.750	1.06	0.750	0.560	uA
Standby	0.120	0.090	0.075	0.068	uA
Shutdown	0.031	0.044	0.053	0.050	uA

1. *The lowest range has been used with the highest frequency allowed for the given range.*

Table 16 shows a comparison of ULPMark scores, demonstrating better energy efficiency of STM32U0 in typical application use cases. For more information about ULPMark, go to https://www.eembc.org/ulpmark.

Table 16. ULPMark score comparison between STM32L4 and STM32U0 devices

ULPMark	STM32L41xxx/ STM32L42xxx	STM32L43xxx/ STM32L44xxx	STM32U08xxx/ STM32U07xxx	STM32U03xxx
ULPMark-CP	442	347	407	430
ULPMark-PP	165	121	143	167
ULPMark-CM	-	-	19.7	20.3

7 Peripheral migration

7.1 STM32 product cross-compatibility

STM32 MCUs embed a set of peripherals that can be classified in three groups:

- The first group is for the peripherals that are common to all products. These peripherals have the same structure, registers, and control bits. There is no need to perform any firmware changes to keep the same functionality at the application level after migration. Peripheral features and behavior remain the same across devices.
- The second group is for the peripherals that present minor differences from one product to another (usually due to the support of new features). Migrating from one product to another is easy and does not require any significant new development effort.
- The third group is for peripherals that have been considerably modified from one product to another (new architecture or new features, for instance). For this group of peripherals, the migration requires a new development at application level.

Table 17 gives a general overview of this classification. The software compatibility mentioned in the table refers only to the register description for low-level drivers.

The STM32Cube hardware abstraction layer (HAL) is compatible between the STM32L4 and STM32U0 series.

Table 17. Peripheral compatibility analysis between STM32L4 series and STM32U0 series

Peripheral		Number of instances			Compatibility with STM32U0 series		
		STM32L4	STM32U073xx/ STM32U083xx	STM32U031xx	Software	Pinout	Comments
SPI		2/3	3	2	Partial		Some alternate functions are not mapped on the same GPIO for SPI1.
FIREWALL		1	0		NA		-
WWDG		1	1		Full	NA	JTAG is not available on the STM32U0 series.
IWDG		1	1				
DBGMCU		1	1			Partial	
CRC		1	1		Partial	NA	-
EXTI		1	1			Full	-
USB FS		1	1	0	Full		-
USB OTG FS		1	0	0	Partial		-
DMA		2	2	1		NA	• Significant flexibility due to DMAMUX extension. • DMA mapping request may differ (refer to Section 7.3: Direct memory access controller (DMA)).
TIM	Basic	2	2	2	Full	Partial	• STM32U0 brings one 32-bit timer. • Some pins are not mapped on the same GPIO. • Timer instance names may differ. • Internal connections may differ.
	General-purpose	7	4	4			
	Advanced	2	1	1			
	Low-power	2	3	2			
	IRTIM	1	1	1			
SDIO		1	0		NA		-
FSMC/FMC		Up to 1	0				-
PWR		1	1		Partial	NA	-
RCC		1	1				

Peripheral	Number of instances			Compatibility with STM32U0 series		
	STM32L4	STM32U073xx/ STM32U083xx	STM32U031xx	Software	Pinout	Comments
USART UART LPUART	3 Up to 2 1	4 0 3	4 0 2	Partial	Full	-
I2C	Up to 4	4	3	None		-
DAC channels	Up to 2	1		Partial		-
ADC	Up to 3	1		None	Partial	• No differential channels. • Single ADC instance only. • Different channels are mapped on the same GPIO.
RTC	1	1		Partial	Full	• Additional features on the STM32U0 series. • Can be powered by V_{BAT}.
FLASH	1	1		None	NA	Dual bank not supported.
GPIO	Up to 115 IOs	Up to 69 IOs	Up to 53 IOs	Full	Partial	• Additional GPIO thanks to sharing with system pins. • A few changes, mentioned in Section 4: Hardware migration.
LCD controller	Up to 1	1	0			• VLCD muxed on PC3 GPIO. • SEG21 mapped on a different GPIO. • Integrated voltage output buffers for higher LCD driving capability
COMP	2	2	1	None		Some pins are mapped on different GPIOs.
SYSCFG	1	1		Partial	NA	-
AES	1	1	0	Full		Available only on products supporting cryptography.
OPAMP	Up to 2	1		None		-

7.2 Memory mapping

The peripheral address mapping has been changed in the STM32U0 series compared to the STM32L4 series. Table 18 provides the peripheral address mapping differences between the STM32L4 and STM32U0 series.

Table 18. Peripheral address mapping differences between STM32L4 and STM32U0 series

Peripheral	STM32L4 series		STM32U0 series	
	Bus	Base address	Bus	Base address
GPIOG	AHB2	0x4800 1800	AHB	NA
GPIOH(1)		0x4800 1C00		NA
GPIOF(1)		0x4800 1400		0x5000 1400
GPIOE		0x4800 1000		0x5000 1000
GPIOD		0x4800 0C00		0x5000 0C00
GPIOC		0x4800 0800		0x5000 0800
GPIOB		0x4800 0400		0x5000 0400
GPIOA		0x4800 0000		0x5000 0000
CRC	AHB1	0x4002 3000		0x4002 3000
FLASH		0x4002 2000		0x4002 2000
RCC		0x4002 1000		0x4002 1000
DMA1		0x4002 0000		0x4002 0000
DMA2		0x4002 0400		0x4002 0400
DMAMUX		0x5006 0000		0x4002 0800
DMA2D		0x4002 6000		NA
TSC		0x4002 4000	APB	0x4002 4000
AES	AHB2	0x5006 0000		0x4002 6000
RNG		0x5006 0800		0x5006 0800
HASH		0x5006 0400		NA
DCMI		0x5005 0000		NA
GPIOI		0x4800 2000		NA
USB OTG FS		0x5000 0000		NA
ADC1		0x4001 2400		0x4001 2400
FSMC/FMC	AHB3	0xA000 0000		NA
USART1	APB2	0x4001 3800		0x4001 3800
SPI1		0x4001 3000		0x4001 3000
SDMCC		0x4001 2800		NA
EXTI		0x4001 0400		0x4001 0400
SYSCFG		0x4001 0000		0x4001 0000
COMP		0x4001 0200		0x4001 0200
DFSDM		0x4001 6000		NA
SAI2		0x4001 5800		NA
SAI1		0x4001 5400		NA
TIM17		0x4001 8000		NA
TIM16		0x4001 4400		NA
TIM15		0x4001 4000		NA
TIM8		0x4001 3400		NA
TIM1		0x4001 2C00		NA
FIREWALL		0x4001 1C00		NA

Peripheral	STM32L4 series		STM32U0 series	
	Bus	Base address	Bus	Base address
VREF	APB2	0x4001 0030	APB	NA
OPAMP	APB1	0x4000 7800		0x4000 7800
DAC		0x4000 7400		0x4000 7400
PWR		0x4000 7000		0x4000 7000
USB device FS SRAM		0x4000 6C00		0x4000 9800
USB device FS		0x4000 6800		0x4000 5C00
I2C4		0x4000 8400		0x4000 A000
I2C3		0x4000 5C00		0x4000 8800
I2C2		0x4000 5800		0x4000 5800
I2C1		0x4000 5400		0x4000 5400
UART5		0x4000 5000		NA
USART4		0x4000 4C00		0x4000 4C00
USART3		0x4000 4800		0x4000 4800
USART2		0x4000 4400		0x4000 4400
LPUART1		0x4000 4800		0x4000 8000
SPI3		0x4000 3C00		0x4000 3C00
SPI2		0x4000 3800		0x4000 3800
IWDG		0x4000 3000		0x4000 3000
WWDG		0x4000 2C00		0x4000 2C00
RTC (inc. BKP registers)		0x4000 2800		0x4000 2800
LCD		0x4000 2400		0x4000 2400
TIM7		0x4000 1400		0x4000 1400
TIM6		0x4000 1000		0x4000 1000
TIM5		0x4000 0C00		NA
TIM4		0x4000 0800		NA
TIM3		0x4000 0400		0x4000 0400
TIM2		0x4000 0000		0x4000 0000
LPTIM1		0x4000 7C00		0x4000 7C00
CAN2		0x4000 6800		NA
CAN1		0x4000 6400		NA
CRS		0x4000 6000		0x4000 6C00
LPTIM2	NA			0x4000 9400
LPTIM3				0x4000 9000
LPUART3				0x4000 8C00
LPUART2				0x4000 8400

1. *On STM32U0 devices, GPIOF is mapped instead of GPIOH on STM32L4 devices. GPIOF pins present on the STM32L4 series are not present on the STM32U0 series.*

The system memory mapping has been updated between the STM32L4 series and STM32U0 series. Refer to the reference manuals and datasheets for more details.

The STM32U0 series features an additional SRAM (SRAM2) of the following size:

- 8 Kbytes on STM32U073xx/83xx devices.
- 4 Kbytes on STM32U031xx devices.

SRAM2 includes the additional features listed below:

- Maximum performance through I-Code bus access without physical remap.
- Parity check option (32-bit + 4-bit parity check).
- Write protection with 1 Kbyte granularity.
- Read protection (RDP).
- Erase by system reset (option byte) or by software.
- Content preserved in Low-power run, Low-power sleep, Stop 0, Stop 1, and Stop 2 modes.
- Content can be preserved (RRS bit set in PWR_CR3 register) in Standby mode (not the case for SRAM1).

Bit-banding

Both the STM32L4 and STM32U0 series support bit-banding on the lowest 1 Mbyte of the SRAM and on the peripheral memory region. However, the peripherals mapped in this bit-banding region are different for each series.

The following peripherals are accessible with bit-banding:

- STM32L4 series: all peripherals except AES and FSMC.
- STM32U0 series: all peripherals except GPIOx, ADC, AES, and RNG.

7.3 Direct memory access controller (DMA)

STM32U0 embeds DMAMUX, extending the capabilities of the regular DMA present in STM32L4 products. For the DMA in the STM32L4 series, each channel is dedicated by hardware connection to managing the memory access requests from one or more peripherals and has an arbiter for handling the priorities among the DMA requests.

For the STM32U0 series, each DMA request line is connected in parallel to all the channels of the DMAMUX request line multiplexer, providing a high level of flexibility.

The DMAMUX request multiplexer allows a DMA request line to be routed between the peripherals and the DMA controllers of the product. The routing function is ensured by a programmable multi-channel DMA request line multiplexer. Each channel selects a unique DMA request line, unconditionally or synchronously with events from its DMAMUX synchronization inputs. Existing application software using DMA needs to be updated to integrate this new DMAMUX feature.

Table 19 presents the differences between the DMA requests of the peripherals in the STM32L4 series and the peripherals in the STM32U0 series.

Table 19. DMA request differences between STM32L4 and STM32U0 series

Peripheral	DMA request	STM32L4 series	STM32U0 series
ADC	ADC1	DMA1_Channel1 DMA2_Channel3	DMAMUX request 5
	ADC2	DMA1_Channel2 DMA2_Channel4	NA
	ADC3	DMA1_Channel3 DMA2_Channel5	
DAC	DAC1_CH1	DMA1_Channel3 DMA2_Channel4	DMAMUX request 8
	DAC1_CH2	DMA1_Channel4 DMA2_Channel5	NA
DFSDM	DFSDM0	DMA1_Channel4	NA
	DFSDM1	DMA1_Channel5	

Peripheral	DMA request	STM32L4 series	STM32U0 series
DFSDM	DFSDM2	DMA1_Channel6	NA
	DFSDM3	DMA1_Channel7	
SPI1	SPI1_RX	DMA1_Channel2	DMAMUX request 36
	SPI1_TX	DMA1_Channel3	DMAMUX request 37
SPI2	SPI2_RX	DMA1_Channel4	DMAMUX request 38
	SPI2_TX	DMA1_Channel5	DMAMUX request 39
SPI3	SPI3_RX	DMA1_Channel1	DMAMUX request 40
	SPI3_TX	DMA1_Channel2	DMAMUX request 41
USART1	USART1_RX	DMA1_Channel5 DMA2_Channel7	DMAMUX request 69
	USART1_TX	DMA1_Channel4 DMA2_Channel6	DMAMUX request 70
USART2	USART2_RX	DMA1_Channel6	DMAMUX request 71
	USART2_TX	DMA1_Channel7	DMAMUX request 72
USART3	USART3_RX	DMA1_Channel3	DMAMUX request 73
	USART3_TX	DMA1_Channel2	DMAMUX request 74
USART4	UART4_RX	DMA2_Channel5	DMAMUX request 75
	UART4_TX	DMA2_Channel3	DMAMUX request 76
USART5	UART5_RX	DMA2_Channel2	NA
	UART5_TX	DMA2_Channel1	
LPUART1	LPUART1_RX	DMA2_Channel7	DMAMUX request 30
	LPUART1_TX	DMA2_Channel6	DMAMUX request 31
LPUART2	LPUART2_RX	NA	DMAMUX request 32
	LPUART2_TX		DMAMUX request 33
LPUART3	LPUART3_RX		DMAMUX request 34
	LPUART3_TX		DMAMUX request 35
I2C1	I2C1_RX	DMA1_Channel7 DMA2_Channel6	DMAMUX request 9
	I2C1_TX	DMA1_Channel6 DMA2_Channel7	DMAMUX request 10
I2C2	I2C2_RX	DMA1_Channel5	DMAMUX request 11
	I2C2_TX	DMA1_Channel4	DMAMUX request 12
I2C3	I2C3_RX	DMA1_Channel3	DMAMUX request 13
	I2C3_TX	DMA1_Channel3	DMAMUX request 14
I2C4	I2C4_RX	DMA2_Channel1	DMAMUX request 15
	I2C4_TX	DMA2_Channel2	DMAMUX request 16
SDMCC	SDMCC	DMA2_Channel4 DMA2_Channel5	NA
TIM1	TIM1_CH1	DMA1_Channel2	DMAMUX request 42
	TIM1_CH2	DMA1_Channel3	DMAMUX request 43
	TIM1_CH3	DMA1_Channel7	DMAMUX request 44
	TIM1_CH4	DMA1_Channel4	DMAMUX request 45

Peripheral	DMA request	STM32L4 series	STM32U0 series
TIM1	TIM1_TRIG_UP	DMA1_Channel4	DMAMUX request 46
	TIM1_UP	DMA1_Channel6	DMAMUX request 47
TIM2	TIM2_UP	DMA1_Channel2	DMAMUX request 48
	TIM2_CH1	DMA1_Channel5	DMAMUX request 49
	TIM2_CH2	DMA1_Channel7	DMAMUX request 50
	TIM2_CH3	DMA1_Channel1	DMAMUX request 51
	TIM2_CH4	DMA1_Channel7	DMAMUX request 52
			DMAMUX request 53
TIM3	TIM3_UP	DMA1_Channel3	DMAMUX request 54
	TIM3_CH1	DMA1_Channel6	DMAMUX request 55
	TIM3_TRIG	DMA1_Channel6	DMAMUX request 56
	TIM3_CH3	DMA1_Channel2	DMAMUX request 57
	TIM3_CH4	DMA1_Channel3	DMAMUX request 58
			DMAMUX request 59
TIM4	TIM4_UP	DMA1_Channel7	NA
	TIM4_CH1	DMA1_Channel1	
	TIM4_CH2	DMA1_Channel4	
	TIM4_CH3	DMA1_Channel5	
TIM5	TIM5_UP	DMA2_Channel2	
	TIM5_CH1	DMA2_Channel5	
	TIM5_CH2	DMA2_Channel4	
	TIM5_CH3	DMA2_Channel2	
	TIM5_CH4	DMA2_Channel1	
	TIM5_TRIG	DMA2_Channel1	
	TIM5_COM	DMA2_Channel1	
TIM6	TIM6_UP	DMA1_Channel3 DMA2_Channel4	DMAMUX request 60
TIM7	TIM7_UP	DMA1_Channel4 DMA2_Channel5	DMAMUX request 61
TIM8	TIM8_CH1	DMA2_Channel6	NA
	TIM8_CH2	DMA2_Channel7	
	TIM8_CH3	DMA2_Channel1	
	TIM8_UP	DMA2_Channel1	
	TIM8_CH4	DMA2_Channel2	
	TIM8_TRIG	DMA2_Channel2	
	TIM8_COM	DMA2_Channel2	
TIM15	TIM15_CH1	DMA1_Channel5	DMAMUX request 62
	TIM15_UP	DMA1_Channel5	DMAMUX request 63
	TIM15_TRIG	DMA1_Channel5	DMAMUX request 64
	TIM15_COM	DMA1_Channel5	DMAMUX request 65
TIM16	TIM16_CH1	DMA1_Channel3	

Peripheral	DMA request	STM32L4 series	STM32U0 series
TIM16	TIM16_UP	DMA1_Channel3	DMAMUX request 66
	TIM16_CH1	DMA1_Channel6	DMAMUX request 67
	TIM16_UP	DMA1_Channel6	DMAMUX request 68
TIM17	TIM17_CH1	DMA1_Channel1	NA
	TIM17_UP	DMA1_Channel1	
	TIM17_CH1	DMA1_Channel7	
	TIM17_UP	DMA1_Channel7	
SAI	SAI1_A	DMA2_Channel1 DMA2_Channel6	
	SAI1_B	DMA2_Channel2 DMA2_Channel7	
	SAI2_A	DMA1_Channel6 DMA2_Channel3	
	SAI2_B	DMA1_Channel7 DMA2_Channel4	
SWPMI	SWPMI_RX	DMA2_Channel1	
	SWPMI_TX	DMA2_Channel2	
AES	AES_OUT	DMA2_Channel2 DMA2_Channel3	DMAMUX request 7
	AES_IN	DMA2_Channel1 DMA2_Channel5	DMAMUX request 6
DCMI	DCMI	DMA2_Channel7 DMA2_Channel5	NA
HASH	HASH_IN	DMA2_Channel7	

7.4 Interrupts

Table 20 presents the interrupt vectors on the STM32U0 series compared to the STM32L4 series.

Interrupt lines 32 and higher are not present on the Cortex®-M0+ processor, so interrupts are remapped to available vectors.

Table 20. Interrupt vector differences between STM32L4 and STM32U0 series

Position	STM32L4 series	STM32U0 series
0	WWDG	WWDG
1	PVD/PVM	PVD/PVM
2	TAMPER/CSS	TAMPER/RTC
3	RTC_WKUP	FLASH/WKUP
4	FLASH	RCC/CRS
5	RCC	EXTI0_1
6	EXTI0	EXT2_3
7	EXTI1	EXTI4
8	EXTI2	USB
9	EXTI3	DMA1_Channel1

Position	STM32L4 series	STM32U0 series
10	EXTI4	DMA1_Channel2_3
11	DMA1_Channel1	DMA1_Channel4_5_6_7/ DMAMUX/DMA2_Channel1_2_3_4_5
12	DMA1_Channel2	ADC_COMP
13	DMA1_Channel3	TIM1_BRK_UP_TRG_COM
14	DMA1_Channel4	TIM1_CC
15	DMA1_Channel5	TIM2
16	DMA1_Channel6	TIM3
17	DMA1_Channel7	TIM6/DAC/LPTIM1
18	ADC1_2	TIM7/LPTIM2
19	CAN1_TX	TIM15/LPTIM3
20	CAN1_RX0	TIM16
21	CAN1_RX1	TSC
22	CAN1_SCE	LCD
23	EXTI9_5	I2C1
24	TIM1_BRK/TIM15	I2C2/I2C3/I2C4
25	TIM1_UP/TIM16	SPI1
26	TIM1_TRG_COM/TIM17	SPI2/SPI3
27	TIM1_CC	USART1
28	TIM2	USART2/LPUART2
29	TIM3	USART3/LPUART1
30	TIM4	USART4/LPUART3
31	I2C1_EV	AES/RNG

7.5 Reset and clock control (RCC)

Table 21 presents the differences related to the reset and clock controller (RCC) between the STM32L4 series and the peripherals in the STM32U0 series.

In addition to the differences described in the table above, the following additional adaptation steps may be needed for the migration:

- Performance versus V_{CORE} ranges
- Peripheral access configuration
- Peripheral clock configuration

Table 21. RCC differences between STM32L4 and STM32U0 series

RCC	STM32L4 series	STM32U0 series
MSI	• MSI is a low-power oscillator with programmable frequency up to 48 MHz. It can replace the PLL as system clock (faster wake-up, lower consumption). It can be used as a USB device clock (no need for an external high-speed crystal oscillator) • Multi-speed RC factory and user trimmed (100 kHz, 200 kHz, 400 kHz, 800 kHz, 1 MHz, 2 MHz, 4 MHz (default value), 8 MHz, 16 MHz, 24 MHz, 32 MHz, and 48 MHz) • Auto calibration from LSE	
HSI16	• High speed internal 16 MHz RC oscillator • Factory and user trimmed	
HSI48	• 48 MHz RC for STM32U0x3xx devices. • Can drive USB Full Speed and RNG.	

RCC	STM32L4 series	STM32U0 series
LSI	• 32 kHz RC. • Lower consumption, higher accuracy (refer to product datasheet).	
HSE	• High-speed external clock • 4 to 48 MHz • From external clock or external crystal/ceramic resonator	
LSE	• Low-speed external clock • Low-power • Configurable drive/consumption • High accuracy 32.768 kHz • Available in backup domain (VBAT).	
PLL	• Main PLL for system x2 PLLs for SAI1/2, ADC, RNG, SDMMC, and OTG FS clock (for STM32L4+ series, STM32L49xxx/4Axxx, and STM32L47xxx/48xxx) x1 PLL for SAI1, ADC, RNG, SDMMC, USB FS clock (for STM32L45xxx/46xxx and STM32L43xxx/44xxx) • Each PLL provides up to 3 independent outputs • The PLL sources are MSI, HSI16, and HSE	• Main PLL for system • PLL for ADC, RNG, TIM1, TIM15, and USB FS clock • PLL provides 3 independent outputs • The PLL sources are MSI, HSI16, and HSE
System clock source	MSI, HSI16, HSE, or PLL	MSI, HSI16, HSE, PLL, LSE, or LSI
System clock frequency	• Up to 80 MHz • 4 MHz after reset using MSI	• Up to 56 MHz • 4 MHz after reset using MSI
AHB frequency	Up to 80 MHz	Up to 56 MHz
APB1 frequency	Up to 80 MHz	Up to 56 MHz (APB)
APB2 frequency	Up to 80 MHz	Up to 56 MHz (APB)
RTC clock source	LSI, LSE, or HSE/32	
MCO clock source	MCO pin (PA8): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI, or HSI48 With configurable prescaler, 1, 2, 4, 8, or 16 for each output (except STM32L47xxx/48xxx devices)	MCO pin (multiple pins): SYSCLK, HSI16, HSE, PLLCLK, MSI, LSE, LSI, HSI48, RTCCLK, RTCWAKEUP. MCO1 and MCO2 are available. With configurable prescaler, 1, 2, 4, 8, or 16 for each output
CSS	• CSS (clock security system) • CSS on LSE	
Internal oscillator measurement/ calibration	• LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision • LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision • HSE/32 and MSI connected to TIM17 CH1 IC • HSE/32 and MSI connected to TIM16 CH1 IC (STM32L43xxx/44xxx/45xxx//46xxx)	• Mainly replacing TIM17 in the STM32L4 series by TIM16 in the STM32U0 series • LSE connected to TIM15 or TIM16 CH1 IC: can measure HSI16 or MSI with respect to LSE clock high precision • LSI connected to TIM16 CH1 IC: can measure LSI with respect to HSI16 or HSE clock precision • HSE/32 and MSI connected to TIM16 CH1 IC
Interrupt	• CSS (linked to NMI IRQ) • LSECSS • LSIRDY, LSERDY, HSIRDY, MSIRDY, HSERDY, and PLLRDY (linked to RCC global IRQ)	

7.5.1 Performance versus V_{CORE} ranges

On the STM32L4 series, the maximum CPU clock frequency and the flash memory wait state depend on the selected V_{CORE} voltage range and the selected V_{DD} range.

Table 22 presents the different clock source frequencies depending on different product voltage ranges.

Table 22. Performance versus V_{CORE} ranges for STM32L4 and STM32U0 series

WS = wait state.

CPU performance	Power performance	V_{CORE} range	Typical Value (V)	Max frequency (MHz)					V_{DD} range
				4 WS	3 WS	2 WS	1 WS	0 WS	
STM32L4 series									
High	Medium	1	1.2	80	-	56	48	24	1.71 to 3.6
Medium	High	2	1.0	26	-	18	16	8	1.71 to 3.6
STM32U0 series									
High	Medium	1	1.2	80	-	56	48	24	1.71 to 3.6
Medium	High	2	1.0	26	-	18	16	8	1.71 to 3.6

7.5.2 Peripheral access configuration

The address mapping of several peripherals has changed for the STM32U0 series compared to the STM32L4 series, so different registers must be used to enable/disable or enter/exit the peripheral clock or Reset mode (refer to Table 23).

STM32U0 devices have only one AHB and one APB, resulting in the mapping of AHBx to AHB and APBx to APB.

Table 23. RCC registers used for peripheral access configuration for STM32L4 and STM32U0 series

Bus	Register STM32L4 series	Register STM32U0 series	Comments
AHB	RCC_AHB1RSTR (AHB1) RCC_AHB2RSTR (AHB2) RCC_AHB3RSTR (AHB3)	RCC_AHBRSTR	Used to enter/exit the AHB peripheral from reset.
	RCC_AHB1ENR (AHB1) RCC_AHB2ENR (AHB2) RCC_AHB3ENR (AHB3)	RCC_AHBENR	Used to enable/disable the AHB peripheral clock.
	RCC_AHB1SMENR (AHB1) RCC_AHB2SMENR (AHB2) RCC_AHB3SMENR (AHB3)	RCC_AHBSMENR	Used to enable/disable the AHB peripheral clock in Sleep mode.
APB	RCC_APB1RSTR1 RCC_APB1RSTR2	RCC_APBRSTR1 RCC_APBRSTR2	Used to enter/exit the APB1 peripheral from reset.
	RCC_APB1ENR1 RCC_APB1ENR2	RCC_APBENR1 RCC_APBENR2	Used to enable/disable the APB1 peripheral clock.
	RCC_APB1SMENR1 RCC_APB1SMENR2	RCC_APBSMENR1 RCC_APBSMENR2	Used to enable/disable the APB1 peripheral clock in Sleep mode.
APB2	RCC_APB2RSTR	NA	Used to enter/exit the APB2 peripheral from reset.
	RCC_APB2ENR		Used to enable/disable the APB2 peripheral clock.
	RCC_APB2SMENR		Used to enable/disable the APB2 peripheral clock in Sleep mode.

The configuration to access a given peripheral requires:

- Identifying the bus to which the peripheral is connected.
- Selecting the correct register, depending on the requested action.

For example, USART1 is connected to the APB bus. To enable the USART1 clock, the RCC_APBENR2 register needs to be configured as follows with the STM32Cube HAL driver RCC API:

```
__HAL_RCC_USART1_CLK_ENABLE();
```

To disable the USART1 clock during Sleep mode (to reduce power consumption), the RCC_APBSMENR2 register needs to be configured as follows with the STM32Cube HAL driver RCC API:

```
__HAL_RCC_USART1_CLK_SLEEP_ENABLE();
```

7.5.3 Peripheral clock configuration

Some peripherals have a dedicated clock source, independent from the system clock, which is used to generate the clock required for their operations:

- **USB:**
  - On STM32U0 devices, the USB 48 MHz clock is derived from one of the following sources:
    - The main PLL VCO (PLLUSB1CLK).
    - The MSI clock.
    - PLLSAI1 VCO (PLLUSB2CLK) can be used to provide the clock for the HSI48 internal oscillator.
- **SDIO/SDMMC:**
  - On STM32U0 devices, SDIO/SDMMC is not present.
- **RTC and LCD:**
  The RTC and the LCD glass clocks share the same clock source (RTCCLK).
  On both STM32U0 and STM32L4 devices, the RTC and the LCD glass clocks are derived from one of the three following sources: LSE clock, LSI clock, or HSE clock divided by 32. The PCLK frequency must always be greater than or equal to the RTC clock frequency.
  RTC can also be set to ultra-low-power mode by enabling the LPCAL bit to further reduce consumption.
- **ADC:**
  - On STM32L4 devices, the input clock of the two ADCs (master and slave) can be selected from two different clock sources:
    - Derived (selected by software) from the system clock (SYSCLK), PLLSAI1 VCO(1) (PLLADC1CLK), or PLLSAI2 VCO(2) (PLLADC2CLK). In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to the PREC[3:0] bits).
    - Derived from the AHB clock of the ADC bus interface, divided by a programmable factor (1, 2, or 4). In this mode, a programmable divider factor can be selected (1, 2, or 4 according to the CKMODE[1:0] bits). Refer to the STM32L4/STM32L4+ series reference manual for more details.
  - On STM32U0 devices, the input clock of the ADCs can be selected from two different clock sources:
    - Derived (selected by software) from the system clock (SYSCLK), PLLPCLK, or HSI16. In this mode, a programmable divider factor can be selected (1, 2, …, 256 according to bits PREC[3:0]).
    - Derived from the APB clock of the ADC bus interface, divided by a programmable factor (1, 2, or 4). In this mode, a programmable divider factor can be selected (1, 2, or 4 according to bits CKMODE[1:0]). Refer to the STM32U0 series reference manual for more details.
- **DAC:**
  DAC clock sources are identical on both series.
- **U(S)ART:**
  - On both series, the USART clock is derived from one of the four following sources: system clock (SYSCLK), HSI16, LSE, or APB (APB1 and APB2 for the STM32L4 series).
    Using a source clock independent from the system clock (like HSI16) allows an on-the-fly change of the system clock without reconfiguration of the USART peripheral baud rate prescalers.

- **I2C:**
  - On both series, the I2C clock is derived from one of the three following sources: system clock (SYSCLK), HSI16, or APB (PCLK) (APB1 (PCLK1) for the STM32L4 series).
    Using a source-clock independent from the system clock (like HSI16) allows an on-the-fly change of the system clock without reconfiguration of the I²C peripheral timing register.
- **I2S/SAI:**
  - I2S is not present on STM32U0 devices.

1. *Not available on STM32L41xxx/42xxx devices, which can only use SYSCLK.*
2. *PLLSAI2VCO (PLLADC2CLK) is a clock source only on STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices.*

7.6 Power control (PWR)

The PWR controller for STM32U0 devices presents some differences compared to the STM32L4 series, which are summarized in Table 24.

Table 24. PWR differences between STM32L4 and STM32U0 series

PWR	STM32L4	STM32U0
Power supplies	• V_{DD} = 1.71 to 3.6 V: external power supply for I/Os and internal regulator. • It is provided externally through VDD pins.	
	• V_{CORE} = 1.0 to 1.28 V. • V_{CORE} is the power supply for the digital peripherals, SRAM, and flash memory. • It is generated by an internal voltage regulator. • Two V_{CORE} ranges can be selected by software depending on the target frequency.	
	Independent power supplies (V_{DDA}, V_{DDUSB}) allow the improvement of power consumption by running the MCU at a lower supply voltage than analog and USB.	
	• V_{SSA}, V_{DDA} = 1.62 V (ADCs/COMPs) to 3.6 V 1.8 V (DAC/OPAMPs) to 3.6 V 2.4 V (VREFBUF) to 3.6 V • V_{DDA} is the external analog power supply for the A/D and D/A converters, voltage reference buffer, operational amplifiers, and comparators. • The V_{DDA} voltage level is independent from the V_{DD} voltage.	
	• V_{LCD} = 2.5 to 3.6 V. • The LCD controller can be powered either externally through the VLCD pin, or internally from an internal voltage generated by the embedded step-up converter.	
	• V_{DDUSB} = 3.0 to 3.6 V. • V_{DDUSB} is the external independent power supply for the USB transceivers. • The V_{DDUSB} voltage level is independent from the V_{DD} voltage.	
	• V_{DDIO2} = 1.08 V to 3.6 V. • V_{DDIO2} is the external power supply for 14 I/Os (Port G[15:2]). • The V_{DDIO2} voltage level is independent from the V_{DD} voltage. Not applicable for STM32L45xxx/46xxx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx devices.	V_{DDIO2} is not present on comparable STM32U0 devices
Battery backup domain	• V_{BAT} = 1.55 to 3.6 V: the power supply for the RTC external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present. • RTC with backup registers (up to 9 bytes). • LSE. • PC13 to PC15 I/Os. • Up to 5 tamper pins.	
Power supply supervisor	• Integrated POR/PDR circuitry. • Programmable voltage detector (PVD).	

PWR	STM32L4	STM32U0
Power supply supervisor	• Brownout reset (BOR). • BOR is always enabled, except in Shutdown mode.	
	3 peripheral voltage monitoring (PVM): • PV1 for V_{DDUSB}. • PVM3/PVM4 for V_{DDA} (~1.65 V/ ~2.2 V).	
	PVM2 for V_{DDIO2} (for STM32L4+ series, STM32L49xxx/4Axxx and STM32L47xxx/48xxx only).	NA
Low-power modes	Sleep mode	
	• Low-power run mode (up to 2 MHz). • Low-power sleep mode (up to 2 MHz). • The system clock is limited to 2 MHz, but I2C and U(S)ART/LPUART can be clocked with HSI16 at 16 MHz.	
	• Stop 0, Stop 1, and Stop 2 mode. • Some additional functional peripherals (cf. wake-up source).	
	Standby mode (V_{CORE} domain powered off) with new features: • BOR is always on. • SRAM2 content can be preserved. • Pull-up or pull-down can be applied to each I/O.	
	Shutdown mode (V_{CORE} domain powered off and power monitoring off).	
External SMPS	Support for external SMPS for high-power efficiency. (Refer to AN4978, available from www.st.com.)	NA
Wake-up sources	Sleep mode Any peripheral interrupt/wake-up event.	
	Stop mode • Any EXTI line event/interrupt. • BOR, PVD, PVM, COMP, RTC, USB, IWDG, U(S)ART, LPUART, I2C, SWP, LPTIM, LCD.	
	Standby mode • Up to 5 WKUP pins rising or falling edge. • RTC event. • External reset in NRST pin. • IWDG reset.	
	Shutdown mode • Up to 5 WKUP pins rising or falling edge. • RTC event; • External reset in NRST pin.	
Wake-up clocks	Wake-up from Stop mode HSI16 16 MHz or MSI (all ranges up to 48 MHz) allow a 5-µs wake-up at high speed without waiting for the PLL startup time.	
	Wake-up from Standby mode MSI (ranges from 1 to 8 MHz)	
	Wake-up from Shutdown mode MSI 4 MHz.	
Configuration	• 4 control registers. • 2 status registers. • 1 status clear register. • 2 registers per GPIO port for controlling pull-up and pull-down. Most configuration bits from the STM32L4 series can be found in the STM32U0 series (but some may have a different programming mode).	

7.7 Real-time clock (RTC)

The STM32U0 and STM32L4 series implement almost identical RTC features. Table 25 summarizes the differences. The embedded RTC is similar to the one embedded in STM32L41xxx/42xxx devices

Table 25. RTC differences between STM32L4 and STM32U0 series

RTC	STM32L4 series	STM32U0 series
Features	Only smooth calibration available	
	NA	• Ultra-low-power calibration saving further consumption is available when the LPCAL bit is set.
	3 tamper pins (available in VBAT)	5 tamper pins (available in VBAT)
	128-byte backup registers	Up to 9 backup registers
Configuration	NA	• Additional bit LPCAL for drastic reduction of RTC consumption. • Backup domain reset as RTC is connected to VBAT. • Modified register memory map.

For more information about the RTC features of the STM32U0 series, refer to the RTC section of the STM32U0 series reference manual.

7.8 System configuration controller (SYSCFG)

The STM32U0 and STM32L4 series implement almost identical SYSCFG features. Table 26 summarizes the differences.

Table 26. SYSCFG differences between STM32L4 and STM32U0 series

SYSCFG	STM32L4 series	STM32U0 series
SYSCFG features	• Remapping memory areas. • Managing the external interrupt line connection to the GPIOs. • Robustness management. • Configuring SRAM2 write protection and software erase. • Enabling/disabling voltage booster for I/Os analog switches. • Enabling/disabling I2C fast mode plus driving capability is now controlled by I2C directly. Registers in SYSCFG have been kept for legacy reasons.	
	• Configuring FPU interrupts. • Enabling the firewall.	NA
Configuration	NA	• Most registers from the STM32L4 series are identical in the STM32U0 series. • A few bits are different and EXTI configuration may differ (number of GPIOs is different depending on the product).

7.9 General-purpose I/O (GPIO) interface

The GPIO peripheral of the STM32U0 series embeds identical features compared to the one in the STM32L4 series.

Minor adaptations of the code written for the the STM32L4 series using the GPIO may be required on the STM32U0 due to:

- The mapping of specific functions on different GPIOs (see pinout differences in Section 4: Hardware migration).
- The additional mapping of GPIOs sharing pins with BOOT and NRST to provide more GPIOs in the same package.

The GPIOH port of STM32L4 devices is replaced by the GPIOF port on STM32U0 devices. The GPIOF port on STM32L4 devices is available only on packages with 100 pins or more, and has no replacement on STM32U0 devices.

For more information on the STM32U0 series GPIO programming and usage, refer to the *I/O pin multiplexer and mapping* section in the GPIO chapter of the STM32U0 series reference manual. For a detailed description of the pinout and alternate function mapping, refer to the product datasheets.

7.10 Extended interrupt and event controller (EXTI) source selection

The external interrupt and event controller (EXTI) is very similar in the STM32U0 and STM32L4 series. Table 27 shows the main differences.

Table 27. EXTI differences between STM32L4 and STM32U0 series

EXTI	STM32L4 series	STM32U0 series
Number of event/interrupt lines	Up to 41 lines: • 12 direct, 26 configurable on STM32L4Rxxx/4Sxxx • 15 direct, 26 configurable on STM32L49xxx/4Axxx devices • 14 direct, 26 configurable on STM32L47xxx/48xxx devices • 12 direct, 25 configurable on STM32L43xxx/44xxx and STM32L41xxx/42xxx devices	Up to 37 lines: • 16 direct • 22 configurable

7.11 Flash memory

The STM32U0 and STM32L4 series instantiate different flash memory modules, both in terms of architecture/technology and interface. Consequently, the STM32U0 series flash memory programming procedures and registers are different from those in the STM32L4 series, and any code written for the flash memory interface in the STM32L4 series needs to be rewritten to run on STM32U0 devices.

There is no dual bank flash memory option for the STM32U0 series.

Table 28 presents the differences between the flash memory interface in the STM32L4 and STM32U0 series.

For more information on programming, erasing, and protection of the STM32U0 series flash memory, refer to the STM32U0 series reference manuals.

Table 28. Flash memory differences between STM32L4 and STM32U0 series

Flash	STM32L4 series	STM32U0 series
Main/Program memory	0x0800 0000 to (up to) 0x0805 FFFF	0x0800 0000 to (up to) 0x0803 FFFF
	• Up to 1024 Kbytes • 1 or 2 banks • Each bank: up to 512 Kbytes • Sector size = 4 Kbytes	• STM32U0x3xx: – Up to 256 Kbytes – 1 bank – 128 pages of 2 Kbytes – Each page: 8 rows of 256 Kbytes • STM32U031xx: – Up to 64 Kbytes – 1 bank – 32 pages of 2 Kbytes – Each page: 8 rows of 256 bytes
	Programming and read granularity: 72-bit (including 8 ECC bits)	
Features	Read while write (RWW)	
	Dual bank boot	NA
	• ECC • Flash empty check	
	Default memory value after erase: 0x00	Default memory value after erase: 0xFF
Wait-states	Up to 5 (depending on the supply voltage and frequency)	Up to 2 (depending on the core voltage and frequency)
ART Accelerator	Allowing 0 wait state when executing from the cache.	
Data EEPROM memory	NA Can be emulated by software. For more details, refer to the application note *How to use EEPROM emulation on STM32 MCUs* (AN4894), available from www.st.com.	
System memory	• 27 Kbytes 0x1FFF 0000 to 0x1FFF 6FFF (bank1) • 27 Kbytes 0x1FFF 8000 to 0x1FFF EFFF (bank2) • Only bank1 for STM32L45xxx/46xxx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx	• 26 Kbytes 0x1FFF 0000 to 0x1FFF 67FF
One time programmable (OTP)	1 Kbyte 0x1FFF 7000 to 0x1FFF 73FF	1 Kbyte 0x1FFF 6800 to 0x1FFF 6BFF
Option bytes	factory bytes + 32 user bytes	Improved programming method with no direct access to the option byte storage area
Flash memory interface	0x4002 2000 to 0x4002 23FF	0x4002 2000 to 0x4002 23FF
	-	Different from STM32L4 series
Erase granularity	Page erase (2 Kbytes), bank erase, and mass erase (all banks)	
Read protection (RDP)	• Level 0 no protection • RDP = 0xAA	
	• Level 1 memory protection • RDP ≠ (level 2 and level 0)	
	Level 2 RDP = 0xCC	
	NA	Improved protection scheme with OEM keys allowing the secure regression of protection levels
Proprietary code readout protection (PCROP)	• 1 PCROP area per bank • Granularity: 64-bit • PCROP_RDP option: PCROP area preserved when RDP level decreased	NA

Flash	STM32L4 series	STM32U0 series
Write protection (WRP)	• Two write protection areas • Granularity: 2 Kbytes	
User option bytes	nRST_STOP	nRST_STOP
	nRST_STDBY	nRST_STDBY
	NA	nRST_SHDW
	IWDG_SW	IWDG_SW
	NA	IWDG_STOP, IWDG_STDBY
		WWDG_SW
	NA	NOT_VBAT_VDD_OPT
		RAM_PARITY_CHECK
		BKPSRAM_HW_ERASE_DISABLE
		IRHEN, NRST_MODE[1:0]
	BOR_LEV[2:0]	BOR_LEV[2:0]
	BFB2	BOOT_LOCK
	nBOOT1	
	nBOOT0	
	nSWBOOT0	nBOOT_SEL
	SRAM2_RST, SRAM2_PE	NA
	DUAL_BANK	

7.12 Universal synchronous asynchronous receiver transmitter (U(S)ART)

The STM32U0 and STM32L4 series implement similar USART features, as listed in Table 29.

Table 29. U(S)ART differences between STM32L4 and STM32U0 series

U(S)ART	STM32L4 series	STM32U0 series
Instances	• x3 USART • x2 UART for STM32L4+, STM32L49xxx/4Axxx, and STM32L47xxx/48xxx devices • x1 UART for STM32L45xxx/46xxx devices • x1 LPUART	• x4 USART • x3 LPUART
Baud rate	Up to 10 Mbit/s when the clock frequency is 80 MHz and oversampling is by 8	Up to 6 Mbit/s when the clock frequency is 48 MHz and oversampling is by 8
Clock	Dual clock domain allowing: • UART functionality and wake-up from Stop mode • Convenient baud rate programming independent from the PCLK reprogramming	
Data	• Word length: programmable (7, 8, or 9 bits) • Programmable data order with MSB-first or LSB-first shifting	
Interrupt	14 interrupt sources with flags	
Features	• RS232 hardware flow control (CTS/RTS) • Continuous communication using DMA • Multiprocessor communication • Single-wire half-duplex communication • IrDA SIR ENDEC block • LIN mode • SPI master	
	• Smartcard mode T = 0 and T = 1 is to be implemented by software	Smartcard mode not supported

U(S)ART	STM32L4 series	STM32U0 series
Features	• Number of stop bits: 0.5, 1, 1.5, 2	
Features	• Wake-up from Stop mode (start bit, received byte, address match) • Receiver timeout interrupt (except LPUART) • Auto baud rate detection (except LPUART) • Driver enable • Swappable Tx/Rx pin configuration • LPUART does not support synchronous mode (SPI master), smartcard mode, IrDA, LIN, ModBus, receiver timeout interrupt, or auto baud rate detection	
Configuration	STM32L4 and STM32U0 registers and associated bits are identical.	

7.13 Inter-integrated circuit (I2C) interface

The STM32U0 and STM32L4 series implement similar I2C features, as listed in Table 30.

Table 30. I2C differences between STM32L4 and STM32U0 series

I2C	STM32L4 series	STM32U0 series
Instances	• x3 for STM32L47xxx/48xxx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx devices • x4 for STM32L4+, STM32L49xxx/4Axxx, and STM32L45xxx/46xxx devices	• x3 for STM32U0x3xx. • x2 for STM32U031xx.
Features	• 7-bit and 10-bit addressing mode. • Standard mode (Sm, up to 100 KHz). • Fast mode (Fm, up to 400 KHz).	
	• Fast mode Plus (Fm+, up to 1 MHz). • Independent clock. • Wakeup from stop on address match.	
	• SMBus	NA
Configuration	STM32L4 and STM32U0 registers and associated bits are identical.	

7.14 Serial peripheral interface (SPI)/Inter-IC sound (I2S)

The STM32U0 and STM32L4 series implement similar SPI and I2S features, as listed in Table 31.

Table 31. SPI differences between STM32L4 and STM32U0 series

SPI	STM32L4 series	STM32U0 series
Instances	3 without I2S support	
Features	I2S is not supported by SPI	
Data size	Programmable from 4 to 16 bits.	
Data buffer	32-bit Tx & Rx FIFOs (up to 4 data frames)	
Data packing	Yes (8-, 16-, or 32-bit data access, programmable FIFO data thresholds)	
Mode	• SPI TI mode • SPI Motorola mode • NSSP mode	
Speed	40 MHz (core at 80 MHz)	24 MHz (core at 48 MHz)
Configuration	STM32L4 and STM32U0 registers and associated bits are identical.	

7.15 Cyclic redundancy check calculation unit (CRC)

The CRC calculation unit is very similar in STM32L4 and STM32U0 devices.

Table 32 shows the different CRC features.

Table 32. CRC differences between STM32L4 and STM32U0 series

CRC	STM32L4 series	STM32U0 series
Features	• Single input/output 32-bit data register. • CRC computation done in 4 AHB clock cycles (HCLK) for the 32-bit data size. • General-purpose 8-bit register (can be used for temporary storage).	
	• Fully programmable polynomial with programmable size (7, 8, 16, or 32 bits). • Handles 8-, 16-, and 32-bit data sizes. • Programmable CRC initial value. • Input buffer to avoid bus stall during calculation. • Reversibility option on I/O data.	
Configuration	The STM32L4 and STM32U0 configuration registers are identical.	

7.16 Advanced encryption standard hardware accelerator (AES)

The STM32U0 series implement several new AES features compared to the STM32L4 series, as shown in Table 33.

Table 33. AES differences between STM32L4 and STM32U0 series

AES	STM32L4 series	STM32U0 series
Features	256-bit register for storing the encryption, decryption, or derivation key (8x 32-bit registers).	
Mode	• Electronic codebook (ECB). • Cipher block chaining (CBC). • Counter mode (CTR). • Galois counter mode (GCM). • Galois message authentication code mode (GMAC). • Cipher message authentication code mode (CMAC).	
Key length	128-bit, 256-bit	
Configuration	STM32L4 and STM32U0 registers and associated bits are identical.	

7.17 Liquid-crystal display controller (LCD)

The LCD controller on the STM32U0 series implements the same features as the one on the STM32L4 series. All programmable registers and associated bits in the STM32L4 series are equivalent to the ones in the STM32U0 series.

Refer to the STM32L4 and STM32U0 series reference manuals for more details.

Note: LCD is not available on STM32U031xx devices.

7.18 Universal serial bus interface (USB)

The STM32L4 and STM32U0 series implement similar USB peripherals: they both contain a USB FS device interface.

STM32U0x3xx devices include a clock recovery system (CRS) as an additional feature. It provides a precise clock to the USB peripheral:

- When using USB device mode, the CRS allows crystal-less USB operation.
- When using USB host mode, the CRS allows low-frequency crystal (32.768 KHz) USB operations.

Most features supported by the STM32L4 series are also supported by STM32U0x3xx devices. Table 34 highlights the key differences.

Table 34. USB differences between STM32L4 and STM32U0 series

USB	STM32L4 series	STM32U0x3xx devices
Features	Universal Serial Bus Revision 2.0, including link power management (LPM) support	
	FS mode: • 1 bidirectional control endpoint • 7 IN endpoints (Bulk, Interrupt, Isochronous) • 7 OUT endpoints (Bulk, Interrupt, Isochronous)	
	Full support for USB on-the-go (USB OTG) (only on STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices)	NA
	USB internal connect/disconnect feature with an internal pull-up resistor on the USB D+ (USB_DP) line.	
	CRS allows crystal-less USB operation. Independent V_{DDUSB} power supply, allowing a lower V_{DD} while using USB.	
Mapping	• APB1 for STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices • AHB2 for STM32L45xxx/46xxx, STM32L43xxx/44xx, and STM32L41xxx/42xxx	APB
Buffer memory	• For STM32L49xxx/4Axxx and STM32L47xxx/48xxx devices: 1.25 Kbyte data FIFOs Management of up to 6 Tx FIFOs (1 for each IN end point) + 1 Rx FIFO • For STM32L45xxx/46xxx, STM32L43xxx/44xx and STM32L41xxx/42xxx devices: 1024 bytes of dedicated packet buffer memory SRAM	1024 bytes of dedicated packet buffer memory SRAM.
Low-power modes	• USB suspend and resume. • Link power management (LPM) support.	
Configuration	USB FS has similar registers on both series.	

7.19 Analog-to-digital converter (ADC)

The main ADC difference between the STM32L4 and STM32U0 series is the presence of only a single ADC instance with a slower ADC sampling rate on STM32U0 devices. Table 35 lists the different ADC features.

Table 35. ADC differences between STM32L4 and STM32U0 series

ADC	STM32L4 series	STM32U0 series
ADC type	SAR structure	
Instances	ADC1 • x3 instances for STM32L49xxx/4Axxx and STM32L47xxx/48xxx • 2 instances for STM32L41xxx/42xxx • x1 instance for STM32L45xxx/46xxx and STM32L43xxx/44xxx	ADC
Maximum sampling frequency	• 5.1 Msps for fast channels • 4.8 Msps for slow channels	2.5 Msps
Number of channels	Up to 19 channels per ADC	Up to 19 channels

ADC	STM32L4 series		STM32U0 series	
Resolution	12-bit		12-bit + digital oversampling up to 16-bit	
Conversion modes	Single/continuous/scan/ discontinuous/dual mode		Single/continuous/scan/discontinuous	
DMA	Yes			
External trigger	Yes			
	External event for regular group	External event for injected group	External event for regular group:	External event for injected group:
	TIM1 CC1	TIM1 TRGO	TIM1_TRGO2	TIM1_TRGO2
	TIM1 CC2	TIM1 CC4	TIM1_CC4	TIM1_CC4
	TIM1 CC3	TIM2 TRGO	TIM2_TRGO	TIM2_TRGO
	TIM2 CC2	TIM2 CC1	TIM3_TRGO	TIM3_TRGO
	TIM3 TRGO	TIM3 CC4	TIM15_TRGO	TIM15_TRGO
	TIM4 CC4	TIM4 TRGO	TIM6_TRGO	TIM6_TRGO
	EXTI line 11	EXTI line15	EXTI11	EXTI11
	TIM8_TRGO	TIM8_CC4		
	TIM8_TRGO2	TIM1_TRGO2		
	TIM1_TRGO	TIM8_TRGO		
	TIM1_TRGO2	TIM8_TRGO2		
	TIM2_TRGO	TIM3_CC3		
	TIM4_TRGO	TIM3_TRGO		
	TIM6_TRGO	TIM3_CC1		
	TIM15_TRGO	TIM6_TRGO		
	TIM3_CC4	TIM15_TRGO		
Supply requirement	• 1.62 V to 3.6 V. • Independent power supply (V_{DDA}).			
Reference voltage	Reference voltage for STM32U0 series external (2.0 V to V_{DDA}) or internal (2.048 V or 2.5 V).			
Electrical parameters	Consumption proportional to conversion speed: 200 uA/Msps (typ.).			
Input range	$V_{REF-} \leq V_{AIN} \leq V_{REF+}$			

7.20 Digital-to-analog converter (DAC)

The STM32U0 series implement an enhanced DAC compared to the STM32L4 series. Table 36 shows the differences.

Table 36. DAC differences between STM32L4 and STM32U0 series

DAC	STM32L4 series	STM32U0 series
Number of channels	• 1 on STM32L45xx/STM32L46xx • 2 on STM32L43xxx/44xxx, STM32L47xx/ 48xx, and STM32L49xxx/4Axxx • No DAC for other devices	1
Resolution	12-bit	
Features	• Left or right data alignment in 12-bit mode • Noise-wave and triangular-wave generation • Buffer offset calibration • DAC1_OUTx can be disconnected from output pin • Sample and hold mode for low-power operation in Stop mode	

DAC	STM32L4 series	STM32U0 series
Features	DAC with 2 channels for independent or simultaneous conversions	DAC with 1 channel only
DMA	Yes	
External trigger	Yes	
	• TIM6 TRGO • TIM8 TRGO • TIM7 TRGO • TIM5 TRGO • TIM2 TRGO • TIM4 TRGO • EXTI line9 • SW TRIG	• TIM1_TRGO_CKTIM • TIM2_TRGO_CKTIM • TIM3_TRGO_CKTIM • TIM6_TRGO_CKTIM • TIM7_TRGO_CKTIM • TIM15_TRGO_CKTIM • LPTIM1_OUT • LPTMI2_OUT • EXTI line9 • SW TRIG
Supply requirement	• 1.8 V to 3.6 V • Independent power supply (V_{DDA})	
Reference voltage	Reference voltage for STM32U0 and STM32L4 series external (1.8 V to V_{DDA}) or internal (2.048 V or 2.5 V)	
Configuration	Software compatible	

7.21 Comparators (COMP)

Table 37 presents the differences in the COMP interface of the STM32L4 and STM32U0 series.

Table 37. COMP differences between STM32L4 and STM32U0 series

COMP	STM32L4 series	STM32U0 series
Type	• COMP1 • COMP2 rail-to-rail	• COMP1 • COMP2 rail-to-rail
Inputs	COMP1: • Non inverting: 2 (PC5, PB2) • Inverting: 8 (PB1,PC3, DAC1_OUT1/2,V_{REFINT} x 1, 3/4, 1/2, 1/4)	COMP1: • Non inverting: 4 (PA6, PB2, PC5, PC6) • Inverting: 8 (PA0, PA1, PA4, PA5, PC4, PB1, DAC1_OUT1/2, V_{REFINT} x 1, 3/4, 1/2, 1/4)
	COMP2: • Non inverting: 2 (PB4, PB6) • Inverting: 8 (PB3, PB7, DAC1_OUT1/2, V_{REFINT} x 1, 3/4, 1/2, 1/4)	COMP2: • Non inverting: 4 (PA3, PB4, PB6, PD10) • Inverting: 8 (PA2, PA4, PA5, PB3, PB7, DAC1_OUT1/2, V_{REFINT} x 1, ¾, ½, ¼)
Outputs	• Generation of break input signals for timers through GPIO alternate function • TIM1/TIM8 (for STM32L4+ series, STM32L49xxx/4Axxx, and STM32L47xxx/48xxx) • TIM1 (STM32L45xxx/46xxx and STM32L43xxx/44xxx) • Generation of wakeup interrupt or events (EXTI line)	• Generation of break input signals for timers through GPIO alternate function • Generation of wakeup interrupt or events (EXTI line)
Features	Window comparator	
	• Output with blanking source • Programmable hysteresis	
	Programmable speed/consumption (COMP1/COMP2)	

COMP	STM32L4 series	STM32U0 series
Supply requirement	1.62 V to 3.6 V	
Input range	$V_{REF-} \leq V_{IN} \leq V_{REF+}$	

7.22 Operational amplifiers (OPAMP)

The STM32U0 and STM32L4 series implement similar OPAMP features, as listed in Table 38.

Table 38. OPAMP features on series

OPAMP	STM32L4 series	STM32U0 series
Instances	• x2 for STM32L4+, STM32L49xxx/4Axxx, and STM32L47xxx/48xxx devices • x1 for STM32L45xxx/46xxx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx devices	1
Features	• Rail-to-rail input and output voltage range • Low input bias current • Low input offset voltage • Low-power mode • Fast wakeup time • Gain bandwidth of 1 MHz • Programmable gain amplifier (PGA)	

8 Software migration

8.1 STM32 Cortex®-M0+ processor and core peripherals

The Cortex®-M0+ processor is an entry-level 32-bit Arm® Cortex® processor designed for a broad range of embedded applications. It offers significant benefits to developers, including:

- A simple architecture that is easy to learn and program
- Ultra-low-power, energy-efficient operation
- Excellent code density
- Deterministic, high-performance interrupt handling
- Upward compatibility with Cortex®-M processor family
- Platform security robustness, with optional integrated memory protection unit (MPU)

The Cortex®-M0+ processor is built on a 32-bit processor core that is highly optimized for area and power, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier.

The Cortex®-M0+ processor implements the Armv6-M architecture, which is based on the 16-bit Thumb® instruction set and includes Thumb-2 technology. This provides the exceptional performance expected of a modern 32-bit architecture, with a higher code density than other 8-bit and 16-bit microcontrollers.

The Cortex®-M0+ processor closely integrates a configurable nested vectored interrupt controller (NVIC), to deliver industry-leading interrupt performance. The NVIC:

- Includes a non-maskable interrupt (NMI).
- Provides zero jitter interrupt option.
- Provides four interrupt priority levels.

The tight integration of the processor core and NVIC provides fast execution of interrupt service routines (ISRs), dramatically reducing the interrupt latency. This is achieved through the hardware stacking of registers, and the ability to abandon and restart load-multiple and store-multiple operations. Interrupt handlers do not require any assembler wrapper code, removing any code overhead from the ISRs. Tail-chaining optimization also significantly reduces the overhead when switching from one ISR to another.

To optimize low-power designs, the NVIC integrates with the sleep modes that include a deep-sleep function that enables the entire device to be rapidly powered down.

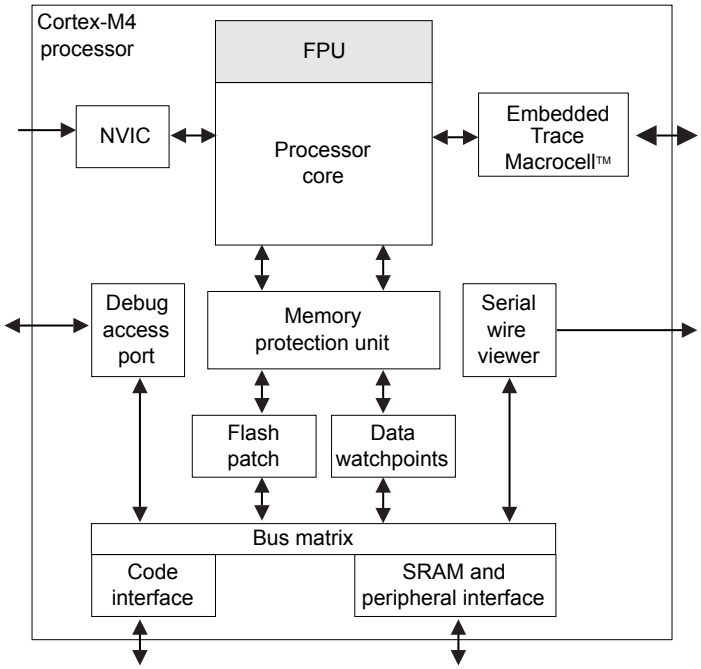
8.2 STM32 Cortex®-M4 processor and core peripherals

The Cortex®-M4 processor is a high-performance 32-bit processor designed for the microcontroller market. It offers significant benefits to the developers, including:

- Outstanding processing performance combined with fast interrupt handling
- Enhanced system debug with extensive breakpoint and trace capabilities
- Efficient processor core, system, and memories
- Ultra-low power consumption with integrated sleep modes
- Platform security robustness, with optional integrated memory protection unit (MPU)

The Cortex®-M4 processor is built on a high-performance processor core, with a three-stage pipeline Harvard architecture, making it ideal for demanding embedded applications. The processor delivers an exceptional power efficiency through an efficient instruction set and extensively optimized design, providing high-end processing hardware including IEEE754-compliant single-precision floating-point computation, a range of single-cycle and SIMD multiplication and multiply-with-accumulate capabilities, a saturating arithmetic, and dedicated hardware division.

Figure 1. **STM32 Cortex®-M4 implementation**



Cortex®-M4 key features

- Architecture 32 bits RISC ARMv7E-M
- Three-stage pipeline with branch speculation
- Instruction set:
  - Thumb, Thumb-2
  - Hardware multiply, hardware divide, saturated arithmetic
  - DSP extensions:
    - Single cycle 16/32-bit MAC
    - Single cycle dual 16-bit MAC
    - 8/16-bit SIMD arithmetic
  - FPU (VFPv4-SP)

8.3 Software point of view

The embedded Cortex®-M0+ core does not support all instructions and capabilities of the Cortex®-M4 core. Therefore, software must be recompiled for this core. Additionally, the set is less efficient, so execution performance is lower. The missing FPU impacts the speed of arithmetic operations.

8.4 Cortex mapping overview

Except for the floating point unit, the mapping is similar on the Cortex®-M4 and Cortex®-M0+ processors. The table below summarizes the differences.

Table 39. Cortex mapping overview for STM32L4 and STM32U0 series

Cortex		STM32L4 series	STM32U0 series
Core	Architecture	Cortex®-M4	Cortex®-M0+
	Nested vectored interrupt controller (NVIC)	• 91 (STM32L49xxx/4Axxx) • 82 (STM32L47xxx/48xxx) • 67 (STM32L45xxx/46xxx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx)	32 maskable interrupt channels
	Extended interrupts and events controller (EXTI)	• Up to 41 event/interrupt (STM32L49xxx/4Axxx) • Up to 40 event/interrupt (STM32L47xxx/48xxx) • Up to 37 event/interrupt (STM32L45xxx/46xxx, STM32L43xxx/44xxx, and STM32L41xxx/42xxx)	Up to 38 event/interrupt
Mapping	System timer	0xE000 E010 to 0xE000 E01F	0xE000 E010 to 0xE000 E01F
	Nested vectored interrupt controller	0xE000 E100 to 0xE000 E4EF	0xE000 E100 to 0xE000 E4EF
	System control block	0xE000 ED00 to 0xE000 ED3F	0xE000 ED00 to 0xE000 ED3F
	Floating point unit coprocessor access control	0xE000 ED88 to 0xE000 ED8B	NA
	Memory protection unit	0xE000 ED90 to 0xE000 EDB8	0xE000 ED90 to 0xE000 EDB8
	Nested vectored interrupt controller	0xE000 EF00 to 0xE000 EF03	0xE000 EF00 to 0xE000 EF03
	Floating point unit	NA	NA

8.5 Security improvements

STM32U0 brings significant improvements in the security domain, like robust read-out protection (RDP) with three protections level states, password-based regression (128-bit PSWD), hardware protection feature (HDP), and more. The application note *Introduction to STM32 microcontrollers security* (AN5156, available from www.st.com) provides detailed descriptions of these features.

Revision history

Table 40. **Document revision history**

Date	Version	Changes
14-Feb-2025	1	Initial release

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