STPMIC25 application hints

1. How to connect unused PINs

In some STPMIC25 + STM32MP25x lines MPU applications, not all the peripherals and functions may be required, and to minimize any possible issues and useless power consumption, the relative pins must be connected correctly.

The following tables provide guidance on how to connect unused pins of the STPMIC25, and they are valid for all pins except V_{IN}, V_{IO}, and all GNDs.

Note 1: To avoid any damage to the STPMIC25, the V_{IN} must be the first and the highest input supply. VBUS input voltage can be applied before the V_{IN}.

Note 2: The DC-DC converter input pins (pins #20, #24, #25, #38, #39, #49, and #50) cannot be separated from the main input pin (pin #11).

Figure 1. Pin configuration WFQFN 56L top view

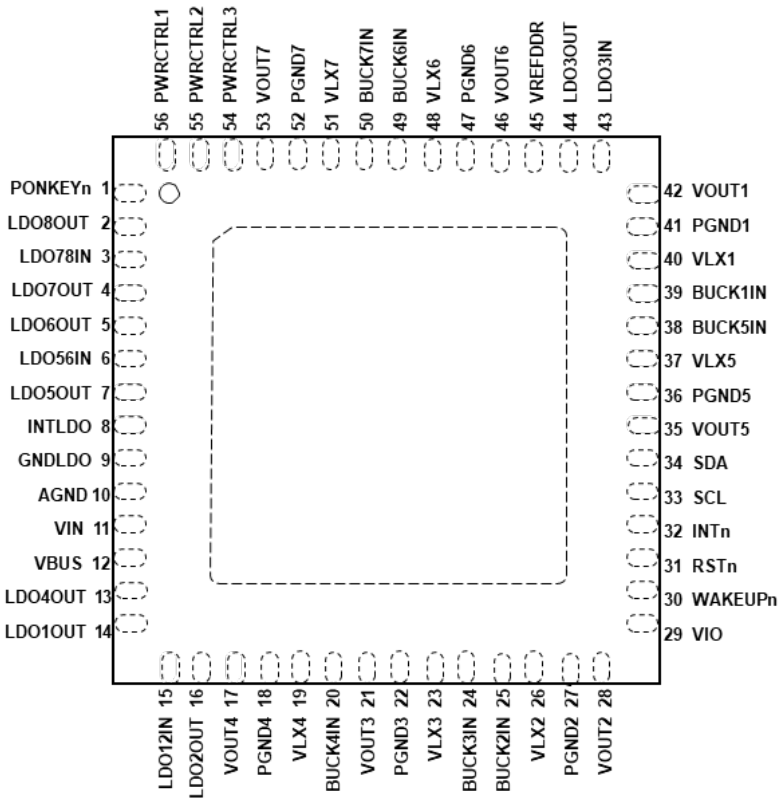

Table 1 shows the possible configuration of the STPMIC25 input/output digital pins if they are not used in the final application:

Table 1. STPMIC25 digital pin configuration

Pin number	Pin name	Type	If not used
1	PONKEYn	I	Floating
30	WAKEUPn	I	Floating
31	RSTn	I/O	Floating
32	INTn	O	Floating
33	SCL	I	VIO
34	SDA	I/O	VIO
54	PWRCTRL3	I	Floating
55	PWRCTRL2	I	Floating
56	PWRCTRL1	I	Floating

Table 1 shows the possible configuration of the STPMIC25 input/output analog pins if they are not used in the final application:

Table 2. STPMIC25 power analog I/O pin configuration

Pin number	Pin name	Type	If not used
2	LDO8OUT	O	Floating
3	LDO78IN	I	VIN
4	LDO7OUT	O	Floating
5	LDO6OUT	O	Floating
6	LDO56IN	I	VIN
7	LDO5OUT	O	Floating
12	VBUS	I	Floating
13	LDO4OUT	O	Floating
14	LDO1OUT	O	Floating
15	LDO12IN	I	VIN
16	LDO2OUT	O	Floating
17	VOUT4	I	Floating
19	VLX4	O	Floating
20	BUCK4IN	I	VIN
21	VOUT3	I	Floating
23	VLX3	O	Floating
24	BUCK3IN	I	VIN
25	BUCK2IN	I	VIN
26	VLX2	O	Floating
28	VOUT2	I	Floating
35	VOUT5	I	Floating
37	VLX5	O	Floating
38	BUCK5IN	I	VIN
39	BUCK1IN	I	VIN

Pin number	Pin name	Type	If not used
40	VLX1	O	Floating
42	VOUT1	I	Floating
43	LDO3IN	I	VIN
44	LDO3OUT	O	Floating
45	VREFDDR	O	Floating
46	VOUT6	I	Floating
48	VLX6	O	Floating
49	BUCK6IN	I	VIN
50	BUCK7IN	I	VIN
51	VLX7	O	Floating
53	VOUT7	I	Floating

If the passive components (inductors, capacitors) of the unused LDOs and BUCK converters are not mounted (for cost constraints, to reduce the occupied area around the STPMIC25, etc.), it is mandatory to disable these IPs, setting their respective ranks to 0 in the NVM memory of STPMIC25. This avoids the risk of any possible oscillation or other saturation of the internal circuitry, and at each power ON cycle the unused IPs are not automatically turned ON.

2. STPMIC25 default NVM content shadow register map

Below table shows the default NVM content shadow register map of STPMIC25A, STPMIC25B and STPMIC25D versions.

Table 3. STPMIC25 NVM shadow register map

Reg (Hex)	Register Name	R/W	STPMIC25A/B/D default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x90	NVM_MAIN_CTRL_SHR1	R/W		VINOK_HYST[1:0]		VINOK_RISE[1:0]		NVM_WDG_TMR_SET[1:0]		NVM_WDG_EN	AUTO_TURNON
			A: 0xF1	1	1	1	1	0	0	0	1
			B: 0xD1	1	1	0	1	0	0	0	1
			D: 0xF1	1	1	1	1	0	0	0	1
0x91	NVM_MAIN_CTRL_SHR2	R/W		RANK_DLY[1:0]		RST_DLY[1:0]		NVM_PKEY_LKP_CONFIG[1:0]		NVM_PKEY_LKP_TMR[1:0	
			A: 0x0A	0	0	0	0	1	0	1	0
			B: 0x0A	0	0	0	0	1	0	1	0
			D: 0x0A	0	0	0	0	1	0	1	0
0x92	NVM_RANK_CTRL_SHR1	R/W		-	-	BUCK2_RANK[2:0]			BUCK1_RANK[2:0]		
			A: 0x13	0	0	0	1	0	0	1	1

Reg (Hex)	Register Name	R/W	STPMIC25A/B/D default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x92	NVM_RANK_CTRL_SHR1	R/W	B: 0x13	0	0	0	1	0	0	1	1
			D: 0x13	0	0	0	1	0	0	1	1
0x93	NVM_RANK_CTRL_SHR2	R/W		-	-	BUCK3_RANK[2:0]			BUCK3_RANK[2:0]		
			A: 0x08	0	0	0	0	1	0	0	0
			B: 0x08	0	0	0	0	1	0	0	0
			D: 0x08	0	0	0	0	1	0	0	0
0x94	NVM_RANK_CTRL_SHR3	R/W		-	-	BUCK6_RANK[2:0]			BUCK5_RANK[2:0]		
			A: 0x03	0	0	0	0	0	0	1	1
			B: 0x03	0	0	0	0	0	0	1	1
			D: 0x03	0	0	0	0	0	0	1	1
0x95	NVM_RANK_CTRL_SHR4	R/W		-	-	REFDDR_RANK[2:0]			BUCK7_RANK[2:0]		
			A: 0x04	0	0	0	0	0	1	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x04	0	0	0	0	0	1	0	0
0x96	NVM_RANK_CTRL_SHR5	R/W		-	-	LDO2_RANK[2:0]			LDO1_RANK[2:0]		
			A: 0x21	0	0	1	0	0	0	0	1
			B: 0x21	0	0	1	0	0	0	0	1
			D: 0x21	0	0	1	0	0	0	0	1
0x97	NVM_RANK_CTRL_SHR6	R/W		-	-	LDO4_RANK[2:0]			LDO3_RANK[2:0]		
			A: 0x28	0	0	1	0	1	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
			D: 0x28	0	0	1	0	1	0	0	0
0x98	NVM_RANK_CTRL_SHR7	R/W		-	-	LDO6_RANK[2:0]			LDO5_RANK[2:0]		
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0

Reg (Hex)	Register Name	R/W	STPMIC25A/B/D default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x99	NVM_RANK_CTRL_SHR8	R/W		-	-	LDO8_RANK[2:0]			LDO7_RANK[2:0]		
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x24	0	0	1	0	0	1	0	0
0x9A	NVM_BUCK_MODE_SHR1	R/W		BUCK4_PREG_MODE[1:0]		BUCK3_PREG_MODE[1:0]		BUCK2_PREG_MODE[1:0]		BUCK1_PREG_MODE[1:0]	
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0x9B	NVM_BUCK_MODE_SHR2	R/W		-	-	BUCK7_PREG_MODE[1:0]		BUCK6_PREG_MODE[1:0]		BUCK5_PREG_MODE[1:0]	
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0x9C	NVM_BUCK1_VOUT_SHR	R/W		-	NVM_VOUT[6:0]						
			A: 0x1E	0	0	0	1	1	1	1	0
			B: 0x1E	0	0	0	1	1	1	1	0
			D: 0x1E	0	0	0	1	1	1	1	0
0x9D	NVM_BUCK2_VOUT_SHR	R/W		-	NVM_VOUT[6:0]						
			A: 0x20	0	0	1	0	0	0	0	0
			B: 0x20	0	0	1	0	0	0	0	0
			D: 0x20	0	0	1	0	0	0	0	0
0x9E	NVM_BUCK3_VOUT_SHR	R/W		-	NVM_VOUT[6:0]						
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0x9F	NVM_BUCK4_VOUT_SHR	R/W		-	NVM_VOUT[6:0]						
			A: 0x76	0	1	1	1	0	1	1	0
			B: 0x67	0	1	1	0	0	1	1	1

Reg (Hex)	Register Name	R/W	STPMIC25A/B/D default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0x9F	NVM_BUCK4_VOUT_SHR	R/W	D: 0x76	0	1	1	1	0	1	1	0
0xA0	NVM_BUCK5_VOUT_SHR	R/W		-	NVM_VOUT[6:0]						
			A: 0x67	0	1	1	0	0	1	1	1
			B: 0x67	0	1	1	0	0	1	1	1
			D: 0x67	0	1	1	0	0	1	1	1
0xA1	NVM_BUCK6_VOUT_SHR	R/W		-	NVM_VOUT[6:0]						
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xA2	NVM_BUCK7_VOUT_SHR	R/W		-	NVM_VOUT[6:0]						
			A: 0x76	0	1	1	1	0	1	1	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x76	0	1	1	1	0	1	1	0
0xA3	NVM_LDO2_SHR	R/W		-	NVM_BYPASS	NVM_VOUT[4:0]					-
			A: 0x30	0	0	1	1	0	0	0	0
			B: 0x28	0	0	1	0	1	0	0	0
			D: 0x30	0	0	1	1	0	0	0	0
0xA4	NVM_LDO3_SHR	R/W		SNK-SRC	NVM_BYPASS	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xA5	NVM_LDO5_SHR	R/W		-	NVM_BYPASS	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0

Reg (Hex)	Register Name	R/W	STPMIC25A/B/D default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0xA6	NVM_LDO6_SHR	R/W		-	NVM_BYPASS	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xA7	NVM_LDO7_SHR	R/W		-	NVM_BYPASS	NVM_VOUT[4:0]					-
			A:0x00	0	0	0	0	0	0	0	0
			B:0x00	0	0	0	0	0	0	0	0
			D:0x40	0	1	0	0	0	0	0	0
0xA8	NVM_LDO8_SHR	R/W		-	NVM_BYPASS	NVM_VOUT[4:0]					-
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x40	0	1	0	0	0	0	0	0
0xA9	NVM_PD_SHR1	R/W		NVM_BUCK4_PD[1:0]		NVM_BUCK3_PD[1:0]		NVM_BUCK2_PD[1:0]		NVM_BUCK1_PD[1:0]	
			A: 0x55	0	1	0	1	0	1	0	1
			B: 0x55	0	1	0	1	0	1	0	1
			D: 0x55	0	1	0	1	0	1	0	1
0xAA	NVM_PD_SHR2	R/W		NVM_REFDDR_PD	-	NVM_BUCK7_PD[1:0]		NVM_BUCK6_PD[1:0]		NVM_BUCK5_PD[1:0]	
			A: 0x99	1	0	0	1	1	0	0	1
			B: 0x99	1	0	0	1	1	0	0	1
			D: 0x99	1	0	0	1	1	0	0	1
0xAB	NVM_PD_SHR3	R/W		NVM_LDO8_PD	NVM_LDO7_PD	NVM_LDO6_PD	NVM_LDO5_PD	NVM_LDO4_PD	NVM_LDO3_PD	NVM_LDO2_PD	NVM_LDO1_PD
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
			D: 0xFF	1	1	1	1	1	1	1	1
0xAC	NVM_BUCKS_IOUT_SHR1	R/W		BUCK4_ILIM[1:0]		BUCK3_ILIM[1:0]		BUCK2_ILIM[1:0]		BUCK1_ILIM[1:0]	
			A: 0xBD	1	0	1	1	1	1	0	1

Reg (Hex)	Register Name	R/W	STPMIC25A/B/D default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0xAC	NVM_BUCKS_IOUT_SHR1	R/W	B: 0x7D	0	1	1	1	1	1	0	1
			D: 0xBD	1	0	1	1	1	1	0	1
0xAD	NVM_BUCKS_IOUT_SHR2	R/W		HICCUP_DLY[1:0]		BUCK7_ILIM[1:0]		BUCK6_ILIM[1:0]		BUCK5_ILIM[1:0]	
			A: 0x79	0	1	1	1	1	0	0	1
			B: 0x79	0	1	1	1	1	0	0	1
			D: 0x79	0	1	1	1	1	0	0	1
0xAE	NVM_LDOS_IOUT_SHR1	R/W		LDO7_ILIM[1:0]		LDO6_ILIM[1:0]		LDO5_ILIM[1:0]		LDO2_ILIM[1:0]	
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
			D: 0xFF	1	1	1	1	1	1	1	1
0xAF	NVM_FS_OCP_SHR1	R/W		NVM_FS_OCP_REFDDR	NVM_FS_OCP_BUC K7	NVM_FS_OCP_BUCK6	NVM_FS_OCP_BUCK5	NVM_FS_OCP_BUCK4	NVM_FS_OCP_BUCK3	NVM_FS_OCP_BUCK2	NVM_FS_OCP_BUCK1
			A: 0x1B	0	0	0	1	1	0	1	1
			B: 0x1B	0	0	0	1	1	0	1	1
			D: 0x1B	0	0	0	1	1	0	1	1
0xB0	NVM_FS_OCP_SHR2	R/W		NVM_FS_OCP_LDO8	NVM_FS_OCP_LDO7	NVM_FS_OCP_LDO6	NVM_FS_OCP_LDO5	NVM_FS_OCP_LDO4	NVM_FS_OCP_LDO3	NVM_FS_OCP_LDO2	NVM_FS_OCP_LDO1
			A: 0x01	0	0	0	0	0	0	0	1
			B: 0x01	0	0	0	0	0	0	0	1
			D: 0x01	0	0	0	0	0	0	0	1
0xB1	NVM_FS_SHR1	R/W		VIN_FLT_CNT_MAX[3:0]				PKEY_FLT_CNT_MAX[3:0]			
			A: 0xFF	1	1	1	1	1	1	1	1
			B: 0xFF	1	1	1	1	1	1	1	1
			D: 0xFF	1	1	1	1	1	1	1	1
0xB2	NVM_FS_SHR2	R/W		TSHDN_FLT_CNT_MAX[3:0]				OCP_FLT_CNT_MAX[3:0]			
			A: 0xFF	1	1	1	1	1	1	1	1

Reg (Hex)	Register Name	R/W	STPMIC25A/B/D default NVM shadow register map								
			(1) Hex	BITS[7:0]							
				7	6	5	4	3	2	1	0
0xB2	NVM_FS_SHR2	R/W	B: 0xFF	1	1	1	1	1	1	1	1
			D: 0xFF	1	1	1	1	1	1	1	1
0xB3	NVM_FS_SHR3	R/W		-	FS_LOCK_DIS	RST_FLT_CNT_TMR[1:0]		WDG_FLT_CNT_MAX[3:0]			
			A: 0x7F	0	1	1	1	1	1	1	1
			B: 0x7F	0	1	1	1	1	1	1	1
			D: 0x7F	0	1	1	1	1	1	1	1
0xB5	NVM_I²C_ADDR_SHR	R/W		LOCK_NVM	I2C_ADDR[6:0]						
			A: 0x33	0	0	1	1	0	0	1	1
			B: 0x33	0	0	1	1	0	0	1	1
			D: 0x33	0	0	1	1	0	0	1	1
0xB6	NVM_USER_SHR1	R/W		NVM_USER1[7:0]							
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0
0xB7	NVM_USER_SHR2	R/W		NVM_USER2[7:0]							
			A: 0x00	0	0	0	0	0	0	0	0
			B: 0x00	0	0	0	0	0	0	0	0
			D: 0x00	0	0	0	0	0	0	0	0

1. *This column contains the STPMIC25 default values of NVM content shadow register for STPMIC25A/B/D versions in hexadecimal format.*

Revision history

Table 4. **Document revision history**

Date	Version	Changes
14-May-2024	1	Initial release.
07-Nov-2024	2	Added new Section 2. STPMIC25 default NVM content shadow register map .

Contents

List of figures