The STPMIC25 BOM details

STPMIC25 features

The STPMIC25 is a fully integrated power management IC designed for applications in the STM32MP2x MPU family requiring low power and high efficiency.

The device integrates advanced low power features controlled by a host processor via I²C and IO interfaces.

The STPMIC25 regulators are designed to supply power to the application processor as well as to the external system peripherals such as: DDR, flash memories, and other system devices.

Seven buck SMPS are optimized to provide an excellent transient response and an output voltage precision for a wide range of operating conditions. Very high efficiency in the full output load range is achieved through low power (LPM) and high power (HPM) mode selection.

All the buck converters allow a smooth transition from LPM to HPM and they regulate the output voltage using an advanced PWM phase shift synchronization technique with integrated PLL (low noise and reduced EMI).

The main features of the STPMIC25 are as follows:

- Input voltage range from 2.8 V to 5.5 V
- 7 buck converters with adaptive constant on-time (COT) topology
- 2 MHz switching frequency
- Selectable forced PWM
- Spread spectrum function
- Phase shift synchronization
- 6 adjustable general purpose LDOs
- 1 LDO for DDR4 termination (sink-source), bypass mode for lpDDR or as general purpose LDO
- 1 LDO for USB PHY supply with automatic power source detection
- 1 reference voltage LDO for DDR memory
- User programmable non-volatile memory (NVM), enabling scalability to support a wide range of applications
- Immediate output alternate settings toggle via dedicated power control pins
- Programmable output voltages turn ON/OFF sequences.
- I²C and digital IO control interfaces
- Advanced customizable safety management
- WFQFN 56L (6.5 x 6.5 x 0.9 mm)

Typical applications of the STPMIC25 are:

- Power management for embedded microprocessor units
- Wearable and IoT
- Portable devices
- Human machine interfaces
- Smart home
- Power management unit companion chip of the STM32MP2 MPU family

1 Device configuration table

The STPMIC25 has a non-volatile memory (NVM) that enables scalability to support a wide range of applications:

- Default output voltage, POWER_UP/POWER_DOWN sequence, protection behavior, auto turn-on functionality, and I²C slave address.
- The STPMIC25A and STPMIC25B are pre-programmed devices to support the STM32MP2 series application processor versions.
- Straightforward NVM (re)programming via I²C to facilitate mass production directly in target applications.
- Possibility to lock NVM content to prevent further (re)programming by writing the LOCK_NVM bit.

Table 1. STPMIC25 default configuration table

IP	STPMIC25A			STPMIC25B		
	Default output voltage	Mode	Rank	Default output voltage	Mode	Rank
LDO1	1.80 V	-	1	1.80 V	-	1
LDO2	3.30 V	-	4	2.90 V	-	4
LDO3	NA	NA	0	NA	NA	0
LDO4	3.30 V	-	5	3.30 V	-	5
LDO5	NA	NA	0	NA	NA	0
LDO6	NA	NA	0	NA	NA	0
LDO7	NA	NA	0	NA	NA	0
LDO8	NA	NA	0	NA	NA	0
VREFDDR	NA	NA	0	NA	NA	0
BUCK1	0.80 V	HP mode	3	0.80 V	HP mode	3
BUCK2	0.82 V	HP mode	2	0.82 V	HP mode	2
BUCK3	NA	NA	0	NA	NA	0
BUCK4	3.30 V	HP mode	1	1.80 V	HP mode	1
BUCK5	1.80 V	HP mode	3	1.80 V	HP mode	3
BUCK6	NA	NA	0	NA	NA	0
BUCK7	3.30 V	HP mode	4	NA	NA	0
VINOK_Rise	4.00 V	-	-	3.30 V	-	-
VINOK_hyst	0.50 V	-	-	0.50 V	-	-

The startup sequence is split into four steps (Rank0 to Rank5).

Each BUCK converter or LDO regulator can be programmed to be automatically turned ON in one of these phases. Each rank phase is separated by a delay, which by default is 1.5 ms. This rank delay can be programmed in NVM (Reg0x91[7:6]) between 1.5 ms, 3 ms, 4.5 ms, or 6 ms.

- Rank = 0: rail not turned ON automatically, no output voltage appears after POWER-UP sequence
- Rank = 1: rail automatically turned ON after 7 ms (default), following a Turn_ON condition
- Rank = 2: rail automatically turned ON after a further 1.5 ms compared to Rank1 output rails
- Rank = 3: rail automatically turned ON after a further 1.5 ms compared to Rank2 output rails
- Rank = 4: rail automatically turned ON after a further 1.5 ms compared to Rank3 output rails
- Rank = 5: rail automatically turned ON after a further 1.5 ms compared to Rank4 output rails

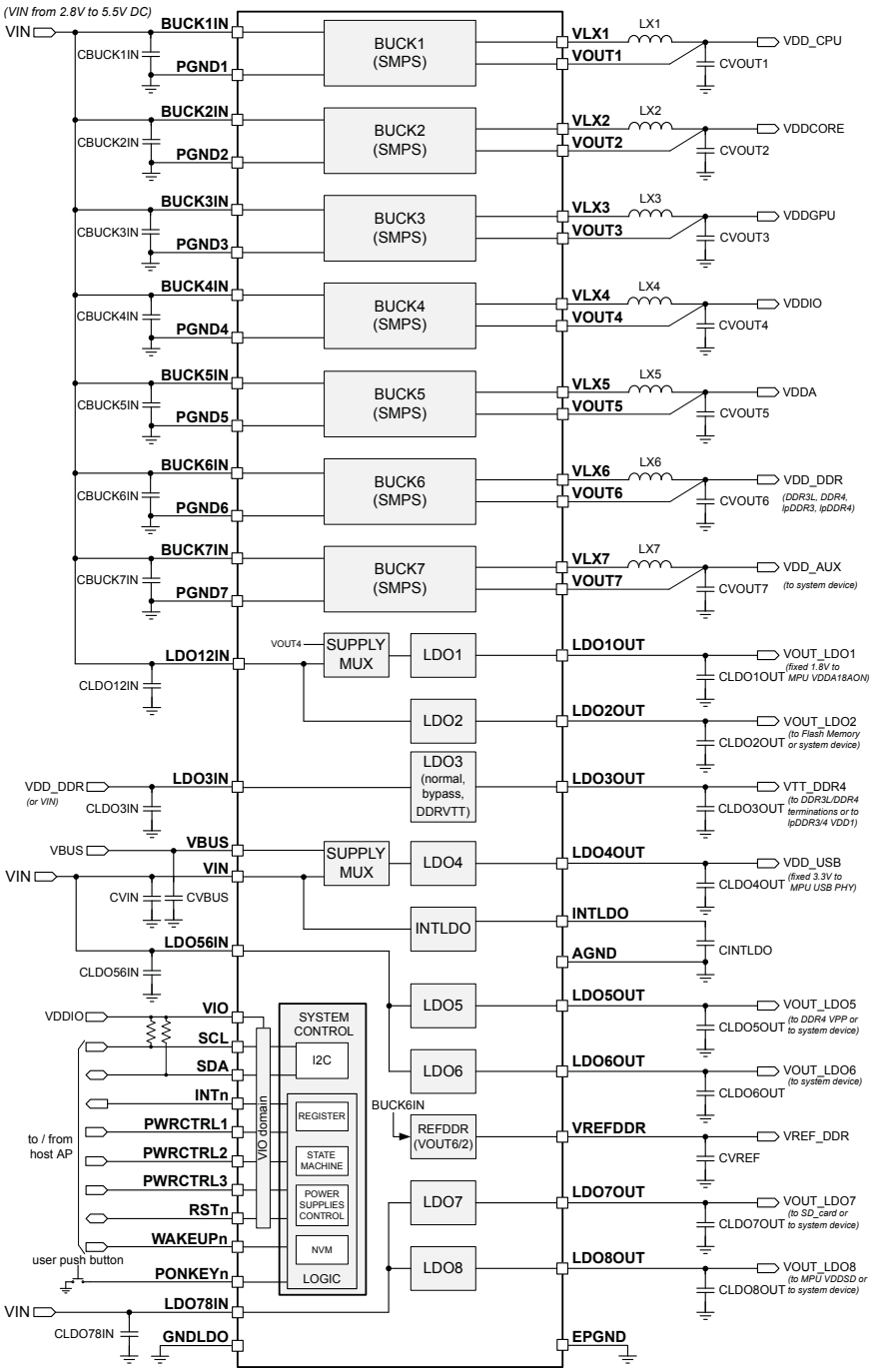
Whatever the STPMIC25 version:

- AUTO_TURN_ON option is set

2 Typical application schematic

A typical application schematic of the STPMIC25 is shown in the figure below:

Figure 1. Typical application schematic



3 Recommended external components

The tables in this section show the passive component values that have to be guaranteed for every BUCK and LDO of the STPMIC25 to satisfy performance and reach the electrical specifications listed in the datasheet, in particular:

For the BUCK converters:

- Input capacitance: typical value
- Output capacitance:
  - Real capacitance range
  - ESR: max value in the frequency range from 2 MHz to 10 MHz
- Output inductor:
  - Real inductor range
  - DCR: max value

For the LDO regulators:

- Input capacitance: typical value
- Output capacitance:
  - Real capacitance range
  - ESR: max value in the frequency range from 100 kHz to 10 MHz

3.1 Buck converters

The STPMIC25 is provided with seven buck converters optimized to supply circuits with high current consumption and comply with fast transient response requirements.

All converters are based on an adaptive constant-on-time controller (COT) that guarantees an excellent transient response and high efficiency across a wide range of operating conditions.

Each converter can work in two power modes: HP mode and LP mode. These modes differ both in performance and quiescent current consumption.

- In HP mode, the highest performance can be reached.
- In LP mode, the STPMIC25 has a much lower consumption and reduced general buck converter performance.

The switching frequency of the converter is typically 2 MHz in a steady-state CCM condition.

In a typical MPU application:

- BUCK1 is primarily dedicated to power supply the VDDCPU domain.
- BUCK2 is primarily dedicated to power supply the VDDCORE domain.
- BUCK3 is primarily dedicated to power supply the VDDGPU domain.
- BUCK4 is primarily dedicated to power supply the VDD (VIO) domain.
- BUCK5 is primarily dedicated to power supply the VDDA18 domain.
- BUCK6 is primarily dedicated to power supply the DDR memory and VDDQDDR domains.
- BUCK7 is a general purpose buck to power supply application peripherals.

BUCK1, BUCK2, BUCK3, BUCK6, and BUCK7 have excellent load transient responses across operating conditions. BUCK4 and BUCK5 supply sensitive power domains and they have a low output voltage ripple across operating conditions.

3.1.1 BUCK1 and BUCK6

The main features of BUCK1 and BUCK6 are shown in the table below:

Table 2. BUCK1 and BUCK6 main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
BUCK1, BUCK6	0.5 V to 1.5 V	10	2000/1500/1000/500	BUCK1 = VDDCPU; BUCK6 = VDDQ (DDR3L, DDR4, lpDDR3, lpDDR4

The table below shows the passive component values that must be guaranteed for BUCK1 and BUCK6 to reach the electrical specifications listed in the datasheet:

Table 3. BUCK1 and BUCK6: passive components value ranges

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CBUCK1IN, CBUCK6IN)			10		µF
Output capacitance (CVOUT1, CVOUT6)		26	66	73	µF
Equivalent series resistance of output capacitors (ESR)	f = 2 to 10 MHz			13	mΩ
Output inductor (VLX1, VLX6)		0.55	0.68	0.82	µH
DC resistance of output inductors (DCR)				44	mΩ

BUCK1 and BUCK6 were tested in the STPMIC25 evaluation board with the following external components:

Table 4. BUCK1 and BUCK6: BOM

PARAMETER	PN
Input capacitance (CBUCK1IN, CBUCK6IN)	GRM188R61A106ME69D (Murata 10 µF/10 V - 0603)
Output capacitance (CVOUT1, CVOUT6)	3xGRM188R60J226MEA0D (3xMurata 22 µF/6.3 V - 0603)
Output inductor (VLX1, VLX6)	DFE201610E-R68M (1) (Murata 0.68 µH/Isat = 4.3 A - 0806)

1. *The DFE201610E-R68M 0.68 µH coil with Isat = 4.3 A was selected to cover the max current capability (2 A) for BUCK1 and BUCK6.*

If the customer wants to program a different output current capability in the NVM, they can select between 500 mA, 1 A and 1.5 A (trough NVM_BUCKS_IOUT_SHR1, Reg 0xAC bit [1:0] for BUCK1 and NVM_BUCKS_IOUT_SHR2, Reg 0xAD bit [3:2] for BUCK6), and a lower Isat coil can be used (Isat ≥ 1.5 A, 2.1 A, 2.8 A with max current step of 500 mA, 1 A and 1.5 A respectively).

3.1.2 BUCK2 and BUCK3

The main features of BUCK2 and BUCK3 are shown in the table below:

Table 5. BUCK2 and BUCK3 main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
BUCK2, BUCK3	0.5 V to 1.5 V	10	2000/1500/1000/500	BUCK2 = VDDCORE; BUCK3 = VDDGPU

The table below shows the passive component values that must be guaranteed for BUCK2 and BUCK3 to reach the electrical specifications listed in the datasheet:

Table 6. BUCK2 and BUCK3: passive component value ranges

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CBUCK2IN, CBUCK3IN)			10		µF
Output capacitance (CVOUT2, CVOUT3)		35	88	97	µF
Equivalent series resistance of output capacitors (ESR)	f = 2 to 10 MHz			13	mΩ
Output inductor (VLX2, VLX3)		0.55	0.68	0.82	µH
DC resistance of output inductors (DCR)				31	mΩ

BUCK2 and BUCK3 were tested in the STPMIC25 evaluation board with the following external components:

Table 7. BUCK2 and BUCK3: BOM

PARAMETER	PN
Input capacitance (CBUCK2IN, CBUCK3IN)	GRM188R61A106ME69D (Murata 10µF/10 V - 0603)
Output capacitance (CVOUT2, CVOUT3)	4xGRM188R60J226MEA0D (4xMurata 22 µF/6.3 V - 0603)
Output inductor (VLX2, VLX3)	DFE252012F-R68M (1) (Murata 0.68 µH/Isat=5.4 A - 1008)

1. *The DFE252012F-R68M 0.68 µH coil with Isat=5.4 A was selected to cover the highest output current step (2 A) for BUCK2 and BUCK3.*

If the customer wants to program a different output current step in the NVM, they can select between 500 mA, 1 A and 1.5 A (trough NVM_BUCKS_IOUT_SHR1, Reg 0xAC bit [3:2] for BUCK2 and NVM_BUCKS_IOUT_SHR1, Reg 0xAC bit [5:4] for BUCK3), and a lower Isat coil could be used (Isat ≥ 1.5 A, 2.1 A, 2.8 A with max current step of 500 mA, 1 A and 1.5 A respectively).

3.1.3 BUCK4 and BUCK5

The main features of BUCK4 and BUCK5 are shown in the table below:

Table 8. BUCK4 and BUCK5 main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
BUCK4, BUCK5	1.5 V to 4.2 V	100	500/250	BUCK4 = VDD (VDDIO); BUCK5 = VDD18x

The table below shows the passive component values that must be guaranteed for BUCK4 and BUCK5 to reach the electrical specifications listed in the datasheet:

Table 9. BUCK4 and BUCK5: passive component value ranges

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CBUCK4IN, CBUCK5IN)			10		µF
Output capacitance (CVOUT4, CVOUT5)		17	66	73	µF
Equivalent series resistance of output capacitors (ESR)	f = 2 to 10 MHz			15	mΩ
Output inductor (VLX4, VLX5)		1.8	2.2	2.7	µH
DC resistance of output inductors (DCR)				140	mΩ

BUCK4 and BUCK5 were tested in the STPMIC25 evaluation board with the following external components:

Table 10. BUCK4 and BUCK5: BOM

PARAMETER	PN
Input capacitance (CBUCK4IN, CBUCK5IN)	GRM188R61A106ME69D (Murata 10 µF/10 V - 0603)
Output capacitance (CVOUT4, CVOUT5)	3xGRM21BR61A226ME51L (3xMurata 22 µF/10 V - 0805)
Output inductor (VLX4, VLX5)	DFE201610E-2R2M (1) (Murata 2.2 µH/Isat = 2.4 A - 0806)

1. *The DFE201610E-2R2M 2.2 µH coil with Isat = 2.4 A was selected to cover the highest output current step (500 mA) for BUCK4 and BUCK5.*

If the customer wants to program a different output current step in the NVM, that is 250 mA (trough NVM_BUCKS_IOUT_SHR1, Reg 0xAC bit [7:6] for BUCK4 and NVM_BUCKS_IOUT_SHR2, Reg 0xAD bit [1:0] for BUCK5), a lower Isat coil could be used (Isat ≥ 1.1 A with max current step of 250 mA).

3.1.4 BUCK7

The main features of BUCK7 are shown in the table below:

Table 11. BUCK7 main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
BUCK7	1.5 V to 4.2 V	10	2500/2000/1500/1000	General purpose

The table below shows the passive component values that must be guaranteed for BUCK7 to reach the electrical specifications listed in the datasheet:

Table 12. BUCK7: passive components value ranges

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CBUCK7IN)			10		µF
Output capacitance (CVOUT7)		22	88	97	µF
Equivalent series resistance of output capacitors (ESR)	f=2 to 10 MHz			15	mΩ
Output inductor (VLX7)		0.55	0.68	0.82	µH
DC resistance of output inductors (DCR)				44	mΩ

BUCK7 was tested in the STPMIC25 evaluation board with the following external components:

Table 13. BUCK7: BOM

PARAMETER	PN
Input capacitance (CBUCK7IN)	GRM188R61A106ME69D (Murata 10 µF/10 V - 0603)
Output capacitance (CVOUT7)	4xGRM21BR61A226ME51L (4xMurata 22 µF/10 V - 0805)
Output inductor (VLX7)	DFE201610E-R68M (1) (Murata 0.68 µH/Isat=4.3 A - 0806)

1. *The DFE201610E-R68M 0.68 µH coil with Isat=4.3 A was selected to cover the highest output current step (2.5 A) for BUCK7.*

If the customer wants to program a different output current step in the NVM, they can select between 1 A, 1.5 A and 2 A (trough NVM_BUCKS_IOUT_SHR2, Reg 0xAD bit [5:4]), and a lower Isat coil could be used (Isat ≥ 2.1 A, 2.6 A, 3.6 A with max current step of 1 A, 1.5 A and 2 A respectively).

4 LDO regulators

The STPMIC25 is provided with eight LDOs and one reference voltage LDO for DDR memories. Further details include:

- LDO1 is a fixed 1.8 V low drop regulator designed to be typically used to supply the VDDA18 MPU application domain. The LDO1 is the first IP, which needs to be powered on before any other power domain.
- LDO2, LDO5, LDO6, and LDO7 are general purpose LDOs suitable to supply MPU application peripherals. All these LDOs are provided with a bypass mode function.
- LDO3 is used for DDR3, DDR3L, DDR4 memory termination (sink-source mode) or for lpDDR3 or lpDDR4 memory (bypass mode) or for a general purpose.
- LDO4 is a fixed 3.3 V regulator designed to supply the 3V3 USB PHY circuit. It has two voltage sources (VIN or VBUS) which allows the LDO4 output voltage to remain at 3.3 V when VIN is powered by a discharged battery < 3.3 V and VBUS powered by 5 V.
- LDO8 is a general-purpose regulator with an extended voltage range. It supports the bypass mode.

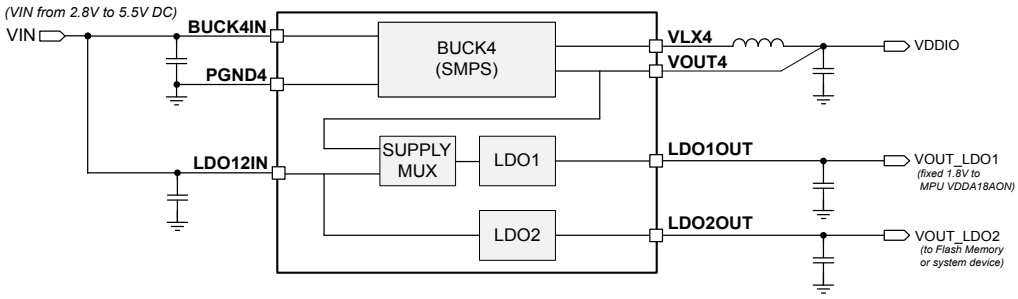
VREFDDR is a sink-source LDO dedicated to provide the voltage reference for lpDDR/DDR memory.

4.1 LDO1 and LDO2

The LDO1 is dedicated to power supply the AP's VDDA18AON, having very low power consumption and load transient. The AP's VDDA18AON must be enabled first in the power on sequence, and it must be disabled last in the power down sequence. So, the LDO1 is powered from VIN and cannot be pre-regulated from a buck converter as all buck converters should be enabled after LDO1 (due to a VDDA18AON constraint). LDO1 has a very low quiescent current, as it is enabled in STANDBY mode.

LDO1 can have two power sources: LDO12IN and VOUT4.

Figure 2. LDO1 input supply mux



By default, at reset, the LDO1 input is always LDO12IN. When the application is powered ON, the software may switch the LDO1 input from LDO12IN to VOUT4, improving LDO1 power efficiency.

LDO1 is always active when it supplies AP's VDDA18AON. However, when BUCK4OUT = 1.8 V, LDO1 is not used, no dropout mode/bypass is required in LDO1 functionality.

Instead, LDO2 is a general purpose LDO suitable to supply MPU application peripherals, and it is provided with 2 operating modes:

- Normal mode → LDO2 = 0.9 V to 4.0 V
- Bypass mode → LDO2 operates as a power switch

The main features of LDO1 and LDO2 are shown in the table below:

Table 14. LDO1 and LDO2 main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
LDO1	1.8	-	20	VDDA18AON
LDO2	0.9 V to 4.0 V bypass mode	100	400/200/100/50	General purpose (eMMC, DDR4 VPP, SD card, LCD camera, etc.)

The table below shows the passive component values that must be guaranteed for LDO1 and LDO2 to reach the electrical specifications listed in the datasheet:

Table 15. LDO1 and LDO2: passive component value ranges

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CLDO12IN)			1		µF
Output capacitance (CLDO1OUT)		2	4.7	5.2	µF
Equivalent series resistance of output capacitors (ESR)				31	mΩ
Output capacitance (CLDO2OUT)		2	4.7	5.2	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz			33	mΩ

LDO1 and LDO2 were tested in the STPMIC25 evaluation board with the following external components:

Table 16. LDO1 and LDO2: BOM

PARAMETER	PN
Input capacitance (CLDO12IN)	GRM155R61E105KA12D (Murata 1 µF/25 V - 0402)
Output capacitance (CLDO1OUT)	GRM155R60J475ME47D (Murata 4.7 µF/6.3 V – 0402)
Output capacitance (CLDO2OUT)	GRM155R60J475ME47D (Murata 4.7 µF/6.3 V – 0402)

4.2 LDO3

The LDO3 is a multipurpose LDO with 3 operating modes:

- Normal mode → the LDO3 works as general purpose LDO as well as LDO2, 5, 6, 7, and 8.
- Bypass mode → the LDO3 operates as a power switch.
- Sink-source mode → the LDO3 can regulate the output voltage working in sink source mode. This mode is dedicated to supply termination of DDR3/DDR3L or DDR4 IC memories with fixed output voltage. If LDO3 is used in this mode, LDO3IN must be powered from the output of BUCK6. The output voltage of LDO3 in S/S mode is fixed and follows VOUT6/2 even during the BUCK6 ramp-up and ramp-down phase. The overcurrent limitation works both during sink and source output current mode.

The main features of LDO3 are shown in the table below:

Table 17. LDO3 main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
LDO3 normal mode	0.9 V to 4.0 V	100	120	General purpose/ lpDDR VDD1
LDO3 sink-source mode	VOUT6/2	-	+/-120 (rms) +/-230 (peak)	DDR3L/DDR4 terminations (VTT)
LDO3 bypass mode	-	-	80	lpDDR VDD1

4.2.1 LDO3 in normal mode

The table below shows the passive component values that must be guaranteed for LDO3 in normal mode (using GRM155R60J106ME05D, 10 µF/6.3 V – 0402 and GRM188R61A106ME69, 10 µF/10 V – 0603 respectively) to reach the electrical specifications listed in the datasheet:

Table 18. LDO3 in normal mode: passive component value ranges (using GRM155R60J106ME05D)

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CLDO3IN)			10		µF
Output capacitance (CLDO3OUT)		2	10	11	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz			22	mΩ

Table 19. LDO3 in normal mode: passive component value ranges (using GRM188R61A106ME69)

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CLDO3IN)			10		µF
Output capacitance (CLDO3OUT)		2	10	12	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz			18	mΩ

LDO3 in normal mode was tested in the STPMIC25 evaluation board with the following external components:

Table 20. LDO3 in normal mode: BOM

PARAMETER	PN
Input capacitance (CLDO3IN)	GRM155R60J106ME05D (Murata 10 µF/6.3 V - 0402)
Output capacitance (CLDO3OUT)	GRM155R60J106ME05D (Murata 10 µF/6.3 V - 0402)
	GRM188R61A106ME69 (Murata 10 µF/10 V - 0603)

4.2.2 LDO3 in sink-source mode

The table below shows the passive component values that must be guaranteed for LDO3 in sink-source mode (using GRM155R60J106ME05D, 10µF/6.3V – 0402 and GRM188R61A106ME69, 10 µF/10 V – 0603 respectively) to reach the electrical specifications listed in the datasheet:

Table 21. LDO3 in sink-source mode: passive component value ranges (using GRM155R60J106ME05D)

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CLDO3IN)			10		µF
Output capacitance (CLDO3OUT)		6	10	11	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz			20	mΩ

Table 22. LDO3 in sink-source mode: passive component value ranges (using GRM188R61A106ME69)

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CLDO3IN)			10		µF
Output capacitance (CLDO3OUT)		6	10	11	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz			13	mΩ

LDO3 in sink-source mode was tested in the STPMIC25 evaluation board with the following external components:

Table 23. LDO3 in sink-source mode: BOM

PARAMETER	PN
Input capacitance (CLDO3IN)	GRM155R60J106ME05D (Murata 10 µF/6.3 V - 0402)
Output capacitance (CLDO3OUT)	GRM155R60J106ME05D (Murata 10 µF/6.3 V - 0402)
	GRM188R61A106ME69 (Murata 10 µF/10 V - 0603)

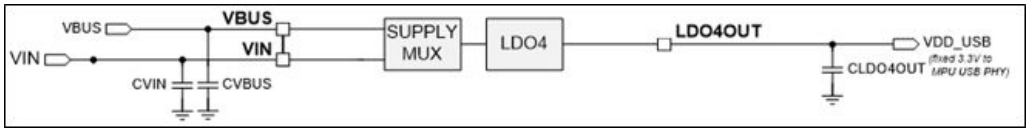
4.3 LDO4

LDO4 is dedicated to supply the AP's USB HS analog PHY power domain (VDD33USB) and the AP's USB Type-C® Power Delivery PHY (VDD33UCPD).

The LDO4 output voltage is fixed at 3.3 V.

LDO4 has two power sources: VIN and VBUS (see the figure below). The selection among these two power inputs is automatic, thus no user intervention is needed. The internal circuit continuously monitors voltage levels on these pins and selects the input source having the highest input voltage.

Figure 3. LDO4 input supply mux



The main features of the LDO4 are shown in the table below:

Table 24. LDO4 main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
LDO4	3.3 V	-	40	VDD33USB, VDD33UCPD

The table below shows the passive component values that must be guaranteed for LDO4 to reach the electrical specifications listed in the datasheet:

Table 25. LDO4: passive component value ranges

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (VIN)			4.7		µF
Input capacitance (CVBUS)			4.7		
Output capacitance (CLDO4OUT)		2	4.7	5.2	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz			34	mΩ

LDO4 was tested in the STPMIC25 evaluation board with the following external components:

Table 26. **LDO4: BOM**

PARAMETER	PN
Input capacitance (VIN)	GRM155R60J475ME47D (Murata 4.7 µF/6.3 V - 0402)
Input capacitance (CVBUS)	GRM188R61C475KE11D (Murata 4.7 µF/16 V - 0603)
Output capacitance (CLDO4OUT)	GRM155R60J475ME47D (Murata 4.7 µF/6.3 V – 0402)

4.4 LDO5 and LDO6

LDO5 and LDO6 are general purpose LDOs suitable to supply MPU application peripherals, and they are provided with two operating modes:

- Normal mode → LDO5, LDO6 = 0.9 V to 4.0 V
- Bypass mode → the LDO5 and LDO6 operate as power switches

The main features of LDO5 and LDO6 are shown in the table below:

Table 27. **LDO5 and LDO6 main output settings**

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
LDO5, LDO6	0.9 V to 4.0 V bypass mode	100	400/200/100/50	General purpose (eMMC, DDR4 VPP, SD card, LCD camera, etc.)

The table below shows the passive component values that must be guaranteed for LDO5 and LDO6 to reach the electrical specifications listed in the datasheet:

Table 28. **LDO5 and LDO6: passive component value ranges**

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CLDO56IN)			1		µF
Output capacitance (CLDO5OUT, CLDO6OUT)		2	4.7	5.2	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz		5	33	mΩ

LDO5 and LDO6 were tested in the STPMIC25 evaluation board with the following external components:

Table 29. **LDO5 and LDO6: BOM**

PARAMETER	PN
Input capacitance (CLDO56IN)	GRM155R61E105KA12D (Murata 1 µF/25 V - 0402)
Output capacitance (CLDO5OUT, CLDO6OUT)	GRM155R60J475ME47D (Murata 4.7 µF/6.3 V – 0402)

4.5 LDO7 and LDO8

LDO7 and LDO8 are general purpose LDOs suitable to supply MPU application peripherals, and they are provided with two operating modes:

- Normal mode → LDO7, LDO8 = 0.9 V to 4.0 V
- Bypass mode → the LDO7 and LDO8 operate as power switches

The main features of LDO7 and LDO8 are shown in the table below:

Table 30. LDO7 and LDO8 main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
LDO7, LDO8	0.9 V to 4.0 V bypass mode	100	400 / 200 / 100 / 50	General purpose (eMMC, DDR4 VPP, SD card, LCD camera, etc.)

The table below shows the passive component values that must be guaranteed for LDO7 and LDO8 to reach the electrical specifications listed in the datasheet:

Table 31. LDO7 and LDO8: passive component value ranges

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Input capacitance (CLDO78IN)			1		µF
Output capacitance (CLDO7OUT, CLDO8OUT)		2	4.7	5.2	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz		5	33	mΩ

LDO7 and LDO8 were tested in the STPMIC25 evaluation board with the following external components:

Table 32. LDO7 and LDO8: BOM

PARAMETER	PN
Input capacitance (CLDO78IN)	GRM155R61E105KA12D (Murata 1 µF/25 V - 0402)
Output capacitance (CLDO7OUT, CLDO8OUT)	GRM155R60J475ME47D (Murata 4.7 µF/6.3 V – 0402)

4.6 VREFDDR

The REFDDR (DDR reference voltage) is a sink/source LDO similar to the LDO3 in sink/source mode but with lower current capability. It is dedicated to supply the reference voltage (VREF) pin of lpDDR3/DDR3/DDR3L and DDR4 memories in addition to the AP's DDR_VREF pin.

The VREFDDR output voltage is fixed at VOUT6/2. The input of REFDDR is internally connected in PMIC.

In the case that BUCK6 is enabled/disabled when the REFDDR is enabled, the output of the REFDDR follows the BUCK6 startup/shutdown waveforms, always keeping VOUT6/2.

The main features of the VREFDDR are shown in the table below:

Table 33. REFDDR main output settings

Regulator	Output voltage (V)	Programming step (mV)	Rated output current (mA)	Typical application use
REFDDR	VOUT6/2	-	+/-5 (rms) +/-10 (peak)	DDR3L, DDR4, lpDDR3, VREF, DDR_VREF

The table below shows the passive component values that must be guaranteed for VREFDDR to reach the electrical specifications listed in the datasheet:

Table 34. REFDDR: passive component value ranges

PARAMETER	Test condition	MIN	TYP	MAX	UNIT
Output capacitance (CVREF)		0.4	1	1.1	µF
Equivalent series resistance of output capacitors (ESR)	f = 100 kHz to 10 MHz			224	mΩ

The VREFDDR was tested in the STPMIC25 evaluation board with the following external components:

Table 35. REFDDR: BOM

PARAMETER	PN
Output capacitance (CVREF)	GRM155R61E105KA12D (Murata 1 µF/25 V – 0402)

5 Recommended BOM

The table below lists all the part numbers of the external BOM used to validate the STPMIC25 IC in the evaluation board:

Component	Manufacturer	Part number	Value	Size
CVIN, CLDO1OUT, CLDO2OUT, CLDO4OUT, CLDO5OUT, CLDO6OUT, CLDO7OUT, CLDO8OUT, CINTLDO	MURATA	GRM155R60J475ME47D	4.7 µF 6.3 V	0402
CBUCK1IN, CBUCK2IN, CBUCK3IN, CBUCK4IN, CBUCK5IN, CBUCK6IN, CBUCK7IN		GRM188R61A106ME69D	10 µF 10 V	0603
CVOUT1, CVOUT6		GRM188R60J226MEA0D	3 x 22 µF 6.3 V	0603
CVOUT2, CVOUT3			4 x 22 µF 6.3 V	
CVOUT4, CVOUT5		GRM21BR61A226ME51L	3 x 22 µF 10 V	0805
CVOUT7			4 x 22 µF 10 V	
CLDO12IN, CLDO56IN CLDO78IN, CVREF		GRM155R61E105KA12D	1 µF 25 V	0402
CLDO3IN, CLDO3OUT		GRM155R60J106ME05D	10 µF 6.3 V	0402
CVBUS		GRM188R61C475KE11D	4.7 µF 16 V	0603
LX1, LX6, LX7		DFE201610E-R68M = P2	0.68 µH	0806
LX2, LX3		DFE252012F-R68M = P2	0.68 µH	1008
LX4, LX5		DFE201610E-2R2M = P2	2.2 µH	0806

Note: All the recommended part numbers reported are X5R and are usable until $T_{amb} \leq 85$ °C.

Consider using X7R or better dielectric capacitors if the whole application has to work in an environment with $T_{amb} > 85$ °C.

Revision history

Table 36. **Document revision history**

Date	Version	Changes
14-June-2024	1	Initial release.

Contents

List of figures