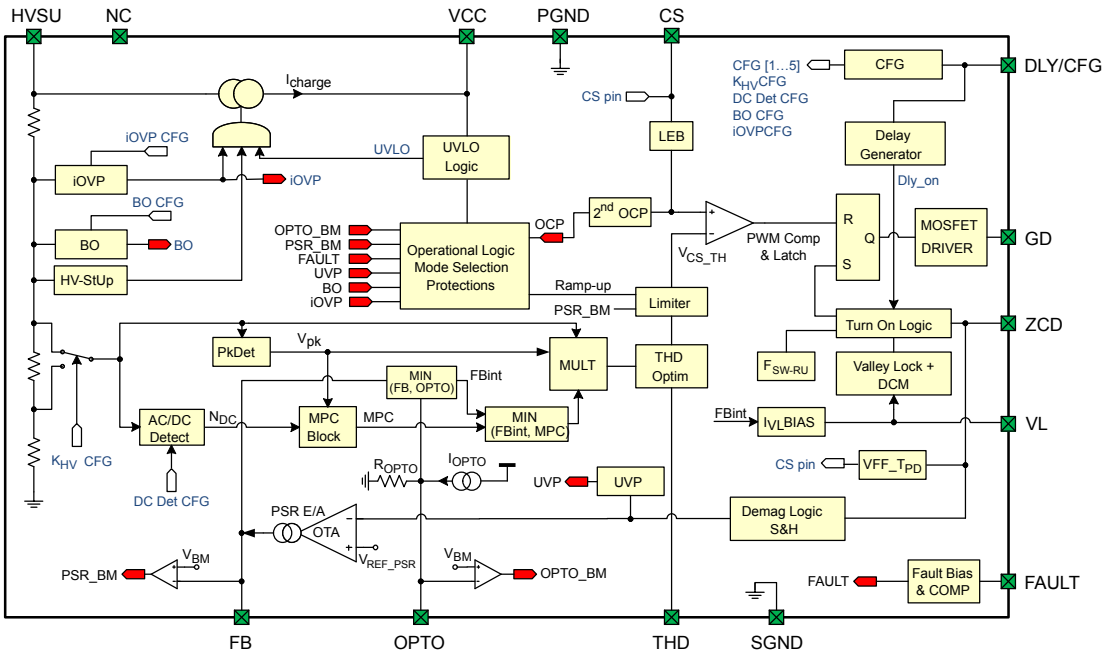
Introduction to the HVLED101: high-power factor flyback controller for advanced power topologies

Introduction

The HVLED101 is an enhanced peak current mode controller designed primarily for high power factor (HPF) flyback or buck-boost topologies having an output power up to 180 W. Additionally, it supports other topologies, such as buck, boost, and SEPIC. Primary Side Regulation (PSR) of output voltage and optocoupler control can be applied independently on the chip both exploiting precise regulation and very low standby power during no-load conditions. The innovative ST high-voltage technology enables direct connection of the HVLED101 to the input voltage in order to both start up the device and monitor the input voltage without the need of external components. Integrated valley locking feature guarantees noise free operation during medium and low load operation and maximum power control allows limiting the input power to a level programmable by the user to increase converter safety. Abnormal conditions like open circuit, output short-circuit, input overvoltage or undervoltage, external protection circuitries and circuit failures like open loop and overcurrent of the main switch are effectively controlled. A smart Auto Restart Timer (ART) function is built in to guarantee an automatic application recover, without any loss of reliability.

Figure 1. Block diagram



1 Pin features description

1.1 Pin function summary

Figure 2. **Pin configuration (top view)**

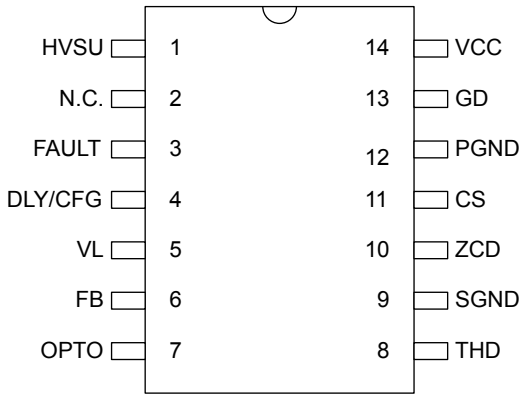


Table 1. **Pin function**

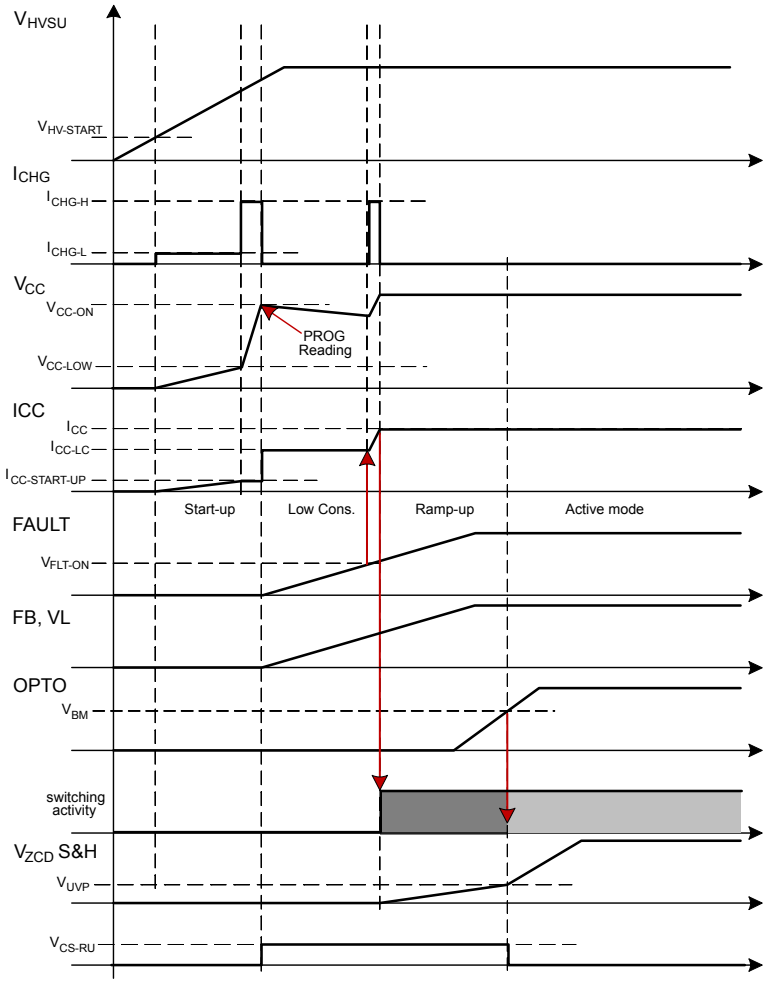
Sym.	Pin	Function name	Paragraph
HVSU	1	High-voltage startup	1.3 Device supply management
		Input voltage detection	1.4 Multiplier and THD optimizer
		Input overvoltage detection (iOVP)	1.11.2 Input overvoltage protection (iOVP)
N.C.	2	Not connected pin	
FAULT	3	Fault detection	1.11.5 General fault pin and NTC connection
DLY/CFG	4	Delay time setting	1.10 Configuration programming and parameters selection
		Configuration setting	1.10 Configuration programming and parameters selection
		Protection setting	1.10 Configuration programming and parameters selection
VL	5	Valley locking frequency foldback	1.9 VL pin structure
FB	6	PSR E/A output connection	1.5.1 Primary side regulation and ZCD divider design
		Burst mode	1.5.2 Burst mode during primary side regulation
OPTO	7	Input for optocoupler connection	1.5.3 Secondary side regulation and relevant burst mode
		Disable input (active low)	1.7 Disabling feature
THD	8	THD optimizer	1.4 Multiplier and THD optimizer
SGND	9	Reference pin for signal's ground potential	
ZCD	10	ZCD detection	1.8 Zero current detection circuit and valley skipping
		Vout sampling input for PSR	1.5.1 Primary side regulation and ZCD divider design
CS	11	Current sense comparator input	1.4.2 Current sense circuit

Sym.	Pin	Function name	Paragraph
CS	11	Maximum power control feature	1.4.1 Maximum power control (MPC) and Rcs design
PGND	12	Reference pin for VCC and gate driver.	
GD	13	Gate driver output	1.6 Gate driving
VCC	14	Supply energy to the IC	1.3 Device supply management
		Internal UVLO logic	1.3 Device supply management

1.2 Operating modes

The IC presents various operating modes, described in the following sections. Figure 3 shows the operation during initial startup phase.

Figure 3. Initial startup phase



1.2.1 Startup phase

As soon as the HVSU pin voltage reaches $V_{HV-START}$, the high-voltage startup unit is turned on to charge the V_{CC} capacitor.

The charging current is limited to I_{CHG-L} until V_{CC} voltage reaches the V_{CC-LOW} threshold, and it is then toggled to a higher charging current (I_{CHG-H}) to minimize the startup time.

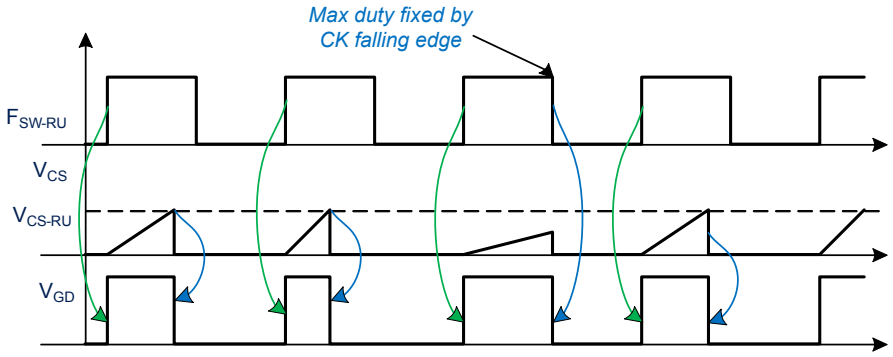
Once the V_{CC} reaches the V_{CC-ON} threshold, the DLY/CFG pin is read to set the configuration of the input voltage protections and input voltage range.

1.2.2 Ramp-up phase

This operating mode is intended to ensure a safe increase of the output voltage. This goal is achieved by transferring an almost constant power to the output by fixing the minimum current sense threshold at V_{CS-RU} and driving the external power MOSFET at constant operating frequency F_{SW-RU}, with the maximum duty cycle fixed at 50%.

The THD optimizer unit is forced to operate with a duty cycle equal to 1 (see relevant section for further details).

Figure 4. Ramp-up waveforms



When both output voltages (read by ZCD sample and hold block) are higher than the V_{UVP} threshold and the OPTO pin is pulled up for at least $T_{OPTO-TRIG}$, the IC enters active mode.

If the ramp-up exit condition is not satisfied within T_{CF}, the IC shuts down, and an automatic restart is attempted after T_{ART}.

During this phase, the internal PSR error amplifier is always on as well as the FAULT pin pull-up current.

1.2.3 Active mode

During active mode, the IC provides the GD signal to drive the external power switch according to application signals.

All the parameters are set at their operating range performance and protections are ready to manage undesired events.

The power consumption of the IC in this phase depends on the switching frequency and the characteristics of the adopted switch.

The OPTO disable feature activates a deep low consumption mode, while the FAULT disable mean activates a standard low consumption mode.

The input OVP is active (in CFG 1, 3, and 5) as well as the brownout and output undervoltage protections.

1.2.4 Low consumption mode

In this state, the IC stops switching activity and turns off the major parts of the internal structures in order to reduce V_{CC} consumption down to I_{CC-LC}.

In this operating mode, the high-voltage startup logic is active to maintain the V_{CC} pin above V_{CC-OFF} (low level) if necessary.

This state is invoked when the following conditions are met:

- Overcurrent protection
- FAULT pin protection
- The inactive phase of brownout level protection is running
- Input overvoltage protection senses an excessive input voltage at pin HVSU.

1.2.5 Deep low consumption mode

This state is intended to reduce the IC consumption to the minimum level in order to reduce the input power consumption during the burst mode condition (FB or OPTO driven).

When the deep low consumption mode condition is removed, the system evolves to the relevant next state without turning on the high-voltage startup unit.

A simplified state diagram is reported in Figure 5.

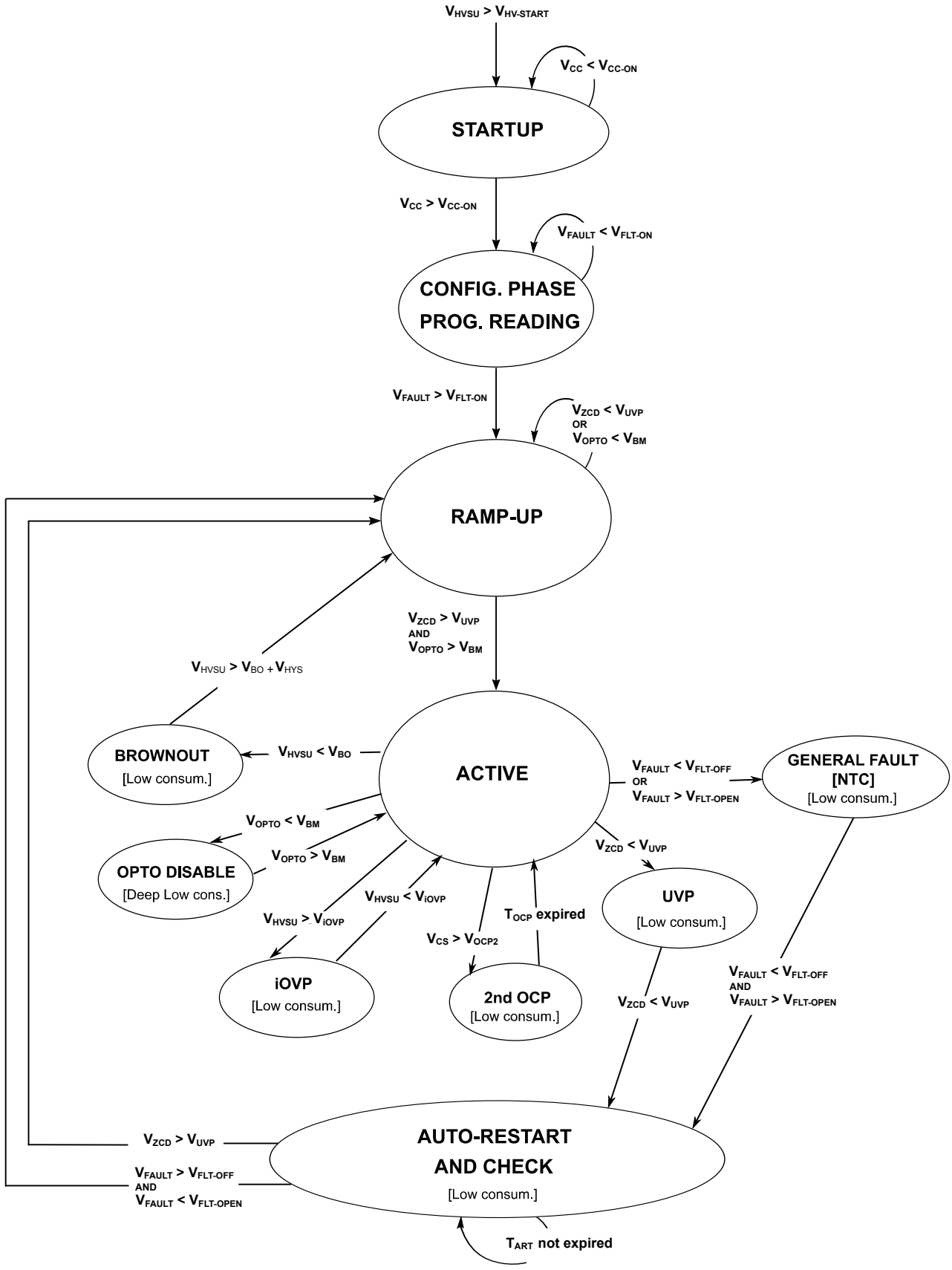
1.2.6 Auto-restart time and check state

These are auxiliary states. The auto-restart time is intended to maintain the device supplied for a time equal to T_{ART} until a new restart procedure is automatically generated.

If V_{CC} drops below V_{CC-OFF}, the timers are frozen, while if V_{CC} drops below V_{CC-SHD}, the internal logic of the device is reset and all automatic procedures are also interrupted.

The check state is a logic state that is invoked after the V_{CC-ON} trigger to check the status of all protections and take the proper actions according to protection logic.

Figure 5. **HVLED101 operation states diagram**



1.3 Device supply management

[Involved pins 1: HVSU, 14: VCC]

The HVLED101 is supplied applying a DC voltage source between the VCC pin and PGND.

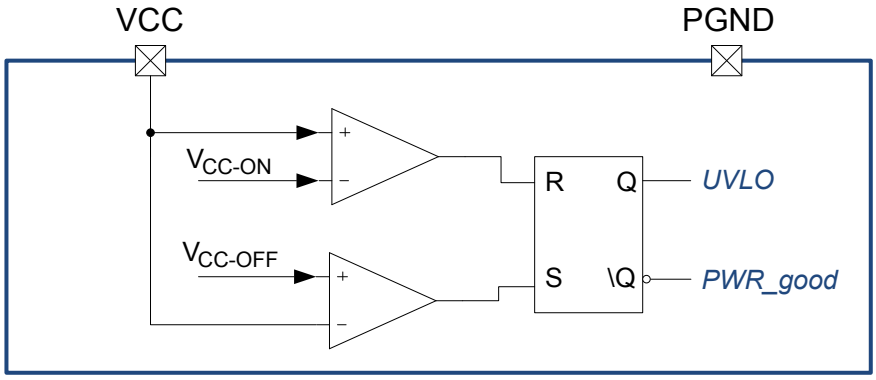
This voltage can be easily obtained, during normal operation, by an auxiliary winding of the flyback transformer, but other voltage sources can also be used.

1.3.1 VCC supply management

The HVLED101 device embeds a smart supply voltage monitor able to both prevent the application from driving the switching MOSFET with insufficient energy and to maintain the precision of the internal references.

The operational scheme is designed to minimize the V_{CC} power consumption, especially during low consumption and deep low consumption modes.

Figure 6. UVLO and VCC regulation block diagram

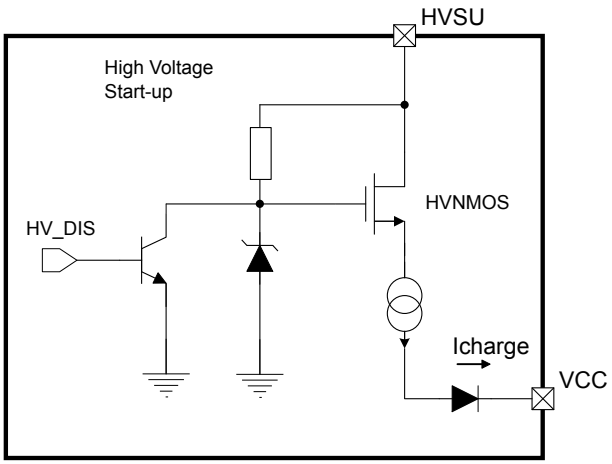


When V_{CC} drops below V_{CC-OFF}, the IC moves to low consumption mode and activates the high-voltage startup to recover a sufficient V_{CC} level (V_{CC-ON}).

1.3.2 High-voltage startup

The high-voltage startup unit is connected to the HVSU pin and allows the startup current to initiate the IC operations and maintain the IC on during low consumption modes.

Figure 7. High-voltage startup unit



The HVSU starts its operation when the applied voltage is higher than $V_{HV-START}$ = 20 V (max.).

The charging current ensures a quick startup independent of the voltage applied to the HVSU pin. Two different currents are generated depending on V_{CC} voltage and the lower value is generated when V_{CC} is below the V_{CC-LOW} threshold.

This unit is invoked:

- At startup
- During low consumption to maintain the V_{CC} level
- During T_{ART} time to maintain the V_{CC} level
- In case of iOVP to discharge the input capacitor

The operation conditions of HVSU are summarized in Table 2.

Table 2. HVSU activation summary

Operating condition	V_{cc} range	OFF	I_{CHG-H}	I_{CHG-L}
All states if $V_{HVSU} < V_{HV-START}$	Any	x		
Startup (initial phase)	0 V ... V_{CC-LOW}			x
Startup (IC startup)	V_{CC-LOW} ... V_{CC-ON}		x	
Active mode	V_{CC-OFF} ... V_{CC-ON}	x		
Input OVP	V_{CC-OFF} ... V_{CC-AMR}			x
Low consumption mode (LC)	V_{CC-ON} ... V_{CC-OFF} (falling)	x		
VCC recover during LC mode	V_{CC-OFF} ... V_{CC-ON} (rising)		x	
Deep low consumption mode (DLC)	Any	x		

The charging time of the capacitor on the VCC pin can be calculated as follows:

$$T_{VCC\text{-}Charge} = \frac{C_{VCC} \cdot V_{CC\text{-}LOW}}{I_{CHG\text{-}L}} + \frac{C_{VCC} \cdot (V_{CC\text{-}ON} - V_{CC\text{-}LOW})}{I_{CHG\text{-}H}} \quad (1)$$

As soon as the V_{CC} voltage reaches the turn-on threshold (V_{CC-ON}), the HVSU is turned off, the IC enters in low consumption mode, and the internal pull-up of the pins OPTO, FB, VL, and FAULT are turned on.

Once the FAULT pin reaches the V_{FLT-ON} threshold, V_{CC} is pulled up again to the V_{CC-ON} threshold before starting switching activity. During the switching activity, the HVSU is off and the pin measures the input voltage through the R_{HVSU} resistor (1 kΩ - 0805 SMD) to obtain high power factor and to detect both input overvoltage and undervoltage, according to protection configuration, selected on the DLY/CFG pin (see Section 1.10: Configuration programming and parameter selection for details).

During low consumption mode, the HVSU is active to maintain the V_{CC} voltage between V_{CC-ON} and V_{CC-OFF}.

Note that any kind of supplying mean (including auxiliary winding) must be de-coupled from the VCC pin using a general purpose diode having the proper reverse voltage rating: this good practice is necessary to preserve the mutual functionality of HVSU and VCC.

1.4 Multiplier and THD optimizer

[Involved pins 1: HVSU, 6: FB, 7: OPTO, 8: THD, 11: CS]

The HVLED101 is optimized to operate as a high power factor peak current mode quasi-resonant (QR) flyback. In order to realize this operating scheme, it embeds a multiplier that creates the threshold for the PWM comparator that turns off the main switch when the current measured across a shunt resistor (R_{CS}), placed between the source of said switch and GND, reaches the above-mentioned threshold.

The THD optimization unit is placed between the multiplier output and the current sense threshold limiter and is active during active mode only.

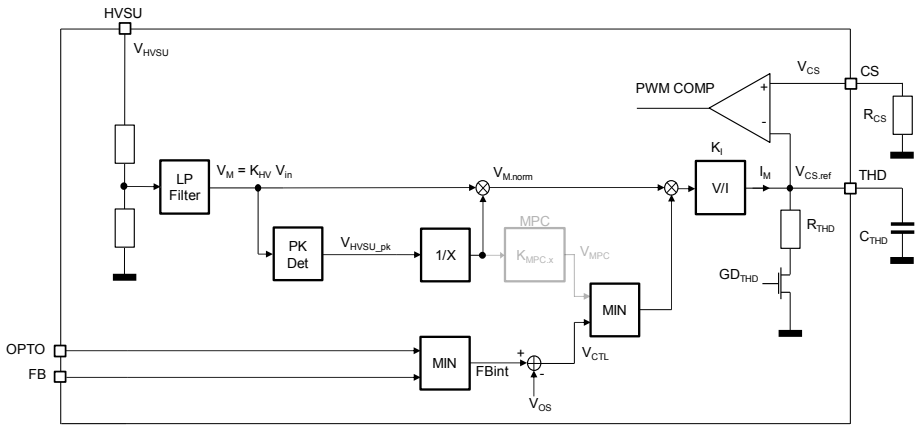
The current sense threshold is given by the following relationship:

$$V_{CS.ref} = \frac{V_{HVSU}}{V_{HVSU\_pk}} \cdot \frac{K_M}{\delta_{THD}(\theta)} \cdot (V_{FBint} - V_{OS}) \quad (2)$$

Where K_M is the DC gain of the THD optimizer and δ_{THD} (θ) is the duty cycle of the internal optimizer MOSFET.

A detail of the blocks involved in this feature is shown in Figure 8.

Figure 8. Multiplier and THD optimizer block diagram



At first, the input voltage connected to the HVSU pin is scaled by an integrated voltage divider, then it is normalized dividing the input voltage by its maximum value obtained from a peak detector circuit; as a result, the term V_{HVSU} / V_{HVSU_pk} is either a half sinusoid having an amplitude of 1 V or a unity DC voltage if the HVSU pin is connected respectively to a rectified mains or to a DC voltage (for example, PFC output).

The peak detector is intended to operate when the peak amplitude (or DC value) of the input voltage is between 105 V and 480 V (CFG1, CFG2, or CFG5) or between 175 V and 760 V (CFG3 or CFG4).

The voltage FBint is the minimum between the FB pin voltage and the OPTO pin voltage and is representative of the energy required by the load; it is firstly purged by the term V_{OS} and then applied to another input of the multiplier.

Finally, the output of the multiplier is sent to the THD optimizer unit.

An external capacitor, C_{THD}, connected between the THD pin and GND is used to filter the switching frequency from the V_{CS} threshold.

The suggested value of the C_{THD} filtering capacitor is:

$$C_{THD} = (3 \text{ to } 5) \cdot \frac{1}{R_{THD} \cdot f_{SW\_MIN}} \quad (3)$$

R_{THD} is the IC internal parameter (22 kΩ)

f_{SW_MIN} is the minimum switching frequency

C_{THD} typical value is few nF (for example, 3.3 nF)

The internal THD switch is normally switched together with GD: if valley skipping operation is running, the THD pin is put in high impedance in correspondence with the 6th valid falling edge of the ZCD signal.

The THD MOSFET activity is described in Table 3.

Table 3. THD gate activity vs. operating modes

Operating mode	THD gate activity
Active mode (QR up to 6th valley)	GD_{THD} same as GD activity
Active mode (from 6th valley DCM mode)	GD_{THD} off (THD pin = HiZ)
Ramp-up time GD_{THD} always on	GD_{THD} always on

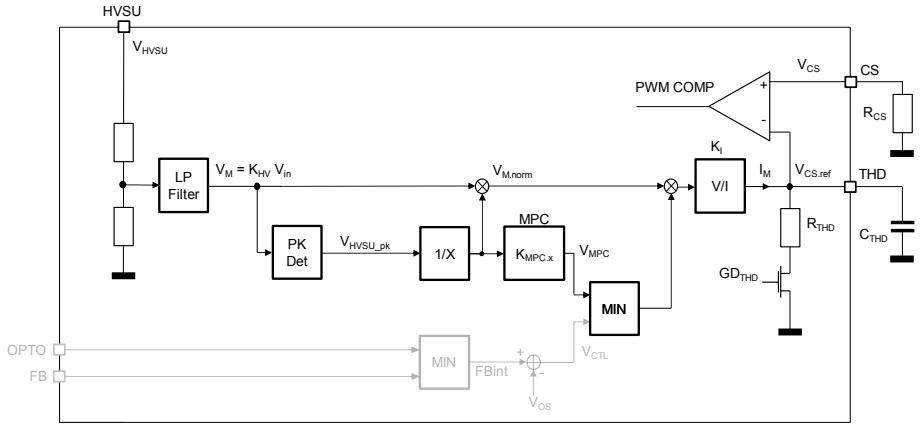
Operating mode	THD gate activity
Burst mode inactive phase (both PSR or OPTO)	GD_{THD} always on
OCP protection period	GD_{THD} always on
iOVP protection period	GD_{THD} always off (THD pin = HiZ)
Brownout protection	GD_{THD} always off (THD pin = HiZ)
Fault protection	GD_{THD} always off (THD pin = HiZ)
Auto-restart time (after UVP)	GD_{THD} always off (THD pin = HiZ)

1.4.1 Maximum power control (MPC) and R_{CS} design

Maximum input power is automatically limited by the HVLED101 internal algorithm (MPC), which helps increase system safety.

Basically, the MPC block is an additional branch of the multiplier section that supplies the Vin information and takes control of the loop if the input power goes over the programmed level.

Figure 9. MPC block diagram



The MPC defines the value of the primary current sense resistor R_{CS} according to the following equation:

$$R_{CS}=\frac{K_M \cdot K_{MPC}}{4 \cdot P_{in\text{-}lim}} \quad (4)$$

Where:

K_M is the multiplier gain = 0.176 V/V

K_{MPC} is the scaling factor = 270 V^2

$P_{in\text{-}lim}$ is the required limiting input power

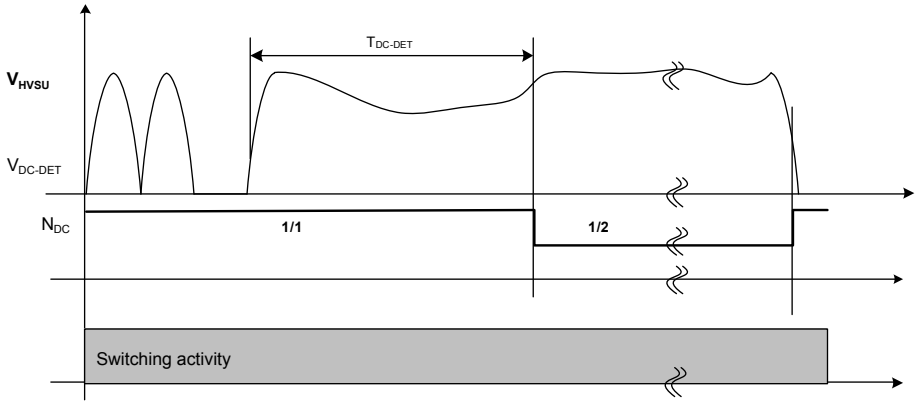
$P_{in\text{-}lim}$ can be calculated by considering the maximum output power and an efficiency of 0.9.

R_{CS} resistor and circuit sense circuit are described in Section 1.4.2: Current sense circuit.

The MPC block automatically detects if the input voltage is AC or DC: if the input voltage does not drop below $V_{DC\text{-}DET}$ for a time longer than $T_{DC\text{-}DET}$, then it is assumed that a DC voltage is connected and the K_{MPC} value is adjusted accordingly (It is divided by 2). Also in this case the R_{CS} is defined by the same equation:

$$R_{CS}=\frac{K_M \cdot \frac{K_{MPC}}{2}}{2 \cdot P_{in\text{-}lim}} \quad (5)$$

Figure 10. **DC detection waveforms**

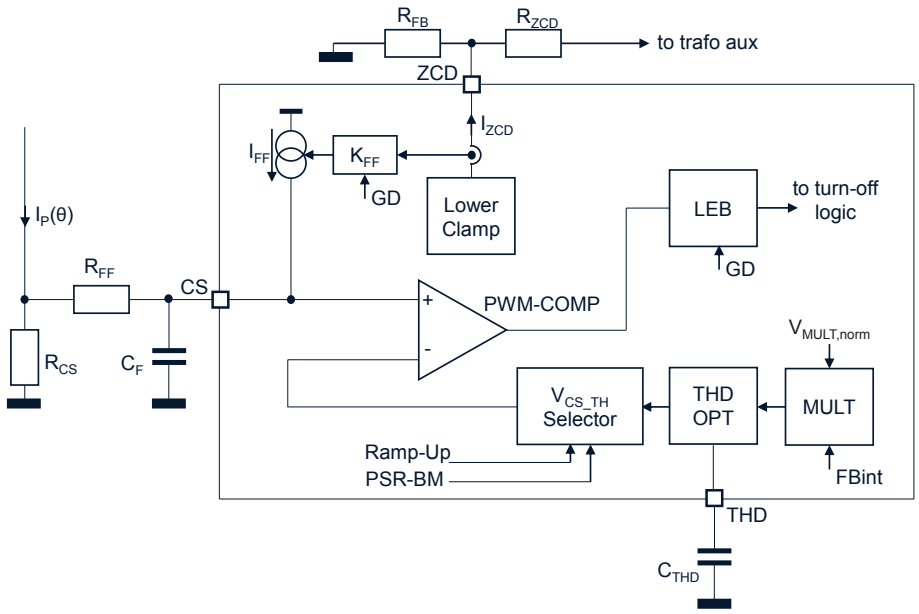


Note: The internal peak detector is always active and triggers the maximum of any fluctuation superimposed to the HVSU voltage. If said voltage is a pure DC, the peak detector stores the input voltage itself.

1.4.2 Current sense circuit

The current flowing in the MOSFET is sensed through a shunt resistor (R_{CS}). The resulting voltage is applied to the CS pin through a series resistor (R_{FF}) and compared with the internal reference V_{CS-TH}, to determine MOSFET's turn-off.

Figure 11. **Current sense circuit block diagram**

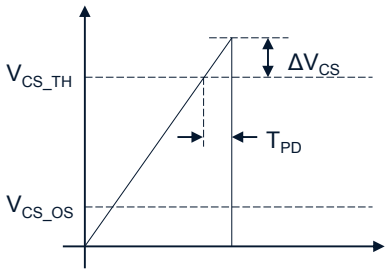


As described in Section 1.4.1: Maximum power control (MPC) and R_{CS} design, the value of R_{CS} is determined by the Maximum Power Control (MPC) algorithm.

The IC embeds a circuit to compensate for the propagation delay time (T_{PD}) of the current sense path (PWM comparator + logic + driver) that causes the MOSFET driving signal to start falling after some time from the voltage $R_{CS} * I_p$ on the CS pin crossing the reference V_{CS_TH}.

The circuit adds an offset (V_{CS_OS}) on the CS pin (during the gate drive on-time only), through a series resistor R_{FF} to compensate for this effect.

Figure 12. **Effect of T_{PD} on V_{CS} and its compensation by means of V_{CS_OS}**



$$V_{CS\_OS} = I_{FF} \cdot R_{FF} \tag{6}$$

The resistor can be calculated as follows:

$$R_{FF} = \frac{R_{CS} \cdot R_{ZCD} \cdot T_{PD}}{L_{pri} \cdot K_{FF}} \cdot \frac{N_{pri}}{N_{aux}} \tag{7}$$

R_{ZCD} is calculated from the ZCD pin current limitation as described in Section 1.5.1: Primary side regulation and ZCD divider design;

T_{PD} is the propagation time to output of current sense detection, 80 ns (typ.);

K_{FF} is an internal parameter, 75 µA/mA (typ.);

At very light load, during PSR burst mode operation, the demagnetization time could be very short, leading to a sample and hold circuit underestimate of the output voltage. To ensure correct S&H operation, a minimum current sense threshold (V_{CS_MIN}) is provided when PSR burst mode is active.

During the ramp-up phase, the current sense threshold is set at $V_{CS\text{-}RU}$, in order to reduce the stress of power components.

An internal LEB structure prevents the loop from reacting to gate driver turn-on spikes; when a proper design of the PCB layout is made, no further filter structure should be necessary.

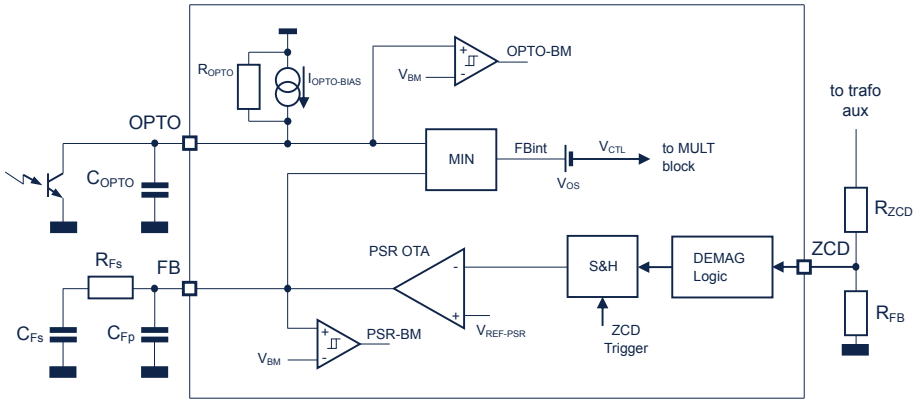
1.5 PSR and SSR control loop

[Involved pins 6: FB, 7: OTPO, 10: ZCD]

The HVLED101 has two separate pins (OPTO and FB) to operate with a secondary control loop (SSR) and a primary side control loop (PSR) (Constant Output Voltage only) on the same application.

Both pins are active; the one with the lowest voltage takes the control of the loop so two independent compensation networks can be implemented.

Figure 13. OPTO and FB internal block connection



1.5.1 Primary side regulation and ZCD divider design

By means of the PSR feature, the HVLED101 is able to regulate the output voltage of the converter without the need of an external error amplifier and relevant optocoupler.

The IC reads the Vout sensing the voltage developed across the auxiliary winding during the off-time of the MOSFET.

Auxiliary voltage, connected to the ZCD pin through the voltage divider R_{ZCD} and R_{FB}, is detected at the de-magnetization instant and its amplitude is used as a feedback signal to regulate the Vout.

In fact, the voltage present on the ZCD pin is compared to the reference voltage ($V_{REF-PSR}$ = 2.6 V) of the internal E/A to generate the control voltage.

The E/A is an Operational Trans-Conductance Amplifier (OTA) designed to operate either with a narrow or wide bandwidth so that the HVLED101 is able to control equally a high power factor topology or a DC-DC topology (for example, flybacks fed by PFC pre-regulators).

The output of the E/A is connected to the FB pin, where the suitable compensation network can be placed, referred to the common potential (SGND); an equivalent small signal model of this component, useful for compensation network definition, is illustrated in Figure 14, while the OTA characteristic curve is illustrated in Figure 15.

Figure 14. OTA output equivalent model

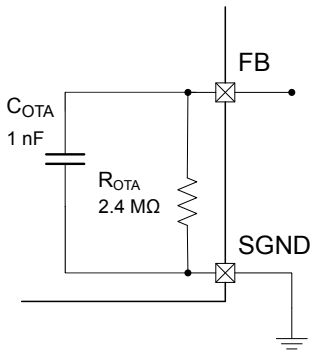
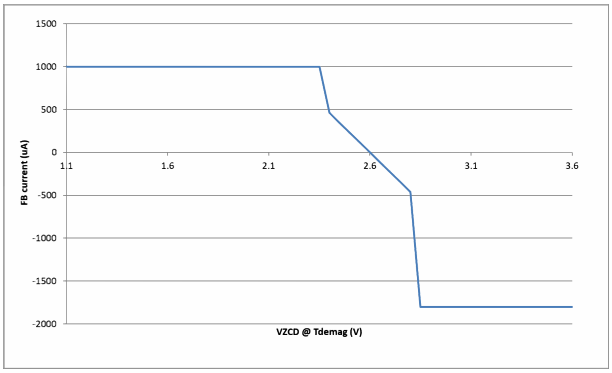


Figure 15. OTA output characteristic



R_{ZCD} must be selected in order not to exceed the maximum ZCD pin current ($I_{ZCD\text{-}src}$ from datasheet recommended operating conditions) during MOSFET on-time.

$$R_{ZCD} > \frac{Vinpk_{max}}{I_{ZCD\_src}} \cdot \frac{N_{aux}}{N_{pri}} \quad (8)$$

The lower part of the divider must be selected to regulate the desired output voltage according to the following equation:

$$R_{FB} = \frac{R_{ZCD} \cdot V_{REF\text{-}PSR}}{V_{OUT} \cdot \frac{N_{aux}}{N_{sec}} - 1} \quad (9)$$

1.5.2 Burst mode during primary side regulation

When the load is very light, the FB pin voltage decreases below the V_{BM} threshold, the HVLED101 enters burst mode operation (deep low-consumption mode) and the IC starts the dedicated burst mode algorithm.

The PSR operation needs to generate some switching activity to refresh the content of the measurement unit. The burst mode algorithm provides four switching cycles following a pure QR scheme (including T_{DLY}) with a repetition time (T_{REP}) that is inversely proportional to the voltage that is present at the FB pin at the end of the four switching cycles.

Figure 16. **PSR burst mode waveforms**

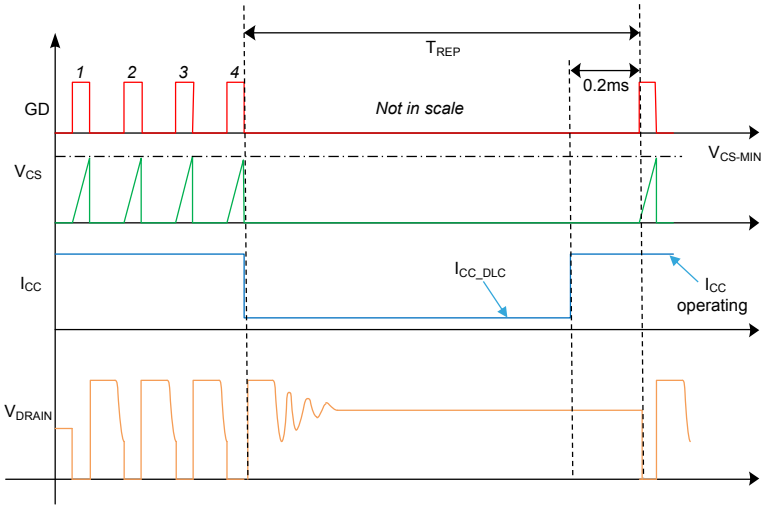
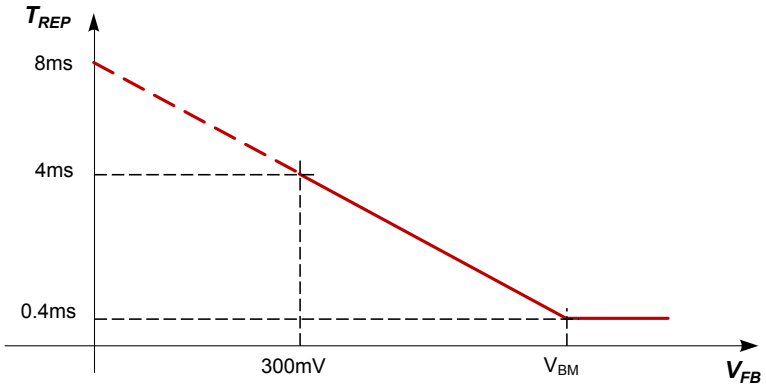


Figure 17. **PSR burst mode repetition rate**



During the inactive phase of the burst mode, the consumption of the HVLED101 is reduced to $I_{CC\text{-}PSR\text{-}BM}$.

During the generation of the four GD cycles, the current sense threshold is bottom limited to generate a minimum demagnetization time and improve the Vout measurement's accuracy.

This minimum current sense level represents, in turn, a small minimum power delivered from the primary to the secondary side: this minimum power delivery has to be dissipated by a simple secondary side bleeder resistor (or equivalent structure).

As the control loop forces the FB pin voltage above V_{BM}+V_{BM_HYST}, the normal mode operation is restored.

1.5.3 Secondary side regulation and relevant burst mode

The secondary side regulation application includes an error amplifier, placed on the secondary side, that drives an optocoupler to regulate the power transfer from input voltage to output load.

The output of the optocoupler is connected directly to the OPTO pin.

The operational OPTO arrangement includes the pull-up current generator (I_{OPTO}) with a parallel resistor (R_{OPTO}) for control loop compensation.

Figure 18. **Optocoupler operation typical arrangement (Constant Output Voltage)**

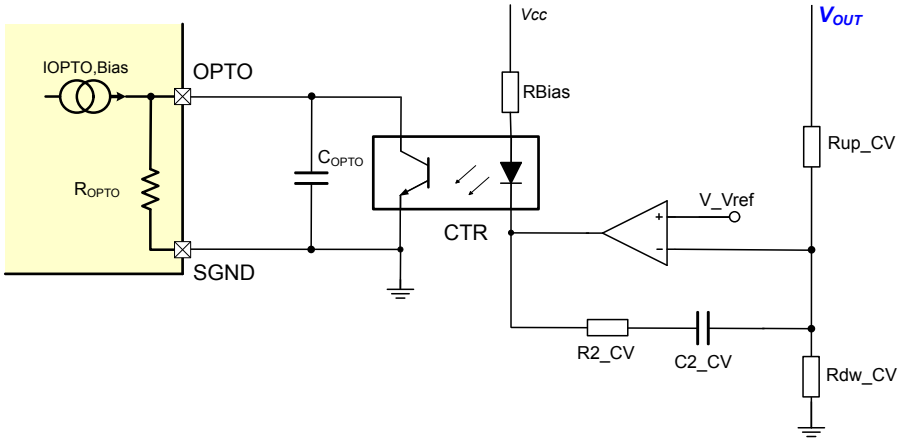


Figure 19. **Optocoupler operation typical arrangement (Constant Output Current)**

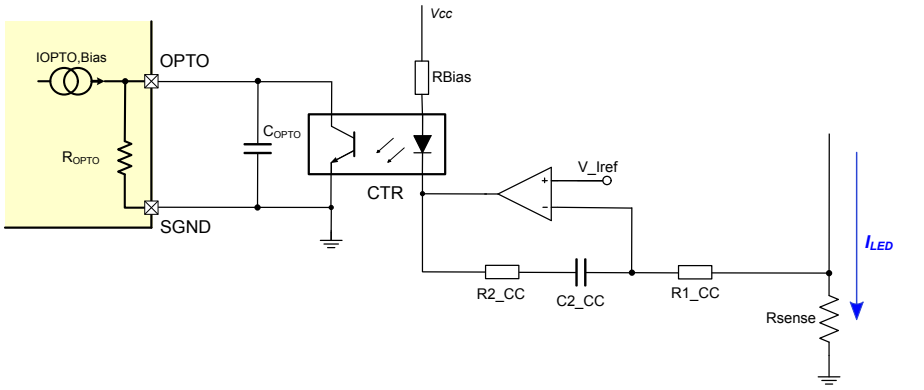
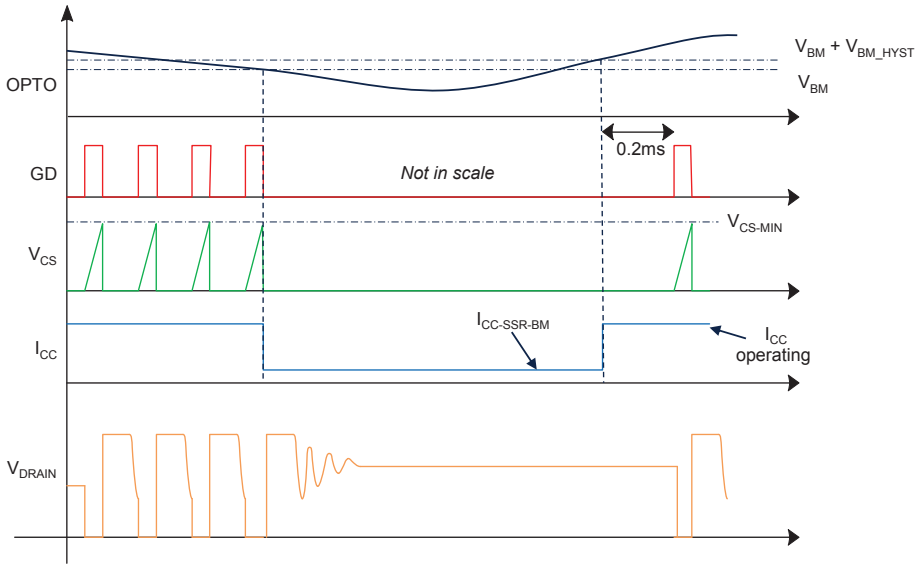


Figure 20. **SSR burst mode waveforms**



When the voltage of the OPTO pin drops below the V_{BM} threshold, the system enters deep low consumption until the OPTO pin voltage returns above the V_{BM}+V_{BM_HYST} threshold: this behavior realizes the burst mode, whose frequency and depth depend on loop bandwidth and load power level.

Note that, at this occurrence, the system restarts after approximately 200 µs: this time is intended to filter spurious glitch that may affect the OPTO pin.

1.6 Gate driving

[Involved pin 9: GD]

The gate driver is able to drive an external switch with 480 mA source and 830 mA sink capability.

To avoid undesired switch-on of the external switch an internal pull-down circuit holds the pin low during low consumption. This circuit ensures 2 V maximum on the pin (@ Isink = 2 mA) when V_{CC} is below the V_{CC-SHD} threshold. This allows omitting the "bleeder" resistor connected between the gate and the source of the external switch used for this purpose.

1.7 Disabling feature

[Involved pin 7: OPTO]

The HVLED101 can be disabled acting on the OPTO pin using a pull-down device (BJT or MOSFET). The behavior of the device at this occurrence is described in Section 1.5.3: Secondary side regulation and relevant burst mode.

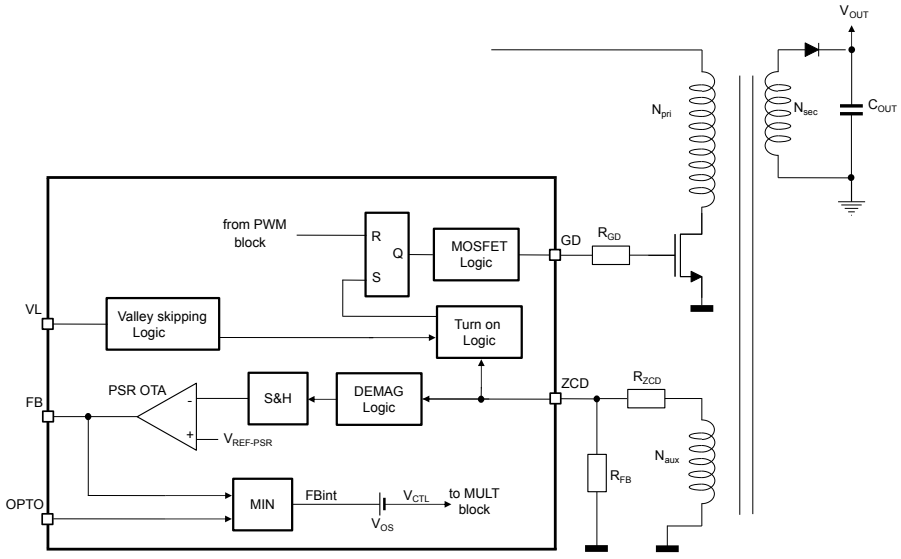
1.8 Zero current detection circuit and valley skipping

[Involved pins 10: ZCD, 5:VL]

The ZCD pin is intended to realize the zero current detection mechanism while VL allows to set at which load level the system starts skipping valleys.

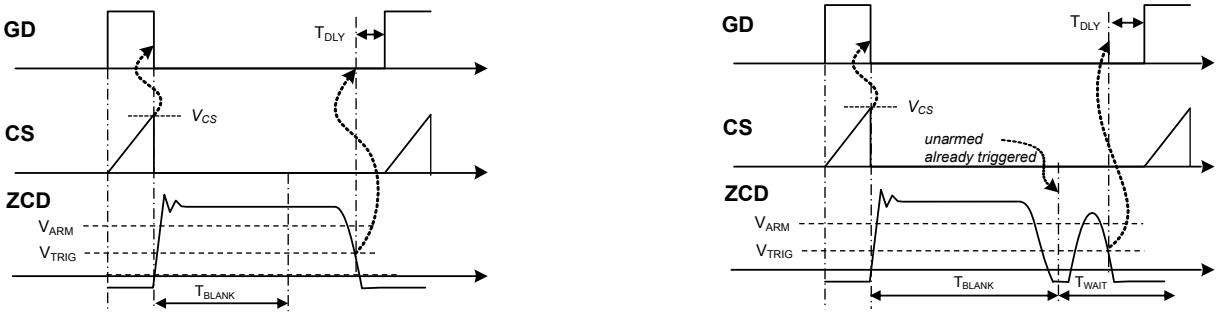
Section 1.8: Zero current detection circuit and valley skipping

Figure 21. Zero current detection circuit and valley skipping block diagram



The voltage developed across the transformer auxiliary winding, which is an image of the voltage present on the drain of the MOSFET, is applied to the ZCD pin.

Figure 22. **Quasi-resonant (QR) operating scheme**



When the MOSFET turns off, the HVLED101 applies a minimum blanking time (T_{BLANK}=1.5 µs) in order to reject spurious oscillations.

After the minimum blanking time, ZCD logic checks the level of ZCD voltage; if it is higher than the arming threshold (V_{ARM}), then it waits indefinitely for the first falling edge on the ZCD pin below the triggering threshold (V_{TRG}).

On the contrary, if the ZCD level is lower than the arming threshold, a maximum waiting time (T_{WAIT}) is started to prevent latching conditions.

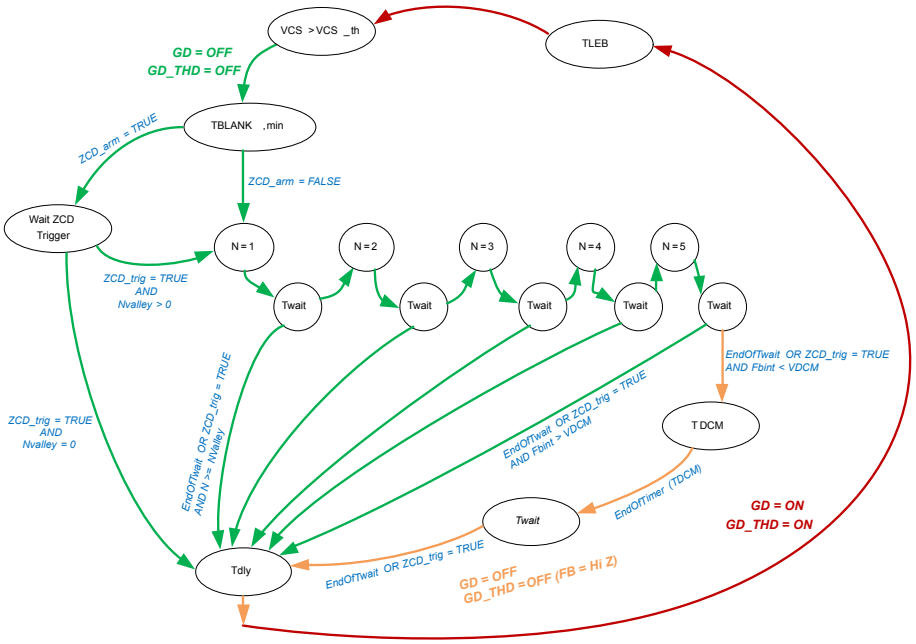
This waiting time (T_{WAIT}) is proportional to the programmed delay time T_{DLY} (see Section 1.10: Configuration programming and parameter selection) configured by the R_{DLY} resistor on the DLY/CFG pin as per the following relationship:

$$T_{WAIT} = 8 \cdot (T_{DLY} - 100ns) + 100ns \quad (10)$$

When the falling edge is detected, the IC can either turn on the MOSFET after the programmed delay time (T_{DLY}) or start counting the number of falling edges (valley) defined by the voltage at the VL pin as per valley skipping algorithm (see Section 1.9: VL pin structure).

Below, the ZCD algorithm diagram is shown.

Figure 23. **ZCD algorithm diagram**



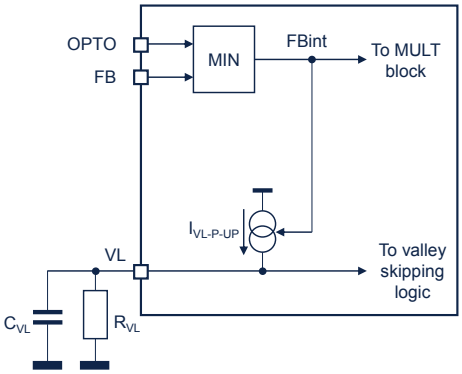
1.9 VL pin structure

[Involved pin 5: VL]

The VL pin is internally connected to a current source proportional to the control signal (OPTO or FB). Placing a resistor between VL and GND allows to obtain a voltage proportional to OPTO or FB.

The capacitor C_{VL} may be needed for noise filtering and ripple reduction.

Figure 24. VL pin structure



The VL voltage, compared to the VL1-VL6 internal thresholds, defines the number of valleys skipped (NVALLEY) as per the algorithm described in Figure 25.

The user can decide at which load level the system starts skipping valleys according to the following relationship:

$$R_{VL} = \frac{VL1}{K_{Ivl} \cdot \left(\frac{4}{\sqrt{2} V_{acx}} \cdot \frac{P_{out}}{\eta} \cdot \frac{R_{CS}}{K_M} + V_{OS} \right)} \quad (11)$$

Where:

VL1 is the valley threshold, internal to the IC, which is compared to the voltage on the VL pin

K_{Ivl} is the valley lock block gain (10 µA/V, it can be derived from the datasheet parameter $I_{VL-P-UP}$: if V_{OPTO} changes from 1 V to 2 V, the VL current changes from 10 µA to 20 µA.)

K_M is the multiplier gain = 0.176 V/V

V_{OS} is the FB and OPTO pin internal offset = 0.5 V

V_{acx} is the input AC mains voltage

Pout is the maximum output power

η is the expected efficiency

R_{CS} is the primary sensing resistor

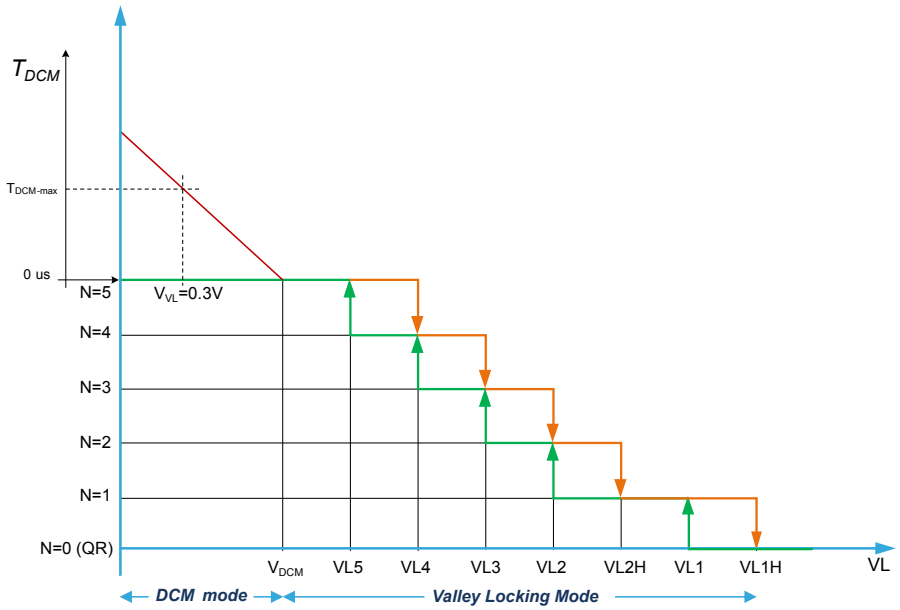
As the load decreases, the voltage on the VL pin (proportional to control voltage) drops, and the HVLED101 increases the number of valleys skipped.

The controller stays locked in a valley until the load changes significantly (valley lock feature).

After skipping 6 valleys, the system operates in discontinuous conduction mode (DCM) and a further delay T_{DCM} is applied before triggering the turn-on.

T_{DCM} increases as the VL voltage decreases.

Figure 25. **Valley skipping algorithm**



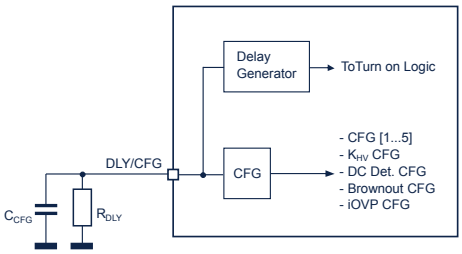
1.10 Configuration programming and parameter selection

[Involved pin 4: DLY/CFG]

The main switch always turns on when the demagnetization occurs, but to minimize the switching losses, it is convenient to turn it on in correspondence with the minima of the oscillation (valley switching).

In the HVLED101, this is achieved by programming the delay time (T_{DLY}) between ZCD detection and switch turn-on by means of R_{DLY} connected to the DLY/CFG pin.

Figure 26. **DLY/CFG pin structure**



The required T_{DLY} can be calculated considering the drain oscillation period after demagnetization.

$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{pri} \cdot C_{DRAIN}}} \quad (12)$$

Where:

L_{pri} is the primary inductance of the transformer

C_{DRAIN} is the estimated total drain node capacitance

$$T_{res} = 2\pi \cdot \sqrt{L_{pri} \cdot C_{DRAIN}} \quad (13)$$

$$T_{DLY} = \frac{T_{res}}{4} \quad (14)$$

The relationship between the T_{DLY} required and R_{DLY} is expressed by the following formula:

$$R_{DLY} = \frac{T_{DLY} - T_{DLY0}}{K_{DLY}} \quad (15)$$

Where:

T_{DLY0} is the minimum delay time, 100 ns

K_{DLY} is ZCD to GD on gain, 2.13 ns/kΩ

The HVLED101 can be programmed with five different configurations of input range, brownout, and surge protections according to user needs (CFG1-CFG5).

Table 4. Programming configurations

Tau_{CFGn} (µs)	CFG	iOVP	BrOut	K_{HV}	DC Det.	I_{BLEED} @ iOVP
30 µs ... 45 µs	CFG1	ON	Low	High	Low	ON
100 µs ... 140 µs	CFG2	OFF	OFF	Low	Low	N.A.
300 µs ... 410 µs	CFG3	ON	High	High	High	ON
860 µs ... 1.2 ms	CFG4	OFF	Low	Low	Low	N.A.
> 2.05 ms	CFG5	ON	Low	High	Low	OFF

Configuration can be chosen by selecting the value of the time constant (Tau_{CFGn}) associated with the RC network placed between the DLY/CFG pin and GND.

Table 5 summarizes the suggested combination of R_{DLY} and C_{CFG} to obtain both delay time and configuration programming.

Table 5. **Suggested R_{DLY}-C_{CFG} programming values**

T_{DLY} (ns)	R_{DLY} (kΩ) (1%)	C_{DLY} (nF) (5% - >6.3V rated)				
		CFG1	CFG2	CFG3	CFG4	CFG5
164	30	1.2n	3.9n	12n	33n	82n
183	39	1n	2.7n	8.2n	27n	56n
219	56	680p	2.2n	6.2n	18n	39n
260	75	470p	1.5n	4.7n	12n	33n
355	120	270p	1n	2.7n	8.2n	18n
420	150	220p	680p	2.2n	6.8n	15n
483	180	180p	560p	1.8n	5.6n	12n
568	220	150p	470p	1.5n	4.7n	10n
675	270	120p	390p	1.2n	3.3n	8.2n
803	330	100p	330p	1n	2.7n	6.8n
1100	470	82p	220p	680p	2.2n	4.7n
1293	560	68p	180p	560p	1.8n	3.9n

The above configurations are intended to be selected in order to fit different application requirements in terms of input voltage. The typical use of the different configurations is shown in Table 6.

Table 6. **Suggested configuration vs. application input voltage requirements**

CFG	Mains voltage range	Typ. Vin range	Note
CFG1	Universal	90 Vac ÷ 305 Vac	
CFG2	Extended	> 80 V ÷ 400 Vac	Suitable for debug purposes
CFG3	European	180 Vac ÷ 305 Vac	
CFG4	Extended	90 Vac ÷ 400 Vac	
CFG5	Universal	90 Vac ÷ 305 Vac	

Note that CFG2 has the brownout detection disabled and input voltage sensing could operate in an unoptimized range when the input voltage is lower than 80 V. For this reason, it is intended to be used for debug purposes.

1.11 Protections

1.11.1 Overcurrent protection (2nd OCP)

[Involved pin 11: CS]

The 2nd OCP is intended to protect against transformer saturation or output rectifier short-circuit.

During these conditions, the primary current rises quickly to a very high value.

To avoid this current becoming dangerous, a second level OCP protection threshold is provided.

An internal comparator referenced to the V_{OCP2} threshold is used to stop the switching activity as soon as the current sense voltage surpasses this threshold and enters low consumption mode.

The switching stop is kept for a long period (up to T_{OCP}) before a new restart attempt.

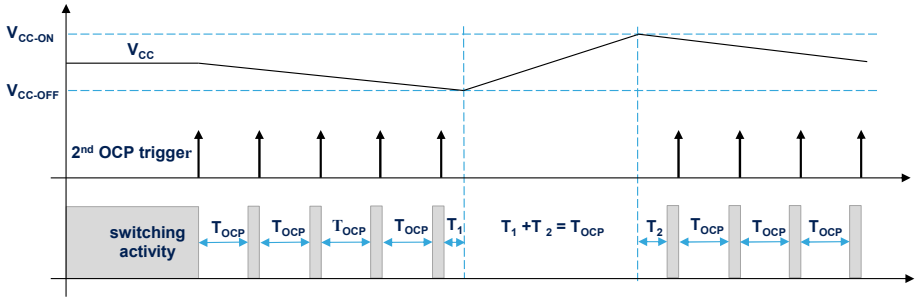
During T_{OCP}, the driving signal GD_{THD} of the internal THD switched resistor is kept always ON, so that at operation resumption the current sense threshold starts from zero, providing a smooth start.

The diagram below shows continuous protection triggering, when V_{CC-OFF} is reached, the HVSU generator is enabled, and the timer is frozen.

The timer restarts as V_{CC-ON} is reached, and protection goes on triggering; if, in the meantime, the output voltage zeros, the UVP triggers and overrides 2nd OCP.

If the protection is only a random event, the IC resumes operation soon after the first trigger.

Figure 27. 2nd OCP waveforms



1.11.2 Input overvoltage protection (iOVP)

[Involved pin 1: HVSU]

iOVP is intended to protect in case of a surge voltage at converter input.

It is only active with configurations CFG1, CFG3, and CFG5, selected by the time decay imposed by the R_{DLY}-C_{CFG} programming network at the DLY/CFG pin (Section 1.10: Configuration programming and parameter selection).

When the input voltage surpasses the programmed value, the input overvoltage protection stops the switching activity and activates the discharge current I_{BLEED} (where required).

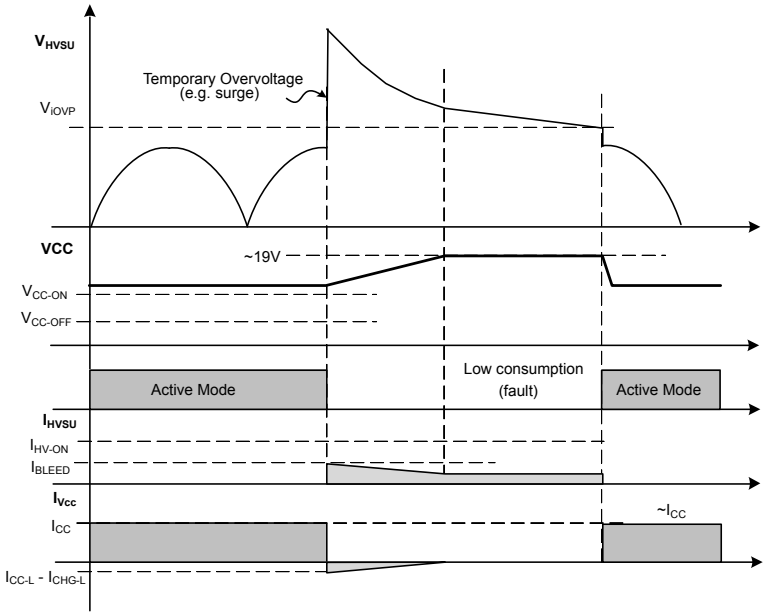
During iOVP, the internal THD optimizer drives the internal switched resistor always OFF and the THD pin is set in high impedance.

The I_{BLEED} current discharges the input capacitor to speed up the recovery from surge occurrence.

In case of steady input overvoltage, the VCC pin rises until the I_{BLEED} generator automatically reduces the absorbed current. At this occurrence, the HVSU unit provides the whole current for the HVLED101 and the input capacitor is discharged by a current that is almost equal to I_{CC} plus the internal consumption of the HVSU unit.

When the HVSU voltage is lower than the protection level, the HVSU charges V_{CC} to reach V_{CC-ON} (if required) and active mode is entered.

Figure 28. **iOVP waveforms**



1.11.3 Brownout protection (BO)

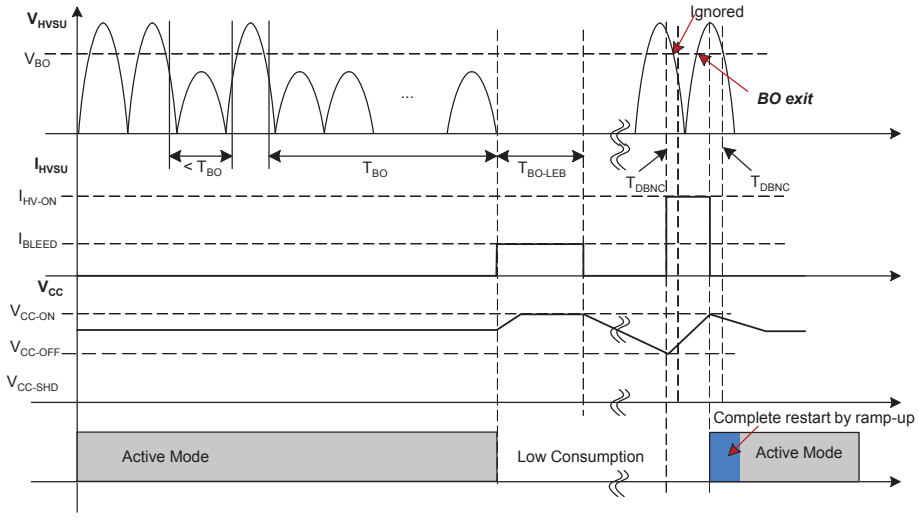
[Involved pin 1: HVSU]

In order to avoid operation at insufficient input voltage, the IC moves to low consumption mode if the input voltage is lower than the programmed threshold (Table 4) for at least T_{BO} (500 ms min.).

During masking time (T_{BO-LEB}), activated after brownout triggering time, the HVSU comparator is ignored to prevent false restart due to EMI filter resonance oscillations, while I_{BLEED} is turned on to discharge any residual oscillation due to the EMI filter operating condition at turn-off instant.

After the end of T_{BO_LEB}, the input voltage is checked to be higher than the threshold only during the charging period of V_{CC}: a small time (T_{DBNC}) is applied after HVSU activation to prevent false reading. Note that the value of the resistance that is in series with the HVSU pin, multiplied by I_{CHG-H}, sets the hysteresis for the brownout threshold voltage.

Figure 29. **Brownout protection**



1.11.4 Undervoltage protection

[Involved pin 10: ZCD]

The primary side regulation sample and hold constantly monitors the output voltage. If it steadily falls below the V_{UVP} threshold for at least T_{UVP}, the IC is shut down and ART state is invoked to try a new operating attempt. Note that, during the V_{CC} recycling, the ART timer is frozen during the V_{CC} recharging phase (from turn-off to turn-on thresholds); furthermore, as T_{ART} elapses, the HV current generator is activated immediately, without waiting for the V_{CC} turn-off threshold to be reached. At operation resumption attempt after ART state, the IC starts from the ramp-up phase.

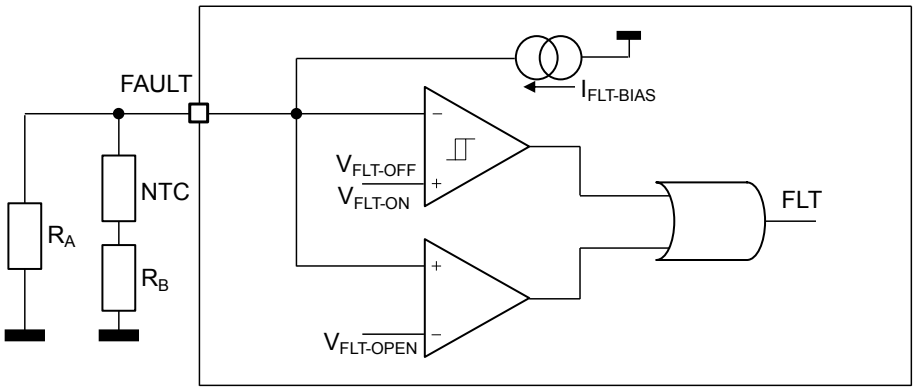
1.11.5 General fault pin and NTC connection

[Involved pin 3: FAULT]

The HVLED101 embeds one general purpose pin intended to disable the switching activity and move the IC into low consumption if the voltage at this pin falls below a threshold level ($V_{FAULT} < V_{FLT-OFF}$) or is left floating ($V_{FAULT} > V_{FLT-OPEN}$). Also, in this case (like for UVP), as the protection is triggered, the ART state is invoked: after T_{ART} elapses, the IC waits for the FAULT condition reset before resuming operation (starting from the ramp-up phase).

The FAULT pin is mainly used to manage an NTC thermistor: in fact, the lower threshold has a well-defined hysteresis and the pin sources a precise current ($I_{FLT-BIAS}$ = 50 µA) to create the desired thermal hysteresis for final application.

Figure 30. Fault pin block diagram



The NTC can be linearized using a resistor network consisting of one resistor in series and one in parallel. The design approach must firstly ensure that the FAULT voltage is greater than $V_{FLT-OPEN}$ if either the temperature is lower than the minimum operating value or the NTC is disconnected. The value of the FAULT voltage is then equal to $V_{FLT-OFF}$ (thermal protection activated) at maximum operating temperature. The pin is also able to sense the absence of NTC, because the pin left open is internally pulled up above an upper threshold.

If NTC is not used, a fixed resistor (22 kΩ to 47 kΩ) should be connected from pin to GND.

During FAULT pin protection, the internal THD optimizer drives the internal switched resistor always OFF (setting δc = 0, as described in Section 1.4: Multiplier and THD optimizer) and the THD pin is set in high impedance.

1.11.6 VCC short-circuit protection

[Involved pins 1: HVSU, 14: VCC]

Overload or short-circuit on the VCC pin prevents the internal high-voltage startup unit from raising the V_{CC} voltage from 0 V. On the other hand, continuous operation of the charging unit at maximum current may result in permanent damage of the device.

For this reason, if the V_{CC} is lower than 1.7 V, then the charging current of the high-voltage startup unit is reduced to a safe value.

1.12 Appendix B: list of abbreviations

The list of the abbreviations adopted in the application note is reported in this appendix. The symbols corresponding to HVLED101 electrical characteristics can be found in the relevant datasheet.

Table 7. List of abbreviations

Symbol	Description
C2_CC	Capacitor of secondary side compensation network belonging to feedback network (CC mode)
C2_CV	Capacitor of secondary side compensation network belonging to feedback network (CV mode)
C_{DRAIN}	Total capacitance of the drain's node
Coss	MOSFET's drain to source capacitance
C_{OUT}	Output capacitor
C_{Fp}	Capacitor of primary side compensation network directly placed between FB pin and GND
C_{Fs}	Capacitor of the R/C of the primary side compensation network
C_{VL}	Filter capacitor placed between VL pin and GND
C_{CFG}	Capacitor for parameter selection
C_{THD}	Filter capacitor for THD optimizer
C_{OPTO}	Capacitor placed between OPTO pin and GND
Cvcc	VCC bulk capacitor
f_{res}	Frequency of the main resonance of the drain oscillation after demagnetization
f_{sw}	Switching frequency (avg, min, or max)
I_{LED}	Average value of LED current
L_{pri}	Primary inductance of flyback transformer
N_{aux}	Number of turns of transformer's auxiliary winding
N_{pri}	Number of turns of transformer's primary side winding
N_{sec}	Number of turns of transformer's secondary side winding
Pin	Input power
Pout	Output power
R1_CC	Resistor of secondary side compensation network connecting E/A with R_{sense} (CC mode)
R2_CC	Resistor of secondary side compensation network belonging to feedback network (CC mode)
R2_CV	Resistor of secondary side compensation network belonging to feedback network (CV mode)
RBias	Optocoupler input biasing resistor
R_{CS}	Primary side shunt resistor connected in series with the source of the MOSFET
Rdw_CV	Lower resistor of secondary side compensation network belonging to feedback network (CV mode)
R_{FB}	Lower resistor of the ZCD network
R_{FF}	Feedforward resistor used to adjust the propagation delay compensation
R_{Fs}	Resistor of the R/C of the primary side compensation network
R_{HVSU}	Resistor in series with high-voltage startup pin
Rsense	Secondary side sensor resistor
Rup_CV	Upper resistor of secondary side compensation network belonging to feedback network (CV mode)
R_{VL}	Resistor between VL and GND used to set the valley skipping

Symbol	Description
R_{ZCD}	Upper resistor of the ZCD network
T_{demag}	Demagnetization time of the transformer
T_{res}	Time period of the main resonance of the drain oscillation after demagnetization
Vin	Input voltage
Vinpk	Peak value of input voltage
V_{ac}	Mains (AC) voltage supply applied to the application
Vout	Output voltage
Vref_CC	Reference voltage for SSR – CC loop
Vref_CV	Reference voltage for SSR – CV loop
η	Efficiency (%)
θ	Angular Phase of the mains voltage

Revision history

Table 8. **Document revision history**

Date	Version	Changes
18-Nov-2024	1	Initial release.

Contents

List of tables

List of figures