SRK1004A/B/C/D synchronous rectification controller for non-complementary Active Clamp Flyback converters evaluation board

Introduction

The EVLSRK1004A, EVLSRK1004B, EVLSRK1004C, and EVLSRK1004D in Figure 1 are evaluation boards, designed for the evaluation of the SRK1004 synchronous rectification controller.

The first part of this application note describes the features of the IC along with some applicative information.

The evaluation board schematics are then described and suggestions are provided on how to connect to an existing flyback converter.

The document concludes with a discussion on thermal and layout optimization principles.

The board codes and descriptions are provided in Table 1.

Figure 1. EVLSRK1004–SR controller demonstration board

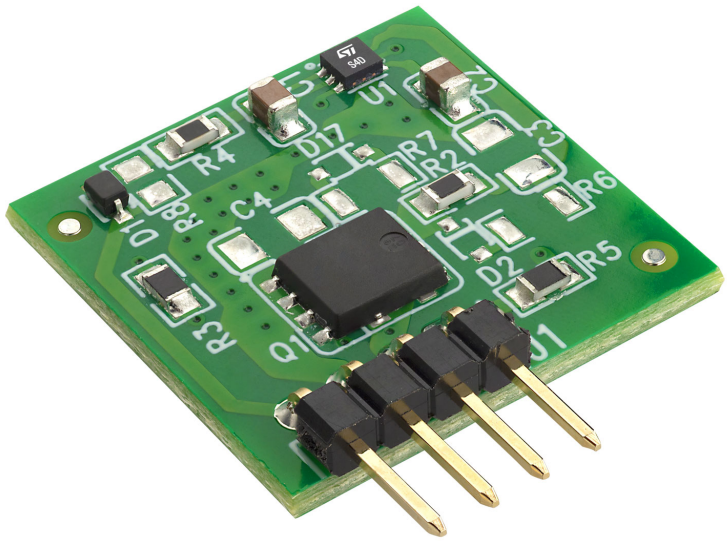


Table 1. Product summary

Board	MOSFET				Controller		
Pn	Pn	VDS [V]	ID [A]	Rds,on [mΩ]	Pn	VCC [V]	Typ. turn-off delay [ns]
EVLSRK1004A	BSC080N12LS-G	120	99	9.5 @4.5V	SRK1004A	5.5	25
EVLSRK1004B	BSC034N10LS5	100	156	4.5 @4.5V	SRK1004B	5.5	150
EVLSRK1004C	BSC093N15NS5	150	87	9.3 @10V	SRK1004C	9	25
EVLSRK1004D	STL120N10F8	100	125	4.6 @10V	SRK1004D	9	150

1 Operating principle of the SRK1004

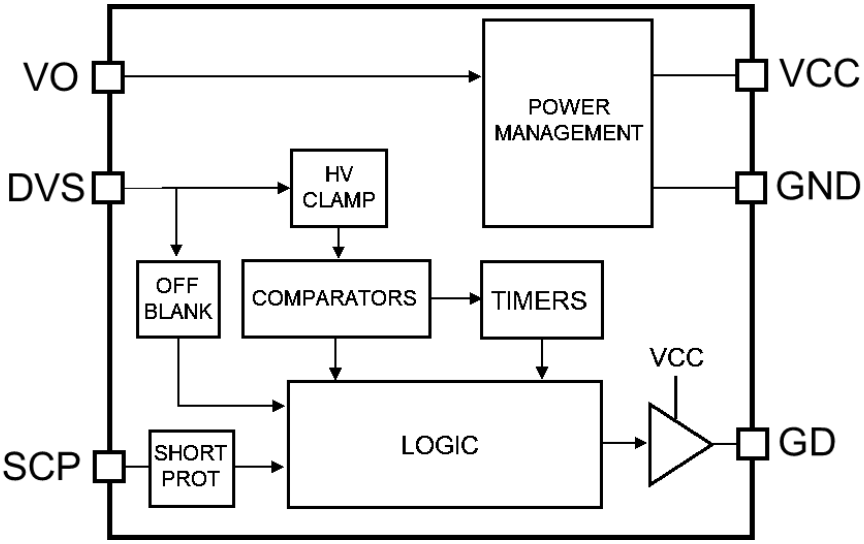
1.1 Application connection

The SRK1004 is a controller intended for secondary-side synchronous rectification (SR) in Non-Complementary Actively Clamped Flyback converters. The four different variants of this IC provide a gate-drive output voltage suitable for N-channel logic-level or standard level power MOSFETs.

The control scheme of this IC is such that the SR MOSFET is switched on as soon as current starts flowing through its body diode and it is then switched off as current approaches zero.

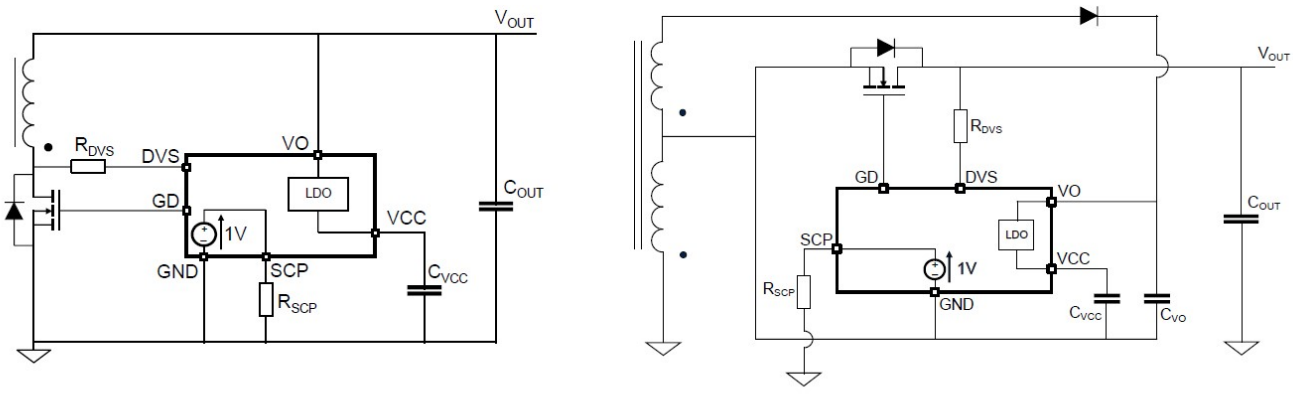
The SRK1004 is supplied by the voltage present at the VCC pin: such voltage is obtained by an internal low dropout regulator connected to the VO voltage, that must be lower than 36 V. When VO is lower than the VCC regulation setpoint, VCC approximates VO. The VO pin embeds UVLO protection to prevent the SR MOSFET being driven by insufficient driving voltage.

Figure 2. SRK1004 internal block diagram



The SRK1004 can be used with the SR MOSFET placed either between the secondary-side GND and transformer (low-side configuration - Figure 3 - *left*) or between the transformer and output voltage (high-side configuration - Figure 3 - *right*).

Figure 3. SRK1004 connection diagrams



Low-side configuration

High-side configuration

In case of low-side configuration of the SR MOSFET, the VO pin of the IC can be supplied by the output voltage bus, while the ground (GND) pin must be connected to secondary-side GND together with the source terminal of the SR MOSFET.

In case of high-side configuration, the source terminal of the SR MOSFET and the ground of the IC are connected to the swinging node of the secondary winding, while VO is typically supplied by an auxiliary winding with a rectifier diode and a buffer capacitor connected, as shown in Figure 3 *right-hand side*.

When operated in high-side configuration, a dedicated short-circuit protection (SCP) function enables a quick detection of short-circuit conditions to inhibit its operation as if the IC were powered directly from the output voltage.

1.2 Control algorithm

The SRK1004 control algorithm operates by sensing the drain-to-source voltage V_{DS_SR} of the SR MOSFET using the DVS pin: this is a high-voltage pin and needs to be properly routed to the MOSFET drain through a resistor (390 Ω - 0805 size to withstand surge currents occurring during transient conditions). The signal captured by DVS is applied to a comparator that, using a set of thresholds, triggers turn-on and turn-off of the SR switch, while internal timers mask undesired SR switch activations as described in detail in the SRK1004 datasheet.

NC-ACF converters are operated either close to the boundary between Continuous Conduction Mode (CCM) and Discontinuous Conduction Mode (DCM) or in Transition Mode (TM).

Burst mode is generally used at very light or no load to optimize efficiency in those conditions and minimize standby consumption.

The NC-ACF converter exhibits a specific behavior during demagnetization time: as shown in the timing diagrams of Figure 4 and Figure 5, during the off phase of the main primary switch two or three temporal windows can be observed: the transformer de-magnetization time (TDEM), an idle time (Twait, Figure 5 only), with no current at both primary and secondary, proper DCM operation, and the reverse current build-up time (TREV).

Figure 4. CCM-DCM boundary operation: timing diagram

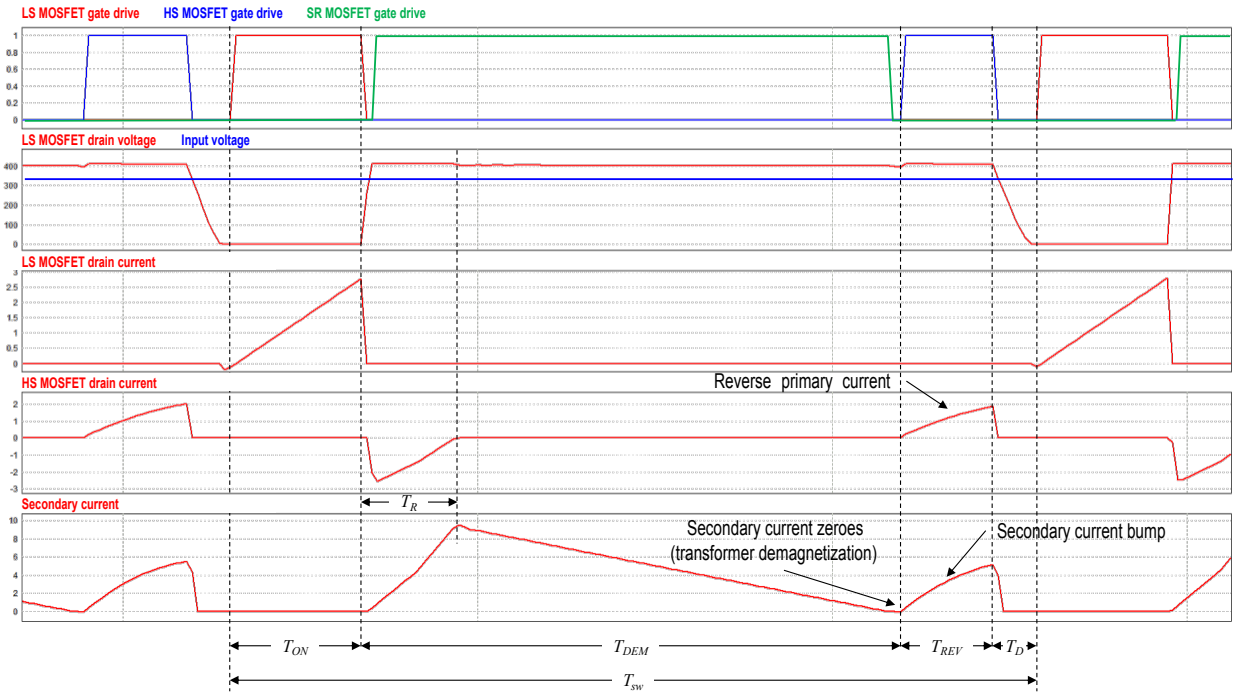
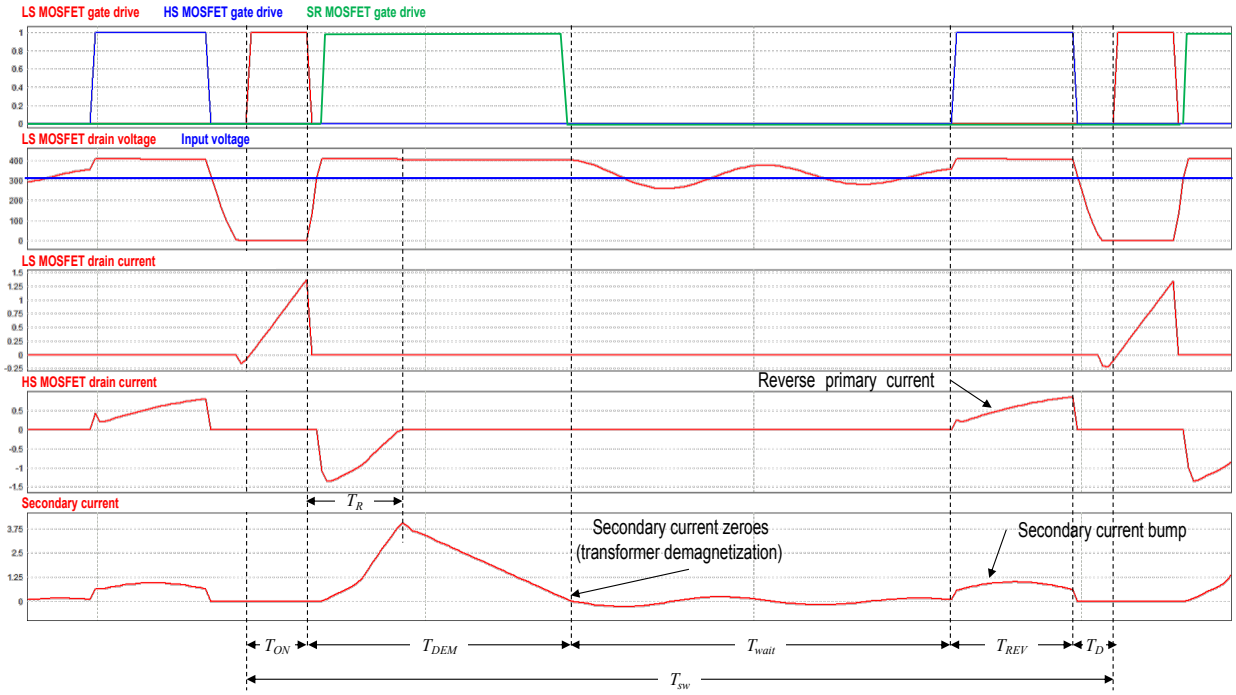


Figure 5. DCM operation: timing diagram



TDEM, the transformer de-magnetization time begins at low-side MOSFET turn-off, and ends when the secondary current reaches zero, or in other words, when transformer complete de-magnetization occurs.

In the first part of TDEM, the energy stored in the magnetizing inductance is released to the secondary, while the energy stored in the leakage inductance is delivered to the clamp capacitor. So, on the one hand, the secondary current builds up, reaching the peak when the primary current is zeroed, and, on the other hand, the drain voltage of the low-side MOSFET is clamped.

In the second part of TDEM, the secondary current linearly decays from peak to zero, that is, the transformer is de-magnetized, while the energy that was in the leakage inductance is maintained into the clamp capacitor.

Once TDEM has elapsed, the high-side switch of the primary half-bridge can be turned on for a proper time that depends on load conditions.

At heavy loads, the converter works at CCM-DCM boundary, TDEM, and TREV are contiguous and the high-side MOSFET is turned on right after the transformer de-magnetization (Figure 4), and the idle time (Twait) is zero.

As the load is reduced, the converter starts operating in DCM: the idle time (Twait) appears between TDEM and TREV, getting longer and longer as the load becomes smaller and smaller (Figure 5). In this DCM condition, the high-side primary switch is turned on either in correspondence with a peak of the low-side MOSFET drain voltage ringing, when the ringing is detectable, or after a certain time-out, when the drain ringing is no longer detectable.

In both cases, CCM-DCM boundary and DCM operations, during TREV the primary current and the secondary current flow contemporarily in a forward mode fashion: at primary, this current creates the conditions to obtain ZVS, while, at secondary, it represents an additional energy delivered to the output in the form of a “current bump”. The current bump during TREV has typically a low amplitude and duration. For this reason, the synchronous rectifier (SR) MOSFET should be on during the first conduction interval only (TDEM), and must be off during TREV to avoid extra power losses.

The control algorithm implemented in the SRK1004 is able to distinguish the two secondary conduction phases.

The controller operation is shown in the following (Figure 6) and (Figure 7), for CCM-DCM boundary and DCM operations respectively.

Figure 6. CCM-DCM boundary: secondary-side signals

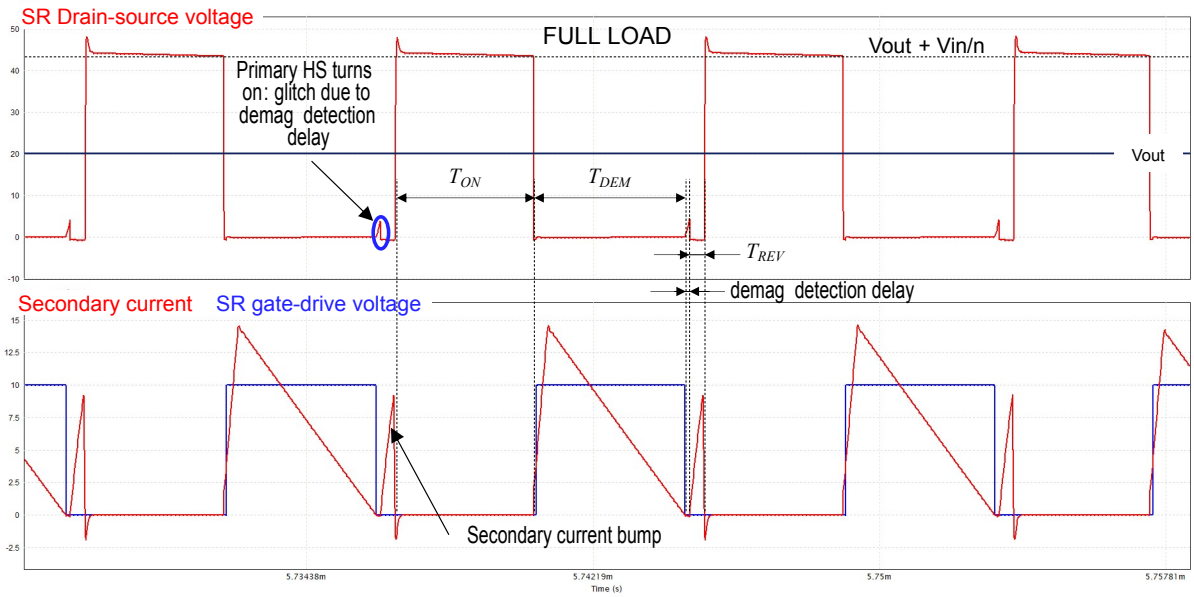
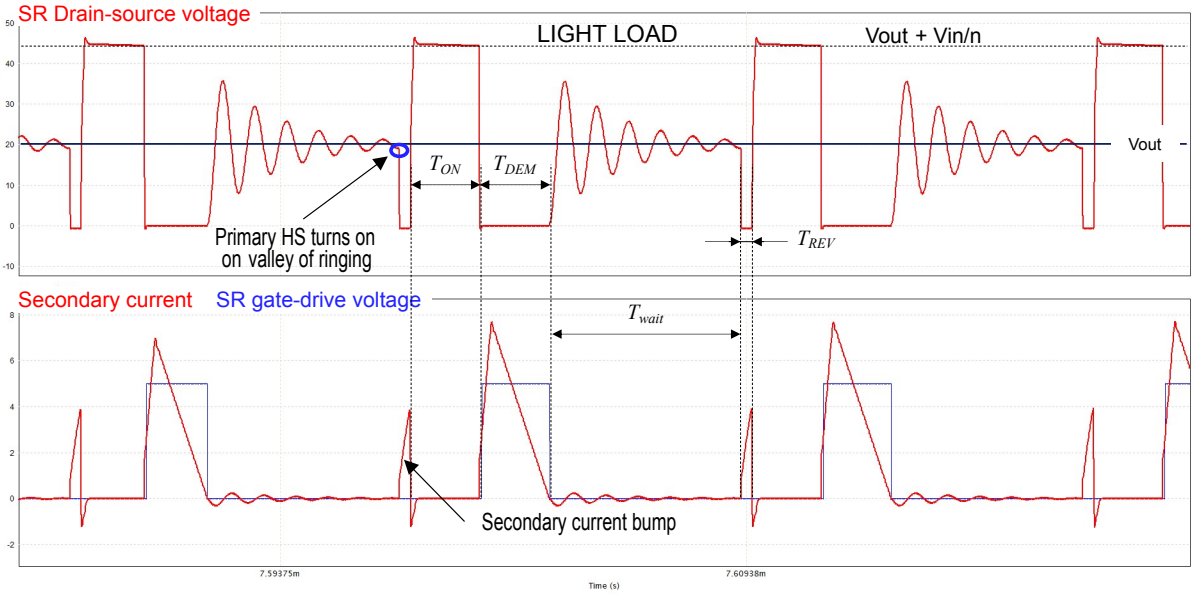


Figure 7. DCM operation: secondary-side signals



1.3 SR MOSFET stray inductance compensation

The SRK1004 is able to compensate for the misdetection of secondary-side current due to the parasitic inductance of the drain terminal of the SR MOSFET. If not compensated, this parasitic causes an earlier detection of the zero-crossing of the DVS voltage signal than the actual zero-crossing of the rectified current and the time lead is given by the ratio:

$$TX = \frac{\mathrm{Ls}}{R_{DS,on}} \quad (1)$$

Where Ls is the parasitic inductance (stray inductance) and R_{DS_ON} is the on-resistance of the SR switch.

The consequence is a premature turn-off, as shown in Figure 7, that means a larger residual diode conduction time, that is, an efficiency degradation.

Considering a current slope of $\frac{di}{dt}$, this residual current (I_{OFF}) is given by:

$$I_{OFF} = -T_X \cdot \frac{di}{dt} \quad (2)$$

Including the internal turn-off delay of a real comparator ($T_{D,off}$). The I_{OFF} current can be better estimated as:

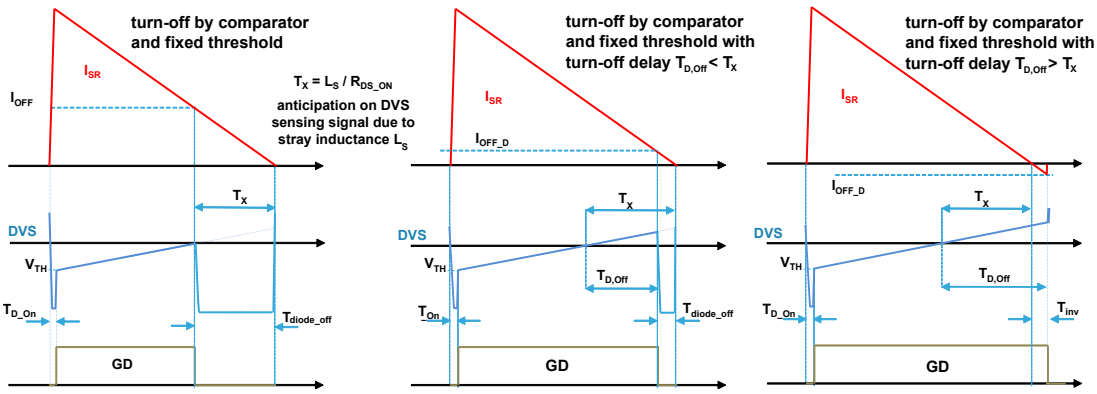
$$I_{OFF\_D} = -(T_X - T_{D,off}) \cdot \frac{di}{dt} \quad (3)$$

If $T_X > T_{D,off}$ (as shown in Figure 8, in the center) the zero-crossing on the voltage signal occurs in advance with respect to the zero-crossing of the rectified current and a residual diode conduction time is still present even if much better than an ideal comparator case.

If $T_X < T_{D,off}$ (as shown in Figure 8, on the right) the MOSFET turn-off occurs after the zero voltage crossing, causing a current inversion that could be dangerous at high current value.

This shows that by properly tuning this propagation delay a perfect match between the zero-crossing of DVS voltage and SR current can be theoretically obtained.

Figure 8. Comparison between comparator turn-off and comparator with extra turn-off delay



To optimize the application, the SRK1004 is provided with different values of extra turn-off delay to avoid a large current flowing into the body diode MOSFET.

Typical extra turn-off delays are as highlighted in Table 2.

Table 2. SRK1004 - internal extra turn-off delay

	Typ. extra turn-off delay [ns]
SRK1004A, C	25
SRK1004B, D	150

1.4 Short-circuit protection – SCP

When the SRK1004 is configured to operate in the low-side configuration (that is, VO = V_{OUT} - Figure 3 – *left-hand side*) in case of short-circuit on the converter's output, as the VO voltage falls below the UVLO threshold (VOOff), the SRK1004 shuts down and stops driving the SR MOSFET. Secondary current conduction through the body diode of the SR MOSFET ensures that, on the primary-side, the ACF controller is still able to correctly detect transformer demagnetization and ensure proper operation of the converter during a short-circuit. The SCP pin, in this configuration, must be connected to GND using a 22 kΩ resistor to disable the short-circuit detection mechanism that is dedicated to high-side configuration.

When the SRK1004 is configured to operate in the high-side configuration (Figure 3 – *right-hand side*), in case of short-circuit on the converter's output, V_{OUT} drops quickly because of the short-circuit impedance, whereas VO decays in a longer time, defined by VCC capacitance and the IC consumption. UVLO protection might not be triggered and the SRK1004 must be stopped by short-circuit protection to prevent operation under a short-circuit condition causing power components to overstress and primary-side controller malfunctioning.

Short-circuit protection is active during demagnetization only and can be configured connecting a resistor (RSCP) between the SCP pin and secondary-side ground. The SCP pin provides a reference voltage VSCP = 1 V, while an internal current comparator triggers SCP if pin source current falls below the ISCP_TH threshold (20 µA). When SCP is triggered, a short-circuit condition is assumed and the SRK1004 turns off the SR MOSFET until the SRK1004 is shut down by VO falling below the UVLO threshold.

The output short-circuit voltage level ($VOUT_{SC}$) can be adjusted selecting RSCP as follows:

$$R_{SCP} = \frac{V_{OUT_{SC}} + 1}{I_{SCP\_TH}} \quad (4)$$

During the primary conduction phase, the SCP pin is clamped to a maximum voltage of 2 V.

2 Evaluation board description

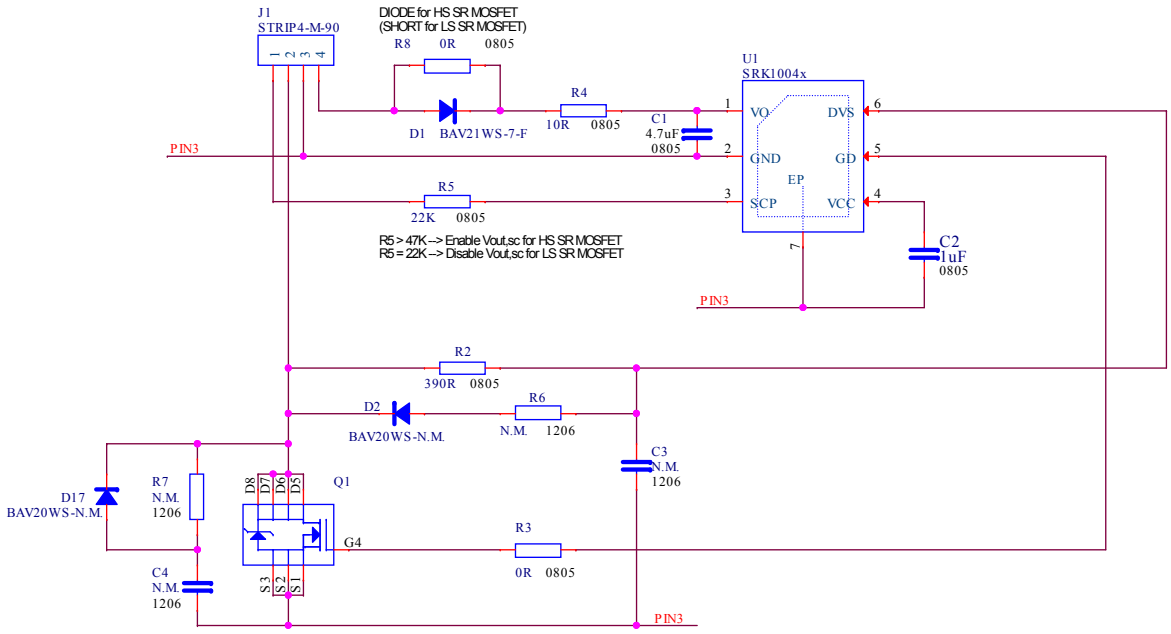
The board is shipped with low-side configuration enabled as per the schematic shown in Figure 9.

Different board variants, equipped by different SRK1004 variants, are listed in Table 1.

The SR MOSFET of the different boards has been selected according to the controller used: logic or standard level and appropriate anticipation.

The breakdown voltages are in the 100 ÷ 150 V range in order to manage applications with output voltages from 5 V to 20 V. This voltage range can also be directly used to supply the SRK1004 VO pin.

Figure 9. Board electrical schematic (LS-mode)



SRK1004 supply voltage, VO, is provided by R8 directly connected to application output voltage. C1 and C2 are the recommended bulk capacitors for SRK1004 supply voltages.

The GND pin and exposed pad are the connection of the IC reference potential: bulk capacitors of supply voltages and SR MOSFET source are then connected to pin3 of J1.

The gate driver (GD) and MOSFET gate terminal are directly connected, but R3 can be substituted by a higher value resistor if needed.

DVS pin current is limited by 390Ω, 0805, SMD resistor. Considering a worst case with dDVS/dt = 5 V/ns, DVS,max = 150 V, dVout/dt = 1.5 V/300µs = 5 V/ms, from device simulations a resistor R1 = 390Ω in series to the DVS pin is required to limit dynamic current injections.

C3 is a spare footprint that can be used if the target application shows excessive dV/dt resulting in excessive dynamic current into the DVS pin.

The board layout offers some spare footprints, namely R7, C4, and D17, to place an additional snubber to mitigate EMI effects if needed (to be evaluated, case by case, on target applications).

SCP protection is inhibited on the board in LS mode, R5 is set to 22kΩ to prevent undesired SCP comparator trigger: UVLO protection of VO pin will serve as short circuit protection.

If the target application requires high-side configuration, very few changes need to be implemented. In particular:

- R5 must be modified by according to equation in Section 1.4: Short-circuit protection – SCP. As a sake of example, considering $VOUT_{SC} = 3V$:

$$R_5 = \frac{V_{OUT_{SC}} + 1}{I_{SCP\_TH}} = 200\text{k}\Omega \quad (5)$$

- R8 must be removed and SRK1004 supply voltage, VO, is provided by auxiliary winding: D1 is used to block negative voltages while R4 limits inrush currents. Hold up time guaranteed by the values provided with the board can be estimated as:

$$T_{res} \approx \frac{C_1 \cdot (V_O - V_{O,OFF,max})}{I_{q,max}} \quad (6)$$

As an example, if nominal VO equals 5V and C1 is 4.7µF the holdup time is approximately equal to:

$$T_{res} \approx \frac{4.7\mu F \cdot (5V - 4.12V)}{290\mu A} = 14ms \quad (7)$$

The bill of material of the four EVLSRK1004x boards (Table 3) are identical, differing only in the MOSFET and SRK1004x part number.

Table 3. EVLSRK1004x - bill of material

Reference	Value	Description	Package	Manufacturer	Part number
C1	4.7uF	50V CERCAP X7R - General purpose	0805	TDK	C2012X7R1H475K125AC
C2	1uF	25V CERCAP - X7R - 10%	0805		
C3	N.M.	500V CERCAP - X7R - 10%			
C4	N.M.	500V CERCAP - X7R - 10%			
D1	BAV21WS-7-F	SMD Schottky rectifier	SOD-323	Diodes Incorporated	BAV21WS-7-F
D2	BAV20WS-N.M.	Small signal switching diode			
D17	BAV20WS-N.M.	Small signal switching diode			
J1	STRIP4-M-90	4 pins strip, right angle, male		WURTH	61304011021
Q1	BSC080N12LS-G (A) BSC034N10LS5 (B) BSC093N15NS5 (C) STL120N10F8 (D)	N-Channel power MOSFET 120 V 12A N-Channel power MOSFET 100V 19A/ 100A N-Channel power MOSFET 100 V 125A N-Channel power MOSFET 150V 87A	8-PowerTDFN	Infineon Infineon Infineon STMicroelectronics	BSC080N12LS-G BSC034N10LS5 BSC093N15NS5 STL120N10F8
R2	390R	SMD standard film RES - 1/8W -5% - 250ppm/°C	0805		
R3	0R	SMD standard film RES - 1/8W -5% - 250ppm/°C	0805		
R4	10R	SMD standard film RES - 1/8W -5% - 250ppm/°C	0805		
R5	22K	SMD standard film RES - 1/8W -5% - 250ppm/°C	0805		
R6	N.M.	SMD standard film RES - 1/8W -5% - 250ppm/°C			
R7	N.M.	SMD standard film RES - 1/8W -5% - 250ppm/°C			
R8	0R	SMD standard film RES - 1/8W -5% - 250ppm/°C	0805		
U1	SRK1004A/B/C/D	SRK1004A/B/C/D - VFDFPN 6L 2x2 pitch 0.65	6DFN_2X2	STMicroelectronics	SRK1004A/B/C/D

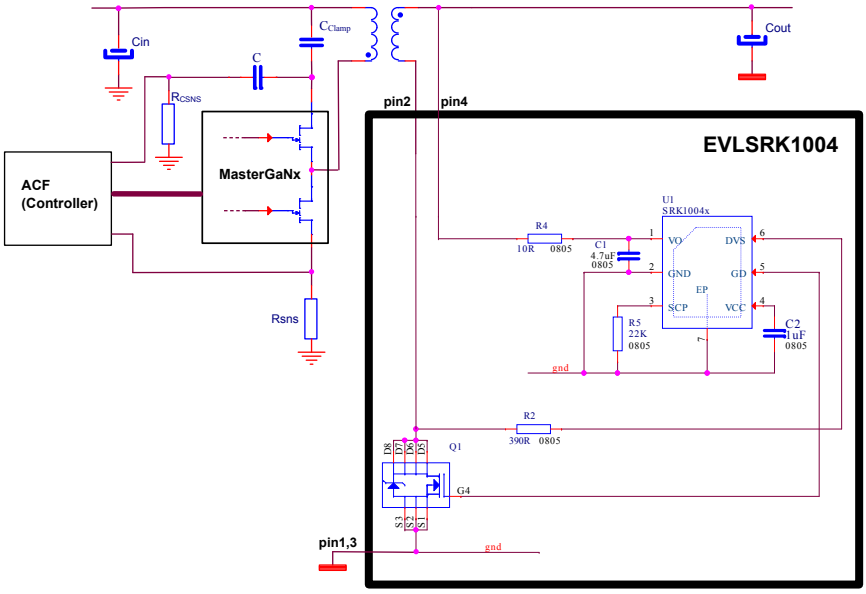
3 How to connect the board to the application

The evaluation board is intended to implement synchronous rectification in an existing flyback converter in the low-side configuration as indicated in Figure 10.

Pin connection must be set as follows:

- Pin 1 to the secondary ground.
- Pin 2 to the transformer negative (flying) terminal.
- Pin 3 to the secondary ground.
- Pin 4 to output voltage.

Figure 10. Low-side connection example



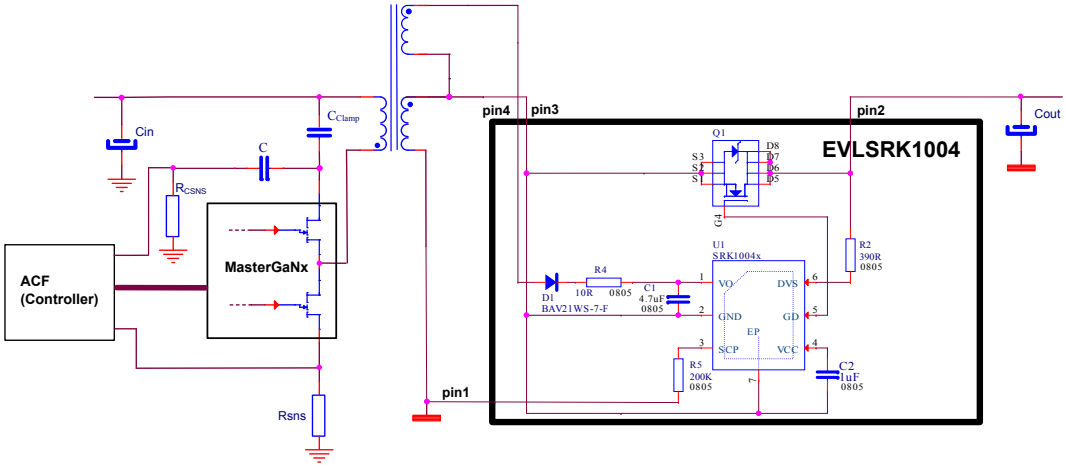
The evaluation board can also be used configured to operate in high-side configuration as indicated in Figure 11.

In this case, referring to connector J1 in the board schematic, different pins have to be connected as follows:

- Pin 1 to the secondary ground.
- Pin 2 to the output voltage.
- Pin 3 to the transformer positive (flying) terminal.
- Pin 4 to auxiliary winding.

In the depicted example, R5 value is modified to 200kΩ to set short circuit V_{out} level to ~3V.

Figure 11. **High-side configuration example**



4 Bench evaluation

The board has been tested on a 65 W 20-5 V ACF converter. The following assertions refer to EVLSRK1004A/B/C/D.

Note that current and voltage probes can affect the IC sensing, leading to malfunctioning.

Signal probing must be accomplished carefully and with minimal modification with respect to the original circuit.

In the figures below, the key signals of the SRK1004 are shown: SRK gate driver (GD), SRK drain voltage sensing (DVS). Other signals shown are SR power MOSFET current (Iq1) and primary-side voltages floating ground (FGND) and high-side driver (HS_prim).

The MOSFET is switched on and off according to its drain-source voltage.

Figure 12. Key signals waveforms of EVLSRK1004 in LS mode on 65 W ACF @115 Vac V_{out}=20 V Iout=3.25 A

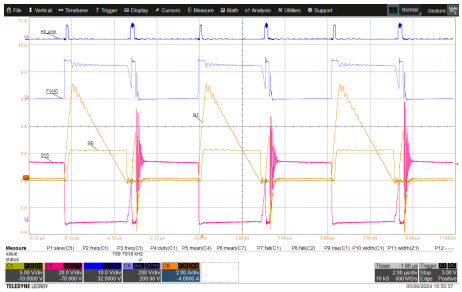
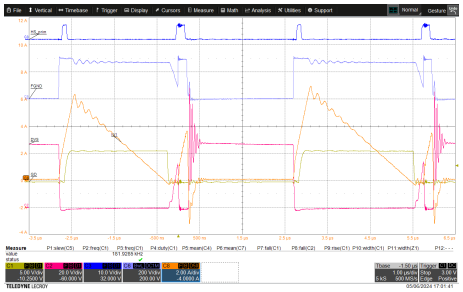
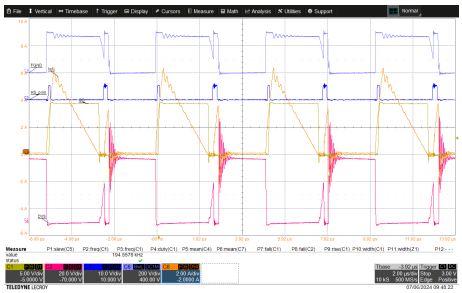
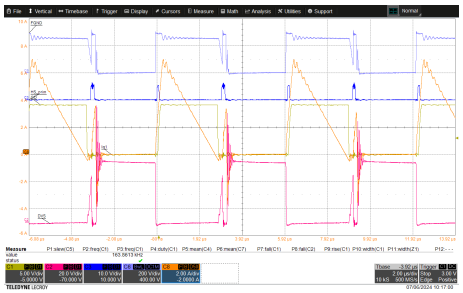
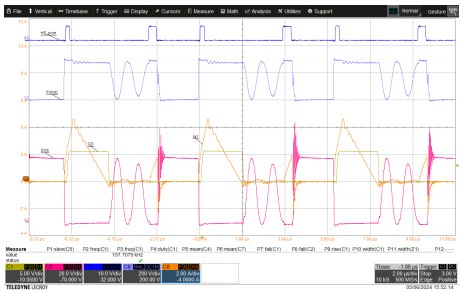
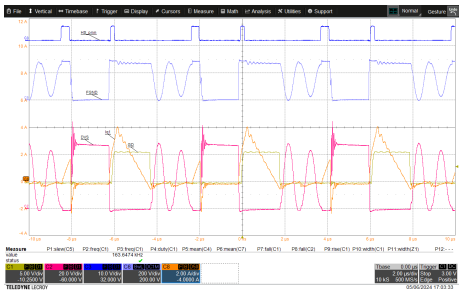
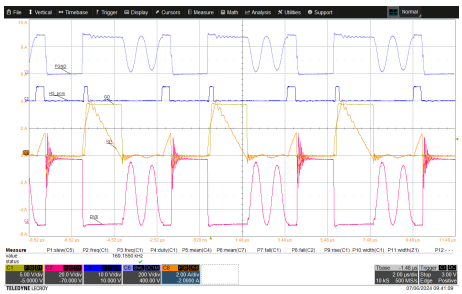
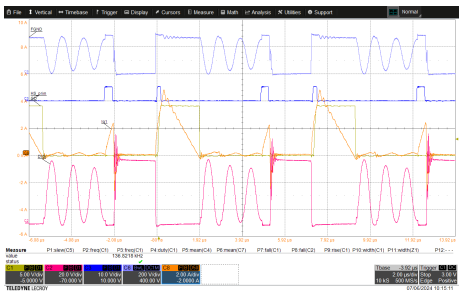
EVLSRK1004A	EVLSRK1004B
	
EVLSRK1004C	**EVLSRK1004D**
	

Figure 13. Key signals waveforms of EVLSRK1004 in LS mode on 65 W ACF @115 Vac V_{out}=20 V Iout=3.25 A

EVLSRK1004A	EVLSRK1004B
	
EVLSRK1004C	**EVLSRK1004D**
	

The MOSFET remains on while the secondary current is flowing through the load (energy is transferred from primary to secondary-side) and turns off (due to DVS crossing the 0 V threshold) when the current is around 0 A.

Note that similar behavior is shown between EVLSRK1004C and EVLSRK1004D. This means that the SRK1004x chosen has turn-off delay adequate to compensate MOSFET anticipation TX = $\frac{\mathrm{Ls}}{R_{DS,on}}$

In addition, these results show that Ls = 3nH based on simulation model are not verified on test bench since turn-off delay 150 ns is enough to compensate the anticipation on DVS.

Similar results are shown @230 Vac as shown below:

Figure 14. Key signals waveforms of EVLSRK1004 in LS mode on 65 W ACF @230 Vac V_{out}=20 V Iout=3.25 A

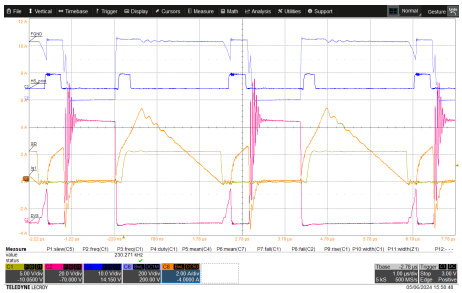
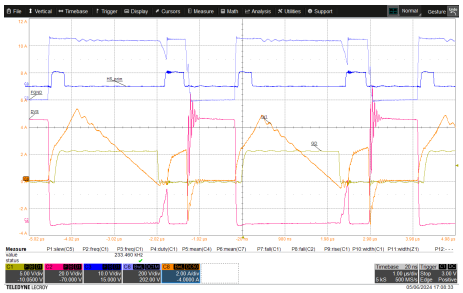
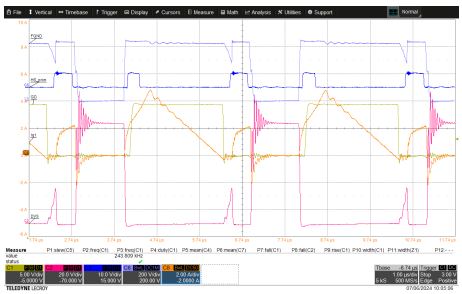
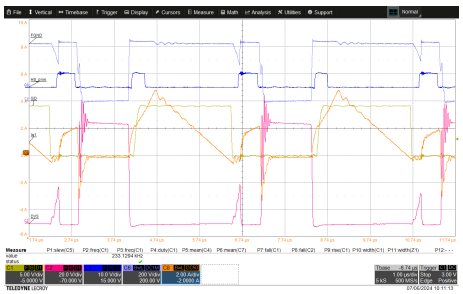
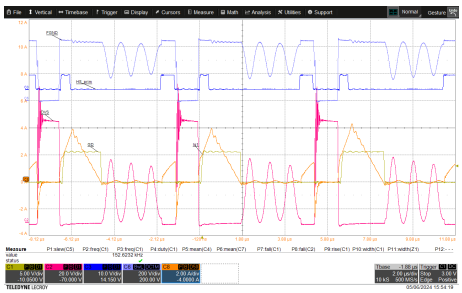
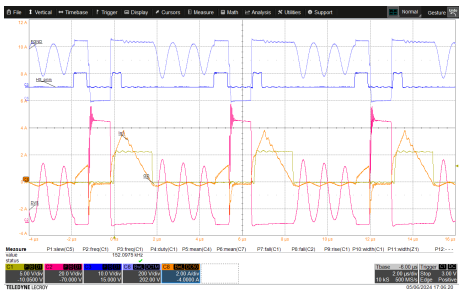
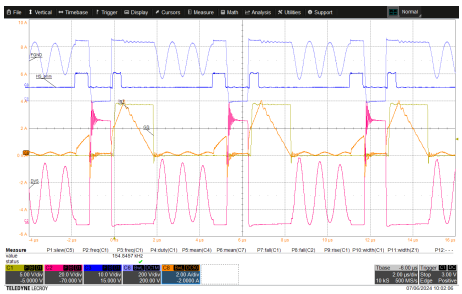
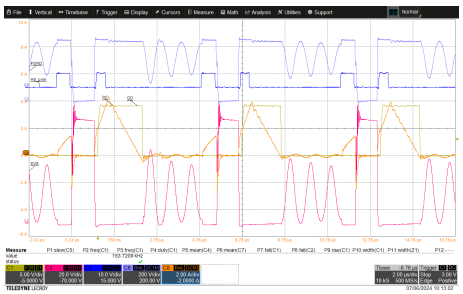
EVLSRK1004A	EVLSRK1004B
	
EVLSRK1004C	**EVLSRK1004D**
	

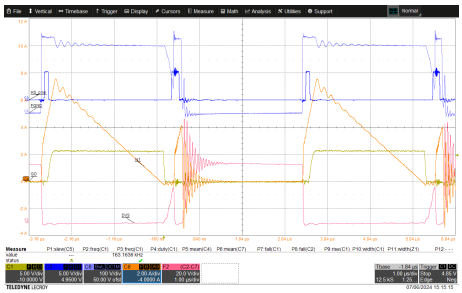
Figure 15. Key signals waveforms of EVLSRK1004 in LS mode on 65 W ACF @230 Vac V_{out}=20 V Iout=1.5 A

EVLSRK1004A	EVLSRK1004B
	
EVLSRK1004C	**EVLSRK1004D**
	

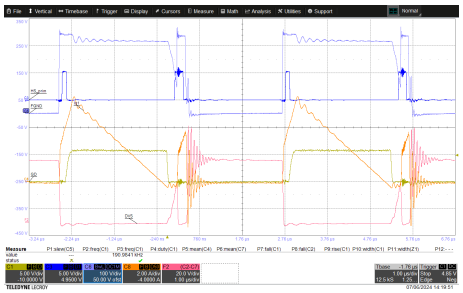
Similar results are shown using EVLSRK1004x in a high-side configuration.
The next image shows a comparison at @high/low input line and full load.

Figure 16. Key signals waveforms of EVLSRK1004 in HS mode on 65 W ACF @115 Vac V_{out}=20 V Iout=3.25 A

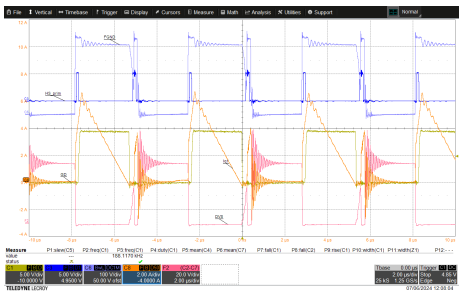
EVLSRK1004A



EVLSRK1004B



EVLSRK1004C



EVLSRK1004D

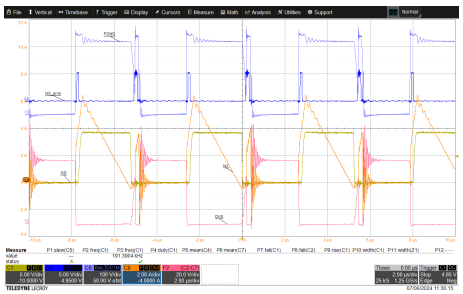
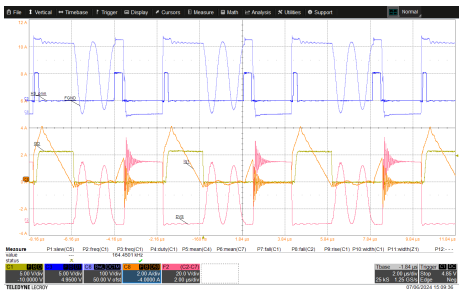
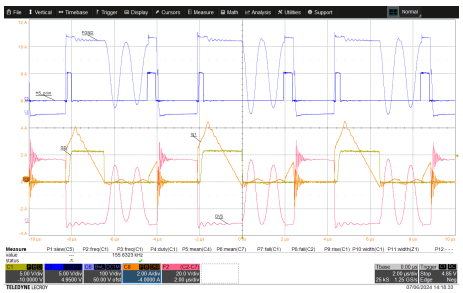


Figure 17. Key signals waveforms of EVLSRK1004 in HS mode on 65 W ACF @115 Vac V_{out}=20 V Iout=1.5 A

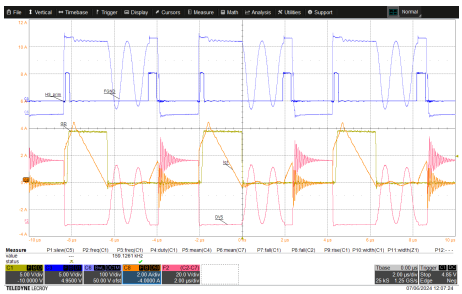
EVLSRK1004A



EVLSRK1004B



EVLSRK1004C



EVLSRK1004D

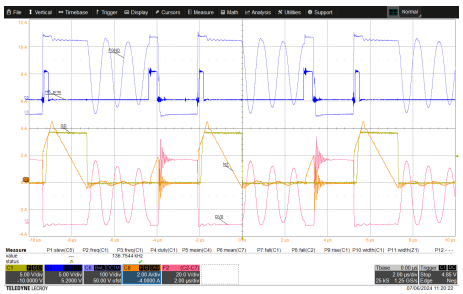


Figure 18. Key signals waveforms of EVLSRK1004 in HS mode on 65 W ACF @230 Vac V_{out}=20 V Iout=3.25 A

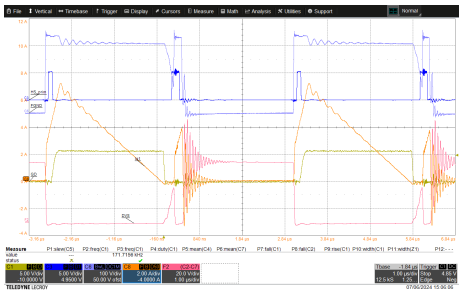
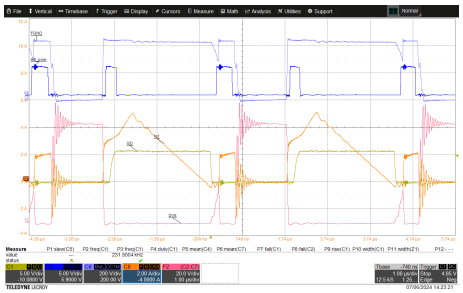
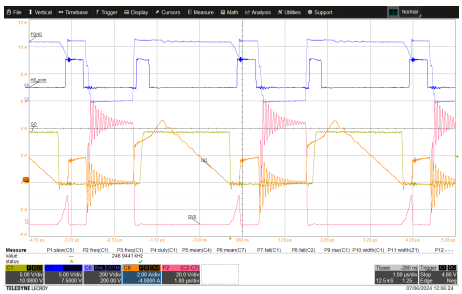
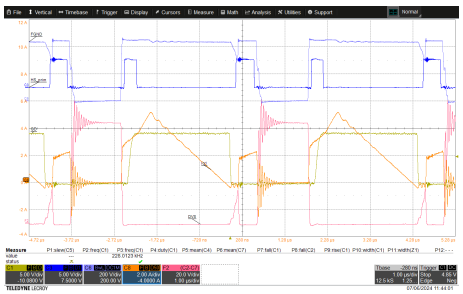
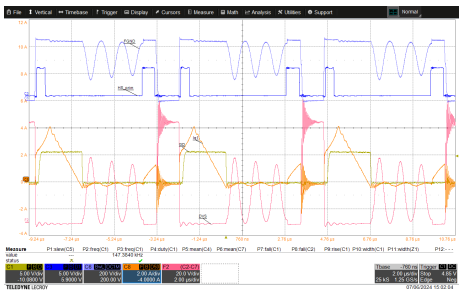
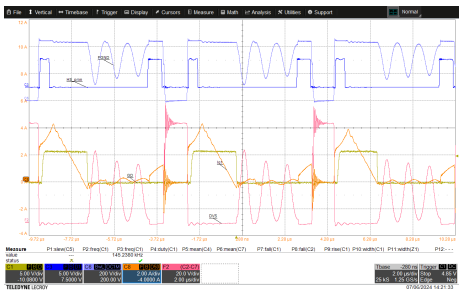
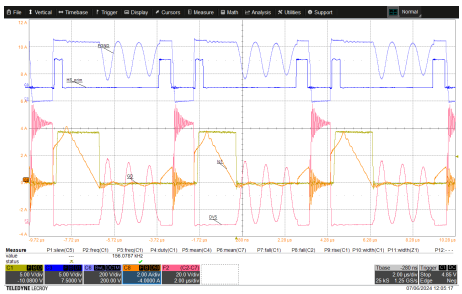
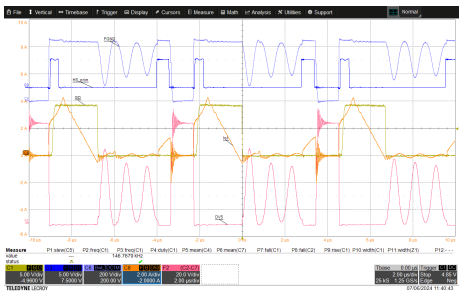
EVLSRK1004A	EVLSRK1004B
	
EVLSRK1004C	**EVLSRK1004D**
	

Figure 19. Key signals waveforms of EVLSRK1004 in HS mode on 65 W ACF @230 Vac V_{out}=20 V Iout=1.5 A

EVLSRK1004A	EVLSRK1004B
	
EVLSRK1004C	**EVLSRK1004D**
	

5 Thermal consideration

The thermal emissions of SRK1004 boards are shown in Figure 20 and Table 4.

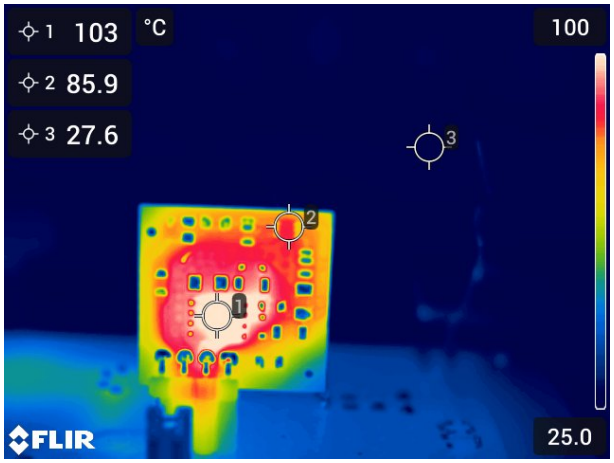
Some markers visible on the images have been placed across key components (SR MOSFET and SRK1004, respectively marked as M1 and M2).

The ambient temperature during both measurements was 27 °C.

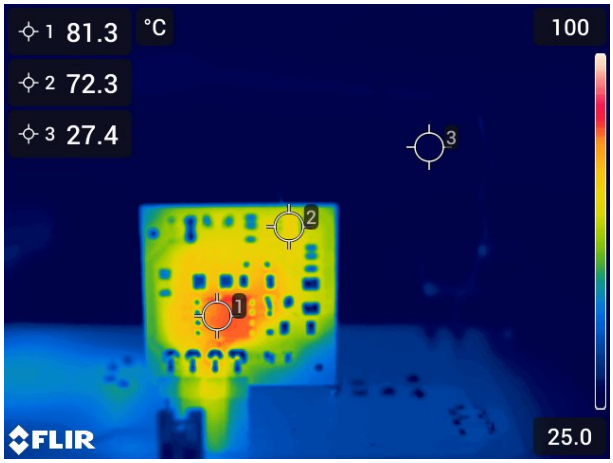
Figure 20 shows the thermal behavior at Vin=90 Vac Vout=20 V Iout=3.25 A, 20 minutes after board turn-on.

Figure 20. Thermal map of EVLSRK1004 @Vin=90 Vac V_{out}=20 V Iout=3.25 A

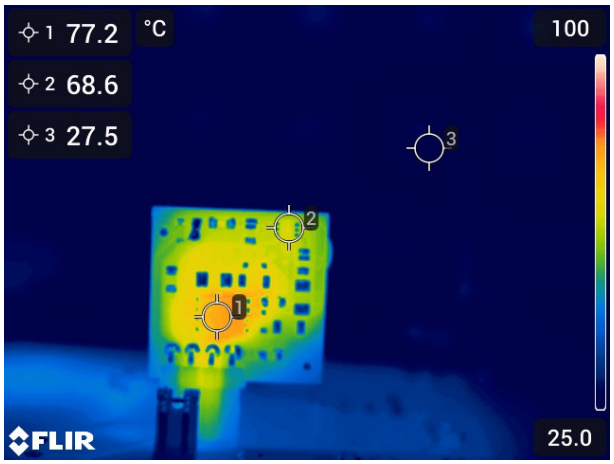
EVLSRK1004A



EVLSRK1004B



EVLSRK1004C



EVLSRK1004D

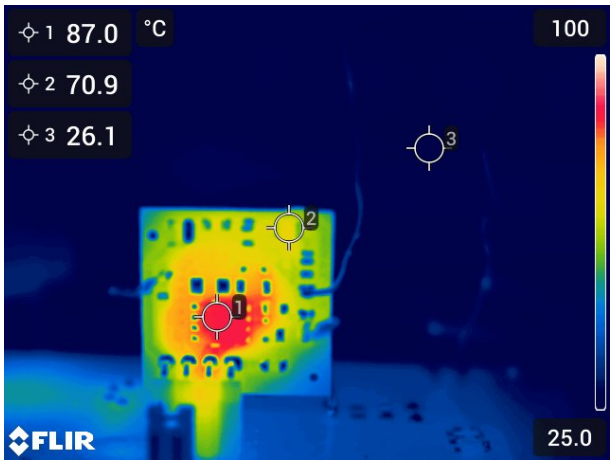


Table 4. Temp. [°C] measured on EVLSRK1004x

	EVLSRK1004A	EVLSRK1004B	EVLSRK1004C	EVLSRK1004D
MOSFET	103°	81.3°	77.2°	87.0°
SRK1004	85.9°	72.3°	68.6°	70.9°

If a current greater than 3.25 A is used in the application, it is recommended to use a fan or MOSFET heat sink.

6 Layout suggestions

The GND pin is the return of the bias current of the device and the return for gate-drive current. It should be routed in the shortest way possible.

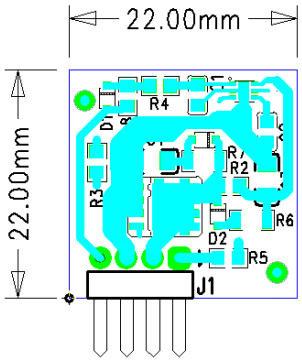
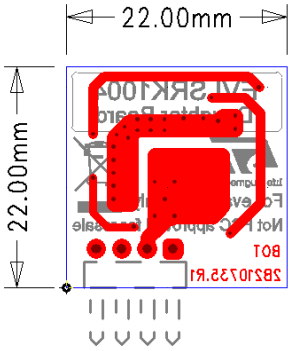
The usage of bypass capacitors between the VCC pin and GND pin is recommended.

They should be low-ESR, low-ESL type and located as close to the IC pins as possible.

The following recommendations should be considered when designing the PCB:

- Use a bypass capacitor across VCC and GND as close to the device pins as possible.
- Reduce the driving current path length and area as much as possible:
- – Minimize the area of circuit done by the GD pin, SR MOSFET, and DVS pin
  – Short trace from DRAIN of SR MOSFET to DVS pin
  – The DVS connection to the SR MOSFET drain terminal is critical (for stray inductances in the SR MOSFET current path). It is preferable to sense the MOSFET voltage as close as possible to its drain terminal.
- Exposed pad: connect to GND pin/net.
- Connect the device GND pin as close as possible to the SR MOSFET source terminal.

Table 5. Board layout

TOP	BOTTOM
	

7 References

1. SRK1004 datasheet: available at SRK1004

Revision history

Table 6. **Document revision history**

Date	Version	Changes
11-Dec-2024	1	Initial release.

Contents

List of tables

List of figures