Application note

Guidelines for the proper use of the L99DZ300G in the door zone control applications

Introduction

This document provides guidelines for the proper use of the L99DZ300G in the door zone control applications. It supports the user with the necessary steps to integrate the device into its application. It shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.

This document is targeted at automotive system engineers, hardware engineers, software engineers, quality managers and project managers involved in the development of electronic door control units for automotive applications.

1 Introduction to L99DZ300 device

The L99DZ300G is a door zone system IC providing electronic control modules with enhanced power management power supply functionality, including various standby modes, as well as LIN and CAN FD physical communication layers. The device has two low drop voltage regulators to supply the system microcontroller and external peripheral loads such as sensors and provides enhanced system standby functionality with programmable local and remote wake-up capability. Moreover, the 10 high-side drivers (9 to supply LEDs and 1 to supply bulbs) increase the system integration level; all the high-side drivers support the constant current mode for LED module with high input capacitance. Up to 5 DC motors and 4 external MOS transistors in H-bridge configuration can be driven in PWM mode up to 25 kHz. An additional gate drive can control an external MOSFET in high-side configuration to supply a resistive load connected to GND (for example mirror heater). An electrochromic mirror glass can be controlled using the integrated SPI-driven module with an external MOS transistor. All the outputs are SC protected and implement an open-load diagnosis. The ST standard SPI interface (4.0) allows control and diagnosis of the device and enables generic software development.

1.1 Application fields and target markets

L99DZ300G is designed for door zone application.

1.2 Purpose of this document

This document is composed of several components of chipset applicable experiences. It can speed up hardware design at the system level and serves as a guideline as well.

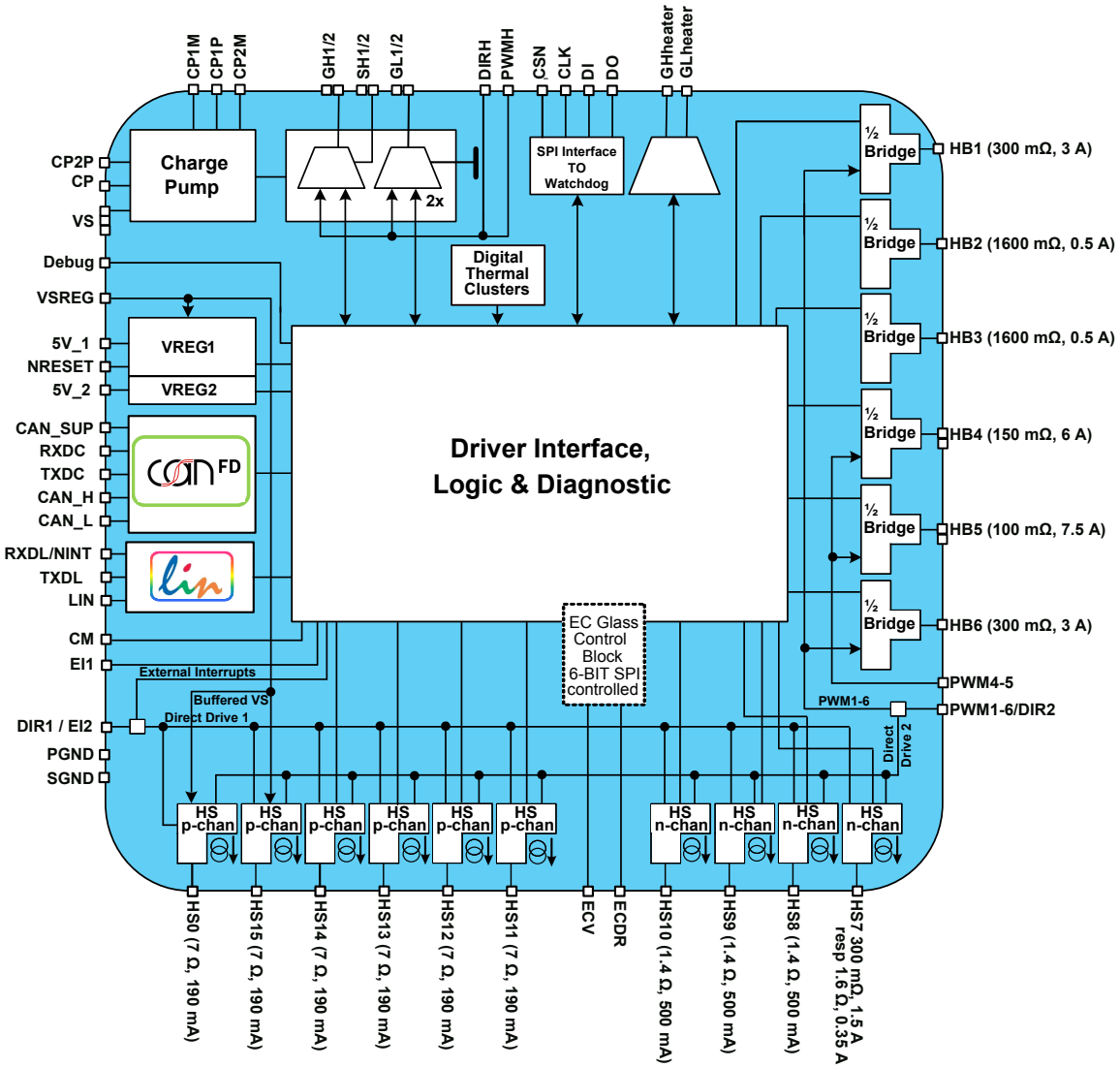
It provides the following contents from several aspects:

- Detailed descriptions of the chip's functions and technical specifications, including its input/output interfaces, clock frequency, and power consumption.
- Guidance on how to properly design and configure systems to use the chip.
- Include circuit diagrams, pin assignments, layout and wiring recommendations, etc.
- Ensure the correct connection and interaction of the chip with other components and peripherals.
- Offer practical application examples and case studies, showcasing the chip's usage in different fields.

If users encounter problems while using the chip, this document typically provides troubleshooting and failure handling guides. These guides list potential issues and their solutions, helping users to quickly solve technical challenges related.

This document also includes information about how to optimize performance, reduce power consumption, and best practice recommendations. It can help designers and engineers fully leverage the functions and performance of the chip.

2 Overview of L99DZ300G chip characteristics



2.1 Packaging and size information

LQFP-64 which size is 10x10x1.4mm with exposed pad down.

3 Operating modes

3.1 Main operating modes

Figure 1. Main operating modes

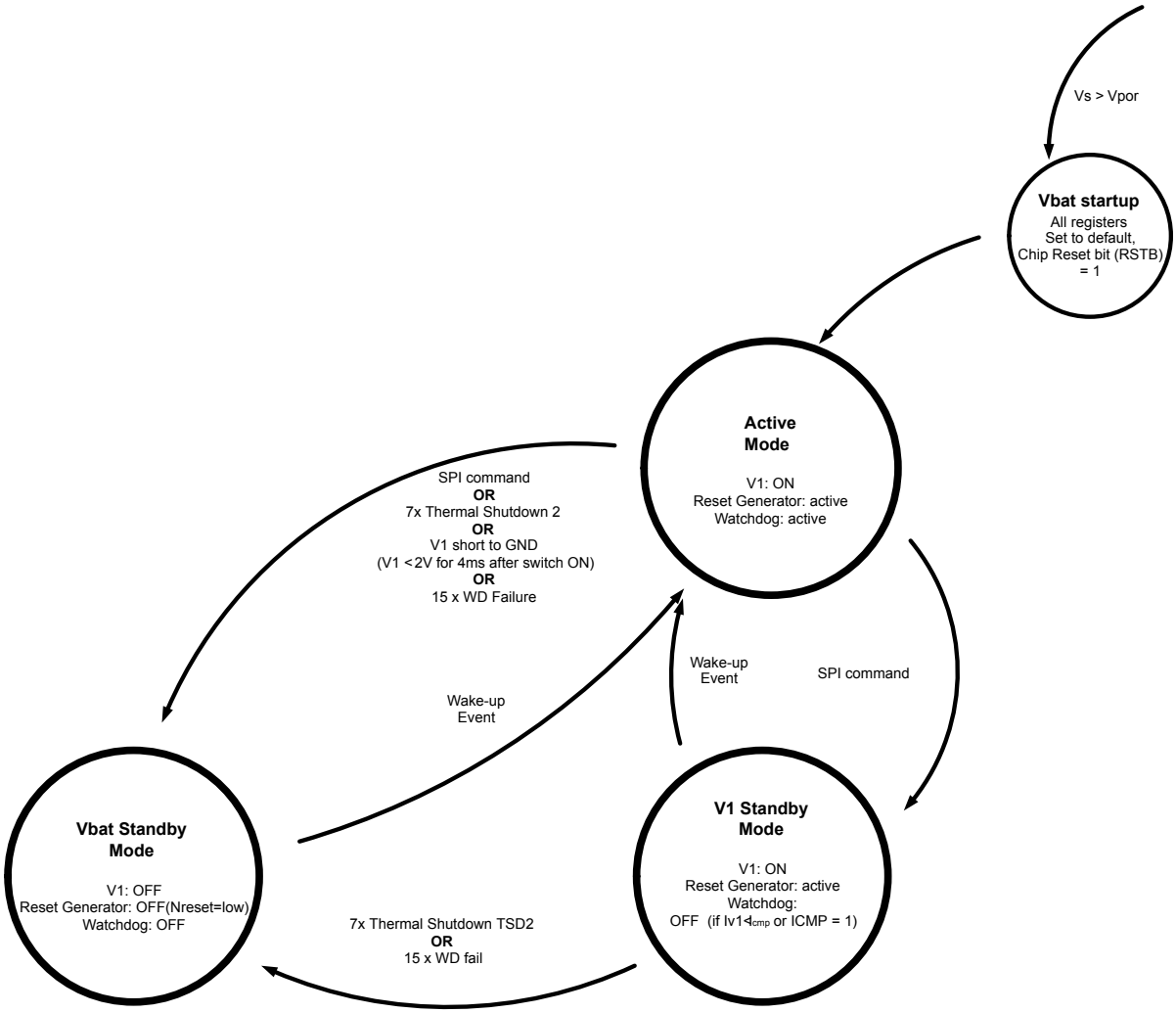


Table 1. Operating mode features

Active	Debug	V1_Standby	VBAT_Standby
all peripherals are ON	– all peripherals are ON – watchdog is OFF – CAN is enabled by default	– 5V1 is ON – CAN, LIN are OFF – Power outputs (except HS0 & HS15) are OFF – HS0 & HS15, 5V2 are switched ON or OFF according to SPI configuration. – Watchdog is OFF(1)	– 5V1, CAN, LIN are OFF – Power outputs (except HS0 & HS15) are OFF – HS0 & HS15, are switched ON or OFF according to SPI configuration. – Watchdog is OFF

1. *In case the V1 load current monitor is activated (bit I_{CMP}=0), watchdog restarts if V1 current is higher than I_{cmp} threshold.*

3.2 Debug mode

To allow software debugging, the L99DZ300 has a debug mode. In debug mode, the watchdog is deactivated, all other functions are able to work, and CAN is enabled by default.

To enter in debug mode, an external voltage shall be applied to the DEBUG pin:

$V_{debug} > V_{diH}$ (Max. V_{diH} = 9.4 V)

To exit from debug mode:

$V_{debug} < V_{diL}$ (Min. V_{diL} = 6.1 V)

After exit from debug mode ($V_{debug} < V_{diL}$), the watchdog starts with a long open window.

Note: making sure properly enter debug mode, it is recommended to connect the debug pin to V_{Sreg} pin or at any voltage source above 9.4 V.

3.3 V1_standby mode

The transition from active mode to V1_stanby is controlled by SPI, writing the bits STBY_SEL and GO_STBY (bit0 and bit1 of CR17 register) as per Table 2. STBY_SEL and GO_STBY bits.

To have the desired low consumption in standby the following conditions must be satisfied:

- $V_{LIN} > (VS - 1.5 V)$
- (CAN_H - CAN_L) < 0.4 V or (CAN_H - CAN_L) > 1.2 V
- $V_{WU} < 1 V$ or $V_{WU} > (VS - 1.5 V)$

After the V1 standby command (CSN low to high transition), the device enters V1_Standby mode immediately and, considering I_{CMP} bit value, there are two scenarios:

If I_{CMP} = 0 (default value), L99DZ300 watchdog starts a long open window and, if V1 load current drops below the I_{CMP_fal} (5 mA-18 mA), the watch dog is deactivated.

If I_{CMP} = 1, the watchdog is deactivated upon transition into V1_Standby mode without monitoring the V1 load current.

Note: The procedure to set the ICMP value is made by two consecutive SPI commands. In other words, writing ICMP (CR 2) = 1 is only possible if ICMP_CONFIG_EN (CR1) is set to 1 in the previous SPI message. The ICMP_CONFIG_EN bit is reset to 0 automatically with the next SPI command.

After entering V1 standby mode, 5V1 remains active to supply the microcontroller in a low-power mode. Power outputs (except HS15 & HS0), as well as the LIN and CAN transmitters are switched OFF.

HS15, HS0 and 5V2 remain in the configuration programmed before the standby command.

The interrupt signal (NINT) indicates a wake-up event from V1_Standby mode. The RXDL/NINT pin is pulled low for 56 µs, after a reaction time t_{Int_react} from the wake-up event.

Note: before going to V1_Standby or VBAT_Standby mode, OL_H1L2, OL_H2L1 and GH_OL_EN bits in CR12 must be set to 0 to achieve the specified current consumption. After woke up from VBAT_Standby or V1_Standby mode the CR17 Bit0 and Bit1 does not return to the default value (0b00).

3.4 VBAT_standby mode

The transition from active mode to VBAT_Stanby is controlled by SPI (2), writing the bits STBY_SEL and GO_STBY (bit0 and bit1 of CR17 register) as per table below.

In VBAT_Standby mode, the voltage regulators 5V1 and 5V2, the power outputs (except HS15 and HS0) as well as LIN and CAN transmitters are switched off.

HS15 and HS0 remain in the configuration programmed before the standby command to enable (cyclic) supply of external contacts.

An NReset pulse is generated upon wake-up from VBAT_Standby mode.

Table 2. STBY_SEL and GO_STBY bits

STBY_SEL	GO_STBY	
1	1	Go to V1_Standby
0	1	Go to VBAT_Standby

STBY_SEL	GO_STBY	
1	0	No transition to standby
0	0	No transition to standby (default)

4 Wake-up

A wake-up event turns the L99DZ300 from standby mode (V1_Standby or VBAT_Standby) back into active mode. To prevent the system from a deadlock condition (no wake-up from standby possible), it is not allowed to disable both CAN wake-up and LIN wake-up (bits LIN_WU_EN and CAN_WU_EN in CR18). In case the user tries to disable CAN and LIN wake-up at the same time (writing LIN_WU_EN = CAN_WU_EN = 1), the device rejects the command, all wake-up sources are configured to default values and the SPI error bit (SPIE) in the global status register is set.

In case of wake-up from VBAT_Standby the NRESET signal (with 2 ms timing) is generated, while for wake-up from V1_Standby the RXDL/NINT (interrupt) signal is generated.

The following table shows all wake-up sources with related description.

Table 3. Wake-up events functions

Wake-up source	Description
LIN bus activity	Can be disabled by SPI
CAN bus activity	Can be disabled by SPI
Level change of EI	Can be configured or disabled by SPI
I_{V1} > Icmp	The device remains in V1_Standby mode but watchdog is enabled (if I_{CMP} = 0). No interrupt is generated.
Timer interrupt / Wake-up of µC by TIMER	Programmable by SPI: - V1_Standby mode: The device wakes up and an interrupt signal is generated at RxDL/NINT when the programmable time-out has elapsed - VBAT_Standby mode: The device wakes up after a programmable timer expiration. 5V1 regulator is turned on and the NReset signal is generated when the programmable time-out has elapsed
SPI access	Always active (except in VBAT_Standby mode) Wake-up event: CSN falling on edge

4.1 LIN wake-up

The device wake-up from LIN occurs only if the LIN_WU_EN bit in CR18 is set.

Two types of signals (configurable by bit LIN_WU_CONFIG in the CR1 register) on the LIN bus are able to wake-up the device:

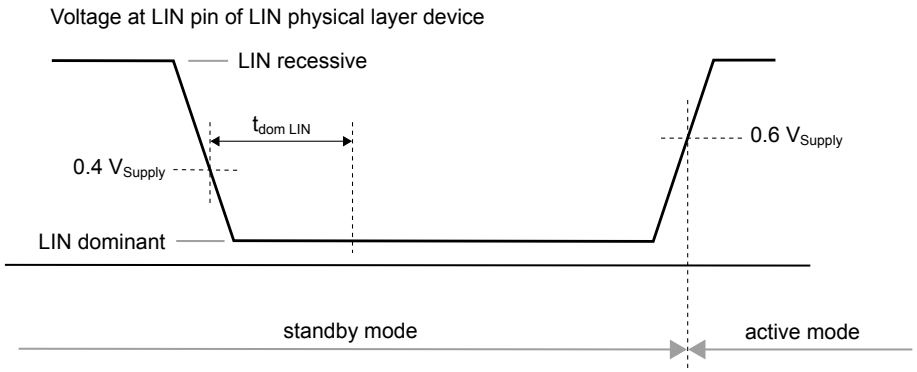
- If LIN_WU_CONFIG = 0 (default value) a Recessive-Dominant-Recessive pattern (according to LIN 2.2a) with dominant state duration higher than t_{dom_LIN} is requested to wake-up L99DZ300G (see the following figure).

A dominant time of at least 150 µs must be identified as a wake-up pattern according to LIN 2.2a, even if shorter dominant times may wake-up the device since tdom_LIN_min = 28 µs.

- If LIN_WU_CONFIG = 1 a state change recessive to dominant or dominant to recessive (according to LIN 2.1) is requested to wake-up L99DZ300G.

An unwanted wake-up can occur if, when the device is set in standby mode with LIN in recessive (dominant) state, there is a dominant (recessive) level at LIN for t_{LINBUS}.

Figure 2. Wake-up behavior according to LIN 2.2a



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Important: if LIN wake-up is not used (LIN_WU_EN bit in CR18 is not set), it is highly recommended to set LIN_WU_CONFIG=1 (bit21 in CR1). This avoids an extra current consumption in standby mode (both in V1_Standby mode and in VBAT_Standby mode) that occurs if LIN bus or LIN_TX pin are stuck to GND during transition from active mode to Standby mode.

4.2 CAN wake-up

The device wake-up from CAN occurs only if the CAN_WU_EN bit in CR18 is set.

The device can be woken up by a pattern on the CAN bus that satisfies the following requirements:

- The CAN interface wake-up receiver must receive a series of two consecutive valid dominant pulses (each one longer than t_{filter}) separated by a recessive one (longer than t_{filter}).
- The two pulses must occur within a time frame not longer than t_{wake}.
- Wake-up occurs when the duration of the second pulse becomes longer than t_{filter}.

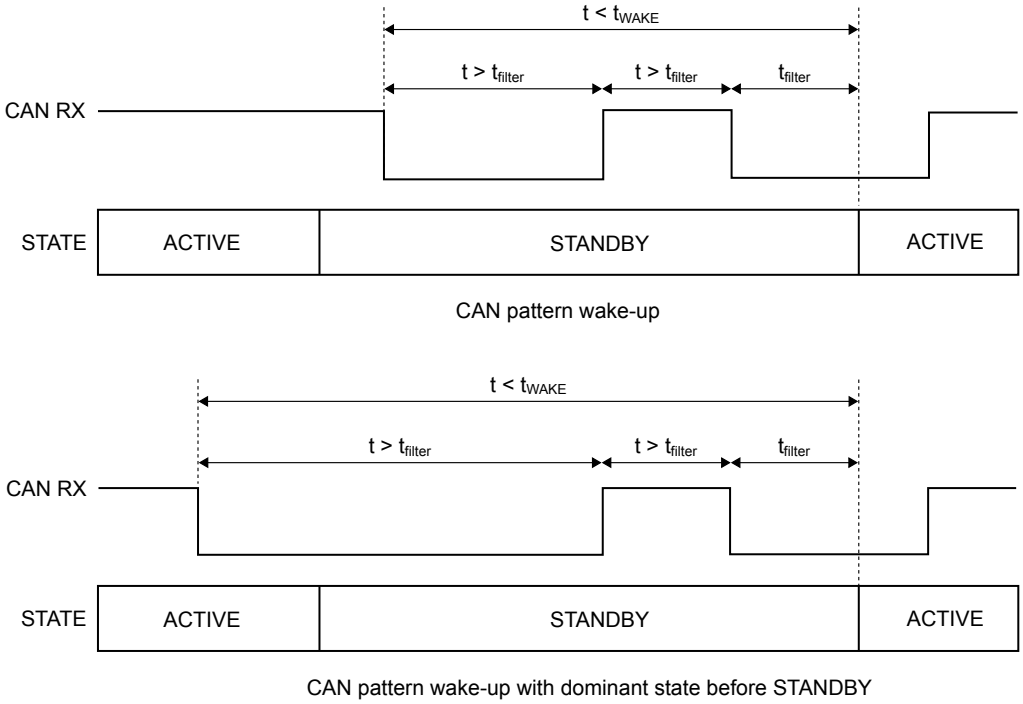
Note: Keep in mind that the t_{filter} range specified in the datasheet (0.5~1.8 µs) is not a safety range. To make sure wake-up the device, the pulses should be longer than 1.8 µs.

Note: Keep in mind that t_{wake} range specified in datasheet (from 0.8 to 5 ms) is not a safety range. To make sure wake-up the device, the pulses should be shorter than 0.8 ms.

When the device enters in standby, independently on CAN bus status (recessive or dominant), the t_{wake} starts from BUS transition recessive to dominant (see the following figure).

In CAN TRX STBY mode, the CAN transmitter is disabled and the RXDC pin is kept at a high (recessive) level. CAN receiver can detect a wake-up pattern (WUP).

Figure 3. CAN wake-up capabilities



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4.3 WU input EI1 and EI2

The EI1 and EI2 inputs can be configured as wake-up sources, which are sensitive to any level transition (positive and negative edge).

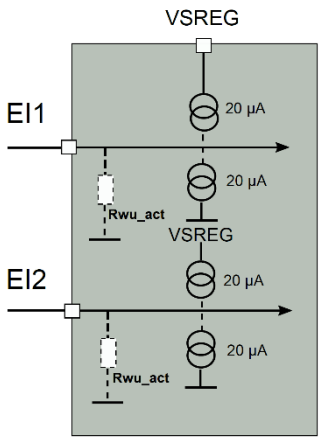
Wake-up mode can be configured for static or cyclic monitoring of the EI1 and EI2 input voltage level (EIx_FILT_0 and EIx_FILT_1 in CR18).

To minimize current consumption in Standby Mode, follow these recommendations:

- Set the current source configuration (EIx_PU=1 in CR18) for active low contacts.
- Set the current sink configuration (EIx_PU=0 in CR18) for active high contacts.
- Keep V_{Eix} < 1V or V_{Eix} > VSreg -1.5V.

If EIx pin is unused, it is recommended to connect it to ground and to disable bits EI1_EN and EI2_EN in CR18. For EI2 it doesn't apply if the pin is configured as DIR1.

Figure 4. Internal scheme of EIx inputs



4.3.1 Static wake-up monitoring

In case of static monitoring, a filter time of t_{wu_stat} (64 µs) is implemented. The filter is started when the input voltage passes the specified threshold V_{wu_th} (typically 0.45 V_{Sreg} for negative edge and 0.55 V_{Sreg} for positive edge) as shown in Figure 5. Wake-up request for active high contact and Figure 6. Wake-up request for active low contact.

Wake-up status bit (EIx_STATE bit in SR4) is set only if the threshold is passed for more than t_{wu_stat}.

To reduce current consumption in standby mode, R_{WU_act} is activated just after the external interrupt request (as soon as V_{Eix} > 1 V or V_{Eix} < VSreg -1.5 V), so it is highly recommended to dimension external resistors to make sure that V_{EIx} < 1 V or V_{EIx} > VS - 1.5 V, when the contact is open, otherwise, the quiescent current will be higher than the specified value on datasheet (Iwu_stdby).

Figure 5. Wake-up request for active high contact

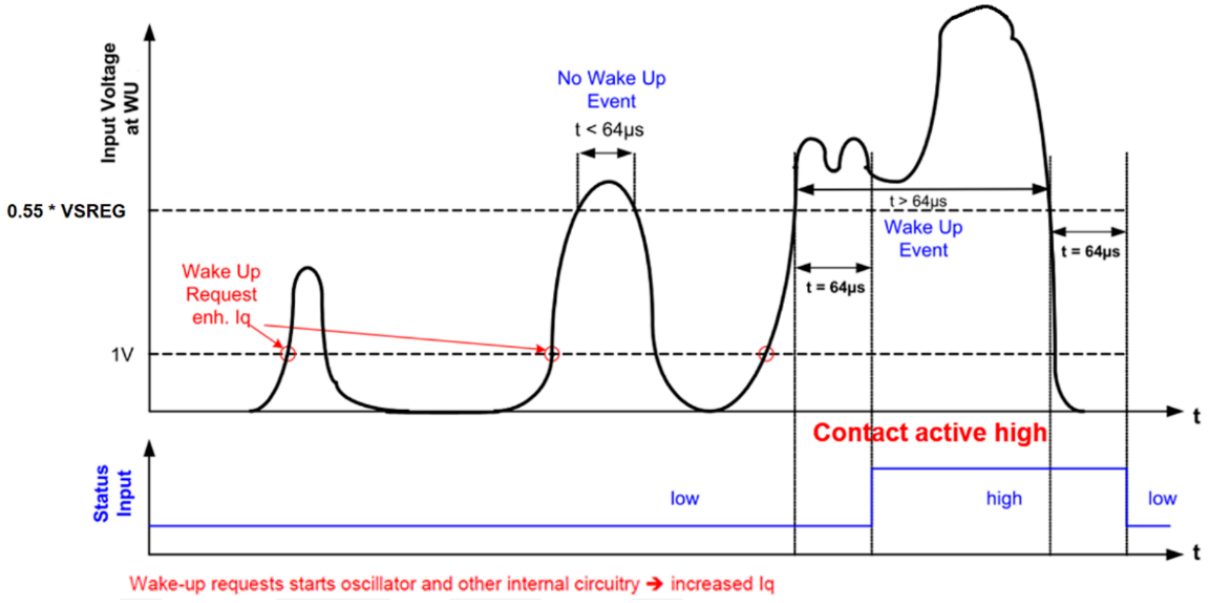
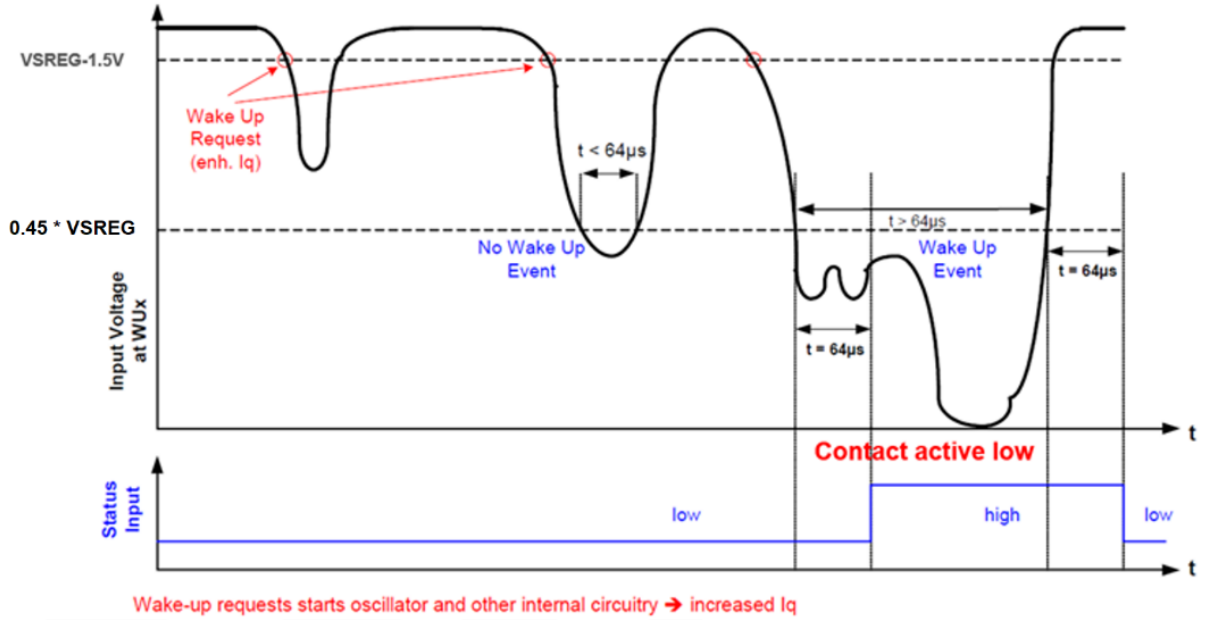


Figure 6. Wake-up request for active low contact



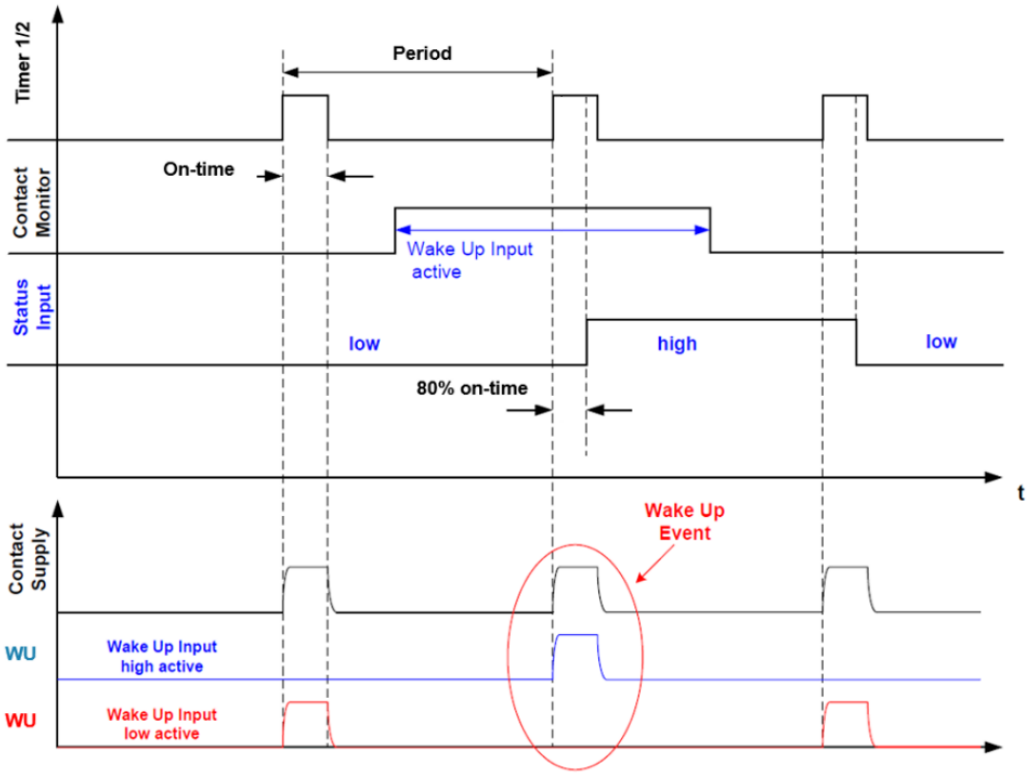
4.3.2 Cyclic wake-up monitoring

Cyclic contact monitoring, conceived to reduce the quiescent current of the device, allows periodical activation of the wake-up input to read the status of the external contact. The periodical activation is driven by timer 1 or timer 2 whose settings (on-time and period) can be configured through bits Tx_PER_y and Tx_ON_y on CR2.

Moreover, in case of cyclic sensing, the internal pull-down resistor (R_{WU_act}) is periodically activated on each rising edge of the TIMER_ON.

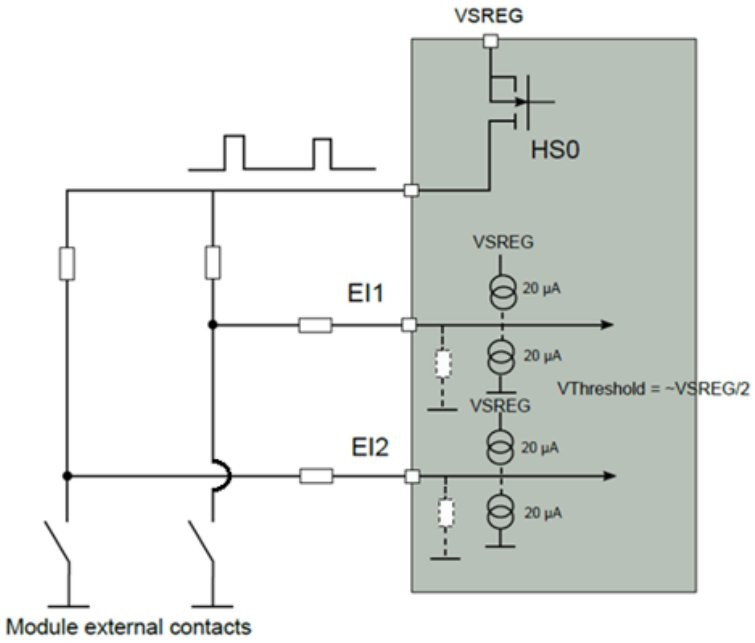
The input signal is filtered with a filter time of t_{WU_CYC} after a delay (80% of the configured timer on-time) as showed in the following figure. A wake-up is processed if the status has changed versus the previous cycle, therefore wake-up status bit (EIx_STATE bit in SR4) is set only if status of two consecutive ON-time pulses is different.

Figure 7. Cyclic wake-up monitoring



The output HS0 or HS15, configured to be driven with timer1 or timer2 (bits HSx_y in CR14-CR15) according to the same timer setting (timer1 or timer2) used for cyclic monitoring of the wake-up input, can be used to supply the external contacts (see next figure).

Figure 8. External contacts supplied periodically by the internal timer through HS0



The following is a practical example of external resistor dimensioning in the case of HS0 being used to supply the external contact (active low).

The external resistors R1 and R2 should be dimensioned according to the following recommendation:

1. if contact is closed: $\frac{Vsreg,max}{R1} < I_{OC0\_min}$
2. if contact is open: $Vsreg,max\frac{R_{wu\_act\_min}}{R1+R2+R_{wu\_act\_min}} > Vsreg,max - 1.5$

Condition 1) has to be satisfied to avoid HS0 over current protection intervention when contact is closed; while condition 2) guarantees the minimum current consumption in Standby Mode when contact is open.

Resolving 1) and 2):

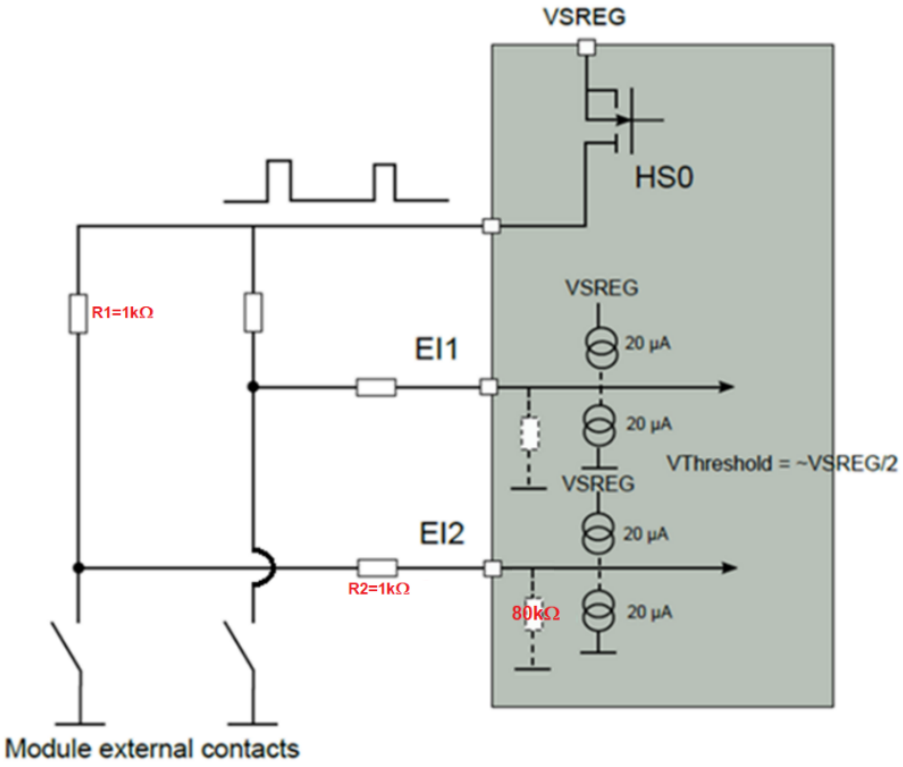
1. $R1 > \frac{Vsreg,max}{I_{oc0\_min}}$
2. $R1 + \mathrm{R2} < \frac{3R_{wu\_act\_min}}{2Vsreg,max - 3}$

Considering the value on datasheet (I_{OC0_min} = 190 mA, $R_{wu\_act\_min}$ = 80k Ω) and supposing Vsreg,max = 18 V:

1. $R1 > 18V/0.19A \approx 100\Omega$
2. $R1 + \mathrm{R2} < \frac{3*80k}{2*18-3} \approx 7.2k\Omega$

A possible combination that satisfies the two previous requirements could be R1 = R2 = 1 kΩ (see next figure).

Figure 9. **Example of R1 and R2 dimensioning**



5 Watchdog

5.1 Startup or wake-up from VBAT/V1 standby

After power-ON or after wake-up from V1/VBAT standby mode, the watchdog starts with a timeout (long open window, t_{LWMin}.=246 ms). This timeout allows the microcontroller to run its own setup before starting the window watchdog by setting the trigger bit (TRIG in CR1 or CR18).

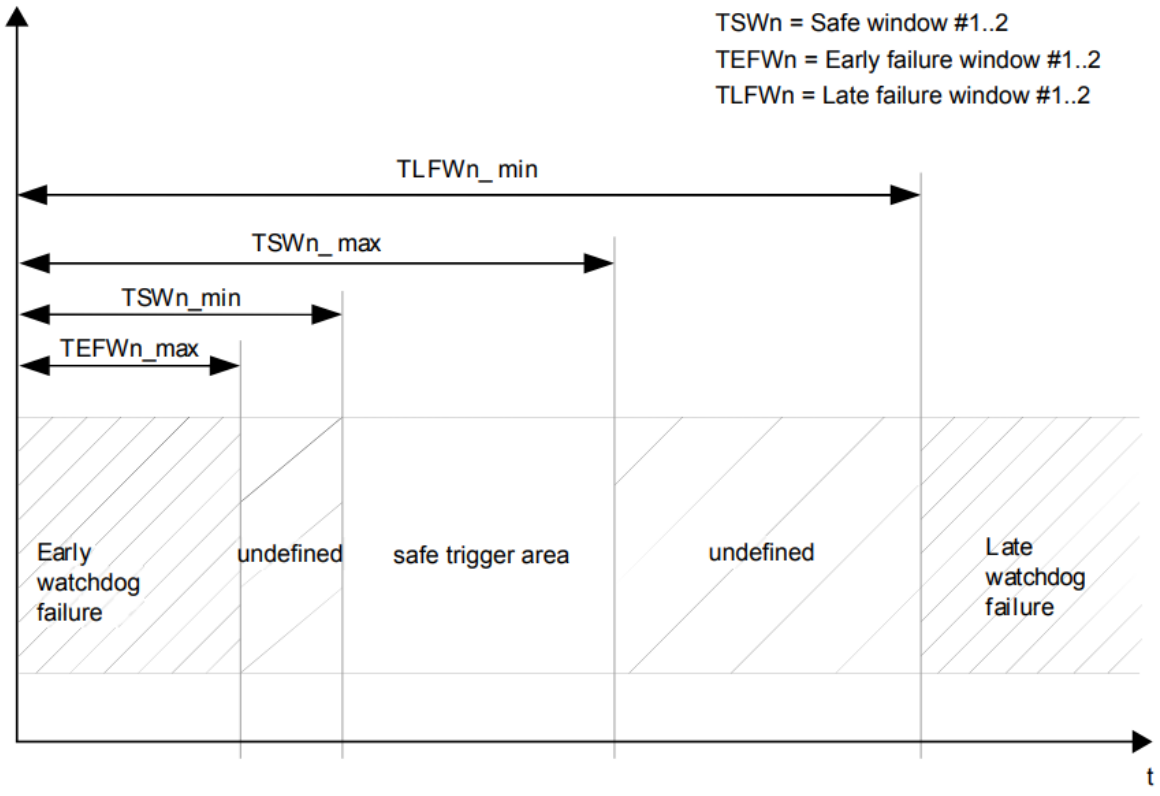
The Long open window starts also in the following cases:

- After entering V1_Standby mode (if I_{V1} > Icmp & WD enable)
- Exit from debug mode.

5.2 Watchdog normal operation

After the Long open window (t_{LW}) MCU must serve the watchdog by alternating the watchdog trigger bit (TRIG in CR1 or CR18) within a time inside the safe trigger area defined by T_{SWx_max} - T_{SWx_min} (configurable, default 7.5-12 ms), as showed in the following figure.

Figure 10. Watchdog safe trigger area



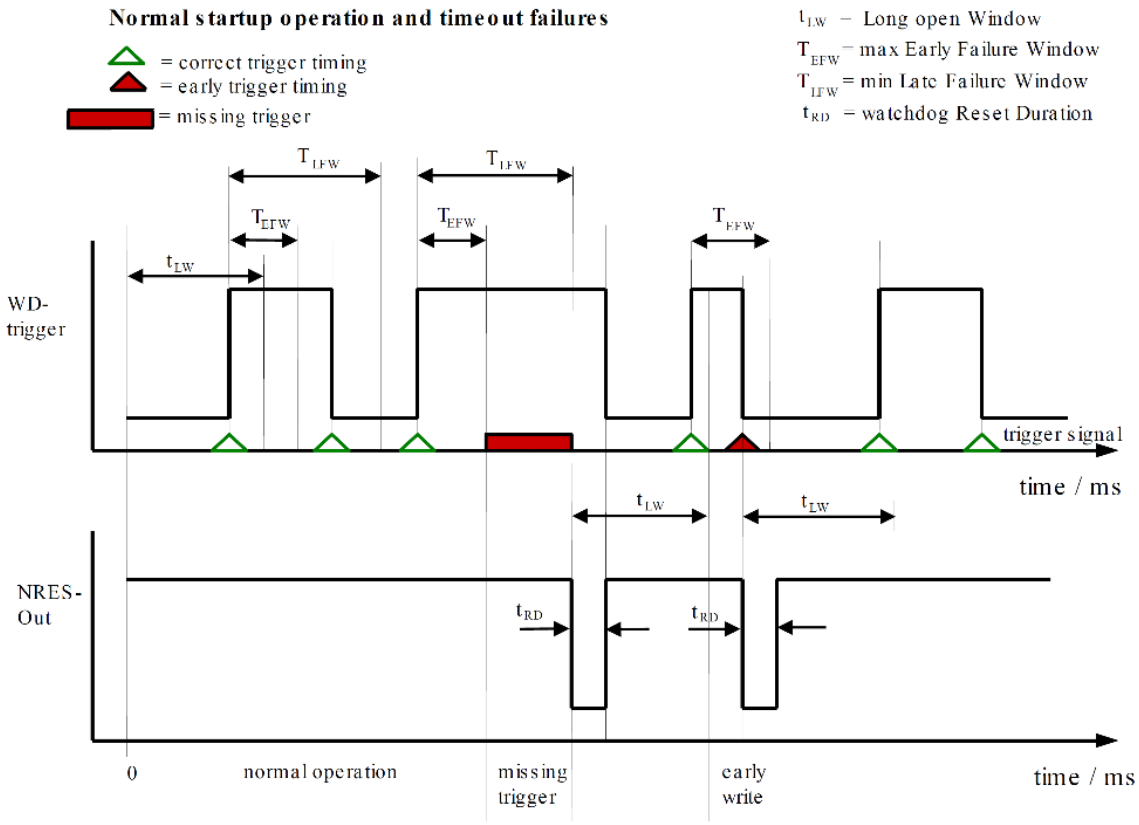
The recommended way to serve the watchdog is the following one:

- Step 1: read the status of TRIG bit in CR1 (or CR18 if CR18 is used as the watchdog trigger register).
- Step 2: serve the watchdog with the inverted trigger bit read back from the previous step.
- Step 3: repeat the previous steps in a time inside the safe trigger area (T_{SWX_min} < t < T_{SWX_max}).

Note: The WD trigger bit in CR1 and CR18 are internally synchronized.

In case the trigger bit is not updated inside the safe trigger area (shorter or longer time) a NRESET pulse is generated and the watchdog restarts with a long open window (t_{LW}).

Figure 11. **Watchdog timing**



Window watchdog trigger time can be configured with two values: T_{SW1} (7,5-12 ms, default after power ON) and T_{SW2} (37.5-60 ms) as are shown in the following table.

The SPI command needed to change watchdog timing is protected; two consecutive SPI write commands are requested as described below:

1. Set to 1 the bit WD_CONFIG_EN in CR1, first.
2. Set the WD_TIME bit in CR17 to the desired value.

As showed in the figure below, the new timing (T_{SW2}) gets active the next cycle, while the old timing configuration (T_{SW1}) has to be maintained till the end of the current TRIG refresh cycle.

Figure 12. **Watchdog at startup with default timing (10 ms)**

Table 4. **Watchdog parameters**

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit	Item
t_{LW}	Long open window	Tested by scan	246	300	375	ms	A.027
T_{EFW1}	Early failure window 1	Tested by scan			4.5	ms	A.028
T_{LFW1}	Late failure window 1	Tested by scan	20			ms	A.029
T_{SW1}	Safe window 1	Tested by scan	7.5		12	ms	A.030
T_{EFW2}	Early failure window 2	Tested by scan			22.3	ms	A.031
T_{LFW2}	Late failure window 2	Tested by scan	100			ms	A.032
T_{SW2}	Safe window 2	Tested by scan	37.5		60	ms	A.033

The next two figures show how the MCU must serve the watchdog at device startup.

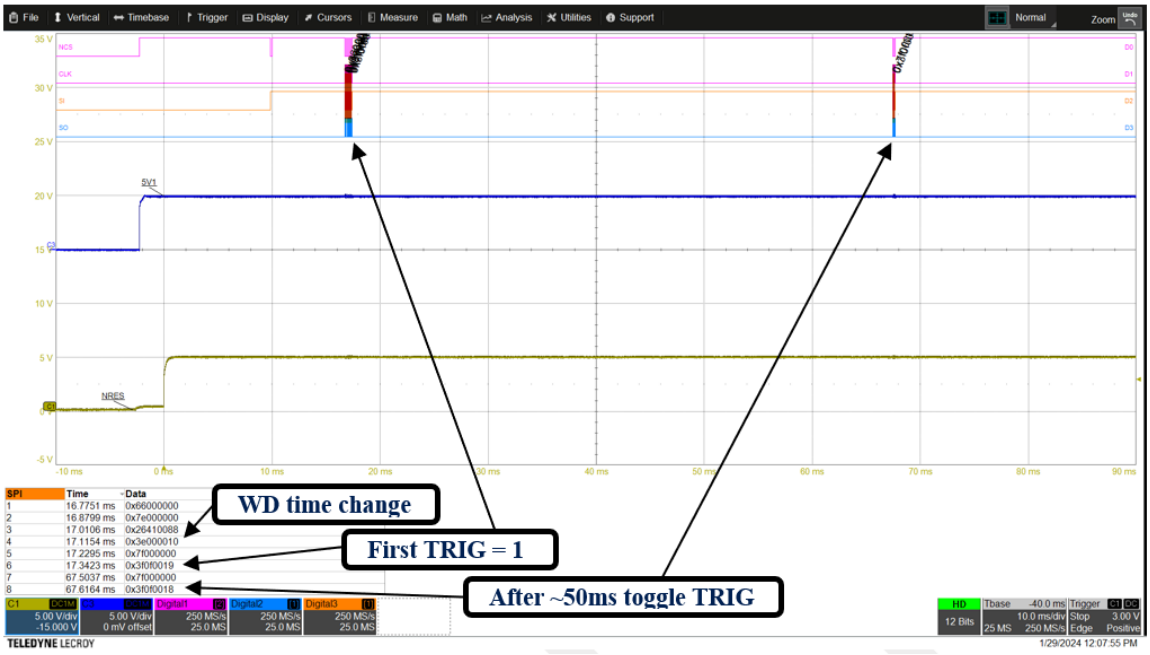
The next figure shows the default configuration (T_{SW1}).

At device startup the NRES is released, and the watchdog starts a Long open window (t_{LW}); before t_{LW} expiration the MCU must write the TRIG bit to 1. After about 10 ms (value inside the safe window 1) there is another write operation on CR18, and the TRIG bit is written to 0. And so on.

Figure 13. **Watchdog at startup with default timing configuration (10 ms)**

The next figure shows the possibility to set timing T_{SW2} at device startup. In this case, before starting TRIG bit writing, the two commands to change watchdog timing are sent, as described before. In this case, the new timing (T_{SW2}) is applied immediately. Then the MCU writes the TRIG bit to 1 (before t_{LW} expiration) and, after about 50 ms (value inside the safe window 2), the TRIG bit is written to 0. And so on.

Figure 14. **Watchdog at startup with 50 ms timing**



5.3 WD in VBAT standby mode / debug mode

In VBAT standby mode and in debug mode, the watchdog is disabled.

5.4 WD in V1 standby mode

In V1 standby mode, depending on the ICMP bit (CR2) value, there are two possible scenarios:

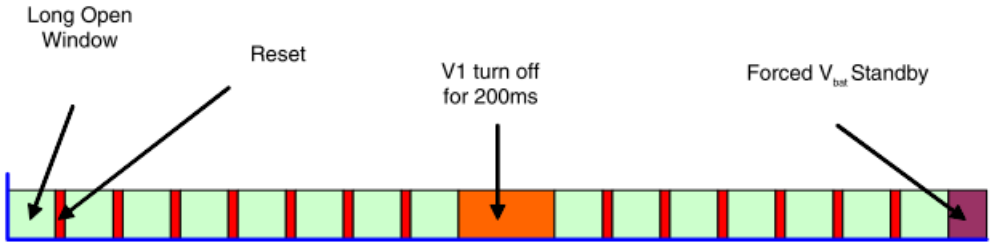
- Watchdog is disabled as soon as I_{V1} < Icmp. (ICMP = 0, I_{V1} current supervisor enabled).
- Watchdog is disabled upon transition into V1_standby mode. (ICMP = 1, I_{V1} current supervisor disabled).

5.5 WD failure

In case of a watchdog failure, the status bit WDFAIL in SR1 is set to 1, a reset pulse (typical duration t_{RD}=2 ms) is generated at NReset pin, and L99DZ300G enters in fail-safe mode starting a WD long open window (t_{LW}).

As showed in the following figure, if after the first WD failure there are 7 additional watchdog failures in sequence, the regulator 5V1 is turned-off for t_{V1OFF} (typ. 200 ms). Then, after 7 additional consecutive watchdog failures, the 5V1 regulator is turned off permanently, the device goes into forced VBAT_standby mode, and the status bit FORCED_SLEEP_WD in SR8 is set.

Figure 15. Consecutive watchdog failures



From forced VBAT_standby mode a wake-up is possible by any activated wake-up source.

After waking up, if the watchdog trigger is still not serviced in a watchdog long open window, the device enters forced VBAT standby mode again at the first WD failure, since the internal failure counter has been NOT cleared, keeping the maximum number of 15 failures. This sequence is repeated until a valid watchdog trigger event is performed by writing TRIG = 1.

A practical example of forced VBAT_standby mode entry due to WD failure is shown in the following figure. Before the WD failure, L99DZ300G was in ACTIVE mode with 5V2 regulator enabled, then the uC stops to serve the watchdog. At the first WD failure device enters in fail-safe mode and the 5V2 regulator is disabled. After the next consecutive 7 WD failures, 5V1 regulator is disabled for about 200 ms. Then, after the additional 7 WD failures, 5V1 regulator is permanently disabled.

Figure 16. **Oscilloscope consecutive watchdog failures**

6 Fail-safe

The Fail-Safe (FS) circuitry is a completely independent mechanism that allows the device to react to critical conditions by immediately switching OFF all outputs.

Specifically, in Fail-Safe mode, the device behaves as follows:

- All outputs are turned off.
- All control registers are set to default values.
- LIN transmitter remains on.
- FS Bit0 (global status byte) and corresponding failure bits in status registers are set.
- Write operations to control registers are blocked. Only the following bits are not WRITE protected:
- CR18 (0x3F):
  - TRIG
  - CAN_ACT
- CR17 (0x3E):
  - Timer settings (bits 8…23)
- CR14 (0x3B):
  - HS15_x (bits 8…11)
  - HS0_x (bits 12…15)
- CR5 (0x32) to CR10 (0x37)
  - PWM frequency and duty cycles
- CR1 (0x26)
  - V2_0, V2_1
  - Trig

There could be different sources of failure:

- Watchdog failure due to a microcontroller failure
- 5V1 regulator failure due to an overload or a short to GND
- Temperature failure (TSD2)
- SGND pin not connected to GND

Failures can be categorized in two types:

- Temporary failures: failure that can automatically recover after a while
- Non-recoverable failures: failure that remains stable till external failure removal action

In case of temporary failures the device enters immediately in FS mode and then it can recover with the actions reported in the following table.

Depending on the different root cause of entering the Fail-Safe, the action to exit fail-safe mode is different as shown in the following table.

In case of non-recoverable failures, L99DZ300G, after different retry tentative, enters in forced VBAT standby and all control registers are set to the default value. After the device wake-up, as soon as the fault has been removed, the cause of the forced VBAT standby mode is indicated in the SPI status registers. In Table 6. Non recoverable failures conditions all possible non-recoverable failures with relevant diagnosis flags are reported.

Table 5. Temporary failures conditions

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
Microcontroller (oscillator)	Watchdog Early write failure or expired window	FS (global status byte) = 1 WDFAIL (SR8) = 1 WDFAIL_CNT_x (SR8) = n+1	TRIG = 1 during long open window Read&Clear SR8
V1	Short at turn on	FS (global status byte) = 1 V1FAIL = 1 FORCED SLEEP TSD2/V1SC (SR8) = 1	Wake-up Read&Clear SR8
	Undervoltage	FS (global status byte) = 1	V1 > V_{rth}

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
V1		V1UV = 1(1) V1FAIL (SR7) = 1(2)	Read&Clear SR8
Temperature	T_J > TSD2	FS (global status byte) =1 TW (SR7) = 1 TSD1 (SR8) = 1 TSD2 (SR8) = 1	T_J < TSD2 Read&Clear SR8

1. *Bit SR8/V1UV is set for t > t_{uv1} (16 µs). Fail-safe bit GSR/FS is set only after t_{RD} (NRESET low pulse).*
2. *If V1 < V1fail (for t > t_{v1fail}). The fail-safe bit is located in the global status register.*

Table 6. Non recoverable failures conditions

Failure source	Failure condition	Diagnosis	Exit from fail-safe mode
Microcontroller (oscillator)	15 consecutive watchdog failures	FS (global status byte) =1 WDFAIL (SR8) = 1 FORCED_SLEEP_WD (SR8) = 1	Wake-up TRIG = 1 during long open window Read&Clear SR8
V1	Short at turn on	FS (global status byte) = 1 V1FAIL = 1 FORCED_SLEEP_TSD2_V1SC (SR8) = 1	Wake-up Read&Clear SR8
Temperature	7 times TSD2	FS (global status byte) =1 TW (SR7) = 1 TSD1 (SR8) = 1 TSD2 (SR8) = 1 FORCED_SLEEP_TSD2_V1SC (SR8) = 1	Wake-up Read&Clear SR8
SGND	Loss of ground at SGND pin	FS (global status byte) = 1 SGNDLOSS (SR3) = 1	Wake-up Read&Clear SR3

7 Reset output – NReset

The NReset pin is a device output pin that should be connected to the MCU reset input pin.

At the 5V1 regulator turns ON (V_{SReg} power on or wake-up from VBAT_Standby mode), NReset is kept low for t_{RD} (2 ms typical) to keep the microcontroller in reset until 5V1 supply voltage is stable. After the NReset is released, the watchdog starts with a Long open window (t_{LW}) to allow the microcontroller to run its own setup before starting the window watchdog.

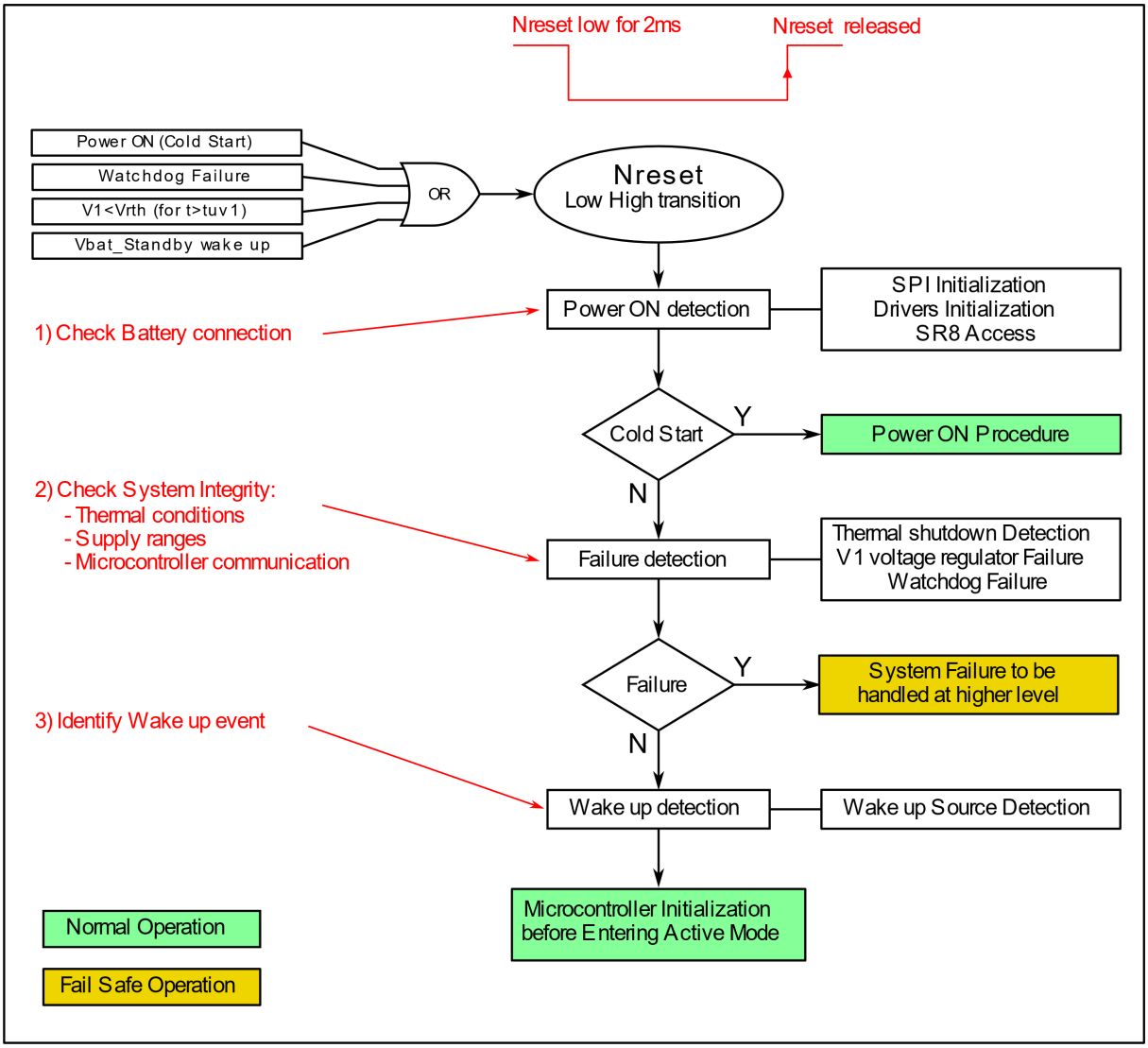
Apart of behavior at device startup, a reset pulse (2 ms typical) on NReset pin is also generated in case of:

- V1 drops below V_{rth} (configurable by SPI) for t > t_{UV1}
- Watchdog failure
- Wake-up from VBAT_Standby mode

Note: The V1 reset threshold can be configured (using bits V1_RESET_x in CR17) with four values: 4.3 V (default value at power ON), 4 V, 3.8 V and 3.5 V.

The flowchart shown in the following figure is a reduced overview of the NReset handling to treat the possible events.

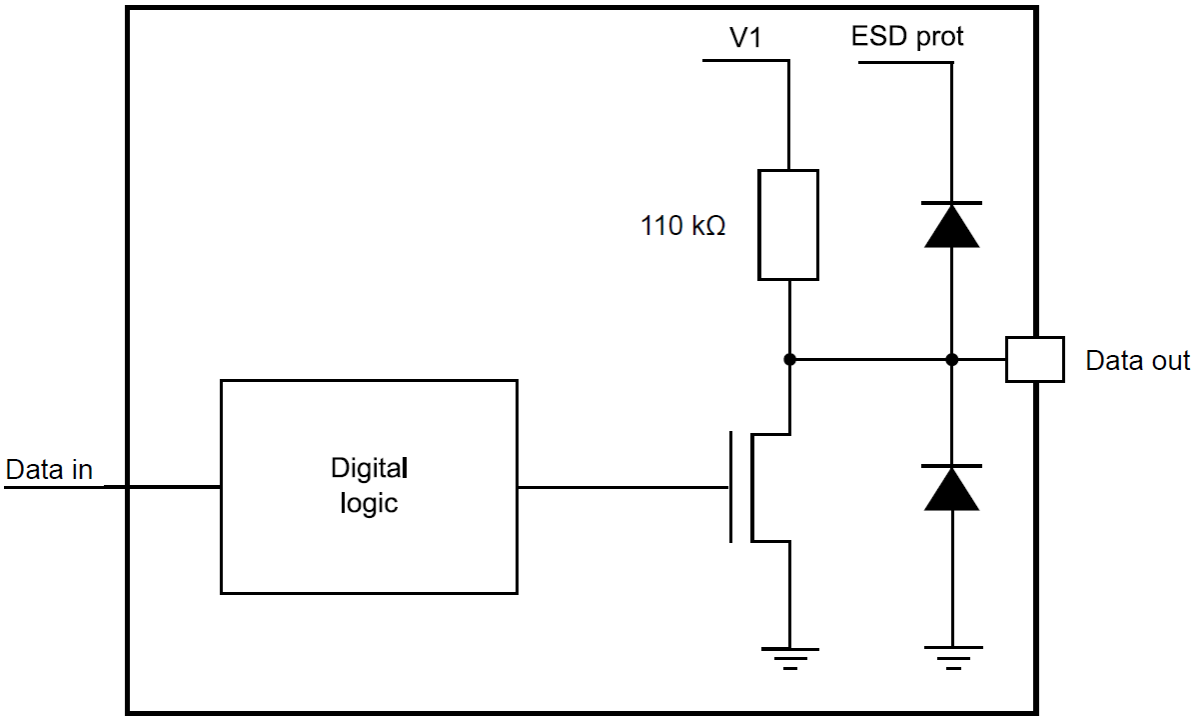
Figure 17. NReset generation and handling overview



As soon as the NRESET is released, the watchdog timing starts with a long open window.

Although there is a 5V1 weak internal pull up (see next figure), an external pull up to 5V1 is recommended.

Figure 18. NReset pin simplified internal structure



Since the NRESET output is realized with an open-drain output, it is also possible to connect other external open-drain structures in parallel to control the MCU reset pin. In other words, the MCU can be reset by a different device, even if this can eventually trigger a watchdog failure error on the L99DZ300G since the MCU is no longer able to serve the watchdog as soon as it has been reset.

8 Interrupt (NINT)

The interrupt pin (RxDL/NINT) is a device output pin that should be connected to the MCU pin which multiplex interrupt and LIN Rx.

The interrupt signal indicates to the MCU a wake-up event from V1_Standby mode.

This is the only case in which the pin is configured as NINT, otherwise it works as RxDL.

In case of a wake-up event from V1_Standby mode by any of wake-up inputs, the NINT pin is pulled low for 56 µs, after a reaction time t_{Int_react} (40 µs) from the related wake-up event.

The interrupt signal is generated in all wake-up events from V1_Standby, apart the case of Iv1 > Icmp during V1_Standby mode. In this specific case the device remains in standby mode while the watchdog starts with a long open window and no interrupt signal is generated.

9 Outputs

9.1 HS output

All HS output can be configured to be driven by:

- An internal DC input (ON/OFF activation)
- 10 internally generated PWM signal (PWM1 to PWM10)
- 2 internal timer (timer1 or timer2)
- 2 external pin (DIR1 or DIR2) which can be connected to an MCU output pin

The configuration can be chosen using the 4-bits HSx_y (x: channel number; y: 0~3) in CR14 and CR15, as shown in the following figure.

Figure 19. Power output settings (HS0 as example)

HS0_3	High-side driver HS0 configuration
HS0_2	**HS0 config**
HS0_1	0000: OFF (default)
HS0_0	0001: ON 0010: Timer 1 0011: Timer 2 0100: PWM1 0101: PWM2 0110: PWM3 0111: PWM4 1000: PWM5 1001: PWM6 1010: PWM7 1011: PWM8 1100: PWM9 1101: PWM10 1110: DIR1 1111: DIR2

The available HS outputs are:

- HS7 to HS14 (supplied by VS)
- HS0 and HS15 (supplied by VSREG)

All high-side outputs are protected and are switched OFF in case of:

- VS/VSREG overvoltage and undervoltage (depending on SPI configuration, see datasheet “Power supply fail” section for details).
- Overcurrent in case $I_{OUT} > I_{OCX}$ (with OCR mode only for HSDs having this feature).
- Over temperature in case Tj > TSD1 (behavior depends on TSD_CLUSTER_EN bit value).
- Fail-safe event.
- Loss of GND at SGND pin.

9.2 Half bridge output

All high side and low side of half bridge outputs can be configured ON or OFF (bits HBx_HS/HBx_LS in CR16).

The overcurrent threshold of HB1, HB5, HB6 is also configurable (bits HBxOCTH_y in CR16).

Furthermore, LS of HB1&HB6 and HB4&HB5 support PWM mode (configurable through bits PWM1-6_x and PWM4-5_x in CR2) and follow the signal at device input pins PWM4-5 and PWM1-6/DIR2.

9.3 Overcurrent recovery and CCM mode

L99DZ300 integrates the CCM (constant current mode) mode and the OCR (over current recovery) mode, to fit respectively motors or incandescent bulbs (inrush current) and LED modules with high capacitor at input.

9.3.1 Constant current mode

CCM mode is available for all HS outputs. This function can be set only if the related driver is in OFF state, and it temporarily disables channel overcurrent and short-circuit detection (open-load detection remains ON).

The CCM mode is not available with internal PWM and Timer. If the CCM bit is set, an SPI write command to configure HS to be driven by PWM or Timer is rejected, and the SPI Invalid command error flag is set.

The default value for CCM bit is OFF.

For correct channel enable in CCM mode, the following sequence has to be used:

- Set HSx_CCM bit (x = 7, …, 15, 0) in CR3.
- Set HSx_0 bit to turn ON the driver in DC mode (PWM or Timer are ignored)

Driver starts with a constant current of about 100 mA (I_{CCM}) for 20 ms ($t_{CCMtimeout}$); during this phase channel overcurrent and short-circuit detection are disabled. When $t_{CCMtimeout}$ has elapsed, the channel switches to ON mode, while the CCM bit is automatically cleared.

Next two figures below show an example of an RC load (2.2 µF with 68 Ω in parallel) driven by HS8 with CCM disabled and with CCM enabled. With CCM disabled the current needed to charge the output capacitor is higher than OC threshold (I_{OC8}) and the channel is immediately switched OFF. If CCM is enabled the load voltage increases (with a constant current) during $t_{CCMtimeout}$ and charges the capacitor, then the device is switched fully ON.

Figure 20. HS8 with an RC as load, with CCM disabled

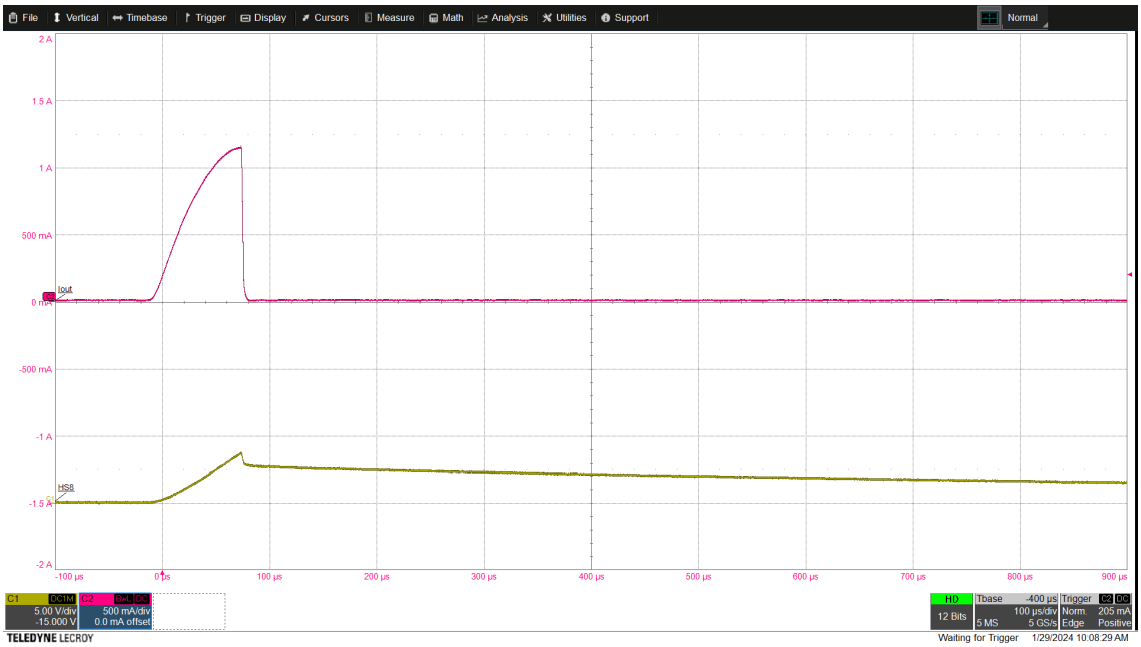
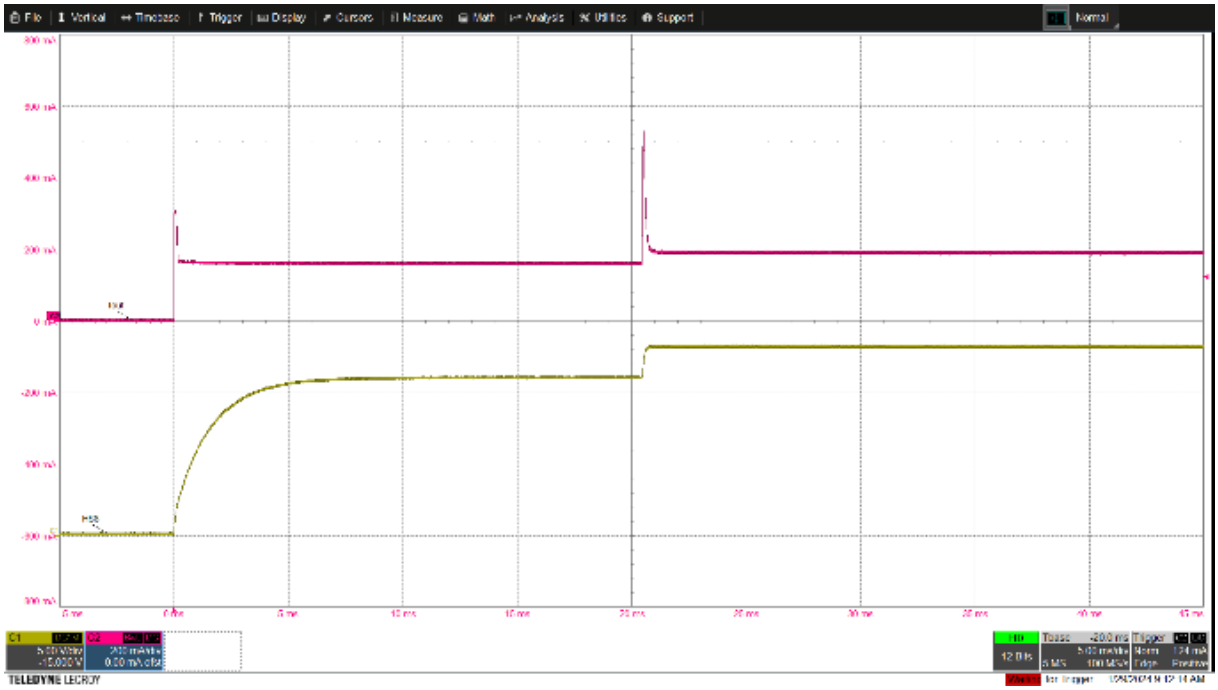


Figure 21. **HS8 with an RC as load, with CCM enabled**



9.4 Overcurrent recovery mode

OCR function is available for all HB and some HS outputs.

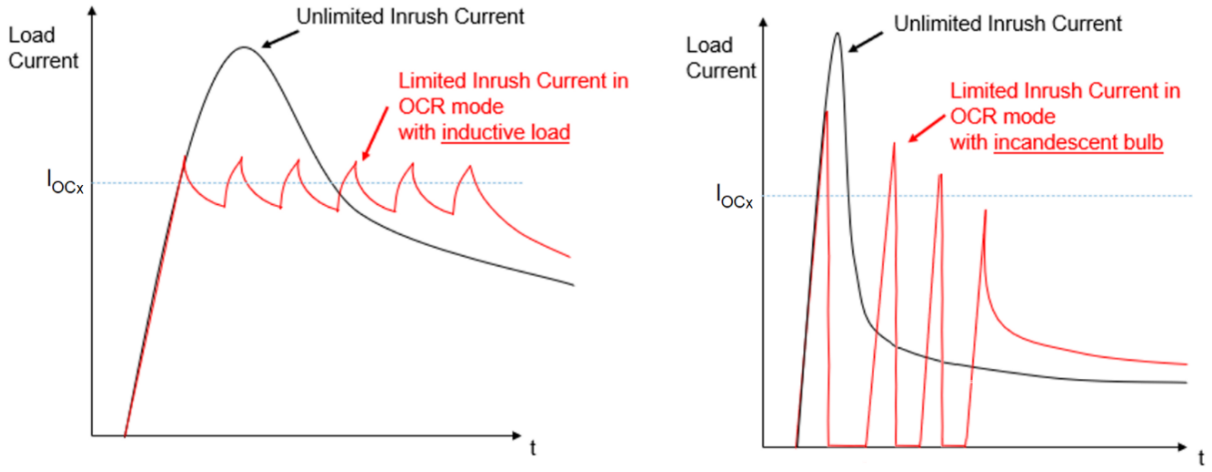
For HB1 to HB6 the overcurrent recovery feature can be enabled by setting the HBx_OCR bit in CR13; for HS7 to HS10 the overcurrent recovery feature can be enabled by setting the HSx_OCR bit in CR13.

If OCR mode is enabled, the corresponding output is turned OFF when the overcurrent threshold is reached, and then it turns automatically ON after a programmable recovery time. The PWM modulated current provides sufficient average current to power up the load (for example: heat up an incandescent bulb or a motor inrush current) until the load current reaches a stable condition.

Note: It is not suggested enabling the OCR function for too long time. Based on the load information, the OCR function should last for a limited time.

In the following figure is shown an example of OCR mode in case of inductive load (like a motor) and in case of incandescent bulb load.

Figure 22. **OCR functions with inductive loads and incandescent bulbs**



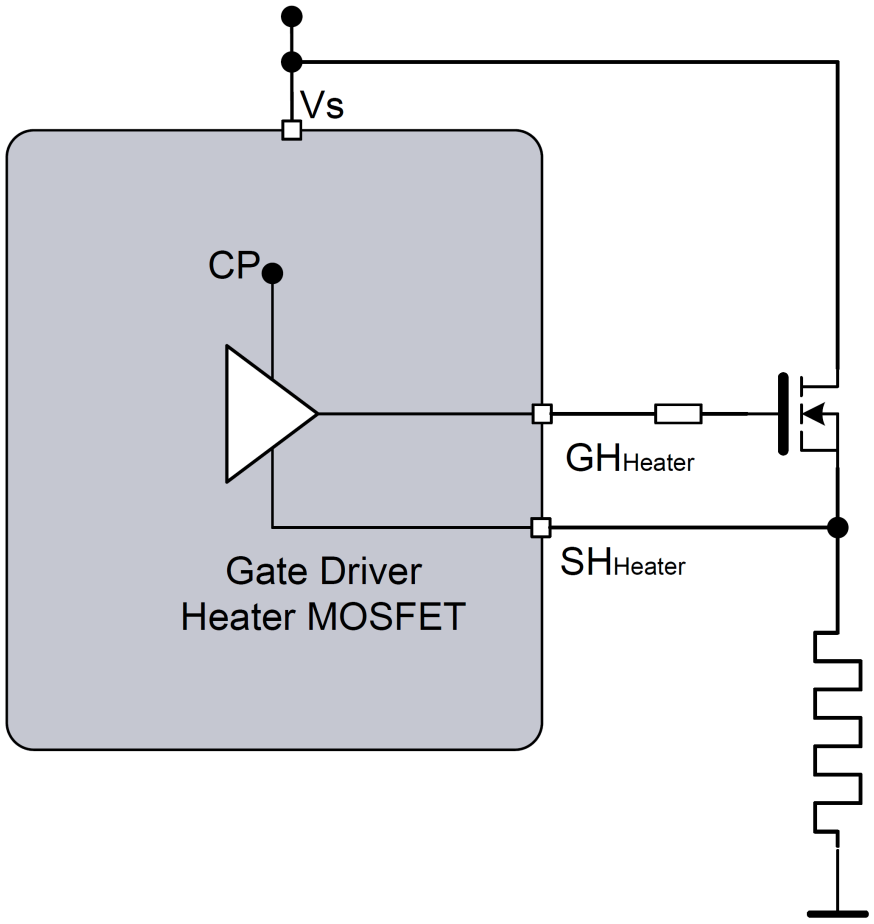
Only HB (HB1 to HB6) drivers have another protection against hard short circuits. Another threshold (I_{SCX}) higher than over current threshold (I_{OCX}) is implemented. In case the output current is higher than the short circuit threshold (I_{SCX}) for more than the filter time (t_{FSC} or t_{FSC_PWM}), the channel is switched OFF and it can be reactivated only after the OC flag (HBx_HS_OC / HBx_LS_OC) is cleared.

A similar protection applies also to HS drivers with OCR feature (HS7 to HS10). If the output voltage level remains low (< 2 V) after the programmed filter time t_{OCRxx}, the related output is switched OFF and it can be reactivated only after the OC flag (HSx_OC) is cleared.

10 Heater power MOSFET driver

L99DZ300G embeds a gate driver stage for N-channel power MOSFET in high-side configuration to control an external heater as shown in the figure below. The heater driver is controlled by the control bit GH in the CR12.

Figure 23. MOSFET driver for external heater



The driver also contains internal circuitry for OL detection in OFF state and V_{DS} monitoring in ON state.

V_{DS} monitoring function protects the external MOSFET in case of short-circuit to GND only when the driver is active (GH = 1). If the DS voltage exceeds the programmed threshold voltage V_{SCdx_HE} (configurable in the range 205 mV~666 mV through the 4-bits GH_TH_x in CR12) for a time higher than filter time t_{SCd_HE} (6 µs typ), the gate driver switches off the external MOSFET and the corresponding drain source monitoring flag (DSMON_HEAT bit in SR6) is set. The DSMON_HEAT bit must be cleared by SPI to reactivate the gate driver.

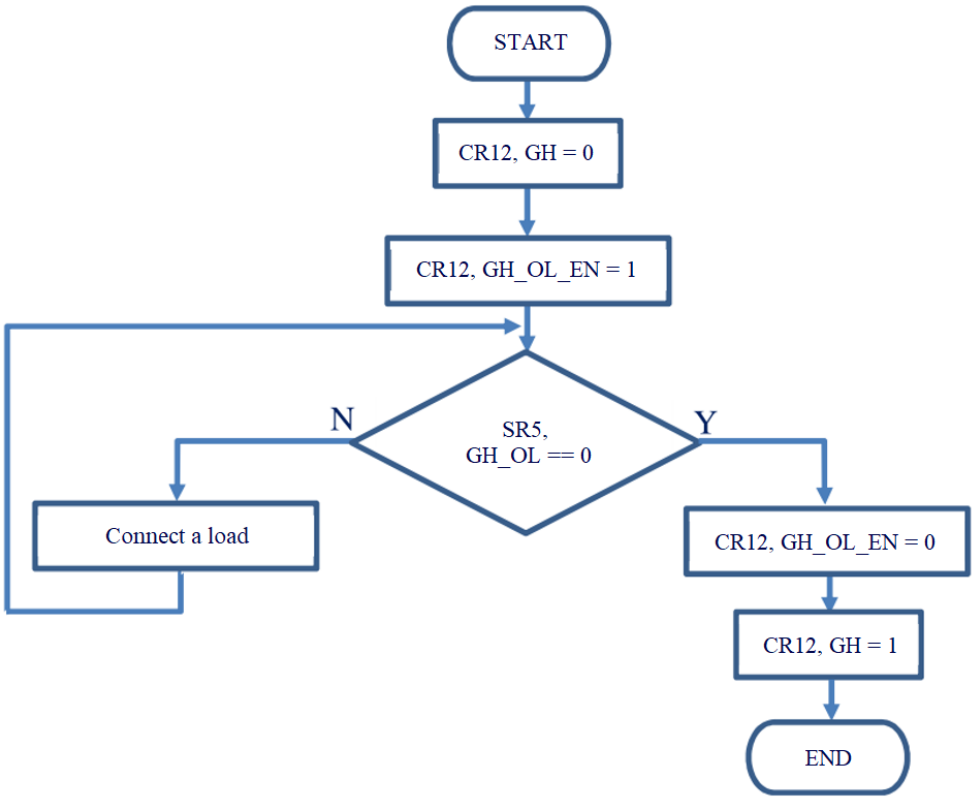
Open-load detection in off state is realized by monitoring the voltage difference between SHheater and GND and supplying SHheater by a pull-up current source that can be controlled via SPI with GH_OL_EN bit in CR12. If no load is connected to the external MOSFET source, the voltage is pulled to VS and if the voltage exceeding the threshold $V_{OLheater}$ for a time longer than the open-load filter time (t_{OL_HE}) the open-load bit GH_OL in SR5 will be set.

The recommended heater activation procedure is the following (see the flow chart in the figure below):

- Put the gate driver in OFF state (CR12, GH = 0)

- Active the open-load detection in the OFF state, by setting GH_OL_EN bit (CR12, GH_OL_EN = 1).
  - If no load is connected to the external MOSFET source, the MOSFET source voltage is charged to VS and the open-load bit GH_OL (SR5, GH_OL = 1) will be set.
  - If the load is connected to the output, no GH_OL flag is set (SR5, GH_OL = 0)
- If the OL diagnosis does not report any issue (SR5, GH_OL = 0), it is necessary to disable the open-load detection stage (CR12, GH_OL_EN = 0) and then the MOSFET can be turn ON (CR12, GH = 1)

Figure 24. Flow chart diagram for heater activation procedure



11 Electrochromic glass control

L99DZ300G can control an electrochromic (EC) mirror glass using the integrated SPI-driven module with an external MOS transistor.

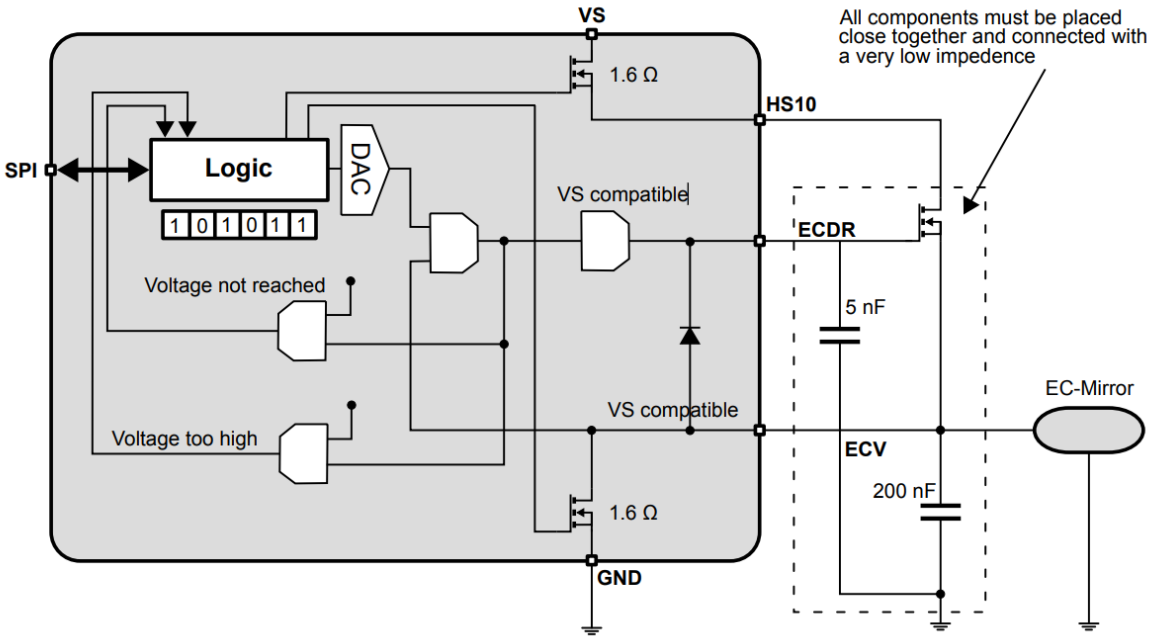
The function can be enabled through the bit ECON in CR11. When ECON = 1, HS10 is automatically turned ON and HS10 settings (CCM, OCR, PWMx, DIRx, TIMERx) are ignored. HS10 settings are recovered as soon as the ECON bit is set to ‘0’.

The ECV pin voltage can be set to a target value using the 6-bits EC_x in CR11. The target voltage is binary coded with a full-scale range of 1.5 V (0V with bits ‘000000’ and 1.5 V with bits ‘111111’).

An internal low side switch can be enabled (ECV_LS bit in CR11) for ECV fast discharge. In this case, the ECV pin is pulled to the ground by a 1.6 Ω low-side switch to reach faster the target voltage. The internal ECV MOSFET is also protected in case of overcurrent (ECV_OC flag) and embeds the OL circuitry (ECV_OL flag).

For loop-stability and EMS reasons, all the relevant external components must be placed as close as possible to device pins. A capacitor of at least 5 nF must be placed between pin ECDR and GND, and a capacitor of at least 200 nF must be placed between pin ECV and GND.

Figure 25. Electro-chrome control block



ECV settings:

- In electro-chrome mode, (ECON=1), the drain of the external power MOSFET transistor (the recommended one is STD17NF03L) is supplied by HS10, which maintains its integrated diagnoses in case of overload or open load conditions (HS10_OC and HS10_OL).
- If ECV_HV = 0 (default value): the maximum electro chrome controller target value is clamped to 1.2 V.
- If ECV_HV = 1: the maximum electro chrome controller target value is set to 1.5 V.
- The resolution of EC output is constant: 1.5V/ (2^6 -1), independently by ECV_HV setting.
- Internal ECV MOSFET overcurrent and open load failures can be monitored respectively through ECV_OC and ECV_OL bits in SR6 and SR5.

Through SPI it is possible to check if the desired voltage has been correctly reached through two live status bits:

- ECV_VHI bit in SR4 is set in case of V_{ECV}-V_{target} > d_{VECVhi}
- ECV_VNR bit in SR4 is set in case of V_{ECV}-V_{target} < d_{VECVnr}.

The voltage is at desired value when these bits are both at ‘0’.

In case of failure (overcurrent, VS/VSREG overvoltage /undervoltage, TSD1, CP_LOW), EC glass control block is disabled (the only exception is VS undervoltage failure with VS_UV_SD_ENA bit set to '0'):

- HS10 is turned OFF
- EC_x bits (CR11) are reset to the default value '000000'
- ECDR pin is pulled to GND.
- ECON (CR11) bit remains set to '1'
- ECV_LS (CR11) maintains its configuration.

The procedure to restart EC control after a failure, supposing that the cause of failure has been removed, is the following:

- Read and Clear of the related error flag (not necessary in case of VS/VSREG overvoltage/undervoltage if CR16 VS/VSREG_LOCK_ENA bit is set to '0', since the error flag is automatically cleared)
- Set the desired value on bits EC_x (CR11)

Consider the following points about the internal ECV low side switch:

- Even if ECV_LS =1, the low side is turned ON only if the ECV_VHI bit is set, otherwise it is maintained in the OFF state.
- If ECV_OC is set, the low side is turned OFF and it is necessary to clear the ECV_OC bit to re-enable the low side driver.
- To discharge a big out capacitance load via internal low side it could be necessary to set ECV_OCR (CR11) = 1. With this configuration, ECV_OC won't be set, and, in case of ECV short to VBATT, device internal temperature could rise. **So, it is strongly recommended to enable the ECV_OCR feature for a limited time**.

12 H-bridge predriver

L99DZ300G embeds a predriver to control 4 external MOS transistors in H-bridge configuration that can be driven in PWM mode up to 50 kHz. This is particularly suitable for door power window lift motor.

The H-bridge driver is disabled by default. It is enabled by setting the bit HEN in CR18.

The MOSFET activation can be controlled by two input pins (DIRH and PMMW) according to SPI setting (both input pins are active only if the bit HEN in CR18 is set).

There are two modes available, selectable by the DM bit in CR12:

- Single mode (bit DM = 0, default): 4 MOSFET in full bridge configuration to drive a single motor.
- Dual mode (bit DM =1): two independent half bridges can be used for two separated motors.

Additionally, with the 2-bits SD and SDS (CR12 register) four different slow decay modes (via drivers and via diode) can be selected using the high-side or the low-side transistors.

All possible input combinations of the previous signal are listed in Table 58 (H-bridge control truth table) of the datasheet.

H-bridge driver block integrates several customization and protection features:

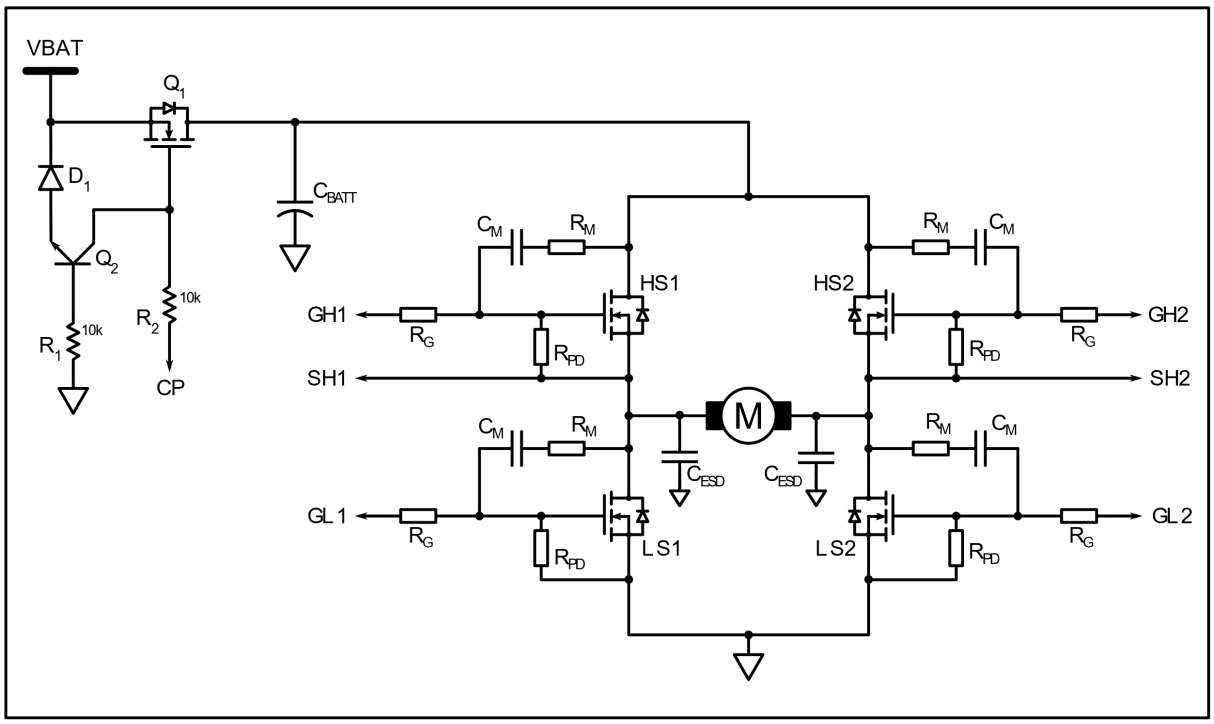
- Slew rate control: it allows to enable current source driving instead of a low impedance driving
- Resistive output mode: it forces MOSFET OFF during standby mode or in case of failure
- Drain source monitoring: for overload short-circuit detection/protection (for each external MOSFET)
- OFF state diagnosis
- Programmable freewheeling strategy (with SD and SDS bits)
- Cross current protection with configurable dead time

Each of these features is described in the datasheet.

12.1 Hardware configuration

The next figure shows a typical H-Bridge configuration with external NMOS transistors, and the circuit for reverse battery protection driven by the device charge pump (CP pin).

Figure 26. H-bridge and reverse battery network



Hereafter some considerations about external components:

H-bridge components

- MOSFETs (HS1, HS2, LS1, LS2) should be chosen according to the motor (maximum current and the required switching speed) and application conditions (maximum voltage and maximum ambient temperature).
- R_G is used for limiting the gate charge/discharge current and its value depends on the chosen MOSFET.
- Pull-down RPD resistors are used to keep the NMOS transistors reliably OFF in case of GHx/GLx three-state.
- Capacitor value on vs pin (C_{BATT}) should be dimensioned according to the maximum load current (rule of thumb is 500 µF each 10 A) and it can be shared among different loads.
- Miller capacitors C_M and RM resistors can be optionally used to improve EMI behavior.
- ESD CESD capacitors must be placed close to the connector (22 nF is the recommended value).

Reverse battery components

- D_1 is required to block battery voltage during normal operation, and it must have a high enough breakdown voltage to sustain positive transients (refers to ISO 7637-2).
- R_1 limits the base current in Q_2 during reverse battery.
- R_2 limits the Q_2 collector current thus allowing a voltage drop between the charge pump output, CP, and the gate of Q_1.
- Q_2 must be dimensioned to drive about 1 mA current (due to 10k resistors), so an inexpensive transistor can be chosen. Due to the internal charge pump, the collector voltage reaches maximum 13.5 V above battery, so Q2 collector to emitter breakdown voltage (BVCEO) will need to be sufficient to sustain that voltage.
- Q_1 should be chosen according to the load maximum current (not only the H-Bridge load but also all the internal channels supplied by VS pin).

Considering a window lift motor (max Iout = 40 A, DC current = 6 A) the following components could be used:

HS1, HS2, LS1, LS2: STL76DN4LF7

R_G: 62 Ω

R_{PD}: 10 kΩ

C_{BATT}: 200 µF

C_{ESD}: 22 nF

D_1: STTH102AY

R1, R2: 10 kΩ

Q_2: BC847

Q_1: STL285N4F7AG

13 LDO diagnosis

L99DZ300G embeds two 5V LDO voltage regulators:

- 5V1 for MCU and the integrated CAN transceiver supply, with up to 250 mA load current.
- 5V2 (tracker of V1 regulator) for additional loads, with up to 50 mA load current.

For both LDO, to guarantee the output voltage stability, a ceramic load capacitor higher than 1 µF is needed. It is recommended to use a 2.2 µF capacitor.

Both LDOs are protected against overload (like short circuit to GND) and overtemperature. They are protected both at startup and when they are already switched ON.

Short to GND protection at LDO turn ON:

1. If V1 < V_{1fail} for t > $t_{V1short}$, 5V1 is switched OFF and device enters immediately in forced VBAT standby mode (bit FORCED_SLEEP_TSD2_V1SC in SR8 and bit V1FAIL in SR7 are set). The 5V1 LDO is automatically re-enabled after the device wake-up.
2. If V2 < V_{2fail} for t > $t_{V2short}$, 5V2 is switched OFF (bit V2SC and bit V2FAIL in SR7 are set). To re-enable the 5V2 LDO the V2SC bit must be cleared.

Overload protection with LDO already turned ON:

1. If V1 < V_{1fail} for t > t_{V1fail}, the status bit V1FAIL in SR7 is set but 5V1 is not switched OFF; its current is limited ($I_{CCmax1)}$, and, if the chip temperature exceeds TSD2, it is switched OFF for about 1.5 s (t_{TSD}). Then it is automatically reactivated. If the restart fails 7 times within one minute the L99DZ300G enters the forced VBAT-standby mode, and the status bit FORCED_SLEEP_TSD2_V1SC in SR8 is set. The 5V1 LDO is automatically re-enabled after the device wake-up.
2. If V2 < V_{2fail} for t > $t_{V2short}$, the status bit V2FAIL in SR7 is set but 5V2 is not switched OFF; its current is limited ($I_{CCmax2)}$, and, if the chip temperature exceeds TSD1 (bit TSD1 in SR8 is set), it is switched OFF. To re-enable the 5V2 LDO the TSD1 bit must be cleared.

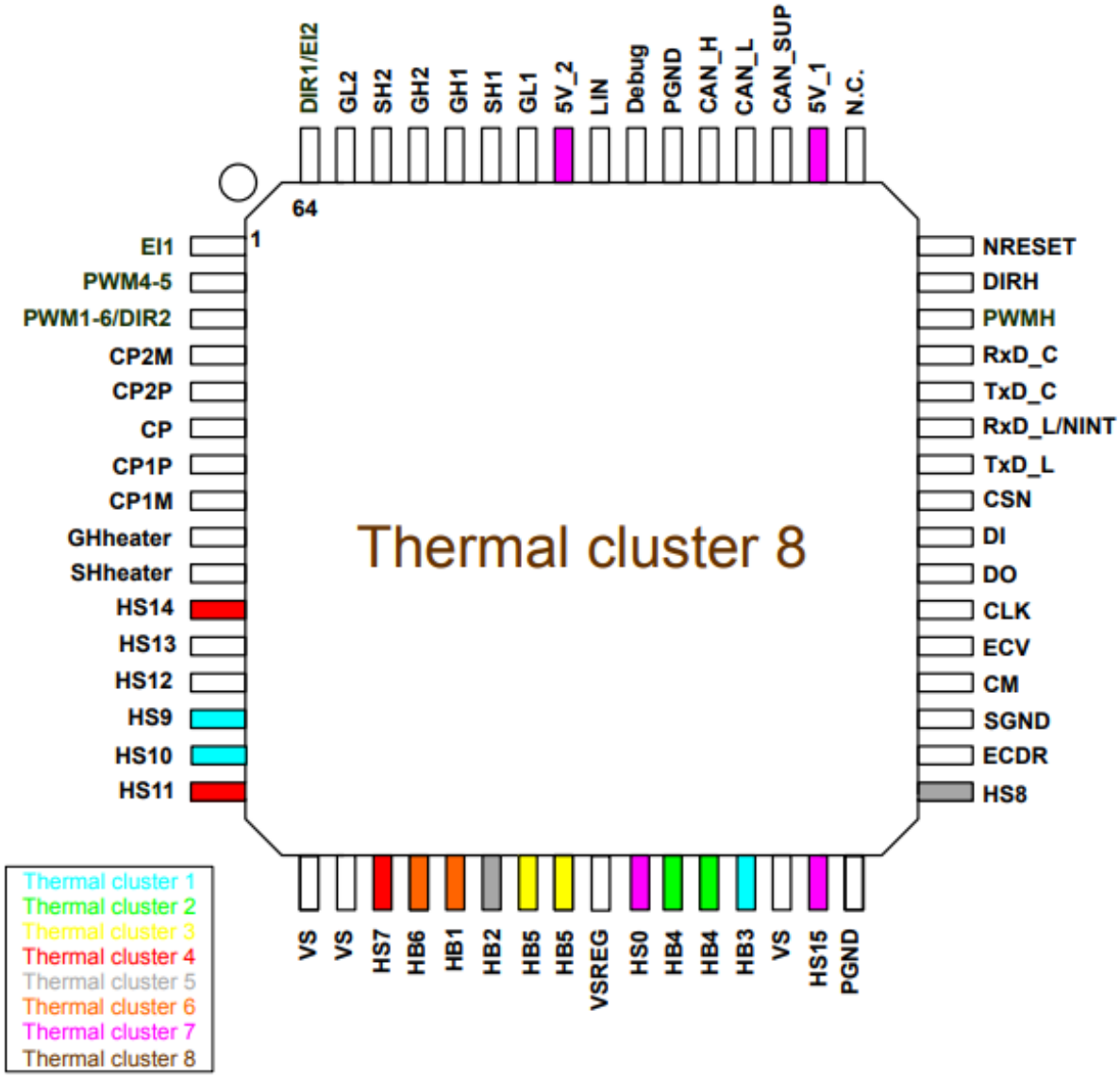
In case of overvoltage on LDO output, no diagnosis is implemented, and depending on LDO:

1. 5V1 cannot withstand a voltage higher than 6.5 V.
2. 5V2 is protected up to 28 V (only in case VSREG is supplied).

14 Thermal clusters

The device temperature is controlled; the power outputs and LDOs grouped into eight clusters (see the following figure), each one with dedicated thermal sensors.

Figure 27. Thermal clusters



When the temperature of a cluster is higher than TSD1 the device reaction depends on thermal cluster configuration bit value (bit TSD_CLUSTER_EN in CR3).

- In standard mode (TSD_CLUSTER_EN = 0, default), as soon as any cluster reaches TSD1:
  - All outputs drivers, charge-pump, and 5V2 regulator are turned OFF
  - 5V1 remains ON until TSD2
  - LIN and CAN transmitter are turned OFF (but they are forced in "receive only" mode)
- In Cluster mode (TSD_CLUSTER_EN = 1), only the cluster, which reaches TSD1 is switched OFF. This applies for all clusters except for thermal cluster 8 (global); in this case, the behavior is like standard mode.

For example, with a device configured in Cluster mode (TSD_CLUSTER_EN = 1):

- If thermal cluster 3 (HB5 related) reaches TSD1:
  - Only HB5 is turned OFF (all other outputs remain active)
  - 5V1 remains ON until TSD2
- If thermal cluster 8 (global cluster) reaches TSD1:
  - All outputs drivers, charge-pump, and 5V2 regulator are turned OFF
  - 5V1 remains ON until TSD2
  - LIN and CAN transmitter are turned OFF (but they are forced in "receive only" mode)

15 Unwanted GND loss event

A specific protection at device level is dedicated to the Loss of Ground event that occurs when the SGND pin (internal ground reference for the device logic) is disconnected from PGND pin (GND of all the H-bridges).

An internal comparator senses the voltage difference between the two pins and, if this voltage is high enough to reach the comparator threshold ($V_{SGNDloss}$, typ. 400 mV) for a time interval higher than the filter time ($t_{SGNDloss}$, typ. 7 µs), the device detects a ground loss situation, and L99DZ300G enters the forced VBAT standby mode to prevent damage to the system.

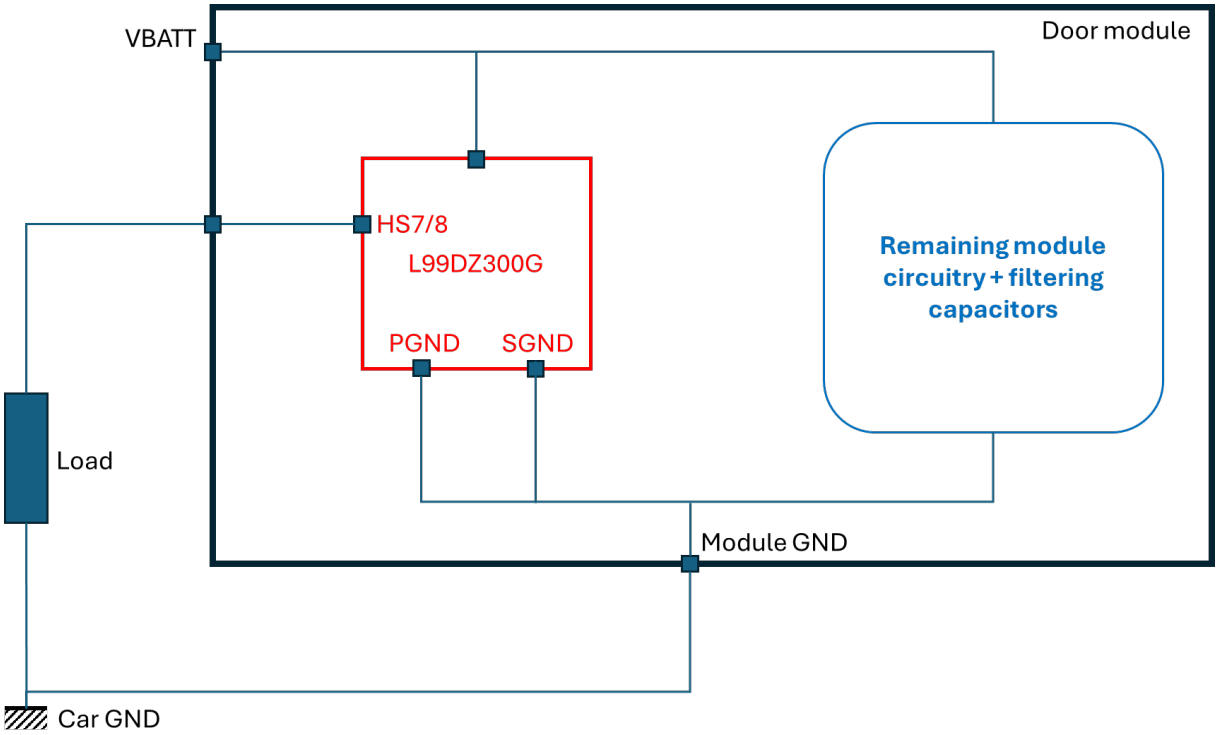
The forced VBAT standby mode can be terminated by any wake-up source, while the cause of the forced VBAT standby mode is indicated in the SPI status registers (SGNDLOSS bit in SR3).

The voltage threshold and filter time values are reported in section 2.4.29 of the L99DZ300G datasheet.

A possible condition that could generate an unwanted GND loss event can be the module power ON (or battery connector hot plug) when the following conditions are met:

- One or more HS outputs (typically HS7 and/or HS8) are connected to a load (for example, bulb) with its return path connected to a local GND (for example, vehicle frame) instead of the module GND (see next figure).
- Vs/Vsreg decoupling capacitors and module capacitors are completely discharged (cold start).

Figure 28. Door module simplified circuitry (unwanted GND Loss event)

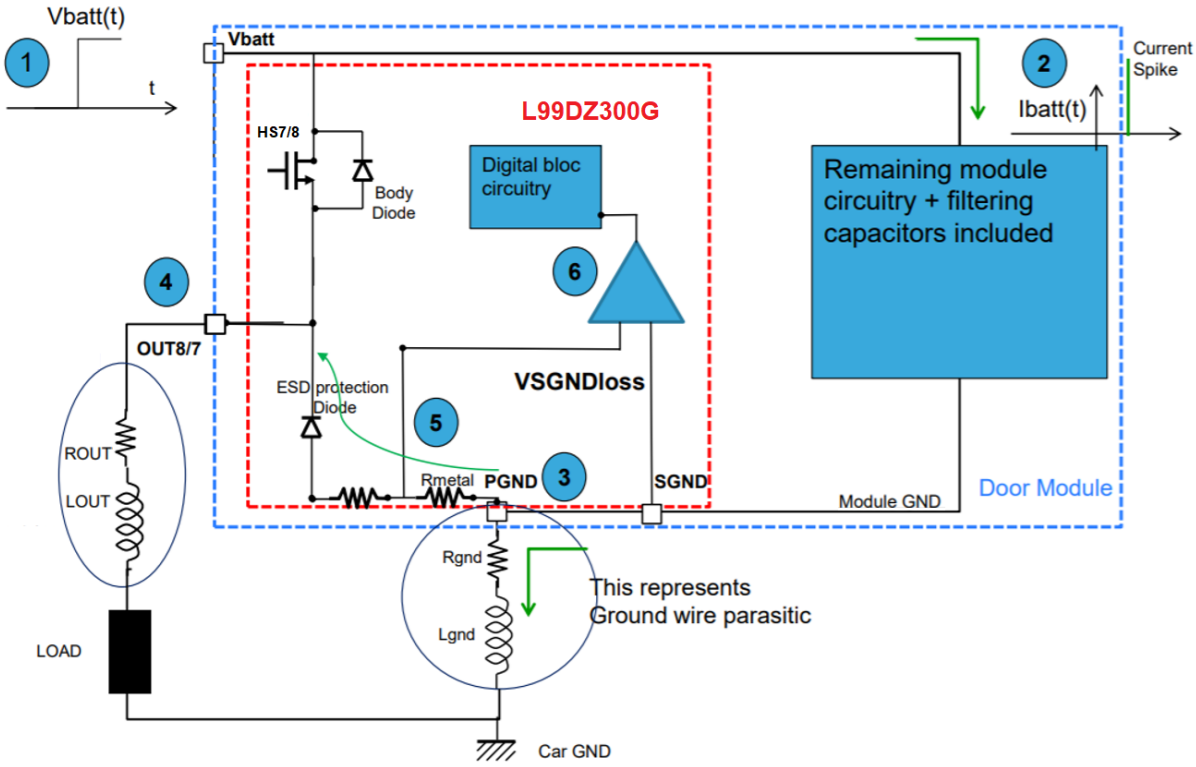


In this situation, it could happen that the device internal GND loss comparator is engaged as graphically described in Figure 29. Unwanted GND Loss event (L99DZ300G simplified internal structure) (numbers from 1 to 6).

At power ON (1), due to the associated dV_{BAT}/dt, a current spike (2) is generated because of the big decoupling capacitors on the module (Ispike,batt = Cmodule * dVBAT/dt). This current spike flows through ground module wires and generates a ground module shift (3) versus car ground (Rgnd * Ispike,batt + Lgnd * dIspike,batt/dt).

OUT8/7 voltage (4), referred to Car GND, becomes dynamically lower than module ground. Consequently, a current flow inside the L99DZ300G internal path (through metal resistance and HS7/8 pin ESD protection diode) and generates a delta voltage (5) on the ground comparator inputs. If this delta voltage is high enough to reach the comparator threshold ($V_{SGNDloss}$), the digital block circuitry (6) detects a ground loss situation, and L99DZ300G enters the forced VBAT standby mode to prevent damage to the system.

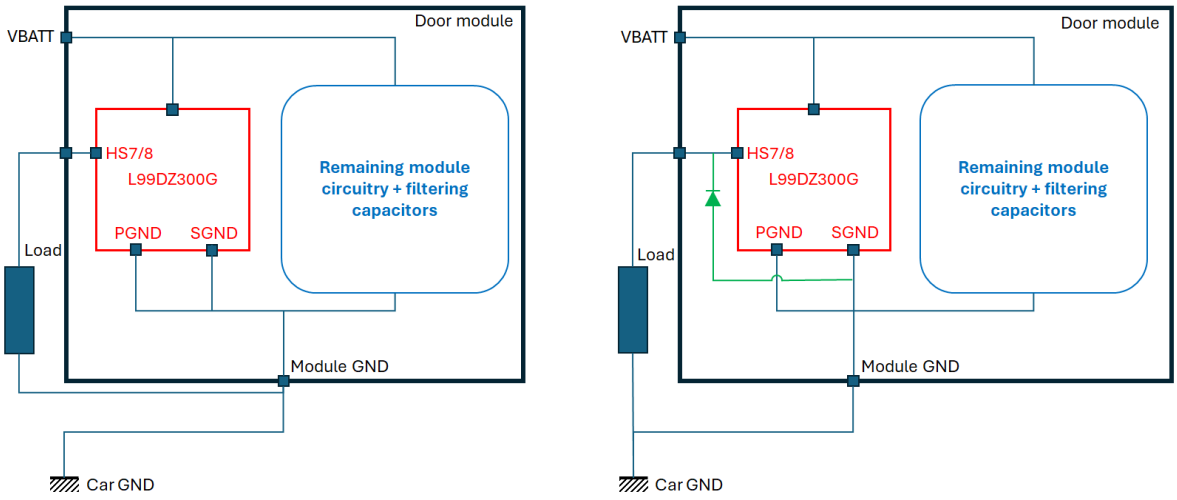
Figure 29. **Unwanted GND Loss event (L99DZ300G simplified internal structure)**



There are two possible solutions to avoid this kind of unwanted GND loss triggering event (see next figure):

1. The load return path must be connected to the module ground instead of the car ground.
2. In case the return path cannot be connected to the module ground, it is possible to add an external clamp between the involved pins (HS7/8 and SGND) such as a Schottky diode. This external diode is in parallel to the internal structure (ESD diode + Rmetal) and will prevent any significant current flow across the internal path that could lead to Ground Loss comparator triggering.

Figure 30. **Solutions: Load connected to module GND (left); diode between HS7/8 and SGND (right)**



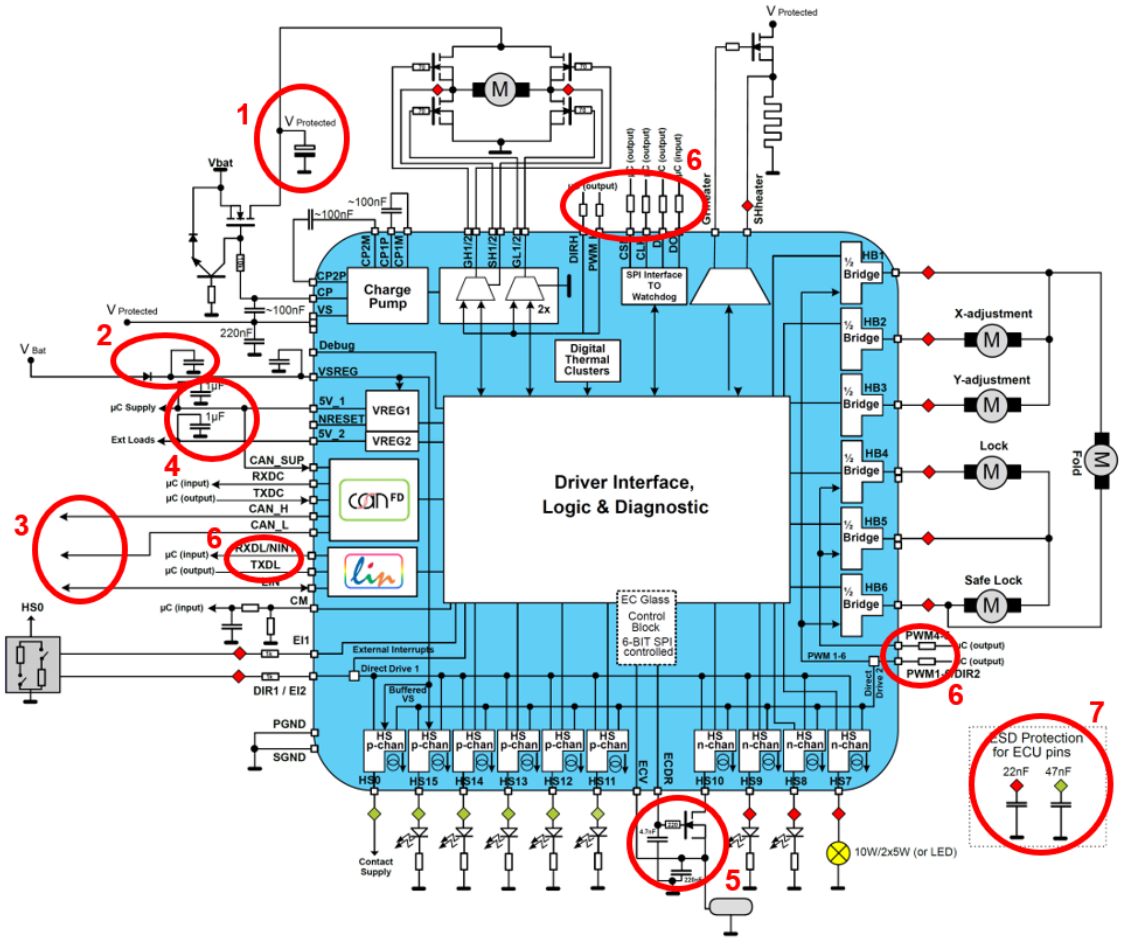
16 Hardware design points

It is recommended to adopt the following rules for external component dimensioning:

1. Capacitance value on vs pin has to be dimensioned according to load (motor) current (rule of thumb is 500 µF each 10 A)
2. The capacitance value on Vsreg pin has to be dimensioned according to LDO voltage drop out requirements and a diode for reverse Vsreg reverse battery protection must be added between Vbat and Vsreg.
3. External components must be dimensioned according to LIN and CAN OEM requirements.
4. For both LDO a capacitor of at least 1 µF is required for output voltage stability. For EMC optimization purposes, capacitance could be redimensioned (2.2 µF recommended).
5. To guarantee EC drive loop stability all components must be placed as close as possible to the relevant pins. To improve loop stability a resistor on MOSFET gate could be added (range 120 Ω to 220 Ω). It is also recommended to enlarge as much as possible the MOSFET heat dissipation area.
6. It is recommended to insert series resistors (1 kΩ) on all signal lines between L99DZ300G and MCU to protect the MCU in case of device failure. If device functionality (that is, CAN-FD at very high frequency) is impacted by such a value, the resistor value can be reduced to zero
7. All output pins (HSx, HBx, Eix, SHx and SHeater) must be protected from ESD with a capacitor placed close to the module connector (not close to device pin). The suggested values (22 nF of 47 nF) comply with “contact discharge, 150 pF, 330 Ω, ±8kV ” specification.

Important: *If HS10 is not used as an EC driver a 22 nF ESD capacitor must be used like other HS channels.*

Figure 31. Hardware design points



17 Unused PIN

If some device features are not used in the application, the unused pins must be treated as follows:

- CAN interface (all CAN control registers must be disabled by SPI configuration)
  - CAN supply pin must be connected to the ground
  - CAN_H and CAN_L must be connected to the ground
  - RxD_C pin must be left floating (high-Z) to avoid extra consumption
  - TxD_C pin must be connected to 5V1 (50K internal pull up to 5V1)
- LIN interface
  - TXDL pin must be connected to 5V1 (29K internal pull up to 5V1)
  - RXDL/NINT pin must be left floating
  - LIN pin must be left floating
- EC block
  - ECV pin must be left floating
  - ECDR pin must be left floating
- Heater power MOSFET driver
  - GH_{HEATER} pin must be left floating
  - SH_{HEATER} pin must be left floating
- Power outputs
  - HBx pin must be left floating
  - HSx pin must be left floating
- LDO regulator 5V2 must be left floating
- Digital inputs
  - DIRx pin must be connected to GND
  - DIRH and PWMH must be connected to GND
  - PWM1_6, PWM4_5 and PWM20_21 must be connected to GND
- EIx pin must be connected to GND
- CM pin must be left floating and must be disabled by SPI configuration.
- DEBUG pin must be connected to GND
  - DEBUG pin is intended to be used only during FW debug and (if necessary) during the first MCU FW programming in the manufacturing plant.
- H-bridge interface:
  - GHx must be left floating
  - SHx must be left floating
  - GLx must be left floating.
- All unused features must be disabled by SPI configuration.

Revision history

Table 7. **Document revision history**

Date	Revision	Changes
11-Oct-2024	1	Initial release.
04-Nov-2024	2	Updated Section 4.2: CAN wake-up. Minor text changes.

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